FAIRCHILD
SEMICONDUCTOR®

SPT7721

8-BIT, 250 MSPS ADC WITH DEMUXED OUTPUTS

TECHNICAL DATA

NOVEMBER 8, 2001

FEATURES

- TTL/CMOS/PECL compatible
- High conversion rate: 250 MSPS
- Single +5 V power supply
- Very low power dissipation: 310 mW
- Power-down mode
- +3.0 V/+5.0 V (LVCMOS) digital output logic compatibility
- Demuxed output ports

APPLICATIONS

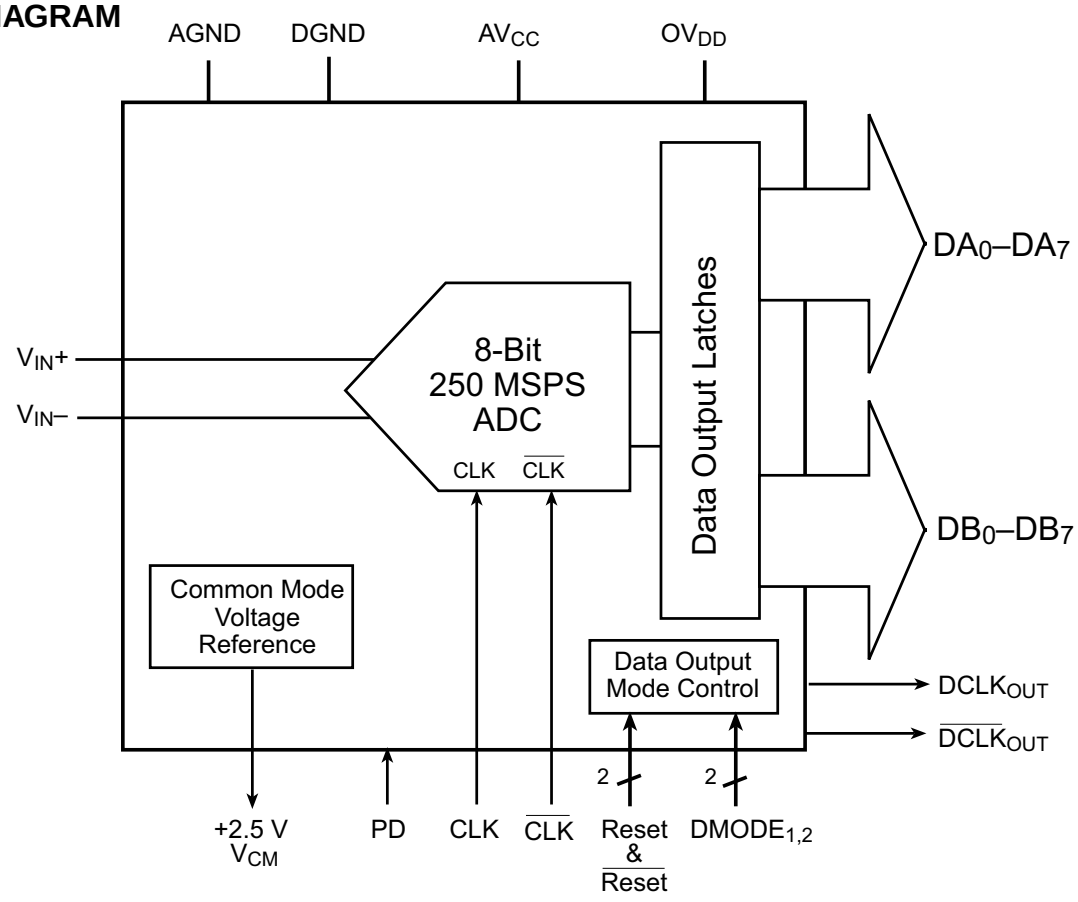
- RGB video processing
- Digital communications
- High-speed instrumentation
- Projection display systems

GENERAL DESCRIPTION

The SPT7721 is a high-speed, 8-bit analog-to-digital converter implemented in an advanced BiCMOS process. An advanced folding and interpolating architecture provides both a high conversion rate and very low power dissipation of only 310 mW. The analog inputs can be operated in either single-ended or differential input mode. A 2.5 V common mode reference is provided on chip for the single-ended input mode to minimize external components.

The SPT7721 digital outputs are demuxed (double-wide) with both dual-channel and single-channel selectable output modes. Demuxed mode supports either parallel aligned or interleaved data output. The output logic is both +3.0 V and +5.0 V compatible. The SPT7721 is available in a 44-lead TQFP surface mount package over the industrial temperature range of –40 to +85 °C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur) 25 °C

Supply Voltages

AV_{CC} ..... +6 V
OV_{DD} ..... +6 V

Input Voltages

Analog Inputs ..... –0.5 V to V_{CC} +0.5 V
Digital Inputs ..... –0.5 V to V_{CC} +0.5 V

Temperatures

Operating Temperature ..... –40 to +85 °C
Storage Temperature ..... –65 to +125 °C

Note: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, AV_{CC} = +5.0 V, f_{CLK} = 250 MHz, V_{CM} = 2.5 V, OV_{DD} = 5.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7721 MIN	SPT7721 TYP	SPT7721 MAX	UNITS
Resolution				8		Bits
DC Performance	f_{IN} = 1 kHz					
Differential Linearity Error (DLE)	+25 °C	V		–0.70/+1.05		LSB
	–40 °C to +85 °C	V		–0.95/+1.5		LSB
Integral Linearity Error (ILE)	+25 °C	V		±1.7		LSB
Best Fit	–40 °C to +85 °C	V		±2.25		LSB
No Missing Codes	+25 °C, f_{IN} = 1 kHz	I		Guaranteed		
Analog Input						
Input Voltage Range						
(with respect to V_{IN}–)	+25 °C	V		±470		mV_{P-P}
Gain Variation		VI		2		%
Input Common Mode (V_{CM})		IV	2.3	2.5	3.0	V
Input Bias Current		VI		10		µA
Input Resistance	+25 °C	V		50		kΩ
Input Capacitance	+25 °C	V		4		pF
Input Bandwidth	+25 °C (–3 dB of FS)	V		220		MHz
Offset Error		VI		±10		mV
Offset Power Supply Rejection Ratio		V		0.5		mV/V
Timing Characteristics						
Maximum Conversion Rate		VI	250			MSPS
Output Delay (Clock-to-Data) (t_{pd1})	–40 °C to +85 °C	IV	6	8	10.5	ns
Output Delay Tempco		V		22		ps/°C
Aperture Delay Time (t_{ap})		IV		0.5		ns
Aperture Jitter Time		IV		2		ps rms
Pipeline Delay (Latency)						
Single Channel Mode		V		2.5		Clocks
Demuxed Interleaved Mode		V		2.5		Clocks
Demuxed Parallel Mode						
Channel B		V		2.5		Clocks
Channel A		V		3.5		Clocks
CLK to $DCLK_{OUT}$ Delay Time						
Single Channel Mode (t_{pd2})		IV	4	6	7	ns
Dual Channel Mode (t_{pd3})		IV	5.3	6.16	7.8	ns
Dynamic Performance						
Effective Number of Bits (ENOB)						
f_{IN} = 70 MHz	+25 °C	VI	5.8	6.4		Bits
f_{IN} = 70 MHz	–40 °C to +85 °C	IV	5.5	6.0		Bits
Signal-to-Noise Ratio (SNR)						
f_{IN} = 70 MHz	+25 °C	VI	42	43		dB
f_{IN} = 70 MHz	–40 °C to +85 °C	IV	36	40		dB

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, AV_{CC} = +5.0 V, f_{CLK} = 250 MHz, V_{CM} = 2.5 V, OV_{DD} = 5 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7721 MIN	SPT7721 TYP	SPT7721 MAX	UNITS
Dynamic Performance						
Total Harmonic Distortion (THD)						
f_{IN} = 70 MHz	+25 °C	VI		–43	–40	dB
f_{IN} = 70 MHz	–40 °C to +85 °C	IV		–42	–37	dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN} = 70 MHz	+25 °C	VI	37	40		dB
f_{IN} = 70 MHz	–40 °C to +85 °C	IV	35	38		dB
Power Supply Requirements						
AV_{CC} Voltage (Analog Supply)		IV	4.75	5.0	5.25	V
OV_{DD} Voltage (Digital Supply)		IV	2.75		5.25	V
AV_{CC} Current		VI		62	70	mA
Power Dissipation with Internal Voltage Reference		VI		310	350	mW
Common Mode Reference						
Voltage		VI	2.45	2.5	2.55	V
Voltage Tempco		V		100		ppm/°C
Output Impedance	I_{OUT} = ±50 µA	V		1		kΩ
Power Supply Rejection Ratio		V		63		mV/V
Clock and Reset Inputs (Differential and Single-Ended)						
Differential Signal Amplitude (V_{DIFF})		VI	400			mV_{P-P}
Differential High Input Voltage (V_{IHD})		IV	1.4		5	V
Differential Low Input Voltage (V_{ILD})		IV	0		3.9	V
Differential Common-Mode Input (V_{CMD})		IV	1.2		4.1	V
Single-Ended High Input Voltage (V_{IH})		IV	1.8			V
Single-Ended Low Input Voltage (V_{IL})		IV			1.2	V
Input Current High (II_H)	V_{ID} = 1.5 V	VI	–100	20	+100	µA
Input Current Low (II_L)	V_{ID} = 1.5 V	VI	–100	20	+100	µA
Power Down and Mode Control Inputs (Single-Ended)						
High Input Voltage		IV	2.0		AV_{CC}	V
Low Input Voltage		IV	0		1.0	V
Maximum Input Current Low		VI	–100	10	+100	µA
Maximum Input Current High <4.0 V		VI	–100	10	+100	µA
Digital Outputs						
Logic "1" Voltage	I_{OH} = –0.5 mA	VI	OV_{DD} – 0.2	OV_{DD} – 0.06		V
Logic "0" Voltage	I_{OL} = +1.6 mA	VI		0.13	0.2	V
T_R/T_F Data	10 pF load					
	OV_{DD} = 3 V	V		3.5		ns
	OV_{DD} = 5 V	V		2.0		ns
T_R/T_F DCLK = (10 pF load)						
	OV_{DD} = 3 V	V		1.3		ns
	OV_{DD} = 5 V	V		0.7		ns

TEST LEVEL CODES

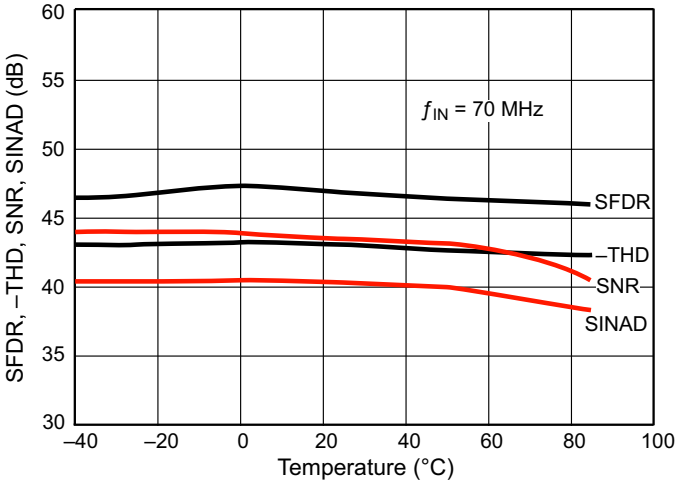
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

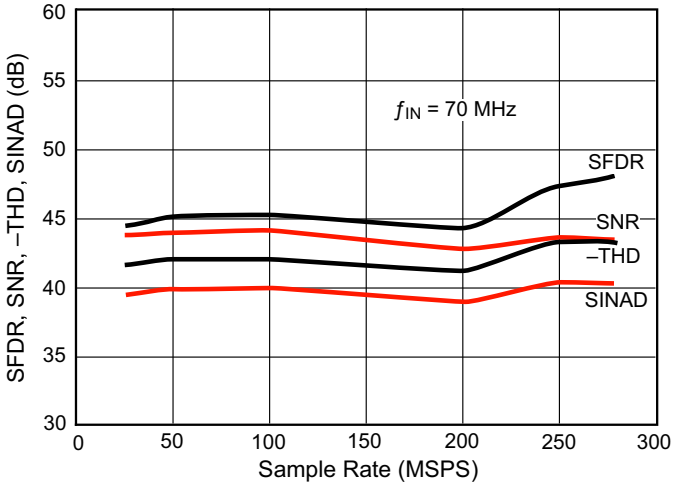
LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

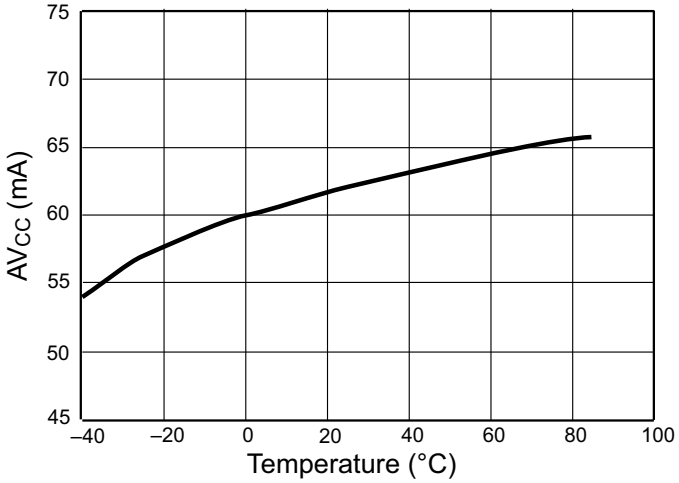
AC Performance vs Temperature



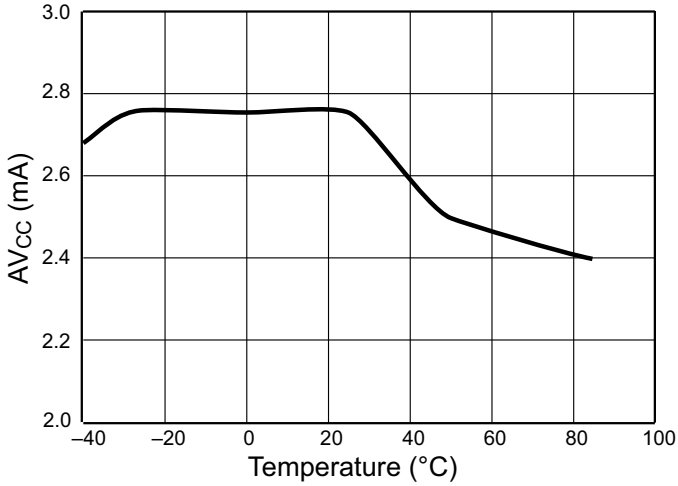
AC Performance vs Sample Rate



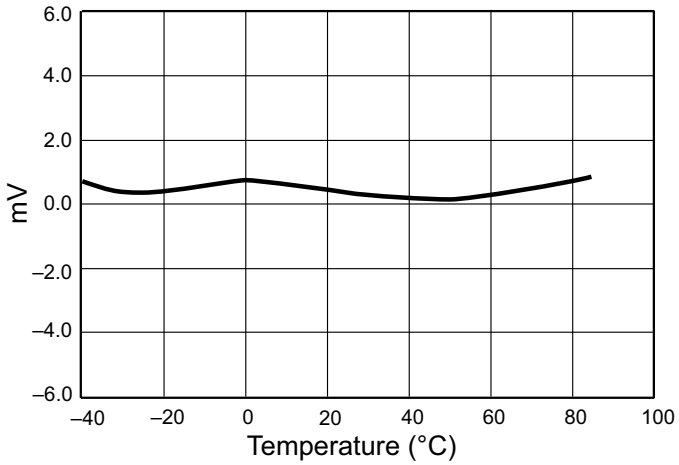
AV_{CC} Current vs Temperature



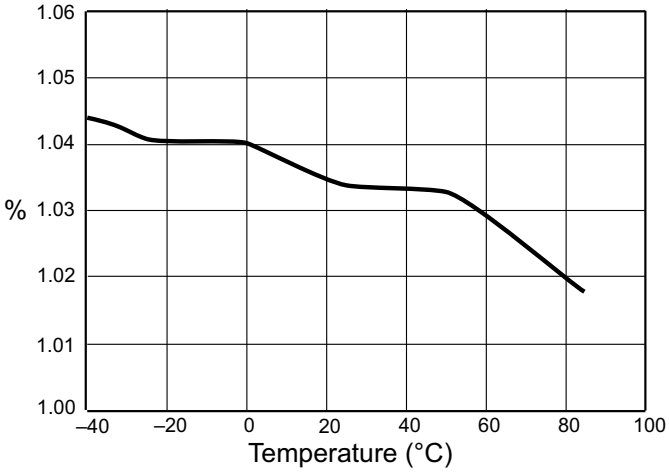
AV_{CC} Current Power Down vs Temperature



Voltage Offset Error vs Temperature

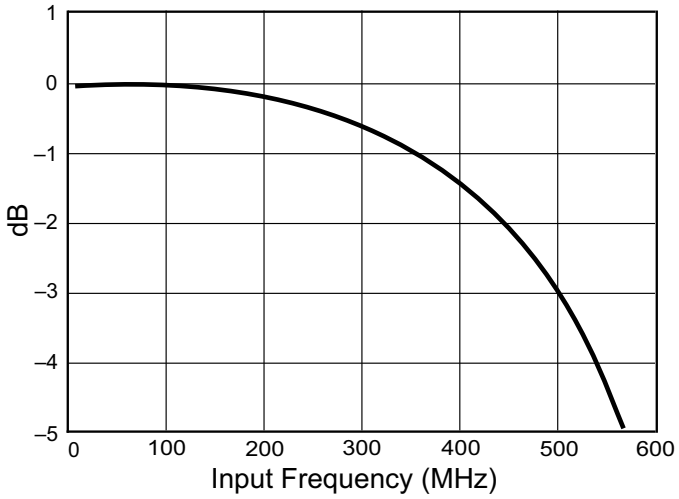


Percent Gain Error vs Temperature

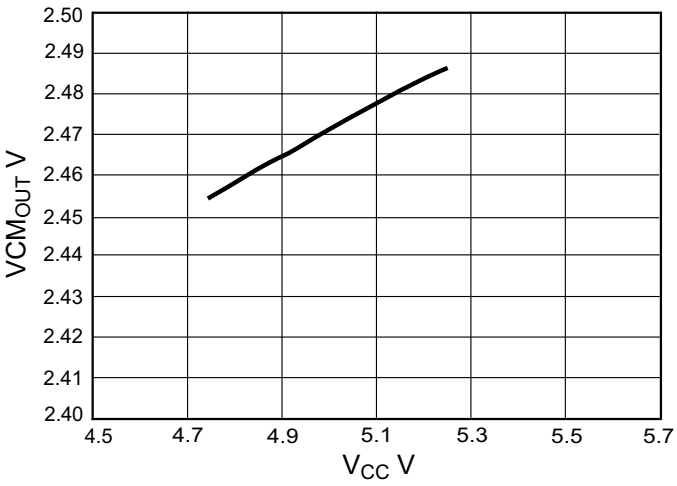


TYPICAL PERFORMANCE CHARACTERISTICS

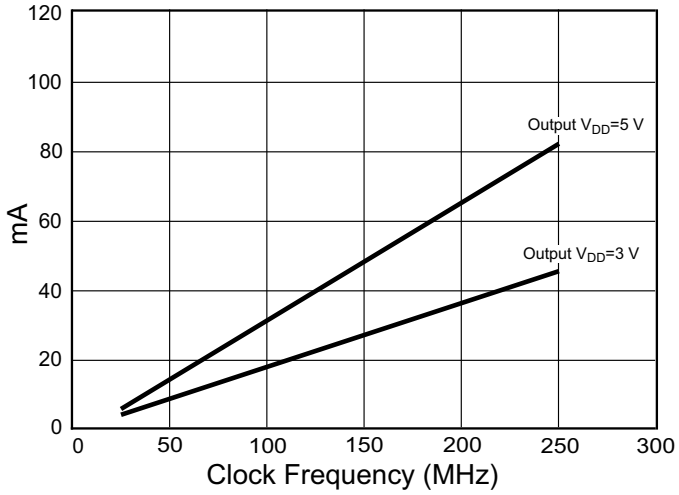
Input Bandwidth



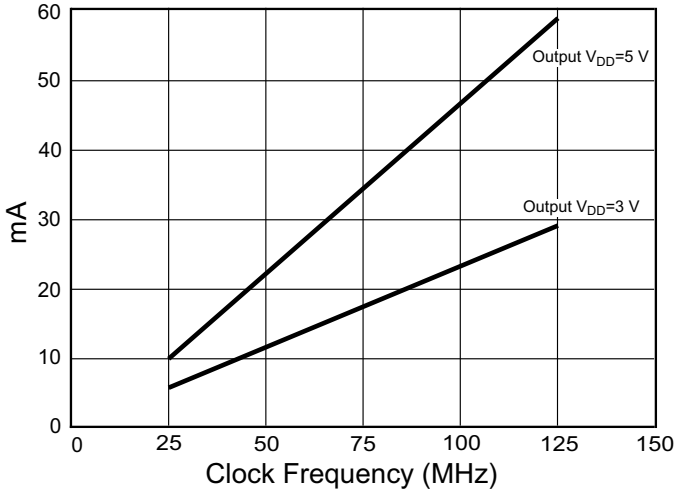
Common-Mode Reference Voltage vs V_{CC}



OV_{DD} Current vs Clock Frequency, Dual Mode

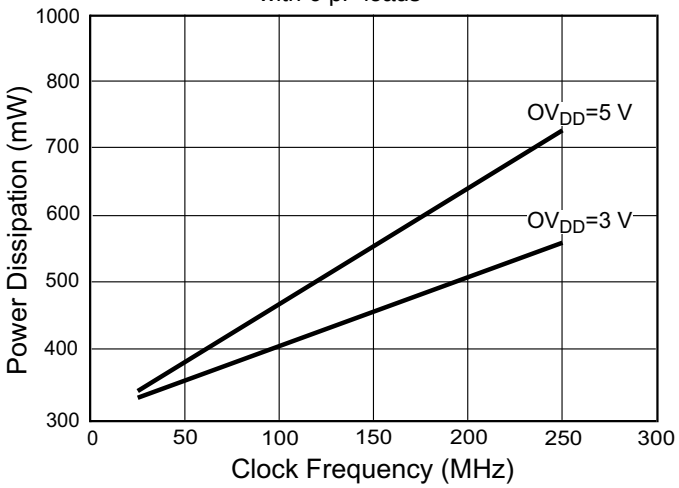


OV_{DD} Current vs Clock Frequency, Single Mode



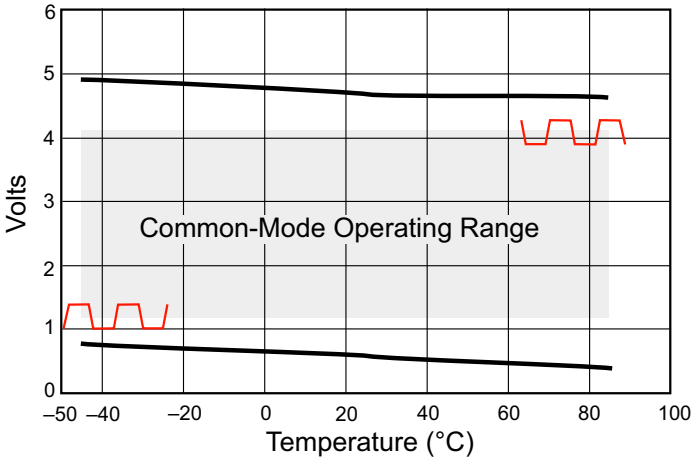
Total Power vs Clock Frequency

with 6 pF loads



Differential Input Common-Mode Operating Range

400 mV_{P-P}



THEORY OF OPERATION

The SPT7721 is a three-step subranger. It consists of two THAs in series at the input, followed by three ADC blocks. The first block is a three-bit folder with over/under range detection. The second block consists of two single-bit folding interpolator stages. There are pipelining THAs between each ADC block.

The analog decode functions are the input buffer, input THAs, three-bit folder, folding interpolators, and pipelining THAs. The input buffer enables the part to withstand rail-to-rail input signals without latchup or excessive currents and also performs single-ended to differential conversion. All of the THAs have the same basic architecture. Each has a differential pair buffer followed by switched emitter followers driving the hold capacitors. The input THA also has hold mode feedthrough cancellation devices.

The three MSBs of the ADC are generated in the first three-bit folder block, the output of which drives a differential reference ladder which also sets the full-scale input range. Differential pairs at the ladder taps generate midscale, quarter and three-quarter scale, overrange, and underrange. Every other differential pair collector is cross-coupled to generate the eighth scale zero crossings. The middle ADC block generates two bits from the folded signals of the previous stages after pipeline THAs. Its outputs drive more pipeline THAs to push the decoding of the three LSBs to the next half clock cycle. The three LSBs are generated in interpolators that are latched one full clock cycle after the MSBs.

The digital decode consists of comparators, exclusive of cells for gray to binary decoding, and/or cells used for mostly over/under range logic. There is a total of 3.5 clock cycles latency before the output bank selection. In order to reduce sparkle codes and maintain sample rate, no more than three bits at a time are decoded in any half clock cycle.

The output data mode is controlled by the state of the demux mode inputs. There are three output modes.

- All data on bank A with clock rate limited to one-half maximum
- Interleaved mode with data alternately on banks A and B on alternate clock cycles
- Parallel mode with bank A delayed one cycle to be synchronous with bank B every other clock cycle

If necessary, the input clock is divided by two. The divided clock selects the correct output bank. The user can synchronize with the divided clock to select the desired output bank via the differential RESET input.

The output logic family is LVCMOS with output VDD supply adjustable from 2.7 volts to 5.3 volts. There are also differential clock output pins that can be used to latch the output data in single bank mode or to indicate the current output bank in demux mode.

Finally, a power-down mode is available, which causes the outputs to become tri-state, and overall power is reduced to about 10 mW. There is a 2.5 V reference to supply common mode for single-ended inputs that is not shut down in power-down mode.

Figure 1 – Single Mode Timing Diagram

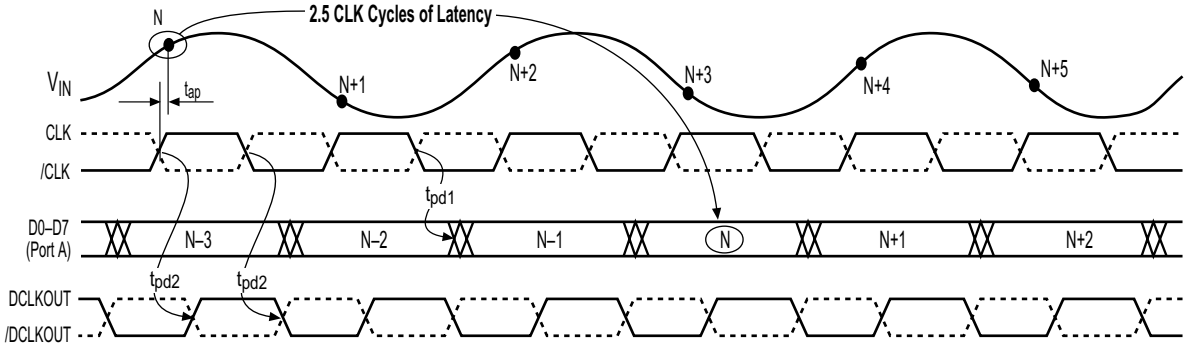


Figure 2 – Dual Mode Timing Diagram

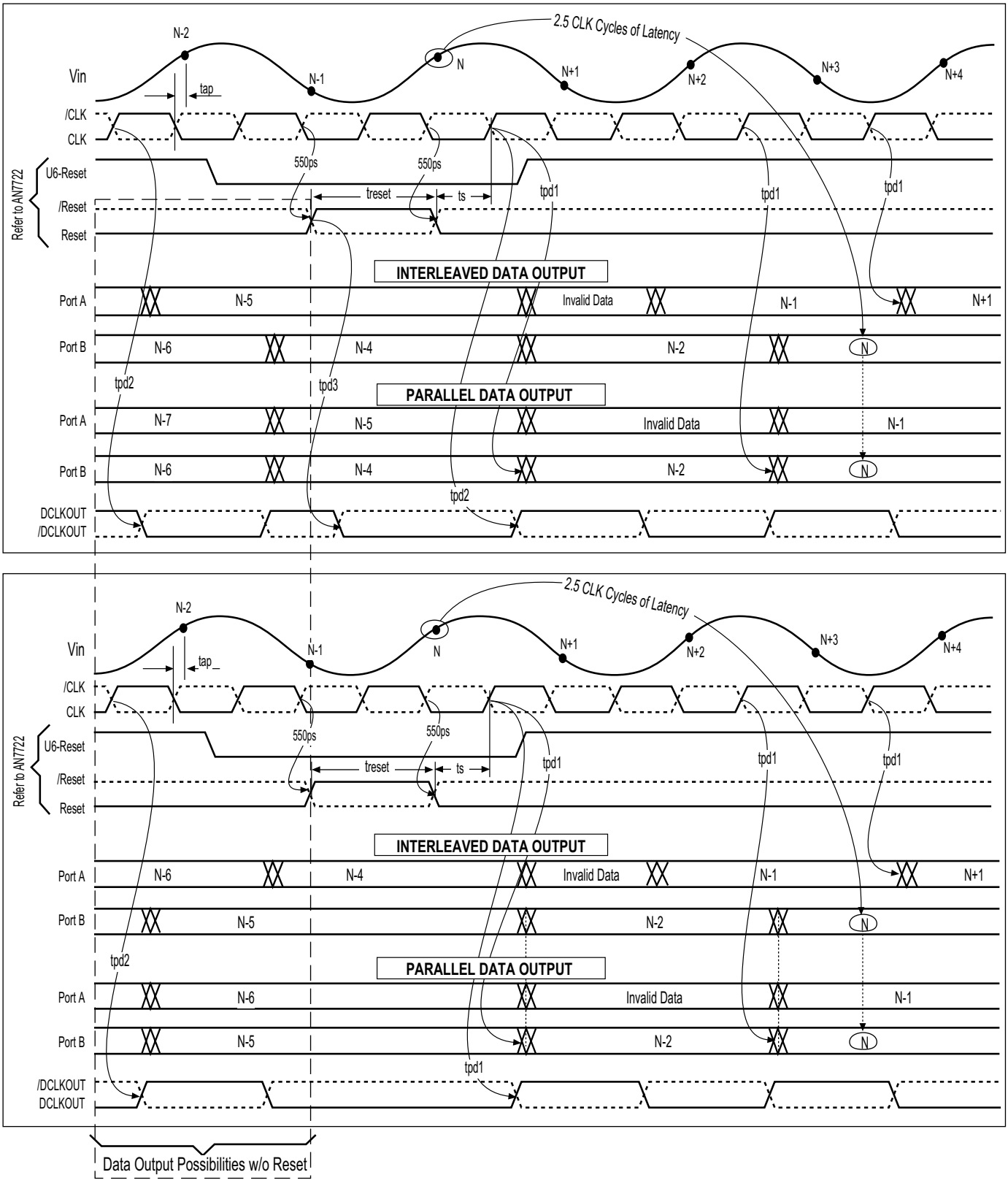
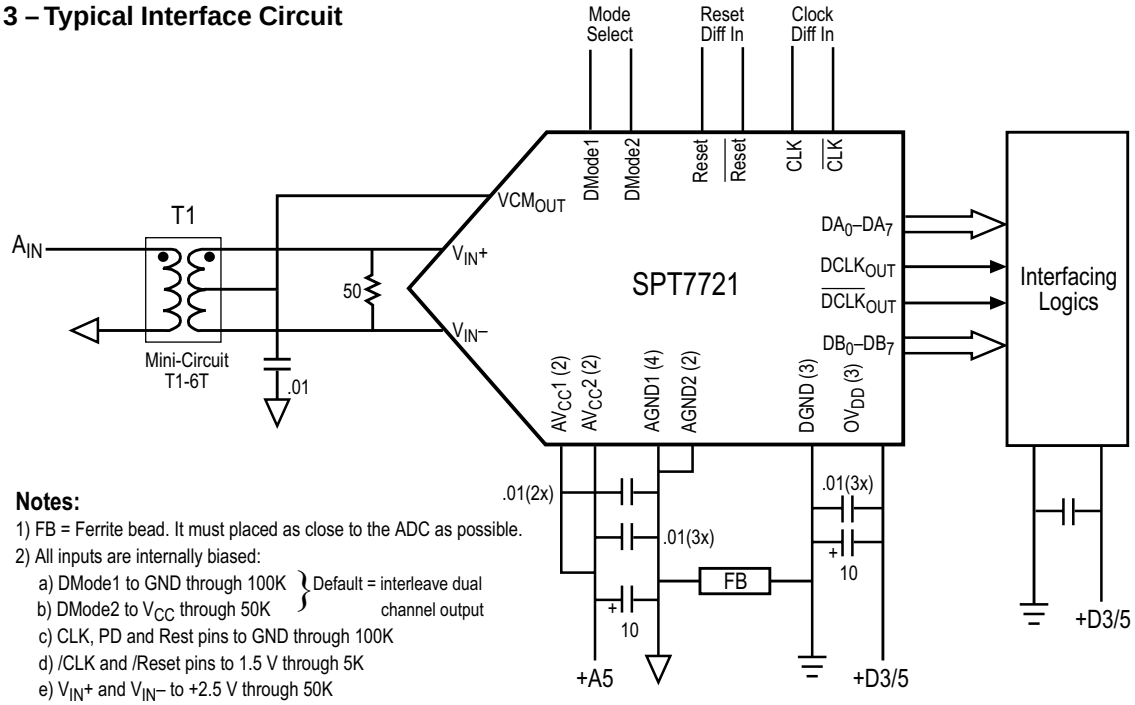


Figure 3 – Typical Interface Circuit



Notes:

1) FB = Ferrite bead. It must placed as close to the ADC as possible.
2) All inputs are internally biased:
   a) DMode1 to GND through 100K } Default = interleave dual
   b) DMode2 to V_{CC} through 50K } channel output
   c) CLK, PD and Rest pins to GND through 100K
   d) /CLK and /Reset pins to 1.5 V through 5K
   e) V_{IN}+ and V_{IN}– to +2.5 V through 50K
3) All 0.01microfarad capacitors are surface mount caps. They must be placed as close to the respective pin as possible

TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 3 shows the typical interface requirements when using the SPT7721 in normal circuit operation. The following sections provide descriptions of the major functions and outline performance criteria to consider for achieving the optimal device performance.

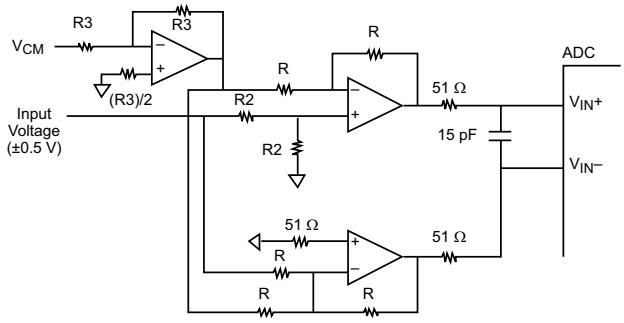
ANALOG INPUT

The input of the SPT7721 can be configured in various ways depending on whether a single-ended or differential input is desired.

The AC-coupled input is most conveniently implemented using a transformer with a center-tapped secondary winding. The center tap is connected to the V_{CM} pin as shown in figure 3. To obtain low distortion, it is important that the selected transformer does not exhibit core saturation at the full-scale voltage. Proper termination of the input is important for input signal purity. A small capacitor across the input attenuates kickback noise from the internal track-and-hold.

Figure 4 illustrates a solution (based on operational amplifiers) that can be used if a DC-coupled single-ended input is desired. It is very important to select op amps with a high open-loop gain, a bandwidth high enough so as not to impair the performance of the ADC, low THD, and high SNR.

Figure 4 – DC-Coupled Single-Ended to Differential Conversion (power supplies and bypassing are not shown)



INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit. This circuit provides ESD robustness and prevents latchup under severe discharge conditions without degrading analog transmission times.

POWER SUPPLIES AND GROUNDING

The SPT7721 is operated from a single power supply in the range of 4.75 to 5.25 volts. Normal operation is suggested to be 5.0 volts. All power supply pins should be bypassed as close to the package as possible. The analog and digital grounds should be connected together with a ferrite bead as shown in the typical interface circuit and as close to the ADC as possible.

POWER DOWN MODE

To save on power, the SPT7721 incorporates a power-down function. This function is controlled by the signal on pin PD. When pin PD is set high, the SPT7721 enters the power-down mode. All outputs are set to high impedance. In the power-down mode the SPT7721 dissipates 10 mW typically.

REFERENCES

To save on parts count, design time, and PC board real estate, the SPT7721 utilizes an internal reference. No other external components are required to implement this feature.

COMMON MODE VOLTAGE REFERENCE CIRCUIT

The SPT7721 has an on-board common-mode voltage reference circuit (V_{CM}). It is 2.5 volts and is capable of driving 50 µA loads typically. The circuit is commonly used to drive the center tap of the RF transformer in fully differential applications. For single-ended applications, this output can be used to provide the level shifting required for the single-to-differential converter conversion circuit.

CLOCK INPUT

The clock input on the SPT7721 can be driven by either a single-ended or double-ended clock circuit and can handle TTL, PECL, and CMOS signals. When operating at high sample rates it is important to keep the pulse width of the clock signal as close to 50% as possible. For TTL/CMOS single-ended clock inputs, the rise time of the signal also becomes an important consideration.

DIGITAL OUTPUTS

The output circuitry of the SPT7721 has been designed to be able to support three separate output modes. The demuxed (double-wide) mode supports either parallel aligned or interleaved data output. The single-channel mode is not demuxed and can support direct output at speeds up to 125 MSPS. The output format is straight binary (table I).

Table I – Output Data Format

Analog Input	Output Code D7–D0
+FS	1111 1111
+FS – 1/2 LSB	1111 111Ø
+1/2 FS	ØØØØ ØØØØ
–FS + 1/2 LSB	0000 000Ø
–FS	0000 0000

Ø indicates the flickering bit between logic 0 and 1

The data output mode is set using the $DMODE_1$ and $DMODE_2$ inputs (pins 32 & 31 respectively). Table II describes the mode switching options.

Table II – Output Data Modes

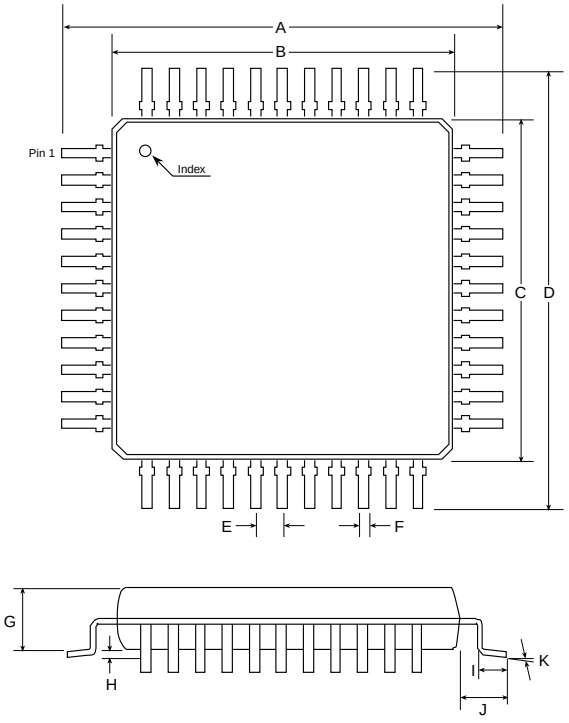
Output Mode	$DMODE_1$	$DMODE_2$
Parallel Dual Channel Output	0	0
Interleaved Dual Channel Output	0	1
Single Channel Data Output (Bank A only 125 MSPS max)	1	X

EVALUATION BOARD

The EB7721/22 evaluation board is available to aid designers in demonstrating the full performance of the SPT7721. This board includes a clock driver and reset circuit, adjustable references and common mode, a single-ended to differential input buffer and a single-ended to differential transformer (1:1). An application note (AN7721/22) describing the operation of this board, as well as information on the testing of the SPT7721, is also available. Contact the factory for price and availability of the EB7721/22.

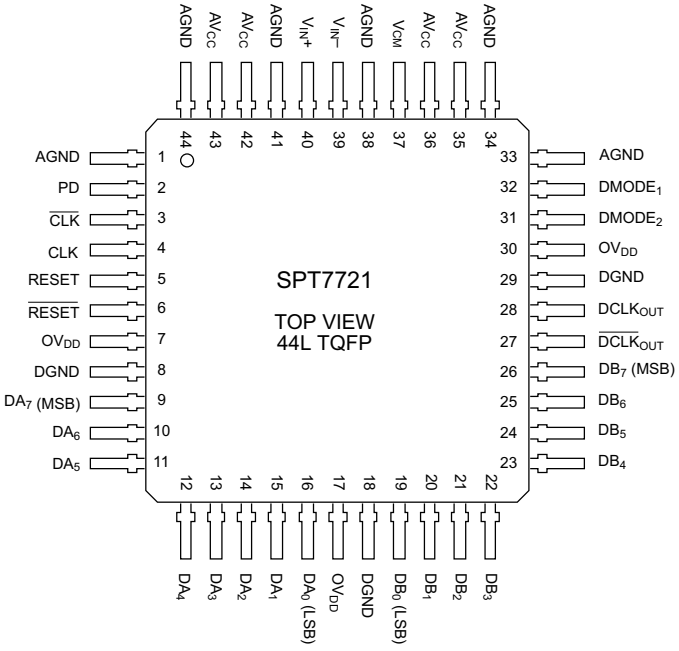
PACKAGE OUTLINE

44-Lead TQFP



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.472 Typ		12.00 Typ	
B	0.394 Typ		10.00 Typ	
C	0.394 Typ		10.00 Typ	
D	0.472 Typ		12.00 Typ	
E	0.031 Typ		0.80 Typ	
F	0.012	0.018	0.300	0.45
G	0.053	0.057	1.35	1.45
H	0.002	0.006	0.05	0.15
I	0.020	0.030	0.500	0.750
J	0.039 Typ		1.00 Typ	
K	0-7°		0-7°	

PIN ASSIGNMENTS



PIN FUNCTIONS

Pin Name	Description
V_{IN}+	Non-Inverted Analog Input; nominally 1 V_{P-P}; 100k pullup to V_{CC} and 100k pulldown to AGND, internally
V_{IN}–	Inverted Analog Input; nominally 1 V_{P-P}; 100k pullup to V_{CC} and 100k pulldown to AGND, internally
DA_0–DA_7	Data output; Bank A. 3 V / 5 V LVCMOS compatible.
DB_0–DB_7	Data output; Bank B. 3 V / 5 V LVCMOS compatible.
$DCLK_{OUT}$	Non-Inverted data output clock. 3 V / 5 V LVCMOS compatible.
$\overline{DCLK}_{OUT}$	Inverted data output clock. 3 V / 5 V LVCMOS compatible.
CLK	Non-Inverted clock input pin; 100k pulldown to AGND, internally
$\overline{CLK}$	Inverted clock input pin; 17.5k pullup to V_{CC} and 7.5k pulldown to AGND, internally
RESET	RESET synchronizes the data sampling and data output bank relationship when in Dual Channel Mode ($DMODE_1$ = 0); 100k pulldown to AGND, internally
$\overline{RESET}$	Inverted RESET input pin; 17.5k pullup to V_{CC} and 7.5k pulldown to AGND, internally
$DMODE_{1,2}$	Internally: 100k pulldown to AGND on DMODE1 50k pullup to V_{CC} on DMODE2 Data Output Mode pins: $DMODE_1$ = 0, $DMODE_2$ = 0: Parallel Dual Channel Output $DMODE_1$ = 0, $DMODE_2$ = 1: Interleaved Dual Channel Output $DMODE_1$ = 1, $DMODE_2$ = X: Single Channel Data Output on Bank A (125 MSPS max)
PD	Power Down pin; PD = 1 for power-down mode. Outputs set to high impedance in power-down mode; 100k pulldown to AGND, internally
V_{CM}	2.5 V Common Mode Voltage Reference Output
AV_{CC}	+5 V Analog Supply
OV_{DD}	+3 V / +5 V Digital Output Supply
AGND	Analog Ground
DGND	Digital Ground

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT7721SIT	–40 to +85 °C	44L TQFP

DISCLAIMER

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.