FAIRCHILD
SEMICONDUCTOR®

SPT7935

12-BIT, 20 MSPS, 79 mW A/D CONVERTER

FEATURES

- 12-Bit, 20 MSPS Analog-to-Digital Converter
- Monolithic CMOS
- Internal Track-and-Hold
- Low Input Capacitance: 1.4 pF
- Low Power Dissipation: 79 mW
- 2.8 – 3.6 V Power Supply Range
- TTL-Compatible Outputs

APPLICATIONS

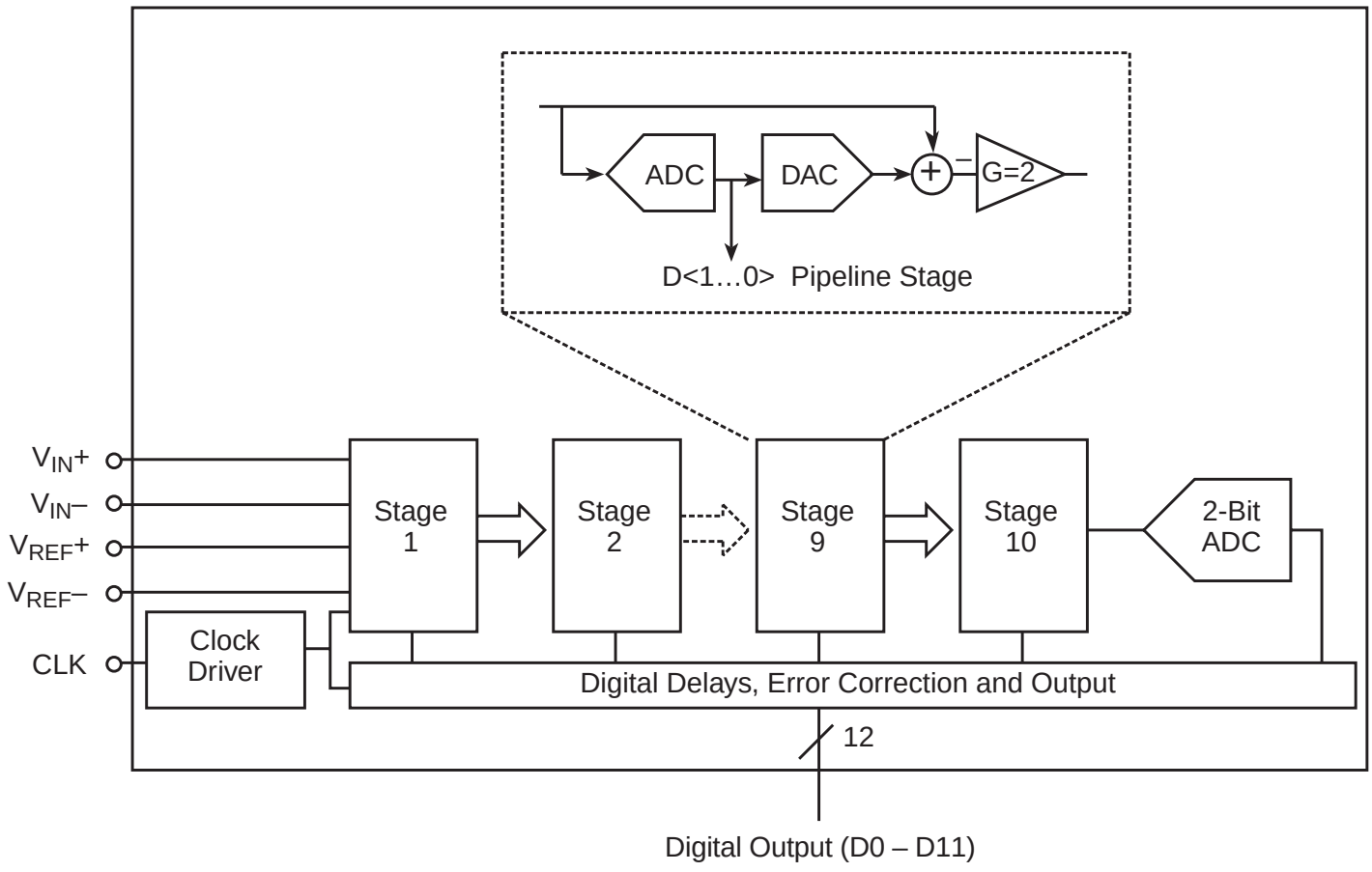
- CCD Imaging Cameras and Sensors
- Medical Imaging
- RF Communications
- Document and Film Scanners
- Electro-Optics
- Transient Signal Analysis
- Handheld Equipment

GENERAL DESCRIPTION

The SPT7935 12-bit, 20 MSPS analog-to-digital converter has a pipelined converter architecture built in a CMOS process. It delivers high performance with a typical power dissipation of only 79 mW. With low distortion and high dynamic range, this device offers the performance needed for imaging, multimedia, telecommunications and instrumentation applications.

The SPT7935 is available in a 44-lead Thin Quad Flat Pack (TQFP) package in the industrial temperature range (–40 to +85 °C).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{DD_1} ..... –0.5 V to +6 V
V_{DD_2} ..... –0.5 V to +6 V
V_{DD_3} ..... –0.5 V to +6 V

Input Voltages

Analog Input ..... –0.5 V to (V_{DD} +0.5 V)
Digital Input ..... –0.5 V to (V_{DD} +0.5 V)
V_{REF}+ ..... –0.5 V to (V_{DD} +0.5 V)
V_{REF}– ..... –0.5 V to (V_{DD} +0.5 V)
CLK ..... –0.5 V to (V_{DD} +0.5 V)

Temperature

Operating Temperature ..... –40 to +85 °C
Storage Temperature ..... –65 to +125 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN}–T_{MAX} , V_{DD_1}=V_{DD_2}=V_{DD_3}=3.3 V, V_{REF}–=1.0 V, V_{REF}+=2.0 V, Common Mode Voltage=1.65 V, f_{CLK}=20 MSPS, Bias 1=90 µA, Bias 2=9.5 µA, Differential Input, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7935 MIN	SPT7935 TYP	SPT7935 MAX	UNITS
DC Accuracy						
Resolution				12		Bits
Differential Linearity		V		±0.6		LSB
Integral Linearity		V		±3.0		LSB
No Missing Codes		VI		Guaranteed		
Analog Input						
Input Voltage Range (Differential)		IV	±0.6	±1.0	±1.7	V
Common Mode Input Voltage		IV	1.2	1.65	1.9	V
Input Capacitance		V		1.4		pF
Input Bandwidth (Large Signal)		V		120		MHz
Offset (Mid-scale)	V_{IN}+=V_{IN}–=V_{CM}	V		±1.0		% FSR
Gain Error		V		0.3		% FSR
Reference Voltages						
Reference Input Voltage Range (V_{REF}+ – V_{REF}–)		IV	0.6	1.0	1.7	V
Negative Reference Voltage (V_{REF}–)		IV	0.9	1.0	1.3	V
Positive Reference Voltage (V_{REF}+)		IV	1.9	2.0	2.6	V
Common Mode Output Voltage (V_{CM})	I_O = –1 µA	VI	1.3	1.65	1.8	V
V_{REF}+ Current		V		35		µA
V_{REF}– Current		V		–25		µA
Switching Performance						
Maximum Conversion Rate		VI	20			MHz
Pipeline Delay		IV		7.5		Clocks
(See Timing Diagram)						
Aperture Delay Time (T_{AP})		V		5		ns
Aperture Jitter Time		V		10		ps-rms
Dynamic Performance						
Effective Number of Bits						
f_{IN} = 5.0 MHz		VI	9.2	9.8		Bits
f_{IN} = 10.0 MHz		V		9.0		Bits
Signal-To-Noise Ratio						
f_{IN} = 5.0 MHz		VI	59	62		dB
f_{IN} = 10.0 MHz		V		58		dB
Total Harmonic Distortion						
f_{IN} = 5.0 MHz		VI		–68	–61	dB
f_{IN} = 10.0 MHz		V		–60		dB

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}–T_{MAX}$, $V_{DD_1}=V_{DD_2}=V_{DD_3}$=3.3 V, V_{REF}–=1.0 V, V_{REF}+=2.0 V, Common Mode Voltage=1.65 V, f_{CLK}=20 MSPS, Bias 1=90 µA, Bias 2=9.5 µA, Differential Input, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7935 MIN	SPT7935 TYP	SPT7935 MAX	UNITS
Dynamic Performance–Continued						
Signal-To-Noise and Distortion						
f_{IN} = 5 MHz		VI	57	61		dB
f_{IN} = 10 MHz		V		56		dB
Spurious Free Dynamic Range						
f_{IN} = 5.0 MHz		VI	62	70		dB
f_{IN} = 10.0 MHz		V		61		dB
Differential Phase		V		0.2		Degrees
Differential Gain		V		0.5		%
Digital Inputs						
Logic 1 Voltage		VI	80% V_{DD}			
Logic 0 Voltage		VI			20% V_{DD}	
Maximum Input Current Low	V_{IN} = GND	VI			±1	µA
Maximum Input Current High	V_{IN} = V_{DD}	VI			±1	µA
Input Capacitance		V		1.8		pF
Digital Outputs						
Logic 1 Voltage	I_O = -2 mA	VI	85% V_{DD}	95% V_{DD}		V
Logic 0 Voltage	I_O = +2 mA	VI		0.1	0.4	V
CLK to Output Delay Time (t_D)		IV	4	8	12	ns
Power Supply Requirements						
Supply Voltages						
V_{DD1}, V_{DD2}, V_{DD3}		IV	2.8	3.3	3.6	V
Supply Current						
I_{DD}		VI		24	30	mA
Power Dissipation		VI		79	100	mW
Power Supply Rejection Ratio (PSRR)		V		67		dB

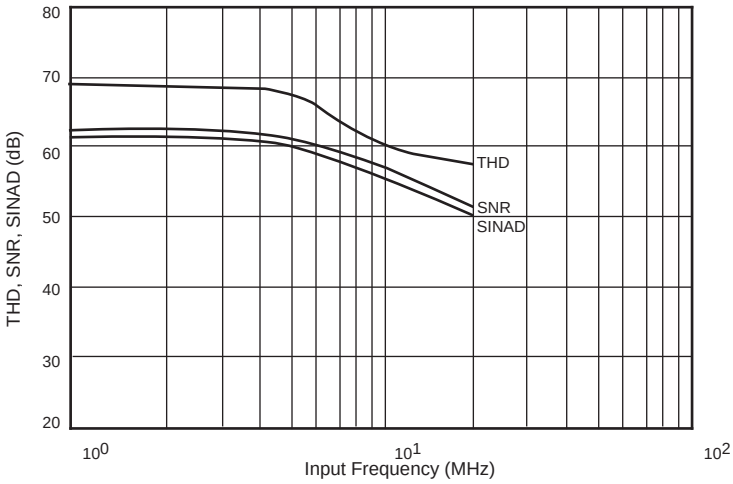
TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

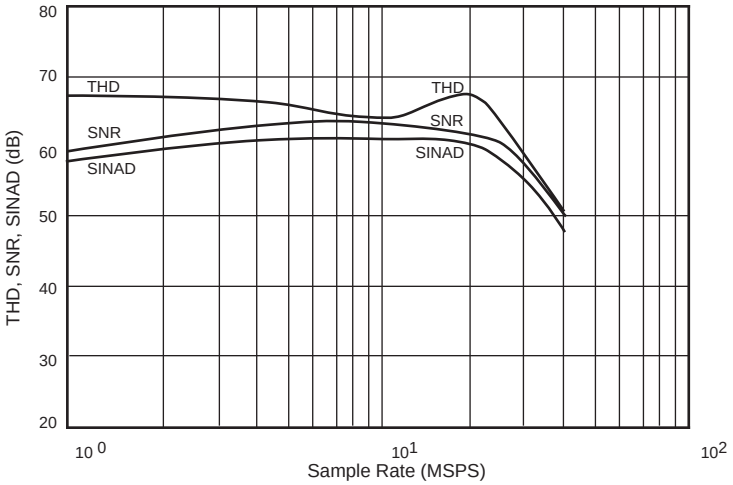
TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

THD, SNR, SINAD vs Input Frequency

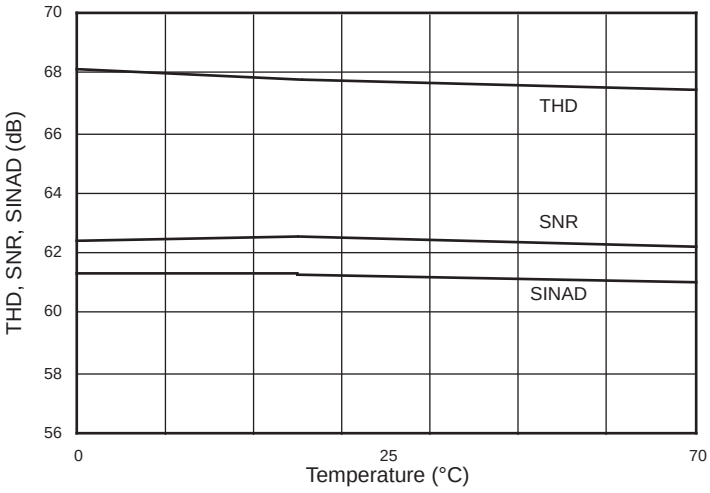


THD, SNR, SINAD vs Sample Rate

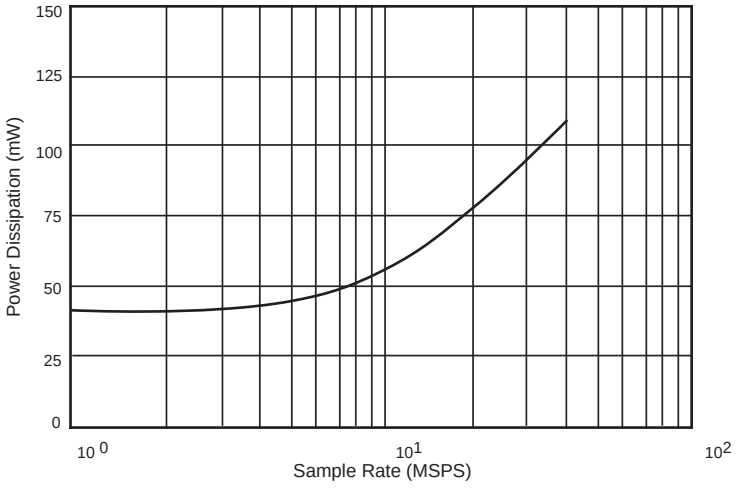


Note: Bias1 and Bias2 currents optimized for each sample rate.

THD, SNR, SINAD vs Temperature

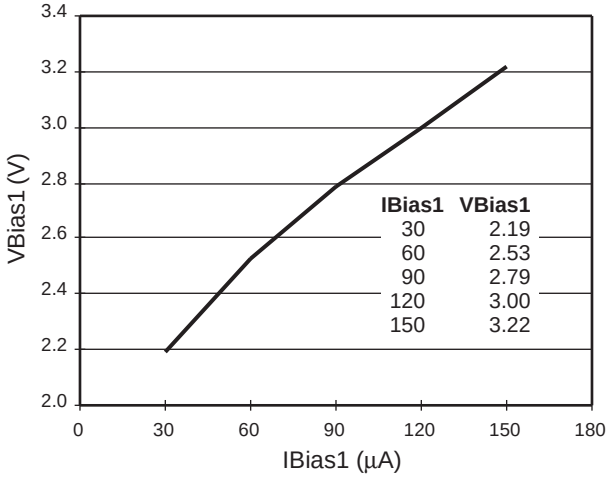


Power Dissipation vs Sample Rate



Note: Bias1 and Bias2 optimized for each sample rate.

Bias 1 Voltage vs Bias 1 Current



Bias 2 Voltage vs Bias 2 Current

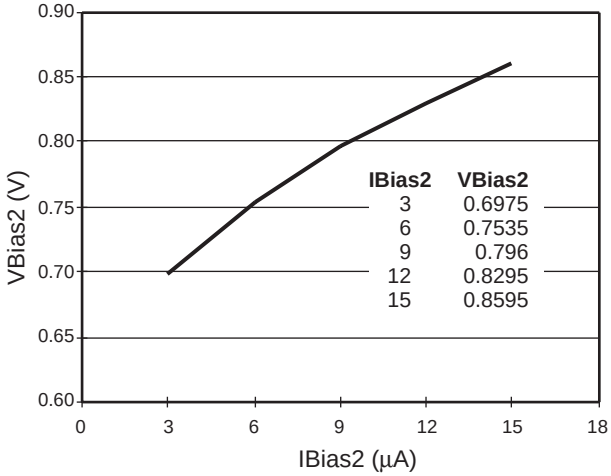
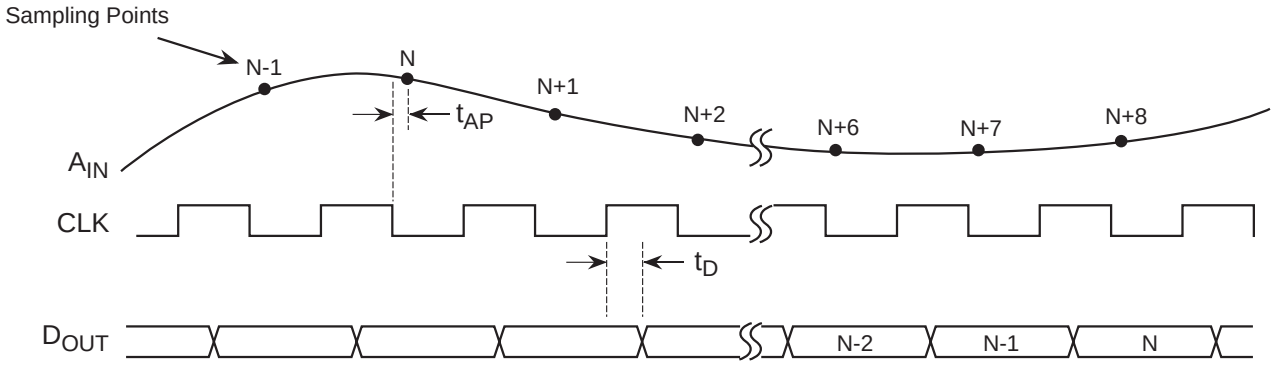


Figure 1 – Timing Diagram



GENERAL DESCRIPTION

The SPT7935 is an ultra-low power, 12-bit, 20 MSPS ADC. It has a pipelined architecture and incorporates digital error correction of the 11 most significant bits. This error correction ensures good linearity performance for input frequencies up to Nyquist. The inputs are fully differential, making the device insensitive to system-level noise. This device can also be used in a single-ended mode. (See analog input section.) With the power dissipation roughly proportional to the sampling rate, this device is ideal for very low power applications in the range of 1 to 20 MSPS.

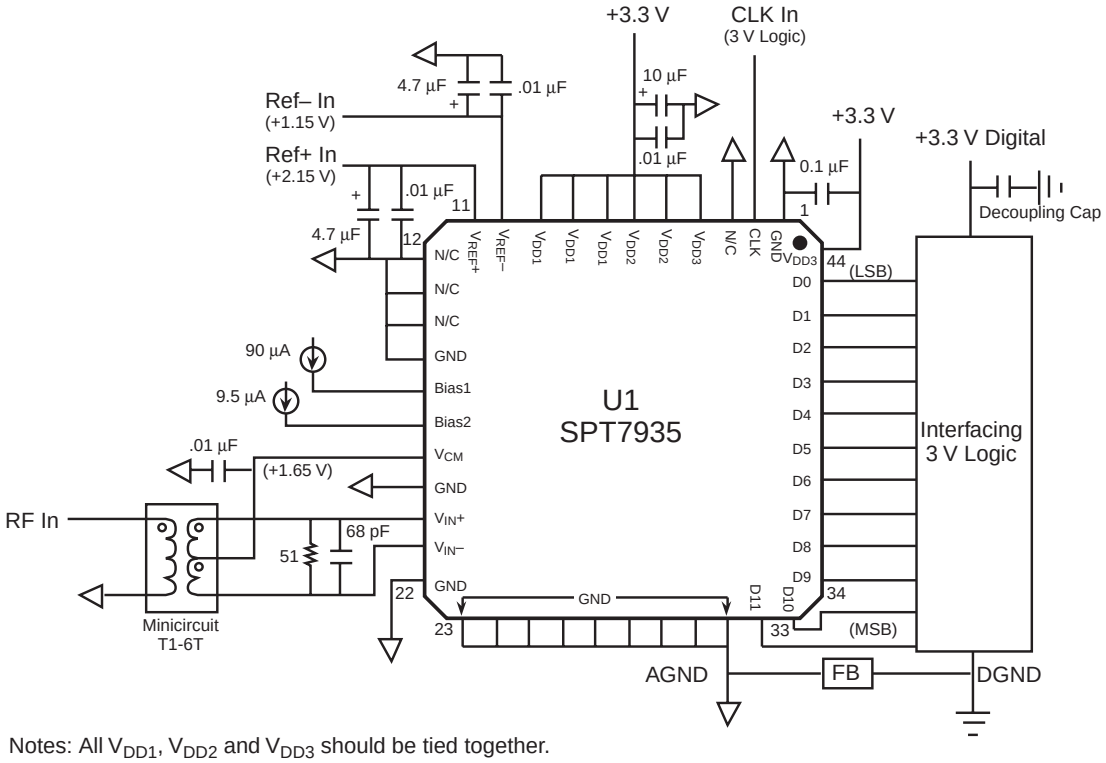
TYPICAL INTERFACE CIRCUIT

The SPT7935 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7935 in normal circuit operation. The following sections provide a description of the functions and outline critical performance criteria to consider for achieving the optimal device performance.

ANALOG INPUT

The input of the SPT7935 can be configured in various ways depending on if a single-ended or differential, AC- or DC-coupled input is desired.

Figure 2 – Typical Interface Circuit



Notes: All V_{DD1}, V_{DD2} and V_{DD3} should be tied together.
FB = Ferrite Bead; must be placed as close to U1 as possible.

The AC coupled input is most conveniently implemented using a transformer with a center tapped secondary winding. The center tap is connected to the V_{CM} pin as shown in figure 2. To obtain low distortion, it is important that the selected transformer does not exhibit core saturation at the full-scale voltage. Proper termination of the input is important for input signal purity. A small capacitor across the inputs attenuates kickback noise from the internal sample and hold.

Figure 3 illustrates a solution (based on operational amplifiers) that can be used if a DC coupled single-ended input is desired. The selection criteria of the buffer op-amps is as follows:

– Open loop gain >75 dB
– Gain bandwidth product >50 MHz
– Total harmonic distortion ≤–75 dB
– Signal to noise ratio >75 dB

POWER SUPPLIES AND GROUNDING

The SPT7935 is operated from a single power supply in the range of 2.8 to 3.6 volts. Nominal operation is suggested to be 3.3 volts. All power supply pins should be bypassed as close to the package as possible. The analog and digital grounds should be connected together with a ferrite bead as shown in the typical interface circuit and as close to the ADC as possible.

REFERENCES

The SPT7935 has a differential analog input. The voltages applied to the $V_{REF}+$ and $V_{REF}-$ pins determine the input voltage range and are equal to $\pm(V_{REF}+ - V_{REF}-)$. This voltage range will be symmetric about the common mode voltage. Externally generated reference voltages must be connected to these pins. (See figure 2, Typical Interface Circuit.) For best performance, these voltages should be symmetrical about the midpoint of the supply voltage.

COMMON MODE VOLTAGE REFERENCE CIRCUIT

The SPT7935 has an on-board common mode voltage reference circuit (V_{CM}). It is typically one-half of the supply voltage and can drive loads of up to 20 μA. This circuit is commonly used to drive the center tap of the RF transformer in fully differential applications. For single-ended applications, this output can be used to provide the level shifting required for the single-to-differential converter conversion circuit.

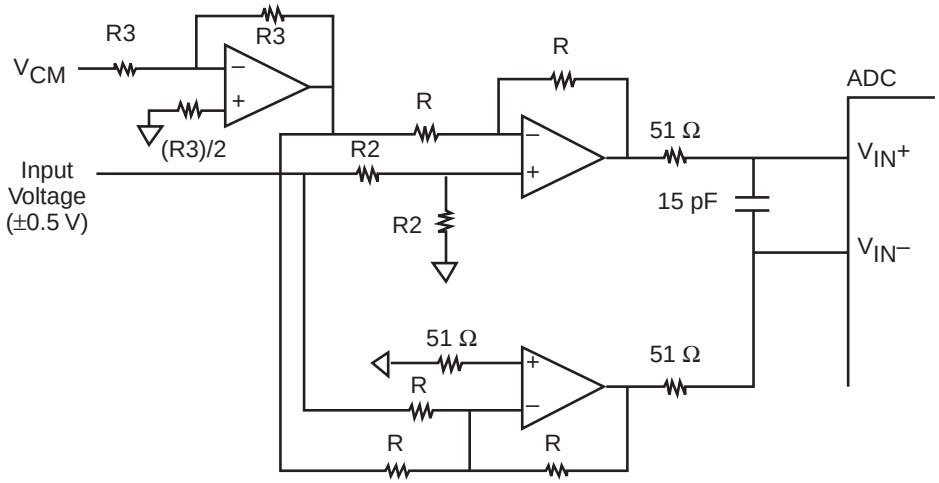
BIAS CURRENT CIRCUITS

The bias currents suggested (Bias 1 and Bias 2 in figure 2) optimize device performance for the stated sample rate of 20 MSPS. To achieve the best dynamic performance when operating the device at sample rates other than 20 MSPS, the bias current levels should be adjusted. Table I shows the settings for Bias 1 and Bias 2 for selected sample rates. The "Bias Voltage vs Bias Current" graphs on page 4 show the relationship between the bias current and the bias voltage.

Table I – Sample Rate Settings

Sample Rate (MHz)	Bias 1 (μA)	Bias 2 (μA)
1	20	3.5
5	50	6.5
10	80	8.0
20	90	9.5

Figure 3 – DC-Coupled Single Ended to Differential Conversion (Power Supplies and Bypassing are Not Shown)



CLOCK

The SPT7935 accepts a low voltage CMOS logic level at the CLK input. The duty cycle of the clock should be kept as close to 50% as possible. Because consecutive stages in the ADC are clocked in opposite phase to each other, a non-50% duty cycle reduces the settling time available for every other stage and thus potentially causing a degradation of dynamic performance.

For optimal performance at high input frequencies, the clock should have low jitter and fast edges. The rise/fall times should be kept shorter than 2 ns. Overshoot and undershoot should be avoided. Clock jitter causes the noise floor to rise proportional to the input frequency. Because jitter can be caused by crosstalk on the PC board, it is recommended that the clock trace be kept as short as possible and standard transmission line practices be followed.

DIGITAL OUTPUTS

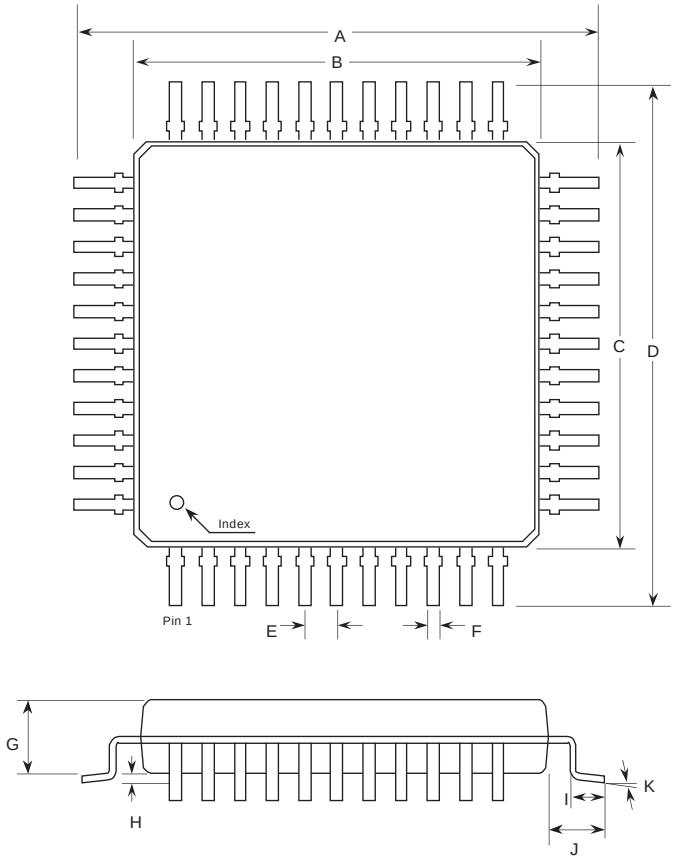
The digital output data appears in an offset binary code at 3.3 V CMOS logic levels. A negative full scale input results in an all zeros output code (000…0). A positive full scale input results in an all 1's code (111…1). The output data is available 7.5 clock cycles after the data is sampled. The input signal is sampled on the high to low transition of the input clock. Output data should be latched on the low to high clock transition as shown in figure 1, the Timing Diagram. The output data is invalid for the first 20 clock cycles after the device is powered up.

EVALUATION BOARD

The EB7935 Evaluation Board is available to aid designers in demonstrating the full performance capability of the SPT7935. The board includes an on-board clock driver, adjustable voltage references, adjustable bias current circuits, single-to-differential input buffers with adjustable levels, a single-to-differential transformer (1:1), digital output buffers and 3.3/5 V adjustable logic outputs. An application note (AN7935) is also available which describes the operation of the evaluation board and provides an example of the recommended power and ground layout and signal routing. Contact the factory for price and availability.

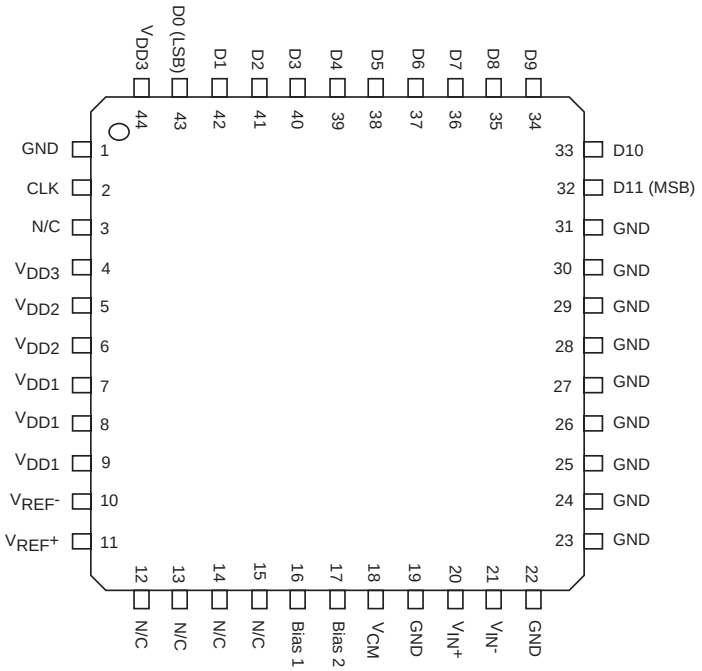
PACKAGE OUTLINE

44L TQFP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.472 Typ		12.00 Typ	
B	0.394 Typ		10.00 Typ	
C	0.394 Typ		10.00 Typ	
D	0.472 Typ		12.00 Typ	
E	0.031 Typ		0.80 Typ	
F	0.012	0.018	0.300	0.45
G	0.053	0.057	1.35	1.45
H	0.002	0.006	0.05	0.15
I	0.018	0.030	0.450	0.750
J	0.039 Typ		1.00 Typ	
K	0-7°		0-7°	

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
$V_{IN}+$, $V_{IN}-$	Analog Inputs
$V_{REF}+$, $V_{REF}-$	External Reference Inputs
CLK	Input Clock
V_{CM}	Common Mode Output Voltage (1.65 V typ)
Bias 1	Bias Current (90 µA typ)
Bias 2	Bias Current (9.5 µA typ)
D0 – D11	Digital Outputs (D0 = LSB)
GND	Analog Ground
V_{DD_1} V_{DD_2} V_{DD_3}	Analog Power Supply Digital Power Supply Digital Output Power Supply
N/C	No Connect Pins. Recommended to connect to analog ground.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7935SIT	–40 to +85 °C	44L TQFP

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