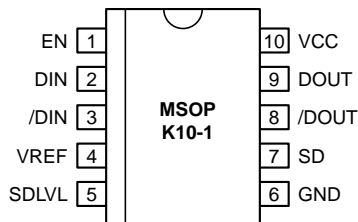


## FEATURES

- 3.3V and 5V power supply options
- Up to 2.5Gbps operation
- Low noise
- Chatter-free signal detect (SD) generation
- Open collector TTL signal detect (SD) output
- TTL EN input
- Differential PECL inputs for data
- Single power supply
- Designed for use with Micrel-Synergy laser diode driver and controller
- Available in a tiny (3mm) 10-pin MSOP

## PIN CONFIGURATION



## DESCRIPTION

The SY88943V limiting post amplifier with its high gain and wide bandwidth is ideal for use as a post amplifier in fiber-optic receivers with data rates up to 2.5Gbps. Signals as small as 5mVp-p can be amplified to drive devices with PECL inputs. The SY88943V generates a chatter-free Signal Detect (SD) open collector TTL output.

The SY88943V incorporates a programmable level detect function to identify when the input signal has been lost. The SD output will change from logic "HIGH" to logic "LOW" when input signal is smaller than the swing set by  $SD_{LVL}$ . This information can be fed back to the EN input of the device to maintain stability under loss of signal condition. Using  $SD_{LVL}$  pin, the sensitivity of the level detection can be adjusted. The  $SD_{LVL}$  voltage can be set by connecting a resistor divider between  $V_{CC}$  and  $V_{REF}$  as shown in Figure 3. Figure 4, 5, 6, and 7 show the relationship between input level sensitivity and the voltage set on  $SD_{LVL}$ .

The SD output is a TTL open collector output that requires a pull-up resistor for proper operation, Figure 1.

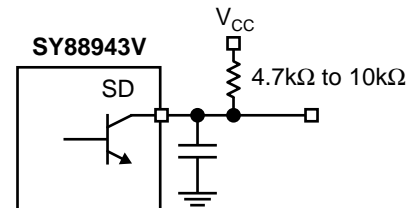
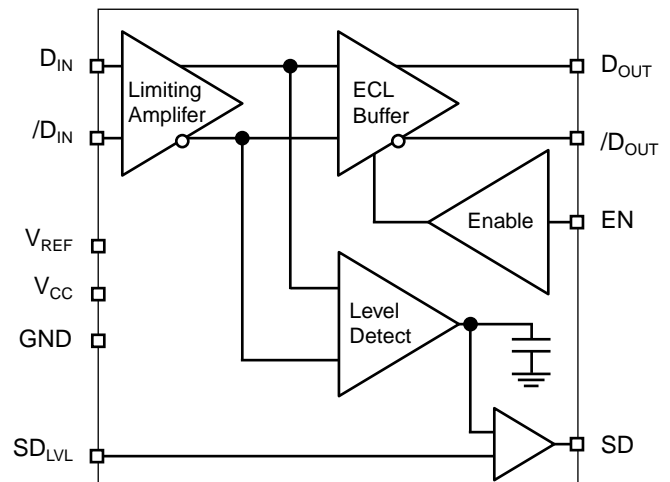


Figure 1. SD Output with Desired Rise Time

## APPLICATIONS

- 1.25Gbps and 2.5Gbps ethernet
- 531Mbps, 1062Mbps and 2.12Gbps Fibre Channel
- 622Mbps SONET
- Gigabit interface converter
- 2.5Gbps SDH/SONET
- 2.5Gbps proprietary links

## BLOCK DIAGRAM



**PIN NAMES**

Pin	Type	Function
D <sub>IN</sub>	Data Input	Data Input
/D <sub>IN</sub>	Data Input	Inverting Data Input
SD <sub>LVL</sub>	Input	SD Level Set
EN	TTL Input	Output Enable (Active High)
SD	TTL Output (Open Collector)	Signal Detect
GND	Ground	Ground
/D <sub>OUT</sub>	PECL Output	Inverting Data Output
D <sub>OUT</sub>	PECL Output	Data Output
V <sub>CC</sub>	Power Supply	Positive Power Supply
V <sub>REF</sub>	Output	Reference Voltage Output for SD Level Set (see Fig. 3)

**GENERAL DESCRIPTION****General**

The SY88943V is an integrated limiting amplifier intended for high-frequency fiber-optic applications. The circuit connects to typical transimpedance amplifiers found within a fiber-optics link. The linear signal output from a transimpedance amplifier can contain significant amounts of noise, and may vary in amplitude over time. The SY88943V limiting amplifier quantizes the signal and outputs a voltage-limited waveform.

The EN pin allows the user to disable the output signal without removing the input signal.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
V <sub>CC</sub>	Power Supply Voltage	0 to +7.0	V
D <sub>IN</sub> , /D <sub>IN</sub>	Input Voltage	0 to V <sub>CC</sub>	V
D <sub>OUT</sub> , /D <sub>OUT</sub>	Output Voltage (with 50Ω load)	V <sub>CC</sub> -2.5 to V <sub>CC</sub> +0.3	V
EN	Input Voltage	0 to V <sub>CC</sub>	V
SD <sub>LVL</sub>	Input Voltage	0 to V <sub>CC</sub>	V
V <sub>REF</sub>	Output Voltage	V <sub>CC</sub> -2.0 to V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>store</sub>	Storage Temperature Range	-55 to +125	°C

**NOTE:**

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS**

$V_{CC} = +5V \pm 10\%$ ,  $R_{LOAD} = 50\Omega$  to  $V_{CC} - 2V$

Symbol	Parameter	$T_A = -40^\circ C$		$T_A = 0^\circ C$		$T_A = +25^\circ C$			$T_A = +85^\circ C$		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
$I_{CC}$	Power Supply Current <sup>(1)</sup>	—	40	—	40	—	33	40	—	45	mA
	5V	—	40	—	40	—	28	40	—	45	
$I_{IL}$	EN Input LOW Current	-0.3 <sup>(6)</sup>	—	-0.3 <sup>(6)</sup>	—	-0.3 <sup>(6)</sup>	—	—	-0.3 <sup>(6)</sup>	—	mA
$I_{IH}$	EN Input HIGH Current	—	20 <sup>(4)</sup>	—	20 <sup>(4)</sup>	—	—	20 <sup>(4)</sup>	—	20 <sup>(4)</sup>	$\mu A$
		—	100 <sup>(5)</sup>	—	100 <sup>(5)</sup>	—	—	100 <sup>(5)</sup>	—	100 <sup>(5)</sup>	
$V_{CMR}$	Common Mode Range	GND +2.0	$V_{CC}$	GND +2.0	$V_{CC}$	GND +2.0	—	$V_{CC}$	GND +2.0	$V_{CC}$	V
$V_{offset}$	Differential Output Offset	—	$\pm 100$	—	$\pm 100$	—	$\pm 17$	$\pm 100$	—	$\pm 100$	mV
$SD_{LVL}$	$SD_{LVL}$ Level	$V_{REF}$	$V_{CC}$	$V_{REF}$	$V_{CC}$	$V_{REF}$	—	$V_{CC}$	$V_{REF}$	$V_{CC}$	V
$V_{OL}$	SD Output Low Level <sup>(2)</sup>	—	0.5	—	0.5	—	—	0.5	—	0.5	V
$I_{OH}$	SD Output Leakage <sup>(3)</sup>	—	100	—	100	—	—	100	—	100	$\mu A$
$V_{OH}$	$D_{OUT}$ and $/D_{OUT}$ HIGH Output	$V_{CC} - 1085$	$V_{CC} - 880$	$V_{CC} - 1025$	$V_{CC} - 880$	$V_{CC} - 1025$	$V_{CC} - 955$	$V_{CC} - 880$	$V_{CC} - 1025$	$V_{CC} - 880$	mV
$V_{OL}$	$D_{OUT}$ and $/D_{OUT}$ LOW Output	$V_{CC} - 1830$	$V_{CC} - 1555$	$V_{CC} - 1810$	$V_{CC} - 1620$	$V_{CC} - 1810$	$V_{CC} - 1705$	$V_{CC} - 1620$	$V_{CC} - 1810$	$V_{CC} - 1620$	mV
$V_{REF}$	Reference Supply	$V_{CC} - 1.38$	$V_{CC} - 1.26$	$V_{CC} - 1.38$	$V_{CC} - 1.26$	$V_{CC} - 1.38$	$V_{CC} - 1.32$	$V_{CC} - 1.26$	$V_{CC} - 1.38$	$V_{CC} - 1.26$	V
$I_{REF}$	$V_{REF}$ Output Current	-0.8	0.5	-0.8	0.5	-0.8	—	0.5	-0.8	0.5	mA
$V_{IH}$	EN Input HIGH Voltage	2.0	—	2.0	—	2.0	—	—	2.0	—	V
$V_{IL}$	EN Input LOW Voltage	—	0.8	—	0.8	—	—	0.8	—	0.8	V

**NOTES:**

1. No output load
2.  $I_{OL} = + 2mA$
3.  $V_{OH} = 5.5V$

4.  $V_{IN} = 2.7V$
5.  $V_{IN} = V_{CC}$
6.  $V_{IN} = 0.5V$

**AC ELECTRICAL CHARACTERISTICS**

$V_{CC} = +5V \pm 10\%$ ,  $R_{LOAD} = 50\Omega$  to  $V_{CC} - 2V$

Symbol	Parameter	$T_A = -40^\circ C$		$T_A = 0^\circ C$		$T_A = +25^\circ C$			$T_A = +85^\circ C$		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
PSRR	Power Supply <sup>(1)</sup> Rejection Ratio	—	—	—	—	—	35	—	—	—	dB	Input referred, 55MHz
$V_{ID}$	Input Voltage Range	5	1800	5	1800	5	—	1800	5	1800	mVp-p	
$V_{OD}$	Differential Output Voltage Swing <sup>(2)</sup>	—	—	—	—	—	700	—	—	—	mV	$V_{ID} = 15mVp-p$ $V_{ID} = 5mVp-p$
		—	—	—	—	—	300	—	—	—	mV	
$t_{ONL}$	SD Release Time <sup>(3)</sup> Minimum Input	—	0.5	—	0.5	—	0.2	0.5	—	0.5	$\mu s$	
$t_{ONH}$	SD Release Time <sup>(4)</sup> Maximum Input	—	0.5	—	0.5	—	0.2	0.5	—	0.5	$\mu s$	
$t_{OFFL}$	SD Assert Time <sup>(3)</sup>	—	0.5	—	0.5	—	0.1	0.5	—	0.5	$\mu s$	
$V_{SR}$	SD Sensitivity Range	5	50	5	50	5	—	50	5	50	MVp-p	2 <sup>23</sup> -1 pattern
HYS	SD Hysteresis	2	8	2	8	2	4.6	8	2	8	dB	2 <sup>23</sup> -1 pattern
$t_r, t_f$	Output Rise/Fall Time	—	175	—	175	—	150	175	—	175	ps	$V_{ID} > 100mVp-p$ $V_{ID} < 100mVp-p$
		—	—	—	—	—	$t_{rin}, t_{fin}$	—	—	—		

**NOTES:**

1. Input referred noise = RMS output noise/low frequency gain.
2. Input is a 622MHz square wave.

3. Input is a 200MHz square wave,  $t_r < 300ps$ , 8mVp-p.
4. Input is a 200MHz square wave,  $t_r < 300ps$ , 1.8Vp-p.

**DESIGN PROCEDURE**

**Output Termination**

The SY88943V outputs must be terminated with a 50Ω load to V<sub>CC</sub> -2V (or Thevenin equivalent).

**Layout and PCB Design**

Since the SY88943V is a high-frequency component, performance can be largely determined by the board layout and design. A common problem with high-gain amplifiers is the feedback from the large swing outputs to the input via the power supply.

The SY88943V ground pin should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

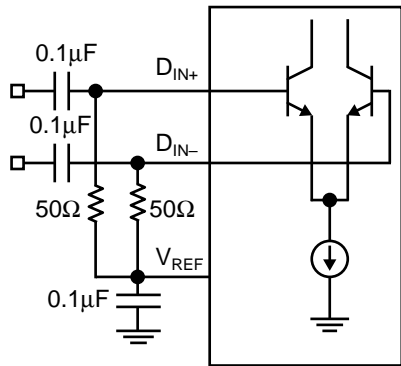


Figure 2. Differential Input Configuration

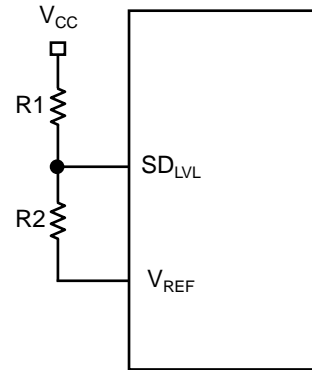


Figure 3. SD<sub>LVL</sub> Circuit

**NOTES:**

$$SD_{LVL} = V_{CC} - 1.32V + \frac{R2 \times 1.32V}{R1 + R2}$$

$$R1 + R2 \geq 2.6k\Omega$$

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY88943VKC	K10-1	Commercial
SY88943VKCTR	K10-1	Commercial

**PERFORMANCE CURVE**

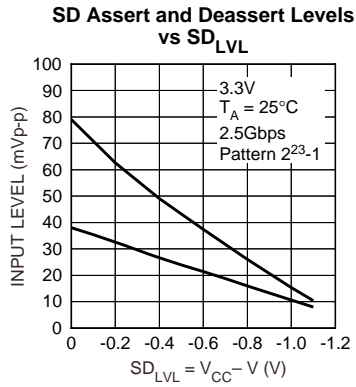


Figure 4.

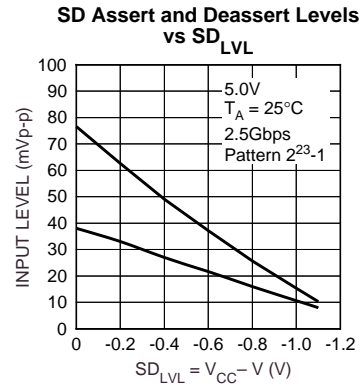


Figure 5.

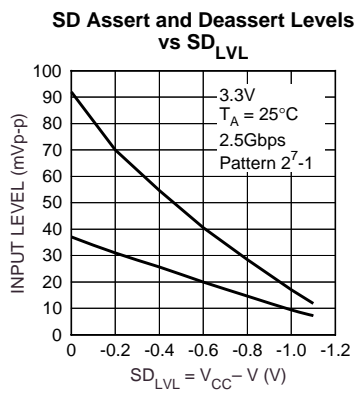


Figure 6.

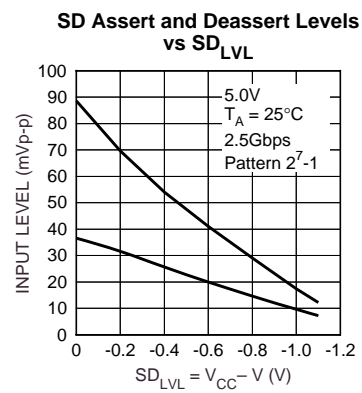
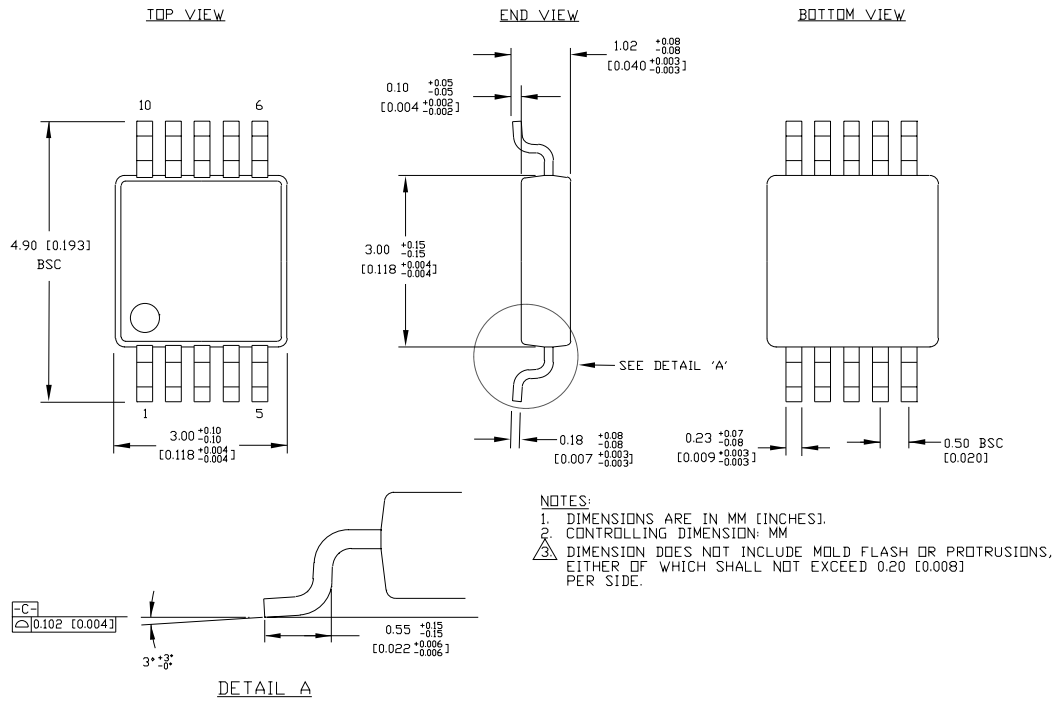


Figure 7.

**10 LEAD MSOP (K10-1)**



Rev. 00



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