TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT   SILICON MONOLITHIC

# T6B20

# DOT MATRIX LCD CONTROLLER AND DRIVER LSI

The T6B20 is a dot matrix LCD controller and driver. The T6B20 realizes low power consumption for an LCD system using CMOS Si-gate technology.

The T6B20 can display alphanumerics, kana and symbols corresponding to serial data received from an MPU.

The T6B20 has all the functions to drive a dot matrix LCD. Therefore, the T6B20 can constitute a minimal LCD drive and control system.

The T6B20 can drive the display of up to 80 characters by using an expansion driver (e.g. T6B23). The T6B20 has an 8×8 key matrix driver and 16 LED drivers (a 2×8 matrix).



QFP100-P-1420-0.65J
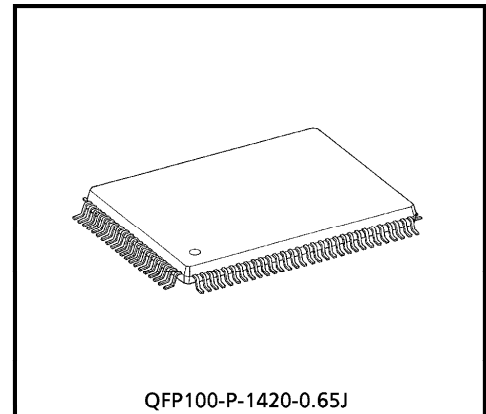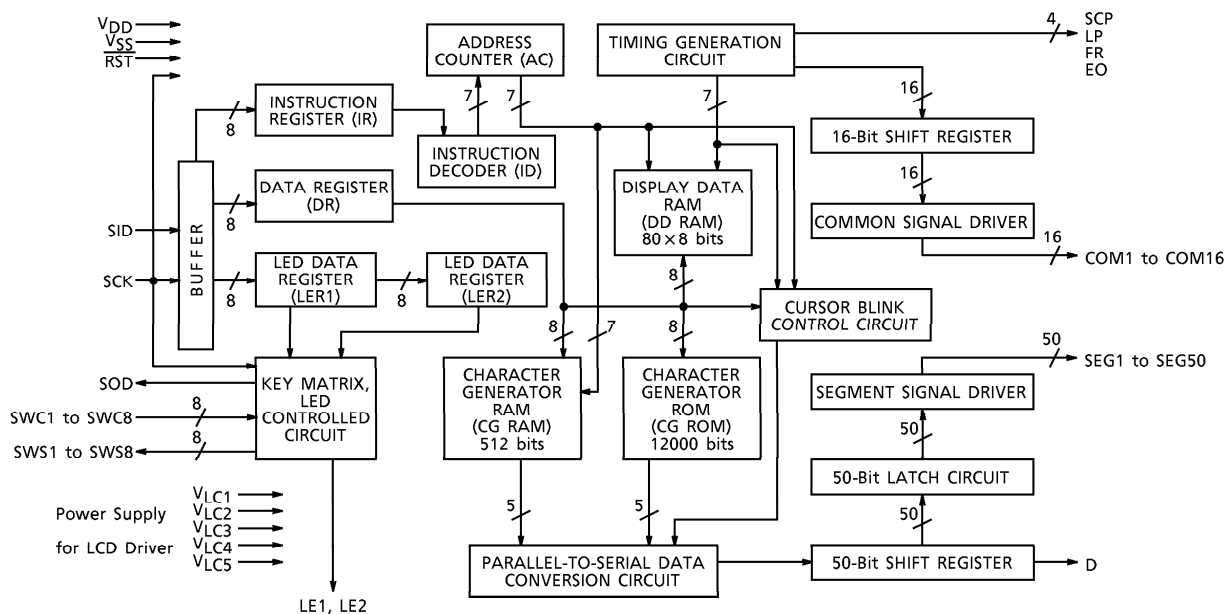
**Weight: 1.6g (typ.)**

## FEATURES

- Built-in controller for character-type LCD (character fonts: 5×7, 5×10)

- Direct interface with MPU (serial interface)

- Data transfer clock         : $f_{osc} = 250kHz$ typ

- Display data RAM         : 80×8 bits

- Character generator ROM : 12000 bits

- Character generator RAM : 512 bits

- Built-in key matrix scan controller

- Built-in 2×8 LED controller (buffer not built-in)

- Built-in LCD drivers
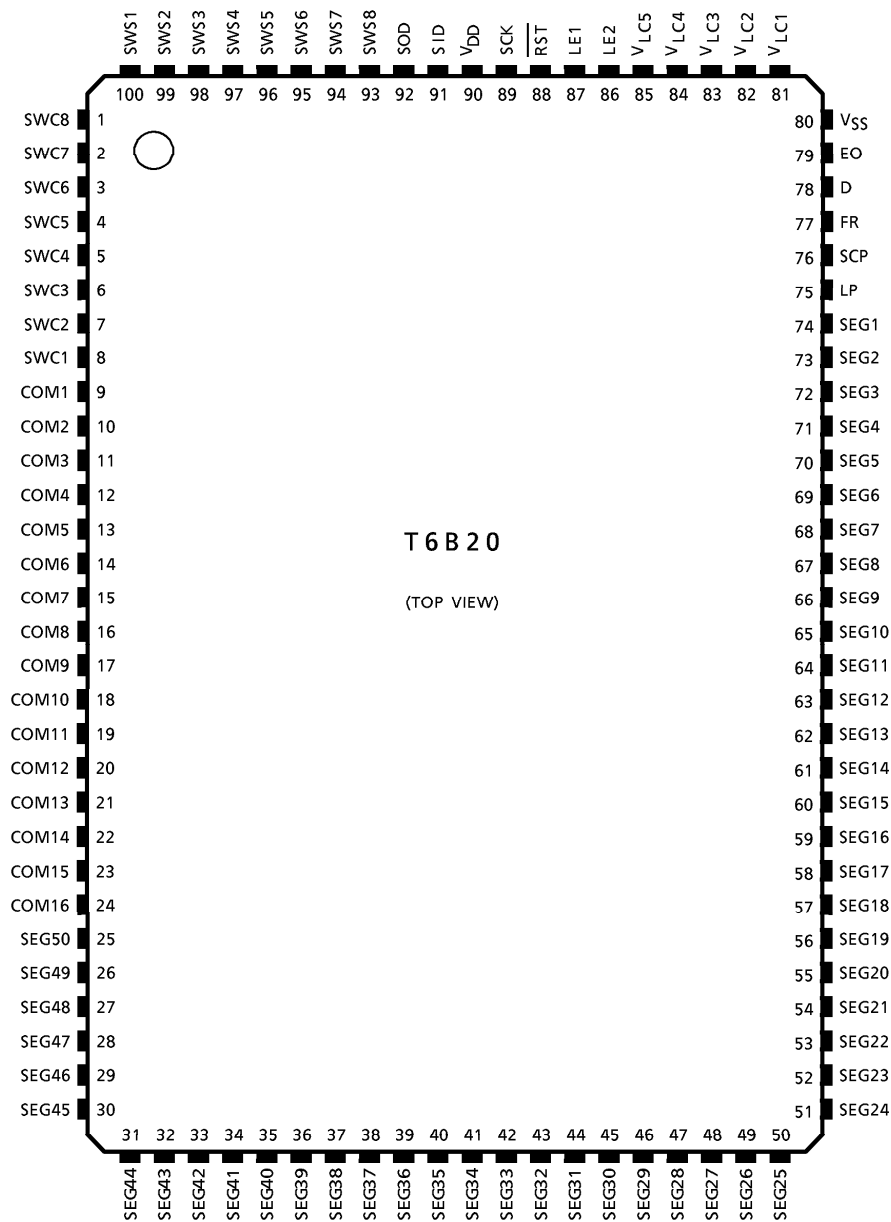
  50-output column driver
  16-output row driver

- Duty factor selection (programmable)

  1 / 8 duty cycle   : (Font : 5 × 7 dots + cursor) × 1 line
  1 / 11 duty cycle  : (Font : 5 × 10 dots + cursor) × 1 line
  1 / 16 duty cycle  : (Font : 5 × 7 dots + cursor) × 2 lines

- Applications

  Display clear, Cursor home, Display ON / OFF, Cursor ON / OFF
  Character blink, Character shift, Display shift, Cursor shift

- Power supply     : 5V ± 10%

- Low power consumption

- 100-pin Flat Plastic Package

## BLOCK DIAGRAM

## PIN ASSIGNMENT



Top row pins (left to right): SWS1 (100), SWS2 (99), SWS3 (98), SWS4 (97), SWS5 (96), SWS6 (95), SWS7 (94), SWS8 (93), SOD (92), SID (91), $V_{DD}$ (90), SCK (89), $\overline{RST}$ (88), LE1 (87), LE2 (86), $V_{LC5}$ (85), $V_{LC4}$ (84), $V_{LC3}$ (83), $V_{LC2}$ (82), $V_{LC1}$ (81)

Left column pins (top to bottom):

| Pin | No. |
|---|---|
| SWC8 | 1 |
| SWC7 | 2 |
| SWC6 | 3 |
| SWC5 | 4 |
| SWC4 | 5 |
| SWC3 | 6 |
| SWC2 | 7 |
| SWC1 | 8 |
| COM1 | 9 |
| COM2 | 10 |
| COM3 | 11 |
| COM4 | 12 |
| COM5 | 13 |
| COM6 | 14 |
| COM7 | 15 |
| COM8 | 16 |
| COM9 | 17 |
| COM10 | 18 |
| COM11 | 19 |
| COM12 | 20 |
| COM13 | 21 |
| COM14 | 22 |
| COM15 | 23 |
| COM16 | 24 |
| SEG50 | 25 |
| SEG49 | 26 |
| SEG48 | 27 |
| SEG47 | 28 |
| SEG46 | 29 |
| SEG45 | 30 |

T6B20 (TOP VIEW)

Right column pins (top to bottom):

| No. | Pin |
|---|---|
| 80 | $V_{SS}$ |
| 79 | EO |
| 78 | D |
| 77 | FR |
| 76 | SCP |
| 75 | LP |
| 74 | SEG1 |
| 73 | SEG2 |
| 72 | SEG3 |
| 71 | SEG4 |
| 70 | SEG5 |
| 69 | SEG6 |
| 68 | SEG7 |
| 67 | SEG8 |
| 66 | SEG9 |
| 65 | SEG10 |
| 64 | SEG11 |
| 63 | SEG12 |
| 62 | SEG13 |
| 61 | SEG14 |
| 60 | SEG15 |
| 59 | SEG16 |
| 58 | SEG17 |
| 57 | SEG18 |
| 56 | SEG19 |
| 55 | SEG20 |
| 54 | SEG21 |
| 53 | SEG22 |
| 52 | SEG23 |
| 51 | SEG24 |

Bottom row pins (left to right): SEG44 (31), SEG43 (32), SEG42 (33), SEG41 (34), SEG40 (35), SEG39 (36), SEG38 (37), SEG37 (38), SEG36 (39), SEG35 (40), SEG34 (41), SEG33 (42), SEG32 (43), SEG31 (44), SEG30 (45), SEG29 (46), SEG28 (47), SEG27 (48), SEG26 (49), SEG25 (50)

**PIN FUNCTIONS**

| SYMBOL | PIN No. | TYPE | NAME AND FUNCTION |
|---|---|---|---|
| SCK | 89 | Input | System Clock |
| SID | 91 | Input | Serial data input |
| SOD | 92 | Output | Serial data output |
| SWC1 to SWC8 | 1 to 8 | Input | Key matrix inputs |
| SWS1 to SWS8 | 93 to 100 | Output | Key matrix outputs |
| LP | 75 | Output | Latch Pulse : Latch pulse for the extension driver (e.g. T6B23) |
| SCP | 76 | Output | Shift Clock Pulse : Shift Clock Pulse for the extension driver (e.g. T6B23) |
| FR | 77 | Output | Frame signal : FR signal for the extension driver (e.g. T6B23) |
| D | 78 | Output | Data : Display data for the extension driver (e.g. T6B23) |
| EO | 79 | Output | Enable Output : Enable signal for the extension driver (e.g. T6B23) |
| COM1 to COM16 | 9 to 24 | Output | Common : Row outputs<br>When 1 / 8 duty cycle is selected, COM9 to COM16 are disabled.<br>When 1 / 11 duty cycle is selected, COM12 to COM16 are disabled. |
| SEG1 to SEG50 | 25 to 74 | Output | Segment : Column outputs. |
| $V_{LC5}$ | 85 | Input | Power supply for LCD drive |
| $V_{LC1}$ to $V_{LC4}$ | 81 to 84 | Input | Power supply for LCD drive |
| $V_{DD}$, $V_{SS}$ | 90, 80 | Input | Power supply and ground pins<br>$V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$ |
| $\overline{RST}$ | 88 | Input | Reset : $\overline{RST} = L \rightarrow$ Reset state |
| LE1, LE2 | 86, 87 | Output | LED Enable outputs |

## FUNCTIONAL DESCRIPTION OF EACH BLOCK

● Registers

The T6B20 has four 8-bit registers. The registers are the Instruction Register (IR), the Data Register (DR), and two LED control data registers (LER1, LER2).
The IR holds an instruction code, a DD RAM address data, or a CG RAM address data.
The DR temporarily holds the data that is to be written into the DD RAM or the CG RAM.
The data in DR are automatically written into the DD RAM or the CG RAM.
The LE1 and LE2 hold the data for controlling the LED.
The relation between the Register Select (RS1, RS2) signals and the selected operation is shown in Fig. 1.

| RS1 | RS2 | OPERATION |
|-----|-----|-----------|
| 0 | 0 | Write into IR |
| 0 | 1 | Write into DR |
| 1 | 0 | Write into LER1 |
| 1 | 1 | Write into LER2 |

Fig. 1

● Address Counter (AC)

The T6B20 has a 7-bit Address Counter. The Address Counter points to an address in DD RAM or CG RAM, or to the cursor position. The Set DD RAM Address or Set CG RAM Address instruction specifies which type of Address Counter contains. The Address Counter is automatically incremented (or decremented) after the data has been written into RAM.

● Display data RAM (DD RAM)

The display data RAM stores display data as 8-bit character codes.
Its capacity is 80 characters × 8 bits. The relation between the DD RAM address and the display position is as shown below.
The DD RAM address corresponds to a HEX code as shown in Fig. 2.

```
     MSB                    LSB
AC  | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
```

Example : When DD RAM address = 4CH

```
     MSB                         LSB
    | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
     \___ 4 ___/\___ C ___/
```
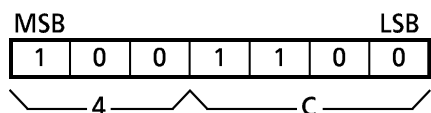
Fig. 2

(1)     The relation between the DD RAM address and the display position in 1-Line Display mode
        (N = 0)

```
        1   2   3   4   5                       79  80  ← Display position
      ┌──┬──┬──┬──┬──┬────────────────┬──┬──┐
      │00│01│02│03│04│ ------------- │4E│4F│ ← DD RAM address
      └──┴──┴──┴──┴──┴────────────────┴──┴──┘
```

a) Using one T6B20, the first ten characters are displayed as shown below.

```
        1   2   3   4   5   6   7   8   9   10
      ┌──┬──┬──┬──┬──┬──┬──┬──┬──┬──┐
      │00│01│02│03│04│05│06│07│08│09│
      └──┴──┴──┴──┴──┴──┴──┴──┴──┴──┘
```

b) When a Display Shift operation is executed, the relation between the DD RAM address
   and the display position is as shown below.

```
                        1   2   3   4   5   6   7   8   9   10
Left shift display    │01│02│03│04│05│06│07│08│09│0A│
```

```
                        1   2   3   4   5   6   7   8   9   10
Right shift display   │4F│00│01│02│03│04│05│06│07│08│
```

(2)     The relation between the DD RAM address and the display position in 2-Line Display mode
        (N = 1)

```
                    1   2   3   4               39  40  ← Display position
1st line        │00│01│02│03│ ----------- │26│27│
                                                    ← DD RAM address
2nd line        │40│41│42│43│ ----------- │66│67│
```

      (Note) The DD RAM address of the 2nd line is not the next address after the last
             address on the 1st line.

a) Using one T6B20, the first 20 characters (10 characters × 2 lines) are displayed as shown
   below.

```
                    1   2   3   4   5   6   7   8   9   10
1st line        │00│01│02│03│04│05│06│07│08│09│
2nd line        │40│41│42│43│44│45│46│47│48│49│
```

b) When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.

Left shift display

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|----|----|----|----|----|----|----|----|----|----|
| 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A |
| 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A |

Right shift display

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|----|----|----|----|----|----|----|----|----|----|
| 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 |
| 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |

● Character generator ROM (CG ROM)

The character generator ROM is used to generate the $5 \times 10$-dot character patterns (for 240 characters) from the 8-bit character codes. The relation between the character codes and character patterns is as shown overleaf.

THE RELATION BETWEEN CHARACTER CODES AND CHARACTER PATTERN

| HIGHER 4 BITS / LOWER 4 BITS | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| XXXX0000 | CGRAM (0) | | | | | | | | | | | | | | | |
| XXXX0001 | (1) | | | | | | | | | | | | | | | |
| XXXX0010 | (2) | | | | | | | | | | | | | | | |
| XXXX0011 | (3) | | | | | | | | | | | | | | | |
| XXXX0100 | (4) | | | | | | | | | | | | | | | |
| XXXX0101 | (5) | | | | | | | | | | | | | | | |
| XXXX0110 | (6) | | | | | | | | | | | | | | | |
| XXXX0111 | (7) | | | | | | | | | | | | | | | |
| XXXX1000 | (0) | | | | | | | | | | | | | | | |
| XXXX1001 | (1) | | | | | | | | | | | | | | | |
| XXXX1010 | (2) | | | | | | | | | | | | | | | |
| XXXX1011 | (3) | | | | | | | | | | | | | | | |
| XXXX1100 | (4) | | | | | | | | | | | | | | | |
| XXXX1101 | (5) | | | | | | | | | | | | | | | |
| XXXX1110 | (6) | | | | | | | | | | | | | | | |
| XXXX1111 | (7) | | | | | | | | | | | | | | | |

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● Character generator RAM (CG RAM)

The character generator RAM is used to display the user's original character patterns.
(5×7 dots×8 types or 5×10 dots×4 types)
The relation between the character codes and the CG RAM address and character patterns is as shown in Fig. 3 and Fig. 4.

(1) For 5×7-dot character patterns

| CHARACTER CODES (DD RAM DATA) | | CG RAM ADDRESS | CHARACTER PATTERNS (CG RAM DATA) | |
|---|---|---|---|---|
| 7 6 5 4 3 2 1 0 | | 5 4 3 / 2 1 0 | 7 6 5 / 4 3 2 1 0 | |
| 0 0 0 0 * 0 0 0 | | 0 0 0 / 0 0 0 | * * * / 1 1 1 1 0 | Character Pattern Example (1) |
| | | 0 0 1 | / 1 0 0 0 1 | |
| | | 0 1 0 | / 1 0 0 0 1 | |
| | | 0 1 1 | / 1 1 1 1 0 | |
| | | 1 0 0 | / 1 0 0 0 1 | |
| | | 1 0 1 | / 1 0 0 0 1 | |
| | | 1 1 0 | / 1 1 1 1 0 | |
| | | 1 1 1 | * * * / 0 0 0 0 0 | ← Cursor Position |
| 0 0 0 0 * 0 0 1 | | 0 0 1 / 0 0 0 | * * * / 0 1 1 1 1 | Character Pattern Example (2) |
| | | 0 0 1 | / 1 0 0 0 0 | |
| | | 0 1 0 | / 1 0 0 0 0 | |
| | | 0 1 1 | / 0 1 1 1 0 | |
| | | 1 0 0 | / 0 0 0 0 1 | |
| | | 1 0 1 | / 0 0 0 0 1 | |
| | | 1 1 0 | / 1 1 1 1 0 | |
| | | 1 1 1 | * * * / 0 0 0 0 0 | ← Cursor Position |
| | | 0 0 0 | * * * / 1 1 1 1 1 | |
| | | 0 0 1 | / 0 0 1 0 0 | |
| 0 0 0 0 * 1 1 1 | | 1 1 1 / 0 1 1 | / 0 0 1 0 0 | Fig. 3 |
| | | 1 0 0 | / 0 0 1 0 0 | |
| | | 1 0 1 | / 0 0 1 0 0 | |
| | | 1 1 0 | / 0 0 1 0 0 | |
| | | 1 1 1 | * * * / 0 0 0 0 0 | * : Invalid |

(Note 1)  Character code bit 0 to bit 2 correspond to CG RAM address bit 3 to bit 5.

(Note 2)  Bit 0 to bit 2 of the CG RAM address indicate the row within the character bit map. The 8th row (the bottom row) corresponds to the cursor position on the LCD display. Normally the 8th row should be blank (all 0s), otherwise the lowest line of the character will be obscured when used with the cursor.

(Note 3)  Character pattern line positions correspond to CG RAM data bit 0 to bit 4. CG RAM data bit 5 to bit 7 is not used for display; the data can be used for general RAM data.

(Note 4)  If bit 4 to bit 7 are all 0, a CG RAM character is indicated. The value of bit 3 does not matter. Character codes 00H and 08H select the same character.

(Note 5)  1 : ON, 0 : OFF

(2) For 5×10-dot character patterns

| CHARACTER CODES (DD RAM DATA) | | | | | | | | | CG RAM ADDRESS | | | | | | | CHARACTER PATTERNS (CG RAM DATA) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | 5 | 4 | 3 | 2 | 1 | 0 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | | | | | | | | 0 | 0 | 0 | 0 | | * | * | * | 0 | 0 | 0 | 1 | 0 |
| | | | | | | | | | | | 0 | 0 | 0 | 1 | | | | | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | | | 0 | 0 | 1 | 0 | | | | | 0 | 0 | 1 | 1 | 0 |
| | | | | | | | | | | | 0 | 0 | 1 | 1 | | | | | 0 | 0 | 0 | 1 | 0 |
| | | | | | | | | | | | 0 | 1 | 0 | 0 | | | | | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | * | 0 | 0 | * | | 0 | 0 | 0 | 1 | 0 | 1 | | | | | 0 | 0 | 0 | 1 | 0 |
| | | | | | | | | | | | 0 | 1 | 1 | 0 | | | | | 0 | 0 | 0 | 1 | 0 |
| | | | | | | | | | | | 0 | 1 | 1 | 1 | | | | | 0 | 0 | 0 | 1 | 0 |
| | | | | | | | | | | | 1 | 0 | 0 | 0 | | | | | 1 | 0 | 0 | 1 | 0 |
| | | | | | | | | | | | 1 | 0 | 0 | 1 | | | | | 0 | 1 | 1 | 0 | 0 |
| | | | | | | | | | | | 1 | 0 | 1 | 0 | | * | * | * | 0 | 0 | 0 | 0 | 0 | ← Cursor Position |
| | | | | | | | | | | | 1 | 0 | 1 | 1 | | * | * | * | * | * | * | * | * |
| | | | | | | | | | | | 1 | 1 | 0 | 0 | | | | | | | | | |
| | | | | | | | | | | | 1 | 1 | 0 | 1 | | | | | | | | | |
| | | | | | | | | | | | 1 | 1 | 1 | 0 | | | | | | | | | |
| | | | | | | | | | | | 1 | 1 | 1 | 1 | | * | * | * | * | * | * | * | * |
| | | | | | | | | | | | 0 | 0 | 0 | 0 | | * | * | * | | | | | |
| | | | | | | | | | | | 0 | 0 | 0 | 1 | | | | | | | | | |
| | | | | | | | | | | | 0 | 0 | 1 | 0 | | | | | | | | | |
| 0 | 0 | 0 | 0 | * | 1 | 1 | * | | 1 | 1 | 1 | 0 | 0 | 0 | | | | | | | | | |
| | | | | | | | | | | | 1 | 0 | 0 | 1 | | | | | | | | | |
| | | | | | | | | | | | 1 | 0 | 1 | 0 | | * | * | * | | | | | |
| | | | | | | | | | | | 1 | 0 | 1 | 1 | | * | * | * | * | * | * | * | * |
| | | | | | | | | | | | 1 | 1 | 0 | 0 | | | | | | | | | |
| | | | | | | | | | | | 1 | 1 | 0 | 1 | | | | | | | | | |
| | | | | | | | | | | | 1 | 1 | 1 | 0 | | | | | | | | | |
| | | | | | | | | | | | 1 | 1 | 1 | 1 | | * | * | * | * | * | * | * | * |

Character Pattern Example

Fig. 4

* : Invalid

(Note 1) Character code bit 1 and bit 2 correspond to CG RAM address bit 4 and bit 5.

(Note 2) Bit 0 to bit 3 of the CG RAM address indicate the row within the character bit map. The 11th row corresponds to the cursor position on the LCD display. Normally the 11th row should be blank (all 0s), otherwise the lowest line of the character will be obscured when used with the cursor. Lines 12 to 16 are not used for display data and can be used for general RAM data.

(Note 3) If bit 4 to bit 7 are all 0, a CG RAM character is indicated. The values of bits 0 and 3 do not matter. Character codes 00H, 01H, 08H and 09H all select the same character.

(Note 4) 1 : ON, 0 : OFF

● Timing generation circuit

The timing generation circuit generates timing signals for operating internal circuits such as the DD RAM, CG ROM and CG RAM.
The circuit is designed so that access by the MPU does not disturb the display. When data is written to the DD RAM, only the portion of RAM being written to is affected.
This circuit also generates timing signals which operate the extension driver (e.g. T6B23).
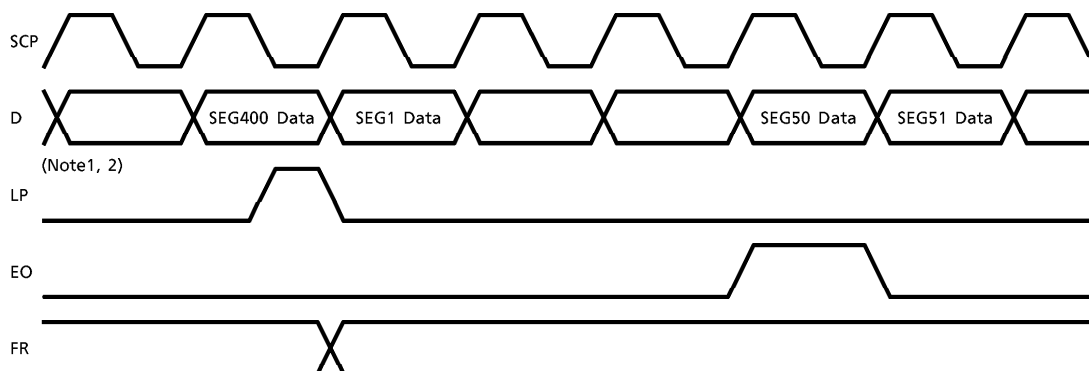The relation between the timing signals in 1-Line Display mode is as shown below.



Fig. 5

(Note1)    SEG1 to SEG50 Data for the T6B20
           SEG51 to SEG400 Data for the extension driver
(Note2)    In 2-Line Display mode, "SEG400 Data" changes to "SEG200 Data".

● LCD driver circuit

The LCD drive circuit consists of 16 row drivers and 50 column drivers.
When the character font type and the number of lines have been selected by the appropriate command, the valid row drivers automatically output drive waveforms, and the other row drivers output OFF waveforms.

● Cursor / blink display control circuit

This circuit generates the cursor or blink display. The cursor or blink is displayed in the digit which corresponds to the DD RAM address set in the Address Counter.
When the Address Counter is set to 05H, the cursor is displayed as shown below.
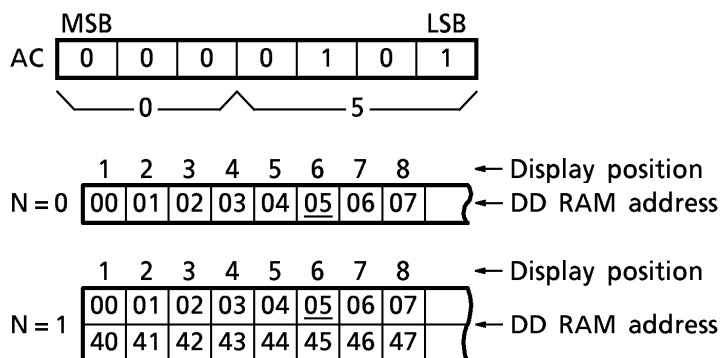


(Note) The cursor or blink is also displayed when a CG RAM address is set in the Address Counter. In this case the cursor or blink is displayed regardless of the DD RAM address.

● Reset

When $\overline{RST}$ = L, the T6B20 is reset and commands (1) to (4) are automatically executed. If a Hand Reset is not used, the MPU should execute commands (1) to (4).

(1)   Display Clear

(2)   Set Function ...............   BL = 1   : The blink is displayed by switching between all dots ON and the displayed characters.
                                     N = 0    : 1-line display
                                     F = 0    : 5 × 7-dot character font

(3)   Set Entry mode ............   I / D = 1 : + 1
                                     S = 0    : No Shift

(4)   Display ON / OFF Control ...  D = 0    : Display OFF
                                     C = 0    : Cursor OFF
                                     B = 0    : Blink OFF

● Key matrix, LED control circuit

This control circuit generates key scan signals and LED control signals. The key data input to SWC1 to SWC8 are converted to serial data and output from SOD. SWS1 to SWS8 output the key scan signals and the LED data signals. LE1 to LE2 output the LED Enable signals.
The T6B20 controls a 2×8 LED matrix using a LED data signal and an Enable signal.
The key scan signals and the LED control signals are shown in Fig. 6.
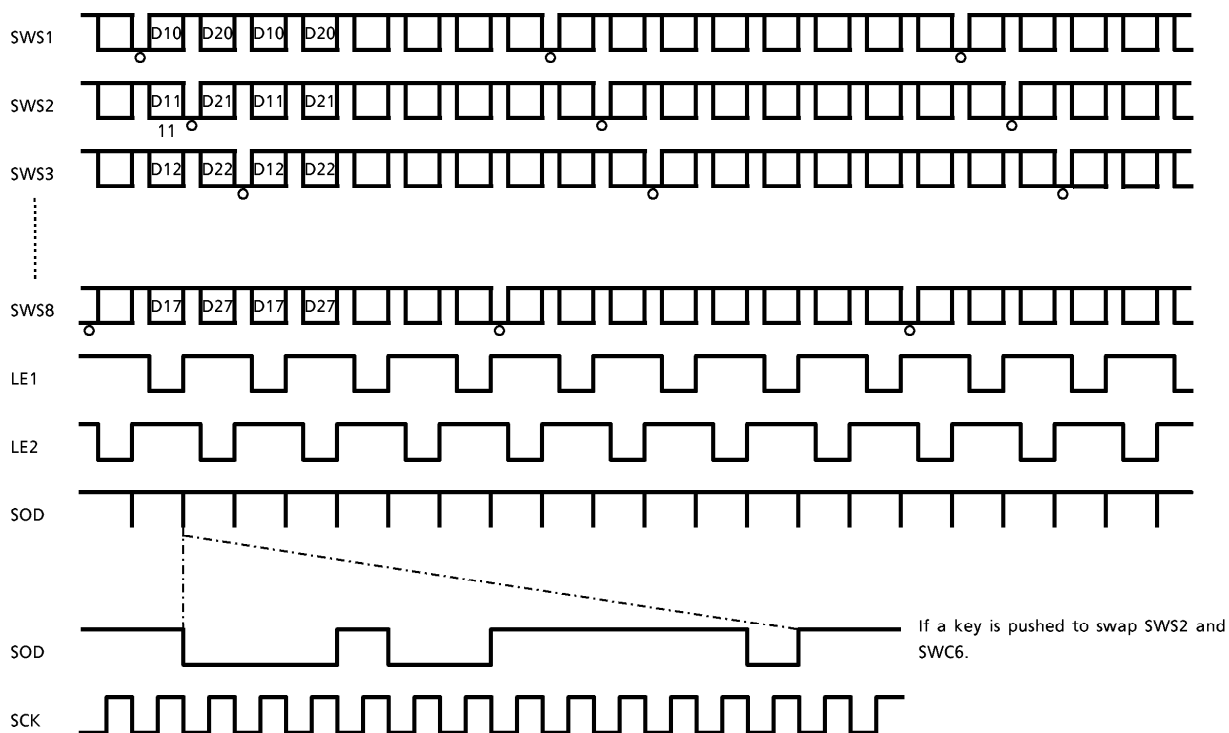


Fig. 6

(Note) D : LED control signals
　　　* 　　D10 to D17 : The data on each bit of the LER1
　　　** 　D20 to D27 : The data on each bit of the LER2
　　° : Key scan signal

The structure of the 8 × 8-key scan matrix and the 2 × 8 LED matrix is shown in Fig. 7.
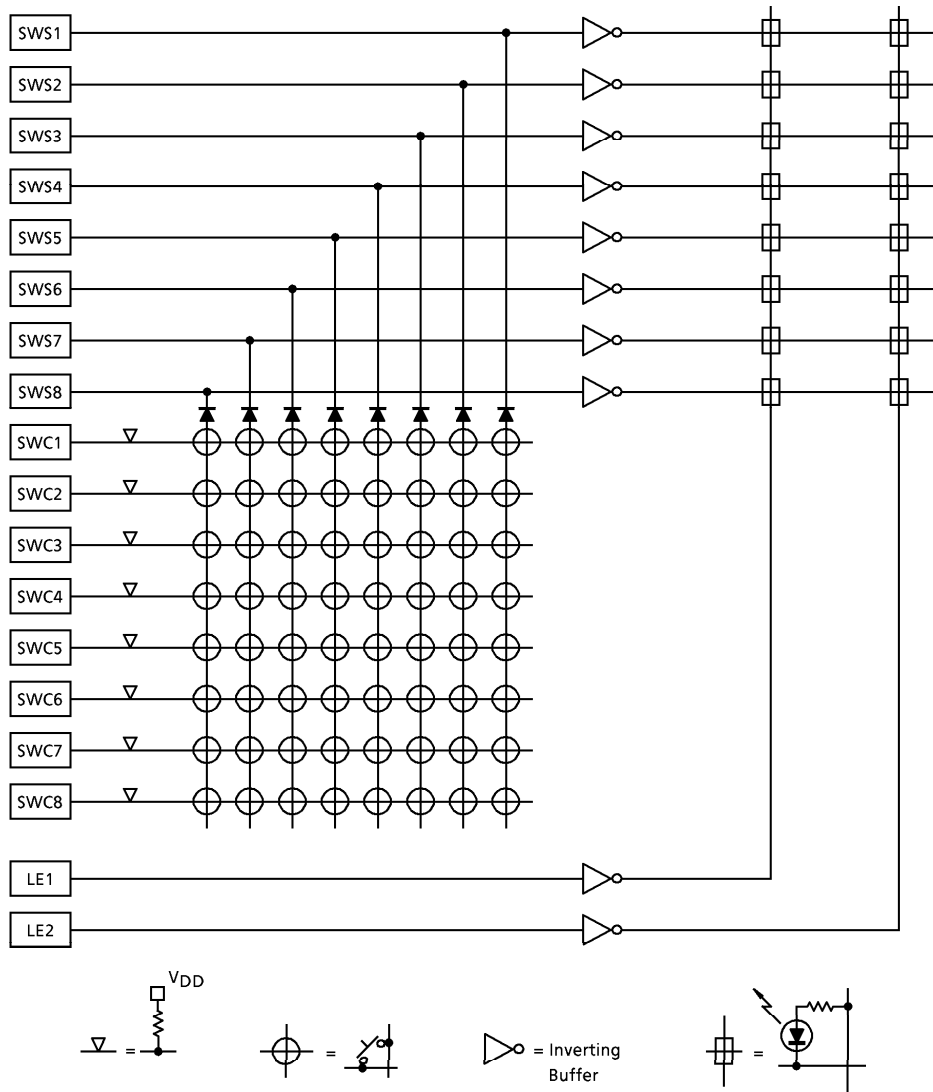


Fig. 7

● Interface to MPU

(1) Input data format



SCK

SID | 1 | 0 | 0 | 0 | RS1 | RS2 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | 1 | 1 | 0 | 0 | 0 | RS1 |

When the Clear Display and Return Home instruction is executed : this timing exceeds 1.64ms
When another instruction is executed : this timing exceeds 80$\mu$s

(2) Output data format



SCK
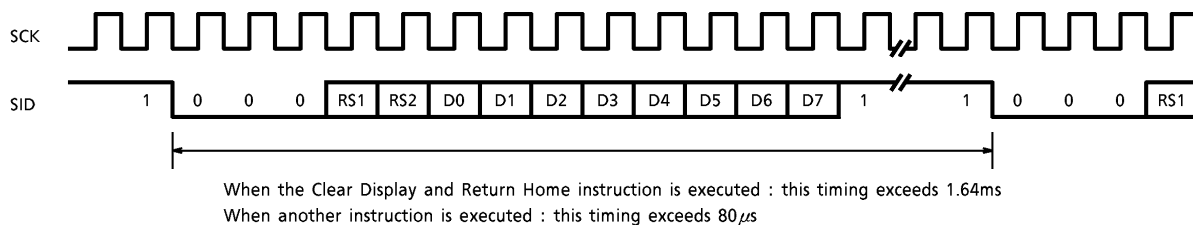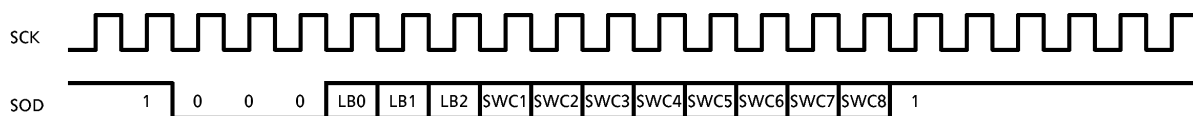
SOD | 1 | 0 | 0 | 0 | LB0 | LB1 | LB2 | SWC1 | SWC2 | SWC3 | SWC4 | SWC5 | SWC6 | SWC7 | SWC8 | 1 |

|       | LB0 | LB1 | LB2 |
|-------|-----|-----|-----|
| SWS1  | 0   | 0   | 0   |
| SWS2  | 1   | 0   | 0   |
| SWS3  | 0   | 1   | 0   |
| SWS4  | 1   | 1   | 0   |
| SWS5  | 0   | 0   | 1   |
| SWS6  | 1   | 0   | 1   |
| SWS7  | 0   | 1   | 1   |
| SWS8  | 1   | 1   | 1   |

If a key is pushed to swap SWS2 and SWC6.



SCK

SOD
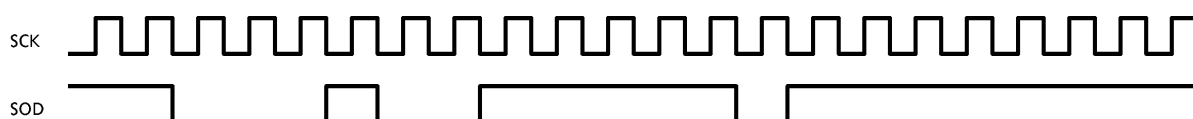
## INSTRUCTION

The MPU can directly control four registers. While the T6B20 is executing an instruction, it cannot execute any other command.
If a command is being executed repeatedly, a wait time must be allowed between successive commands.

## DESCRIPTION OF INSTRUCTIONS

| INSTRUC-TION | CODE | | | | | | | | | | DESCRIPTION | WORKING TIME $f_{osc}$ = 250 kHz (max) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS1 | RS2 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Clears all display data and sets the DD RAM address to 00H. | 1.64ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | Sets the DD RAM address 00H and returns the display to home position. The contents of the DD RAM do not change. | 1.64ms |
| Set Entry Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets cursor shift direction and display shift. These operations are executed, when data is written. | 40$\mu$s |
| Display ON/OFF Control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Sets ON/OFF for entire display (D), cursor ON/OFF (C), cursor position blink (B). | 40$\mu$s |
| Cursor/Display shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | * | * | Shifts cursor and display without changing DD RAM contents. | 40$\mu$s |
| Set Function | 0 | 0 | 0 | 0 | 1 | BL | N | F | T | * | Sets blink mode (BL), sets number of display lines (N), character font (F), and test mode (T). | 40$\mu$s |
| Set the CG RAM Address | 0 | 0 | 0 | 1 | CG RAM Address | | | | | | Sets the CG RAM Address. | 40$\mu$s |
| Set the DD RAM Address | 0 | 0 | 1 | DD RAM Address | | | | | | | Sets the DD RAM Address. | 40$\mu$s |
| Write Data to the CG RAM or DD RAM | 0 | 1 | Write Data | | | | | | | | Writes data into the CG RAM or DD RAM. | 46$\mu$s |
| Write LED Data (1) | 1 | 0 | Write Data | | | | | | | | Writes data into the LED data register (LER1) | 0$\mu$s |
| Write LED Data (2) | 1 | 1 | Write Data | | | | | | | | Writes data into the LED data register (LER2) | 0$\mu$s |

| INSTRUC-TION | CODE | | | | | | | | | | DESCRIPTION | WORKING TIME $f_{osc}$ = 250 kHz (max) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS1 | RS2 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| — | I / D = 1 : Increment<br>I / D = 0 : Decrement<br>S = 1 : Display Shift ON<br>S / C = 1 : Display Shift<br>S / C = 0 : Cursor Shift<br>R / L = 1 : Shift to the Right<br>R / L = 0 : Shift to the Left<br>BL = 1 : Display Blink ON (all dots ON)<br>BL = 0 : Display Blink ON (character-character reverse image)<br>N = 1 : 2-Line display<br>N = 0 : 1-Line display<br>F = 1 : 5 × 10 dots<br>F = 0 : 5 × 7 dots<br>T = 1 : Enable Test Mode<br>T = 0 : Cancel Test Mode | | | | | | | | | | | | |

\* : invalid

● Clear Display

|  | RS1 | RS2 | D7 | -------------------------------- | | | | | | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Instruction Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

When the T6B20 executes this instruction, code 20H (code 20H must be the "Space code") is written to every address in the DD RAM. This command resets the DD RAM address in the Address Counter. The display is inhibited and the cursor or blink is moved to the left of the display. (In 2-Line Display mode, the cursor moves to the left of 1st line of the display.) The I / D of Entry mode is set to 0. The S of Entry mode does not change.

● Return Home

|  | RS1 | RS2 | D7 | ------------------------------ | | | | | | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Instruction Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * |

\* : invalid

The DD RAM address in the Address Counter is reset by this instruction, and the display shift is cancelled (this is known as returning to the home position). The contents of the DD RAM do not change. The cursor or blink moves to the extreme left of the display. (In 2-Line Display mode, the cursor moves to the extreme left of the 1st line of the display.)

● Set Entry mode

| | RS1 | RS2 | D7 | ------------------------------ | | | | | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Instruction Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

I/D : The Address Counter is incremented (I/D = 1) or decremented (I/D = 0) after the data has been written to or read from DD RAM.
The same is true when date is written to or read from CG RAM.

S    : If S = 1, the entire display is shifted left (I/D = 1) or right (I/D = 0) when data is written to the DD RAM. (The cursor position does not move)
If S = 0, the display is not shifted.

● Display ON / OFF control

| | RS1 | RS2 | D7 | ----------------------------- | | | D0 | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Instruction Code | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

D : D = 1, display is ON; D = 0, display is OFF.
When D is reset, the contents of the DD RAM do not change. Therefore, the contents can be displayed as before by setting D.

C : C = 1, cursor display is ON; C = 0, cursor display is OFF.
5 × 7-dot character font   : cursor display uses 5 dots on the 8th line
5 × 10-dot character font  : cursor display uses 5 dots on the 11th line

B : B = 1, character blink is ON (same position of cursor position); B = 0, character blink is OFF.
Selectable blink : All dots on
                   Character-character reverse image

Cursor and blink can operate at same time.
Blink period      : Font 5 × 7-dot, $f_{OSC}$ = 250kHz
$(1 / 250k) \times 5 \times 80 \times 8 \times 32 = 409.6$ (ms)
Font 5 × 10-dot, $f_{OSC}$ = 250kHz
$(1 / 250k) \times 5 \times 80 \times 11 \times 32 = 563.2$ (ms)
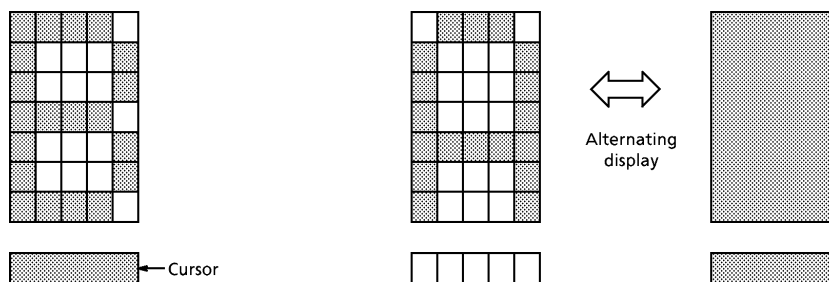


(1)  Cursor display example (5 × 7 dots)          (2)  Blink display example (BL = 1)

● Cursor Display Shift

```
                RS1  RS2  D7  ----------------------------- D0
Instruction Code  0    0   0   0   0   1  S/C R/L  *   *    * : invalid
```

When this instruction is executed, the cursor or display is shifted to the right or left without display data being written or read.
In 2-Line Display mode, the cursor is shifted from the 40th digit of the 1st line to the 1st digit of the 2nd line.

| S/C | R/L | FUNCTIONS | ADDRESS COUNTER (AC) |
|---|---|---|---|
| 0 | 0 | Shift the cursor to the left. | AC = AC − 1 |
| 0 | 1 | Shift the cursor to the right. | AC = AC + 1 |
| 1 | 0 | Shift the whole display to the left. The cursor follows the display shift direction. | AC = AC |
| 1 | 1 | Shift the whole display to the right. The cursor follows the display shift direction. | AC = AC |

When S/C = 1, the contents of the Address Counter do not change.

● Set Function

```
                RS1  RS2  D7  ----------------------------- D0
Instruction Code  0    0   0   0   1  BL  N   F   T   *    * : invalid
```

BL : BL = 1, Blink ON (All dots ON)
     BL = 0, Blink ON (character reverse image-character)

N : N = 0, 1-line display mode
    N = 1, 2-line display mode

F : F = 0, 5 × 7-dot character font
    F = 1, 5 × 10-dot character font

| N | F | DISPLAY LINES | CHARACTER FONT | DUTY |
|---|---|---|---|---|
| 0 | 0 | 1 | 5×7 dots | 1/8 |
| 0 | 1 | 1 | 5×10 dots | 1/11 |
| 1 | * | 2 | 5×7 dots | 1/16 |

(1) BL = 1

(2) BL = 0

T : T = 1, Test mode
    Executing this instruction, sets T = 0.

(Note) Execute this instruction first in a program before executing any other instructions.
After this instruction has been used once, it cannot be used again, except to change the Blink mode setting.

● Set CG RAM Address

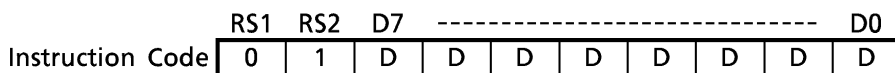| Instruction Code | RS1 | RS2 | D7 | ----- | ----- | ----- | ----- | ----- | ----- | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 1 | A | A | A | A | A | A |
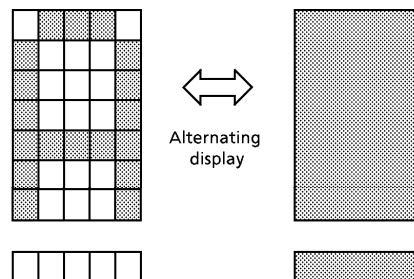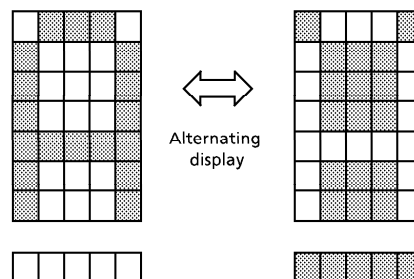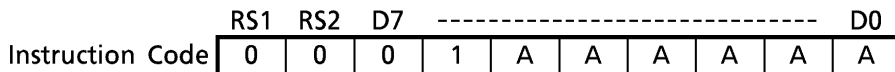
This instruction writes the CG RAM address data (e.g. AAAAAA (bin)) into the Address Counter.

● Set DD RAM Address

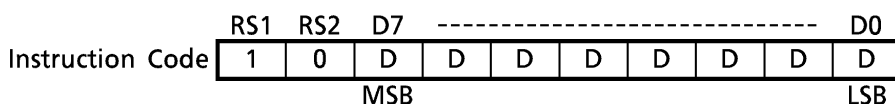| Instruction Code | RS1 | RS2 | D7 | ----- | ----- | ----- | ----- | ----- | ----- | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 1 | A | A | A | A | A | A | A |
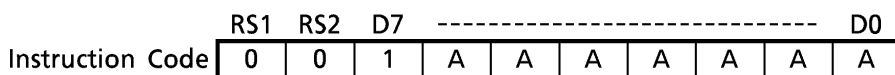
This instruction writes the DD RAM address data (e.g. AAAAAAA (bin)) into the Address Counter.

● Write Data to DD RAM or CG RAM

| Instruction Code | RS1 | RS2 | D7 | ----- | ----- | ----- | ----- | ----- | ----- | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | D | D | D | D | D | D | D | D |

This instruction writes 8-bit data (e.g. DDDDDDDD (bin)) to DD RAM or CG RAM.
The previous instruction (Set DD RAM or CG RAM Address) determines whether the data will be written to DD RAM or CG RAM.
Before this instruction is executed, the Set DD RAM or CG RAM Address instruction must be executed.
After the data has been written, the address is automatically incremented or decremented by 1.

● Write LED data (1)

| Instruction Code | RS1 | RS2 | D7 | ----- | ----- | ----- | ----- | ----- | ----- | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 0 | D | D | D | D | D | D | D | D |
| | | | MSB | | | | | | | LSB |

This instruction writes 8-bit data (e.g. DDDDDDDD (bin)) to LER1 (LED Data register 1).
This data controls eight LEDs using outputs SWS1 to SWS8 and LE1.

● Write LED data (2)

| Instruction Code | RS1 | RS2 | D7 | ----- | ----- | ----- | ----- | ----- | ----- | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 1 | D | D | D | D | D | D | D | D |
| | | | MSB | | | | | | | LSB |
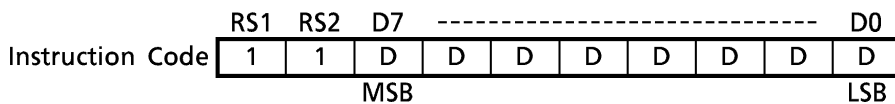
This instruction writes 8-bit data (e.g. DDDDDDDD (bin)) to LER2 (LED Data register 2).
This data controls eight LEDs using outputs SWS1 to SWS8 and LE2.

## POWER SUPPLY FOR LCD DRIVE

Various voltage levels must be applied to the T6B20's pins $V_{LC1}$ to $V_{LC5}$ to obtain the LCD drive waveforms.

The voltage levels vary according to the duty factor. The following table shows the relation between the two.

| DUTY FACTOR / POWER SUPPLY BIAS | 1 / 8, 1 / 11 $\frac{1}{4}$ | 1 / 16 $\frac{1}{5}$ |
|---|---|---|
| $V_{LC1}$ | $V_{DD} - 1/4 V_{LCD}$ | $V_{DD} - 1/5 V_{LCD}$ |
| $V_{LC2}$ | $V_{DD} - 1/2 V_{LCD}$ | $V_{DD} - 2/5 V_{LCD}$ |
| $V_{LC3}$ | $V_{DD} - 1/2 V_{LCD}$ | $V_{DD} - 3/5 V_{LCD}$ |
| $V_{LC4}$ | $V_{DD} - 3/4 V_{LCD}$ | $V_{DD} - 4/5 V_{LCD}$ |
| $V_{LC5}$ | $V_{DD} - V_{LCD}$ | $V_{DD} - V_{LCD}$ |

$$V_{LCD} = V_{DD} - V_{LC5}$$
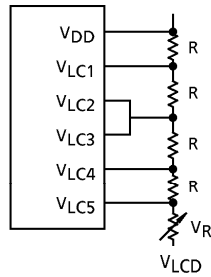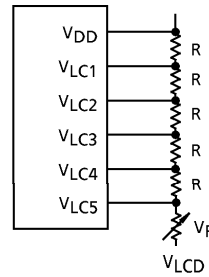


(1) 1 / 4 Bias          (2) 1 / 5 Bias

## THE RELATION BETWEEN OSCILLATION FREQUENCY AND LCD FRAME FREQUENCY

LCD frame frequency example ($f_{osc} = 250$kHz)

(1) 1 / 8 duty cycle
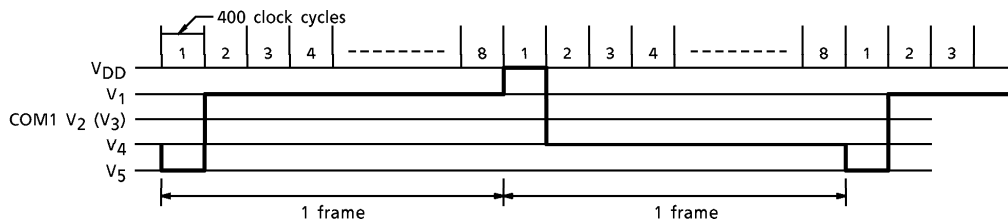


$$1 \text{ frame} = 4\mu s \times 400 \times 8 = 12800 \mu s = 12.8 ms$$

$$\text{frame frequency} = \frac{1}{12.8 ms} = 78.1 Hz$$

## (2) 1 / 11 duty cycle
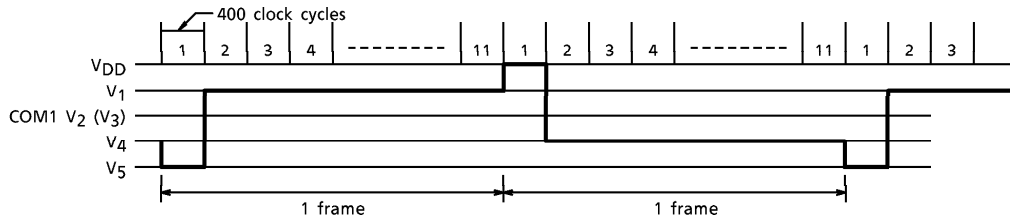


$$1 \ \text{frame} = 4\mu s \times 400 \times 11 = 17600\mu s = 17.6\text{ms}$$

$$\text{frame frequency} = \frac{1}{17.6\text{ms}} = 56.8\text{Hz}$$

## (3) 1 / 16 duty cycle
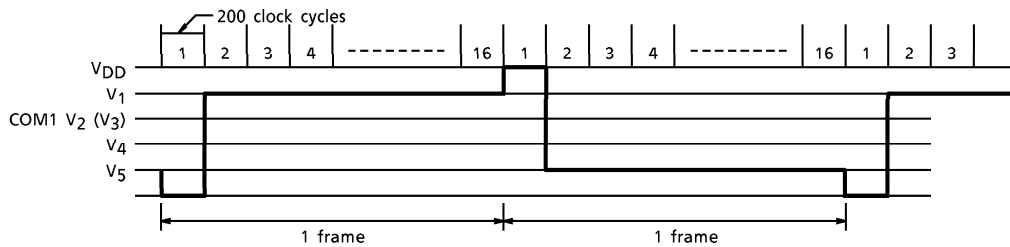


$$1 \ \text{frame} = 4\mu s \times 200 \times 16 = 12800\mu s = 12.8\text{ms}$$

$$\text{frame frequency} = \frac{1}{12.8\text{ms}} = 78.1\text{Hz}$$

## ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

| ITEM | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Power Supply Voltage (1) | $V_{DD}$ | $-0.3$ to $7.0$ | V |
| Power Supply Voltage (2) | $V_{LC1}$ to $V_{LC5}$ | $V_{DD} - 13.5$ to $V_{DD} + 0.3$ | V |
| Input Voltage | $V_{IN}$ | $-0.3$ to $V_{DD} + 0.3$ | V |
| Operating Temperature | $T_{opr}$ | $-20$ to $75$ | °C |
| Storage Temperature | $T_{stg}$ | $-55$ to $125$ | °C |

(Note 1)   All voltage values are referenced to $V_{SS} = 0V$.
(Note 2)   Ensure that the following condition is always maintained.
$$V_{DD} \geqq V_{LC1} \geqq V_{LC2} \geqq V_{LC3} \geqq V_{LC4} \geqq V_{LC5}$$

**ELECTRICAL CHARACTERISTICS**
DC CHARACTERISTICS
TEST CONDITIONS (Unless otherwise noted, $V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$, Ta = -20 to 75°C)

| ITEM | | SYMBOL | TEST CIR-CUIT | TEST CONDITIONS | MIN | TYP. | MAX | UNIT | PIN NAME |
|---|---|---|---|---|---|---|---|---|---|
| Operating Voltage (1) | | $V_{DD}$ | — | — | 4.5 | — | 5.5 | V | — |
| Operating Voltage (2) | | $V_{LCD}$ | — | $V_{LCD} = V_{DD} - V_{LC5}$ | 3.0 | — | 11.0 | V | — |
| Input Voltage (1) | H Level | $V_{IH1}$ | — | — | $V_{DD}$ -1.0 | — | $V_{DD}$ | V | SCK, SID $\overline{RST}$ |
| | L Level | $V_{IL1}$ | — | — | 0 | — | 1.0 | V | |
| Hysterisis Voltage | | $V_H$ | — | — | — | 0.7 | — | V | SCK, SID $\overline{RST}$ |
| Input Voltage (2) | H Level | $V_{IH2}$ | — | — | $V_{DD}$ -1.2 | — | $V_{DD}$ | V | SWC1 to SWC8 |
| | L Level | $V_{IL2}$ | — | — | 0 | — | 1.9 | V | |
| Output Voltage (1) | H Level | $V_{OH1}$ | — | $I_{OH} = -0.625mA$ | $V_{DD}$ -0.3 | — | — | V | D, SCP LP, EO, FR |
| | L Level | $V_{OL1}$ | — | $I_{OL} = 0.625mA$ | — | — | 0.3 | V | |
| Output Voltage (2) | H Level | $V_{OH2}$ | — | $I_{OH} = -1.6mA$ | 2.4 | — | — | V | SOD |
| | | | — | $I_{OH} = -250\mu A$ | $V_{DD}$ -0.8 | — | — | | |
| | L Level | $V_{OL2}$ | — | $I_{OL} = 2.0mA$ | — | — | 0.4 | V | |
| Output Voltage (3) | H Level | $V_{OH3}$ | — | $I_{OH} = -250\mu A$ | $V_{DD}$ -0.8 | — | — | V | SWS1 to SWS8 |
| | L Level | $V_{OL3}$ | — | $I_{OL} = 2.0mA$ | — | — | 0.4 | V | LE1, LE2 |
| Row Output Resistance | | RCOM | — | $I_d = \pm 50\mu A$ | — | — | 20 | kΩ | COM1 to 16 |
| Column Output Resistance | | RSEG | — | $I_d = \pm 50\mu A$ | — | — | 30 | kΩ | SEG1 to 50 |
| Input Leakage Current | | $I_{IL}$ | — | $V_{IN} = 0$ to $V_{DD}$ | — | — | 1 | $\mu A$ | SCK, SID |
| Power Supply Current | | $I_{DD}$ | — | All Outputs Open | — | — | 800 | $\mu A$ | $V_{DD}$ |

## AC CHARACTERISTICS
● Serial interface
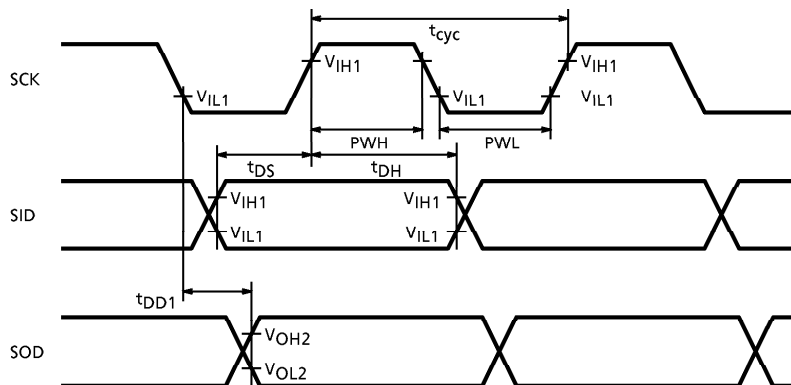


TEST CONDITIONS ($V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$, Ta = $-20$ to 75°C)

| ITEM | SYMBOL | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|
| SCK Cycle Time | $t_{cyc}$ | 2000 | 4000 | 8000 | ns |
| SCK High Width | PWH | $\dfrac{t_{cyc}}{2} - 100$ | — | — | ns |
| SCK Low Width | PWL | $\dfrac{t_{cyc}}{2} - 100$ | — | — | ns |
| Data Set-up Time to SCK | $t_{DS}$ | 50 | — | — | ns |
| Data Hold Time form SCK | $t_{DH}$ | 120 | — | — | ns |
| Data Delay Time form SCK | $t_{DD1}$ | — | — | 300 | ns |

(Note) AC Testing load circuit for SOD
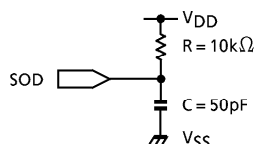


● Power-on sequence
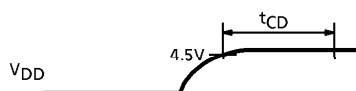


TEST CONDITIONS ($V_{SS} = 0V$, Ta = $-20$ to 75°C)

| ITEM | SYMBOL | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|
| Command Disable Time | $t_{CD}$ | — | — | 15 | ms |

● Expansion driver interface
(e.g. T6B23)
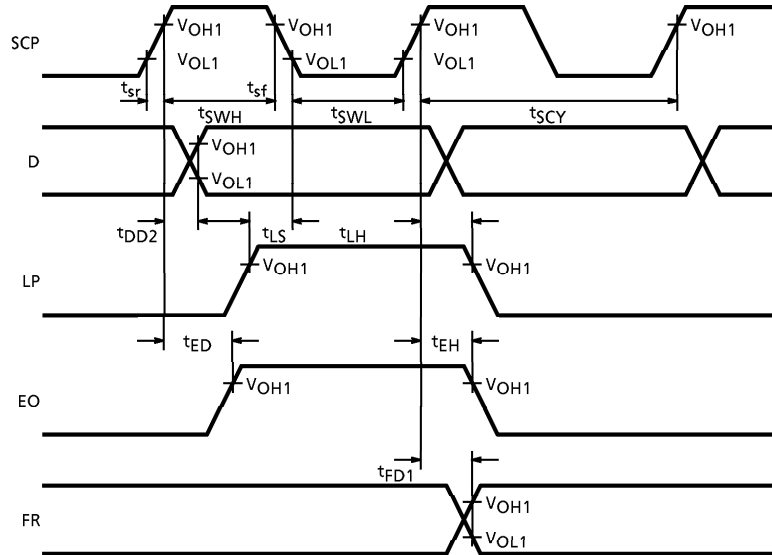


TEST CONDITIONS ($V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $Ta = -20$ to $75°C$)

| ITEM | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| SCP Cycle Time | $t_{SCY}$ | 2000 | — | ns |
| SCP Pulse Width | $t_{SWH, L}$ | 800 | — | ns |
| SCP Rise and Fall Time | $t_{sr}, t_{sf}$ | — | 100 | ns |
| Data Delay from SCP | $t_{DD2}$ | — | 100 | ns |
| LP Set-up Time SCP | $t_{LS}$ | −120 | 0 | ns |
| LP Hold Time from SCP | $t_{LH}$ | −100 | 0 | ns |
| EO Delay Time from SCP | $t_{ED}$ | — | 100 | ns |
| EO Hold Time from SCP | $t_{EH}$ | −100 | 0 | ns |
| FR Delay Time from SCP | $t_{FD1}$ | −100 | 100 | ns |

(Note) AC testing load circuit for interface timing
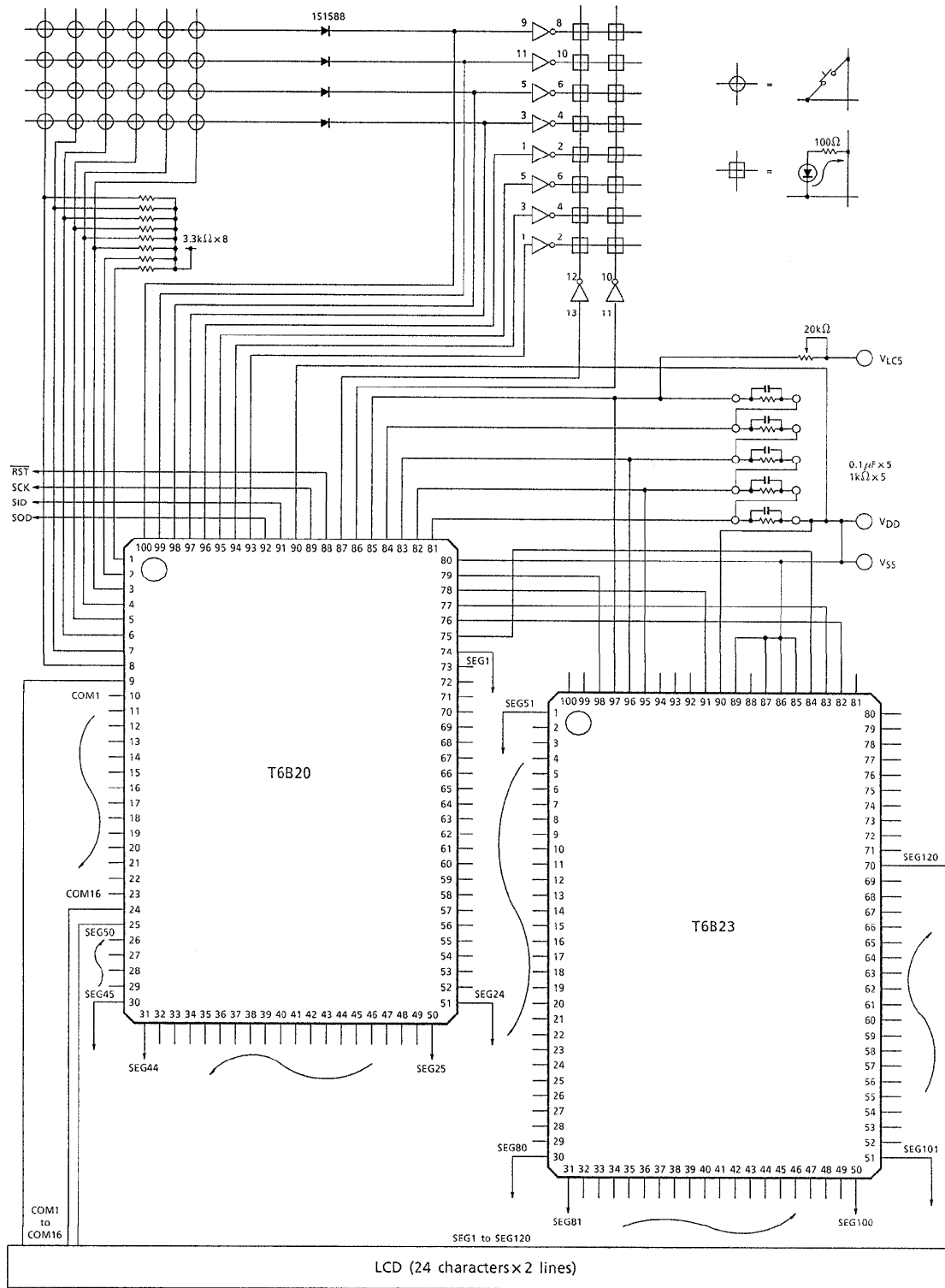
Test Point O———
$C_L$
$C_L = 50pF$
$C_L$ includes jig capacitance.
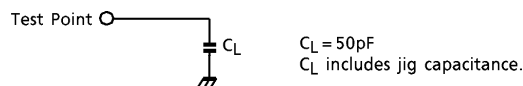
## APPLICATION CIRCUIT
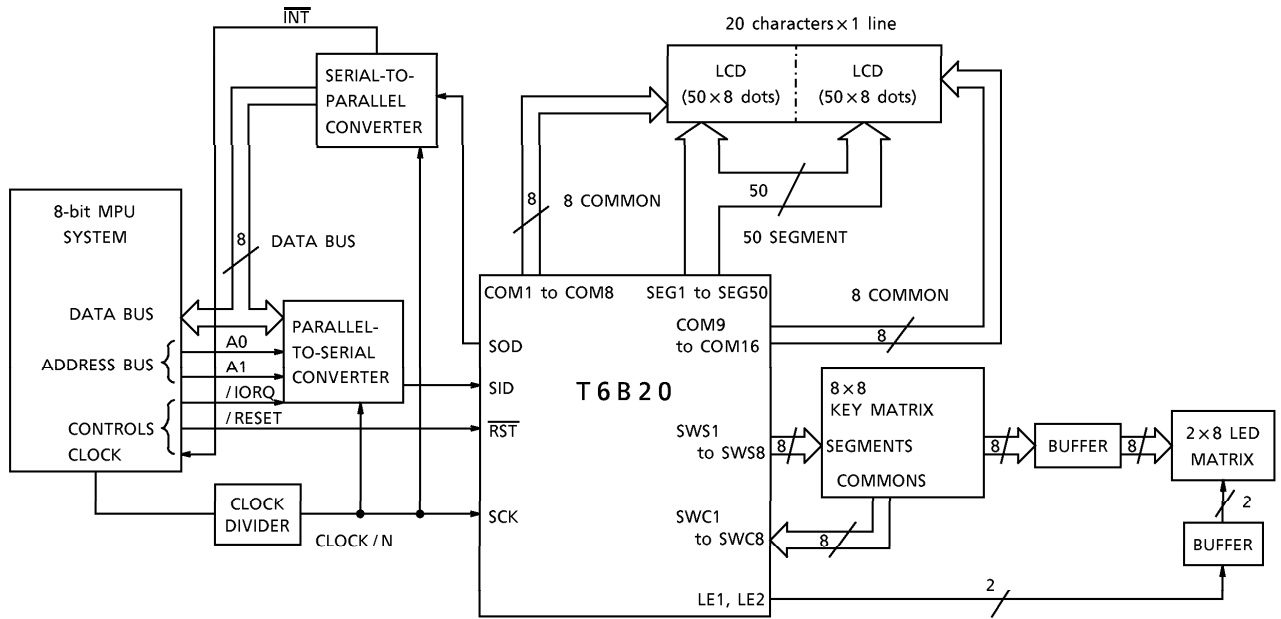
**APPLICATION-A**

APPLICATION-B



LCD (24 characters × 2 lines)

T6B20 – 28
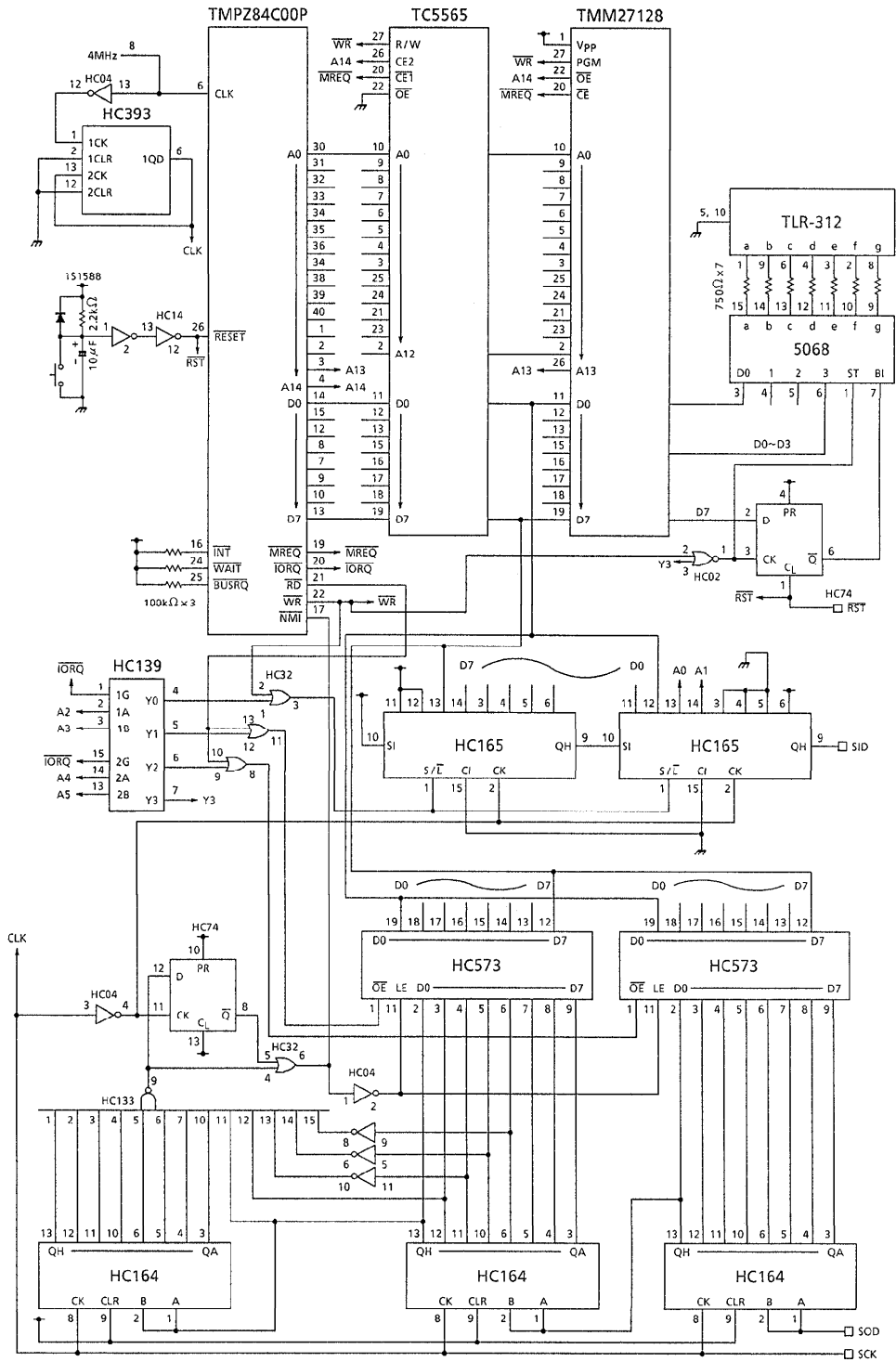
**OUTLINE DRAWING**
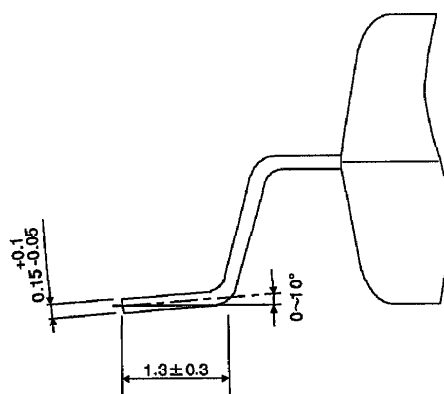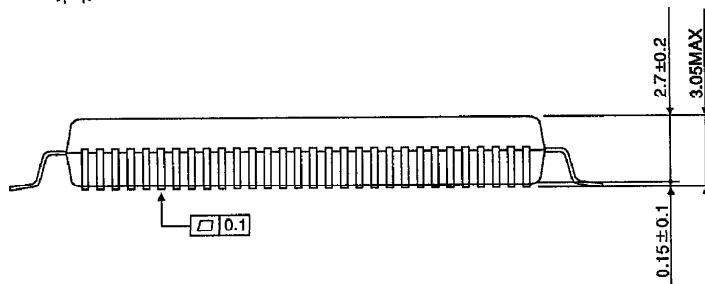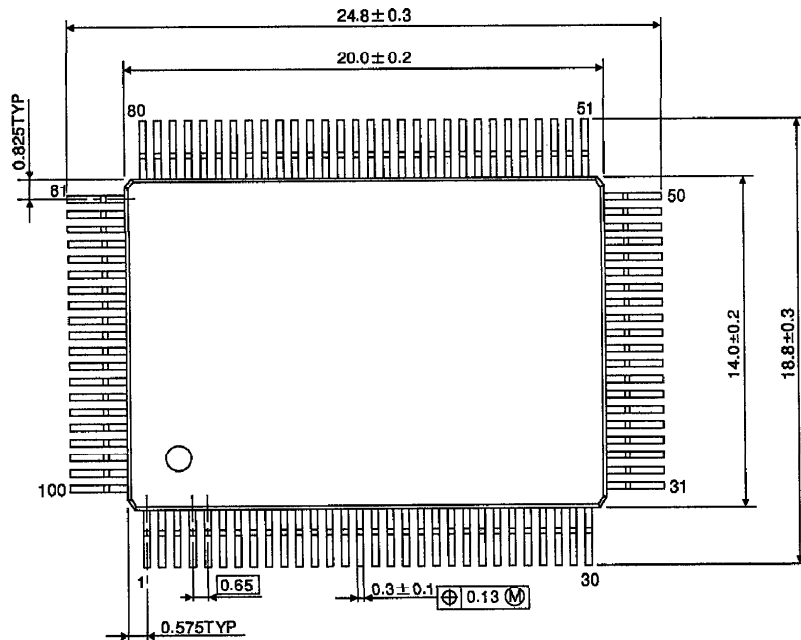QFP100-P-1420-0.65J                                                          Unit : mm



Weight : 1.6g (Typ.)