

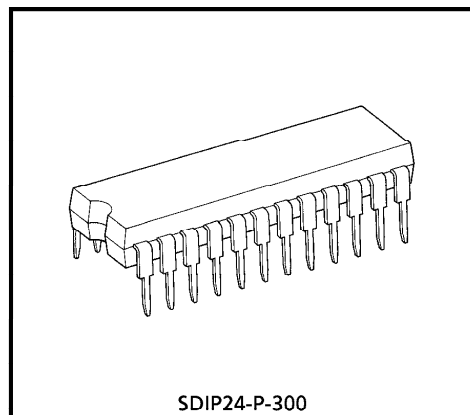
## 16BIT SHIFT REGISTER, LATCH & CONSTANT CURRENT DRIVERS

The TB62701N is specifically designed for LED and LED-DISPLAY constant current drivers.

This constant current output circuit is able to set up external resistor ( $I_{OUT} = 0$  to 50mA).

This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

The devices consist of 16bit Shift Register, Latch, AND-GATE and Constant Current Driver.



Weight : 1.2g (Typ.)

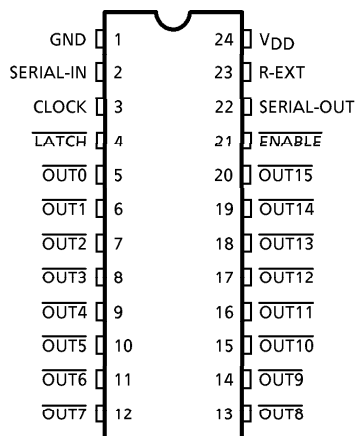
### FEATURES

- OUTPUT CURRENT : Set-up at 0 to 50mA with an external resistor.
- A LITTLE CHANGE OF OUTPUT CURRENT ( $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ )

OUT-GND VOLTAGE	A LITTLE CHANGE OF CHANNEL	$I_{OUT}$ [mA]
$\geq 0.4\text{V}$	$\pm 7\%$	0~50mA
$\geq 0.7\text{V}$		

- 5V CMOS Compatible Input
- PACKAGE : SDIP-24 (SDIP24-P-300)
- MAXIMUM CLOCK FREQUENCY :  $f_{MAX} = 2.5\text{MHz}$  (cascade operation,  $T_a = 25^\circ\text{C}$ )

### PIN CONNECTION (TOP VIEW)

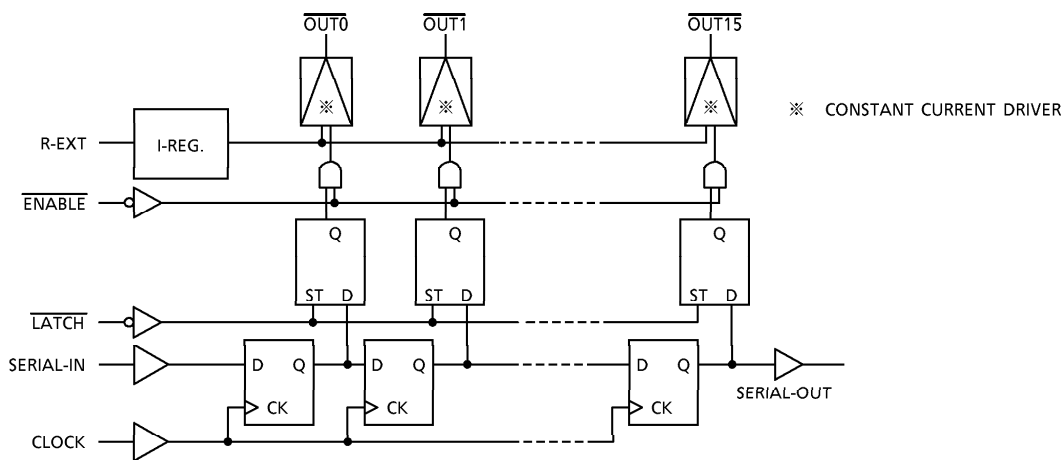


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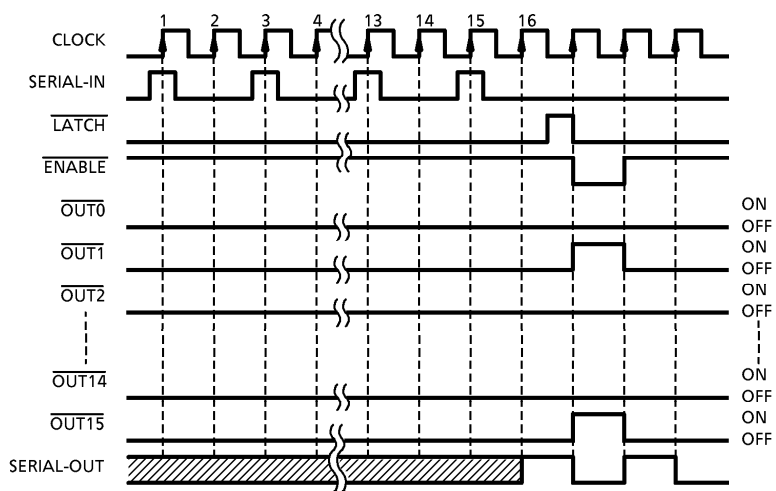
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**BLOCK DIAGRAM**



**TIMING DIAGRAM**



**TERMINAL DESCRIPTION**

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic driver
2	SERIAL-IN	Serial data input terminal for shift register
3	CLOCK	Clock input terminal for data shift to up-edge
4	LATCH	"H" level : data through, "L" level : data hold
24	V <sub>DD</sub>	Supply voltage terminal
5~12 13~20	OUT <sub>n</sub>	Output terminals
21	ENABLE	"H" level output off, "L" level : latch data = "H" level then output on, latch data = "L" level then output off
22	SERIAL-OUT	Serial data output terminal for shift register
23	R-EXT	The register which connects between R-EXT and GND sets the constant output current.

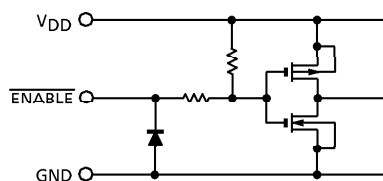
**TRUTH TABLE**

INPUT				OUTPUT OUT <sub>n</sub> (t = n)			
CLOCK	LATCH	ENABLE	SERIAL-IN	OUT <sub>0</sub> ... OUT <sub>7</sub> ... OUT <sub>15</sub>	SERIAL-OUT		
	H	L	D <sub>n</sub>	D <sub>n</sub>	D <sub>n-7</sub>	D <sub>n-15</sub>	D <sub>n-15</sub>
	L	L	D <sub>n</sub>	No change		D <sub>n-15</sub>	
	※	H	D <sub>n</sub>	OFF	OFF	OFF	D <sub>n-15</sub>
	※	※	D <sub>n</sub>	No change		No change	

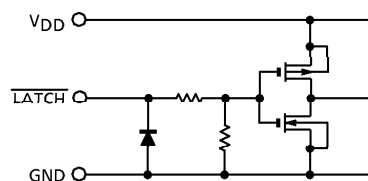
(Note) D<sub>n</sub>~D<sub>n-15</sub> = "H" then OUT<sub>n</sub> is ON, "L" then OUT<sub>n</sub> is OFF.

**EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS**

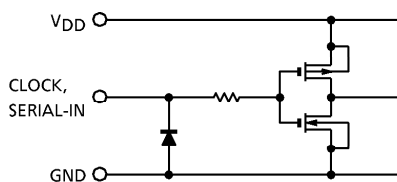
1. ENABLE terminal



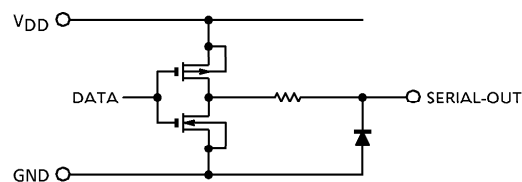
2. LATCH terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



**MAXIMUM RATINGS** (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	0~7.0	V
Output Voltage	V <sub>CE</sub>	-0.5~30	V
Output Current	I <sub>OUT</sub>	50	mA
Input Voltage	V <sub>IN</sub>	-0.4~V <sub>DD</sub> +0.4	V
GND Terminal Current	I <sub>GND</sub>	800	mA
Clock Frequency	f <sub>CK</sub>	2.5	MHz
Power Dissipation	P <sub>D</sub>	1.78	W
Operating Temperature	T <sub>opr</sub>	-40~85	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

(Note) Ambient temperature delated above 25°C in the proportion of 14.2mW/°C.

**RECOMMENDED OPERATING CONDITION** (Ta = -40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage	V <sub>DD</sub>	—	4.5	5.0	5.5	V	
Output Voltage	V <sub>OUT</sub>	—	—	—	30.0	—	
Output Current	OUTn	I <sub>OUT</sub>	DC 1 circuit	—	—	45	mA
	S-OUT	I <sub>OH</sub>	—	—	-1.0	1.0	
		I <sub>OL</sub>	—	—	—		
Input Voltage	V <sub>IN</sub>	—	0	—	V <sub>DD</sub>	V	
Data Set Up Time	t <sub>setup</sub> (D)	—	100	—	—	ns	
Data Hold Time	t <sub>hold</sub> (D)	—	20	—	—	ns	
Latch Set Up Time	t <sub>setup</sub> (L)	—	300	—	—	ns	
Latch Hold Time	t <sub>hold</sub> (L)	—	100	—	—	ns	
Clock Pulse Width	t <sub>w</sub> CLK	—	100	—	—	ns	
	t <sub>w</sub> CLK	—	100				
Latch Pulse Width	t <sub>w</sub> LAT	—	300	—	—	ns	
	t <sub>w</sub> LAT	—	300				
Clock Frequency	f <sub>CK</sub>	Cascade operation	—	—	2.0	MHz	
Power Dissipation	P <sub>D</sub>	Ta = 85°C	—	—	0.72	W	

**ELECTRICAL CHARACTERISTICS** ( $V_{DD} = 5.0V$ ,  $T_a = 25^\circ C$  unless otherwise noted)

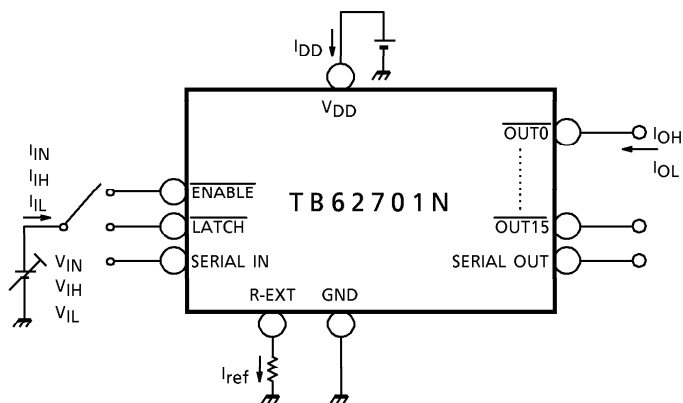
CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" level	$V_{IH}$	—	—	$70\%V_{DD}$	—	$V_{DD}$	V
	"L" level	$V_{IL}$	—	—	GND	—	$30\%V_{DD}$	
Output Leakage Current		$I_{OH}$	—	$V_{OH} = 30V$	—	—	10	$\mu A$
Output Voltage	S-OUT	$V_{OL}$	—	$I_{OL} = +1.0mA$	—	—	0.4	V
		$V_{OH}$	—	$I_{OH} = -1.0mA$	4.6	—	—	
Output Current 1		$I_{OL1}$	—	$V_{CE} = 0.7V$   $R_{EXT} = 560\Omega$	35.2	41.5	47.7	mA
		$I_{OL2}$	—	$V_{CE} = 0.4V$ (include $\Delta I_{OL1}$ )	33.1	39.0	44.9	
Delta $I_{OUT}$		$\Delta I_{OL1}$	—	$R_{EXT} = 560\Omega$ $I_{OUT} = 40mA$ , $V_{CE} = 0.4V$	—	$\pm 3.0$	$\pm 7.0$	%
Supply Voltage Regulation		$\% / V_{DD}$	—	$R_{EXT} = 560\Omega$	—	18	—	$\% / V$
Reference Voltage		$V_{ref}$	—	$R_{EXT} = 560\Omega$ , $T_a = -40 \sim 85^\circ C$	—	1.26	—	V
Pull Up/Down Resister		$R_{IN}$	—	—	100	200	400	$k\Omega$
Supply Current	"OFF"	$I_{DD} (off) 1$	—	$R_{EXT} = OPEN$ , $OUT_n = Off$	—	0.4	0.6	mA
		$I_{DD} (off) 2$	—	$R_{EXT} = 560\Omega$ , $OUT_n = Off$	—	6.5	10.0	
	"ON"	$I_{DD} (on)$	—	$R_{EXT} = 560\Omega$ , $OUT_n = Off$	—	13.5	20.0	

**SWITCHING CHARACTERISTICS** (Ta = 25°C unless otherwise noted)

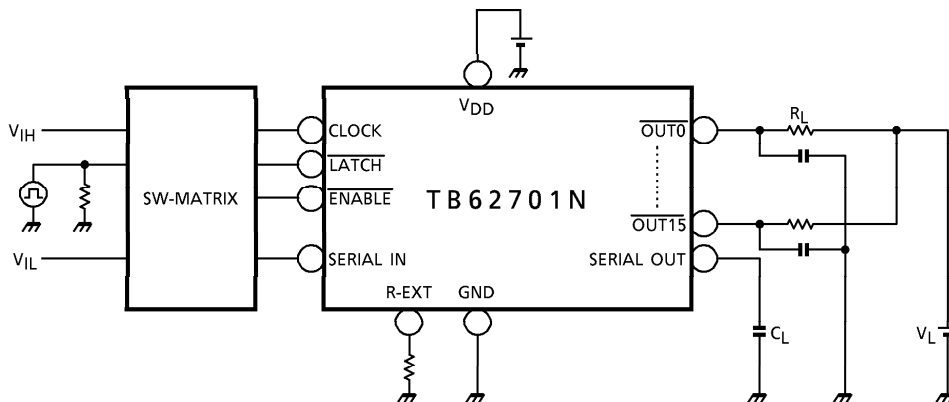
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CK-S-OUT	t <sub>pLH</sub>	V <sub>DD</sub> = 5.0V V <sub>CE</sub> = 1.0V V <sub>IH</sub> = V <sub>DD</sub> V <sub>IL</sub> = GND f <sub>CK</sub> = 2MHz R <sub>EXT</sub> = 560Ω I <sub>OUT</sub> = 30mA	—	95	500	ns
	CK- $\overline{\text{OUTn}}$			—	130	500	
	LATCH- $\overline{\text{OUTn}}$			—	130	500	
	EN- $\overline{\text{OUTn}}$			—	130	500	
Propagation Delay Time ("H" to "L")	CK-S-OUT	t <sub>pHL</sub>		—	95	720	ns
	CK- $\overline{\text{OUTn}}$			—	130	500	
	LATCH- $\overline{\text{OUTn}}$			—	130	500	
	EN- $\overline{\text{OUTn}}$			—	130	500	
Maximum Clock Frequency		f <sub>MAX</sub> (*1)		2.0	—	2.5	MHz
Minimum Pulse Width	CK	t <sub>w</sub> CK		—	45	80	ns
	LATCH	t <sub>w</sub> LAT		—	10	50	
Data Set Up Time		t <sub>setup</sub> (D)		—	17	50	ns
Data Hold Time		t <sub>hold</sub> (D)		—	-7	10	
Latch Set Up Time	LH	t <sub>LAT</sub> setup		—	70	200	ns
	HL		—	70	200		
Latch Hold Time	LH	t <sub>LAT</sub> hold	—	-70	50	ns	
	HL		—	-70	50		
Maximum Clock Rise Time		t <sub>r</sub>	—	—	10	μs	
Maximum Clock Fall Time		t <sub>f</sub>	—	—	10		
Maximum Output Rise Time		t <sub>or</sub>	—	35	80	ns	
Maximum Output Fall Time		t <sub>of</sub>	—	40	80		

\*1 : Cascade operation

**DC CHARACTERISTIC TEST CIRCUIT**

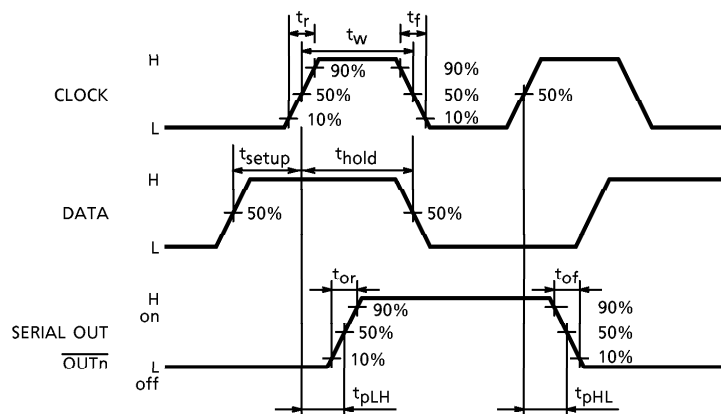


**AC CHARACTERISTIC TEST CIRCUIT**

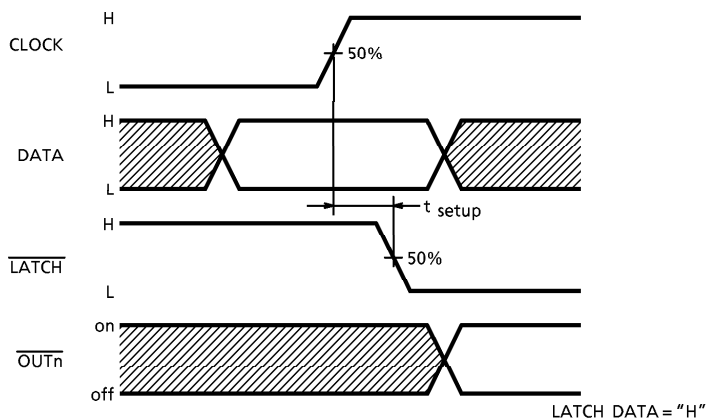


**TIMING WAVE FORM**

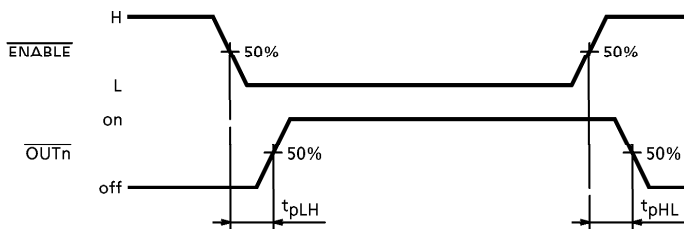
**1. CLOCK-SERIAL OUT,  $\overline{\text{OUTn}}$**



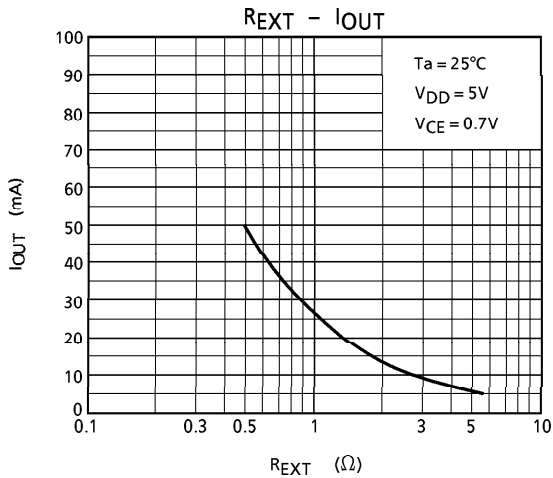
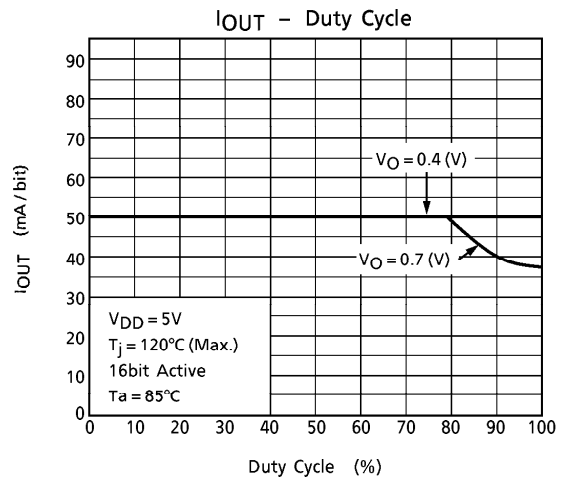
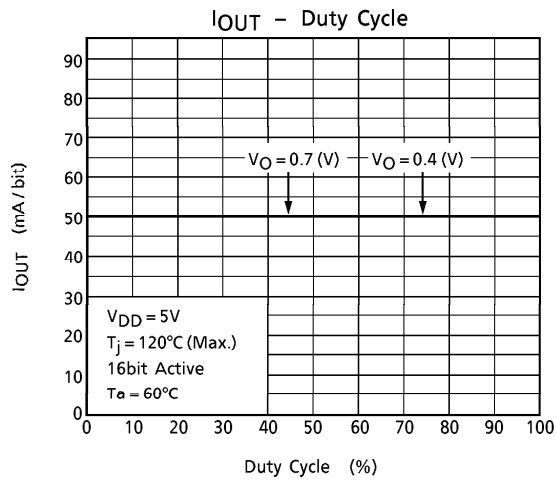
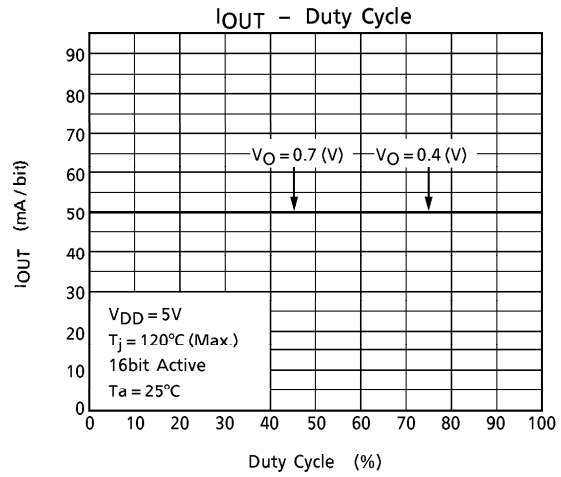
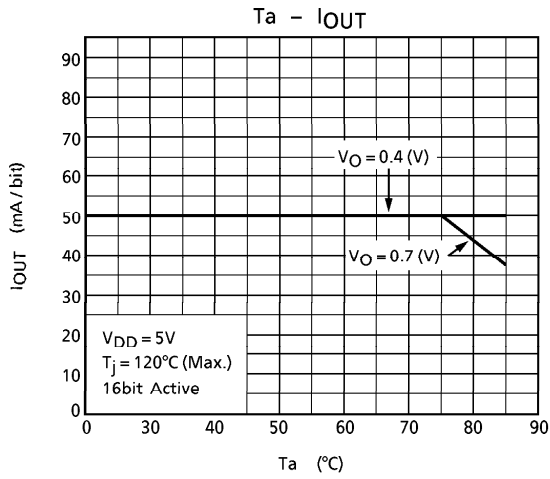
**2. CLOCK-LATCH**



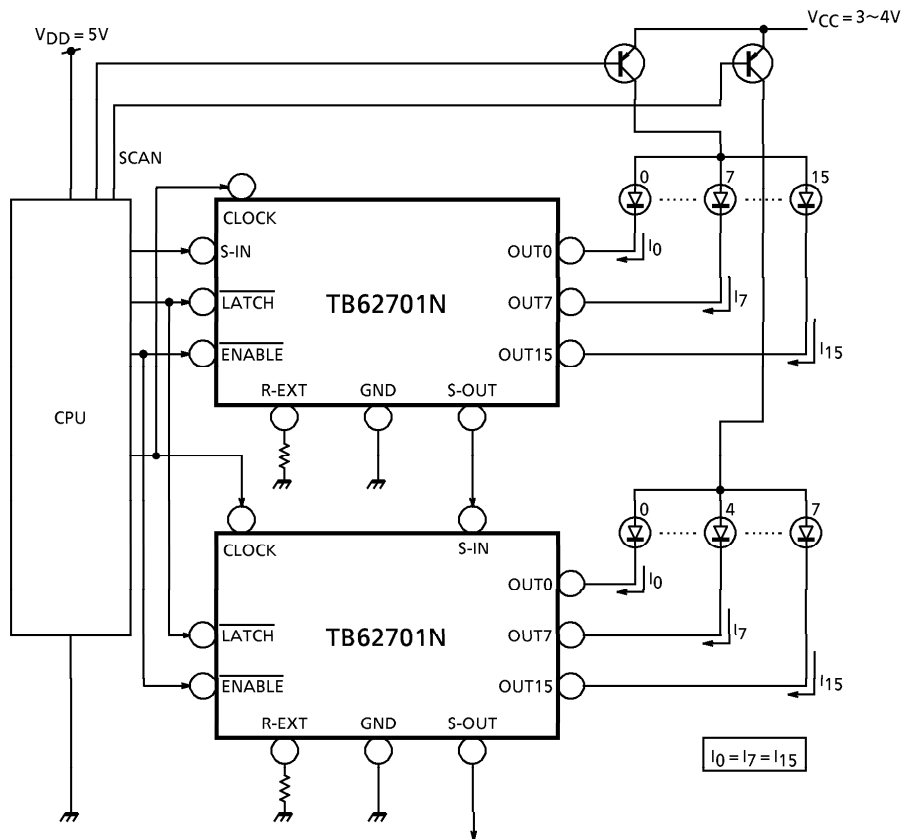
**3. ENABLE**





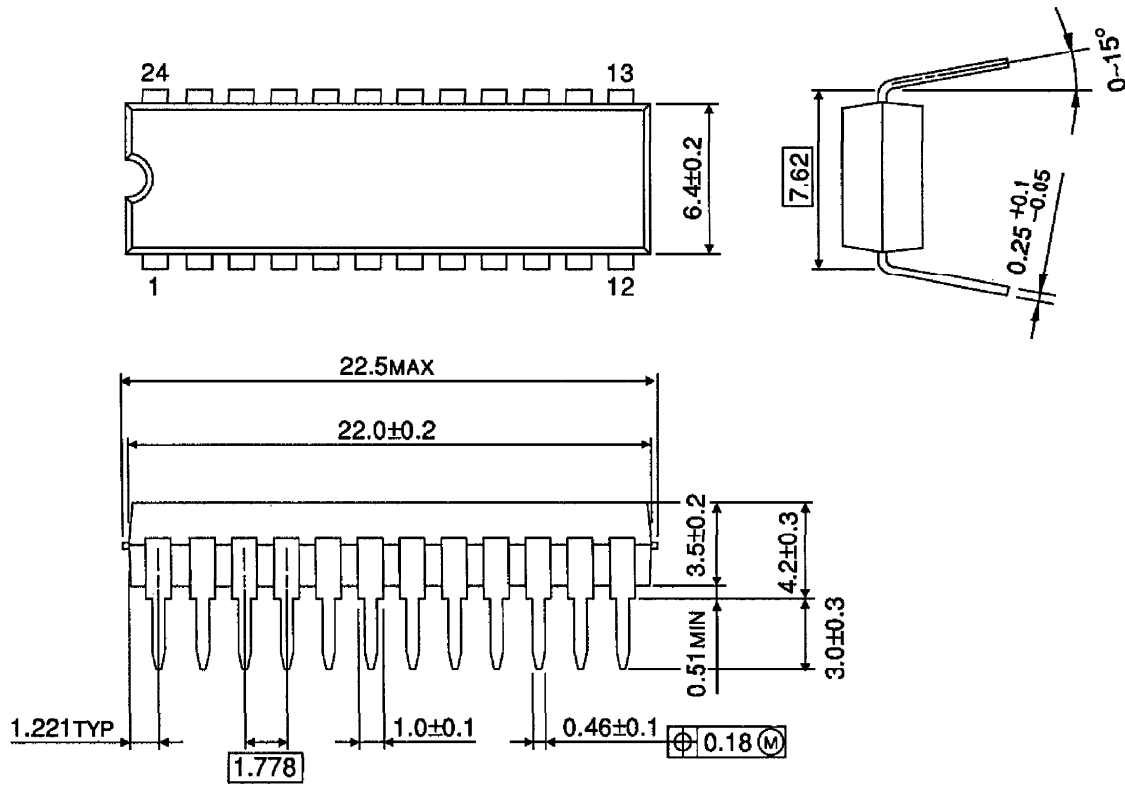


**APPLICATION CIRCUIT**



**OUTLINE DRAWING**  
SDIP24-P-300

Unit : mm



Weight : 1.2g (Typ.)