TC850

15-Bit, Fast Integrating CMOS A/D Converter

Features

- 15-bit Resolution Plus Sign Bit
- Up to 40 Conversions per Second
- Integrating ADC Technique
  - Monotonic
  - High Noise Immunity
  - Auto Zeroed Amplifiers Eliminate Offset Trimming
- Wide Dynamic Range: 96dB
- Low Input Bias Current: 30pA
- Low Input Noise: 30μV_{P-P}
- Sensitivity: 100μV
- Flexible Operational Control
- Continuous or On Demand Conversions
- Data Valid Output
- Bus Compatible, 3-State Data Outputs
  - 8-Bit Data Bus
  - Simple μP Interface
  - Two Chip Enables
  - Read ADC Result Like Memory
- ± 5V Power Supply Operation: 20mΩ
- 40-Pin Dual-in-Line or 44-Pin PLCC Packages

Applications

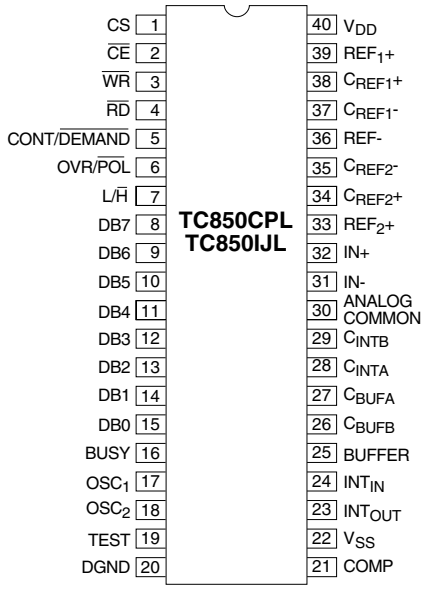
- Precision Analog Signal Processor
- Precision Sensor Interface
- High Accuracy DC Measurements

Device Selection Table

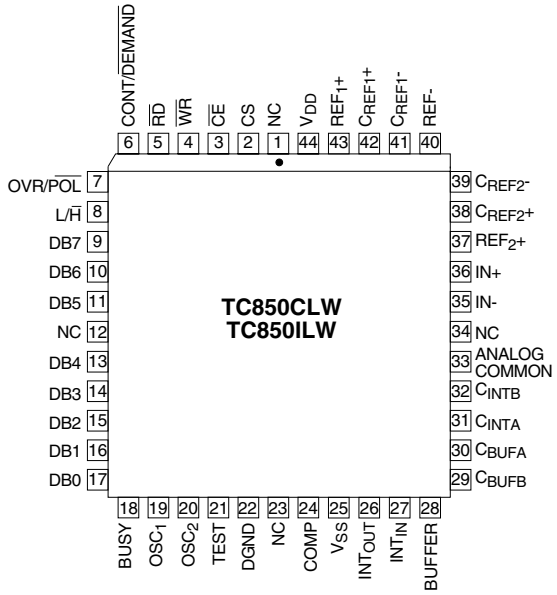
Part Number	Package	Temperature Range
TC850CPL	40-Pin PDIP	0°C to +70°C
TC850IJL	40-Pin CERDIP	-25°C to +85°C
TC850CLW	44-Pin PLCC	0°C to +70°C
TC850ILW	44-Pin PLCC	-25°C to +85°C

Package Types

40-Pin PDIP/CERDIP



44-Pin PLCC



NC = No Internal Connection

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General Description

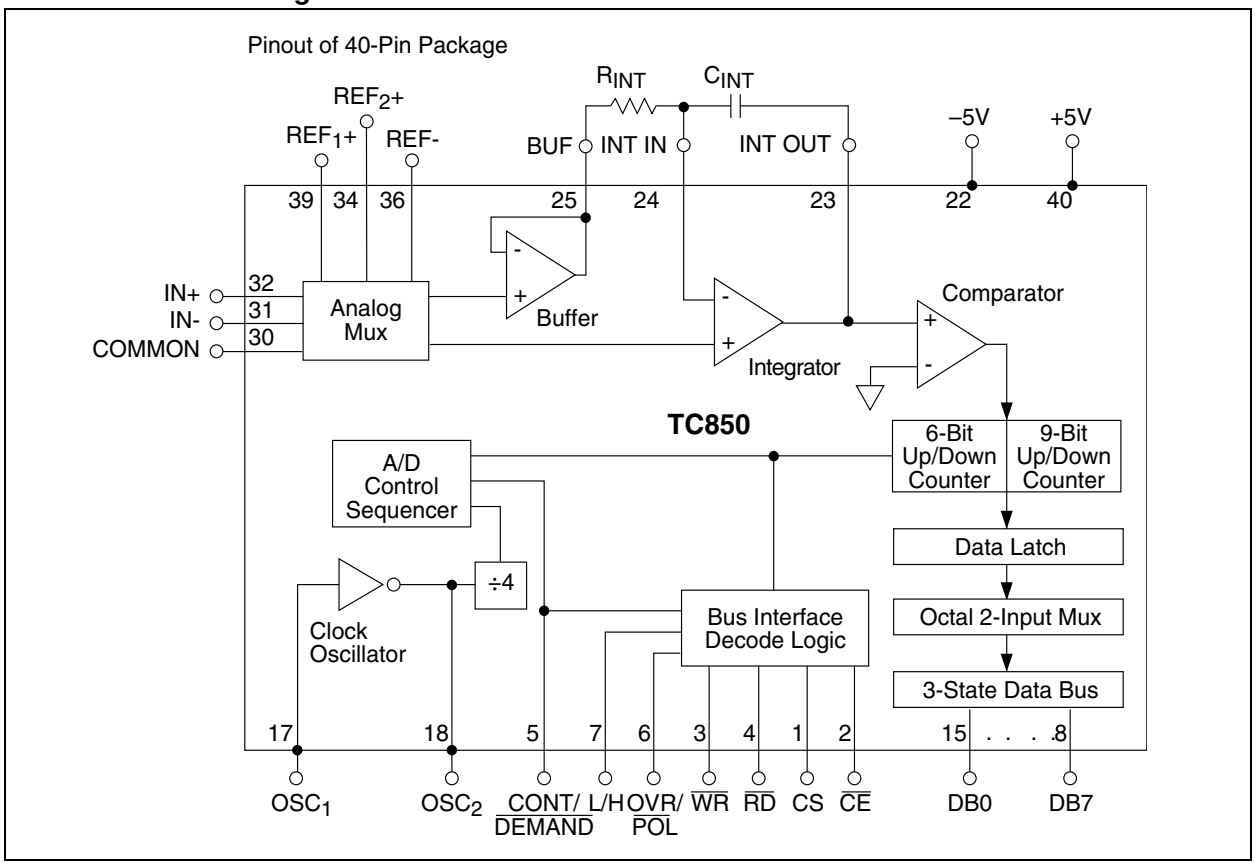
The TC850 is a monolithic CMOS A/D converter (ADC) with resolution of 15-bits plus sign. It combines a chopper-stabilized buffer and integrator with a unique multiple-slope integration technique that increases conversion speed. The result is 16 times improvement in speed over previous 15-bit, monolithic integrating ADCs (from 2.5 conversions per second up to 40 per second). Faster conversion speed is especially welcome in systems with human interface, such as digital scales.

The TC850 incorporates an ADC and a µP-compatible digital interface. Only a voltage reference and a few, noncritical, passive components are required to form a complete 15-bit plus sign ADC. CMOS processing provides the TC850 with high-impedance, differential inputs. Input bias current is typically only 30pA, permitting direct interface to sensors. Input sensitivity of 100µV per least significant bit (LSB) eliminates the need for precision external amplifiers. The internal amplifiers are auto zeroed, ensuring a zero digital output, with 0V analog input. Zero adjustment potentiometers or calibrations are not required.

The TC850 outputs data on an 8-bit, 3-state bus. Digital inputs are CMOS compatible while outputs are TTL/CMOS compatible. Chip-enable and byte-select inputs, combined with an end-of-conversion output, ensures easy interfacing to a wide variety of microprocessors. Conversions can be performed continuously or on command. In continuous mode, data is read as three consecutive bytes and manipulation of address lines is not required.

Operating from ±5V supplies, the TC850 dissipates only 20mΩ. The TC850 is packaged in a 40-pin plastic or ceramic dual-in-line package (DIPs) and in a 44-pin plastic leaded chip carrier (PLCC), surface-mount package.

Functional Block Diagram



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1.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Positive Supply Voltage.....+6V
Negative Supply Voltage..... - 9V
Analog Input Voltage (IN+ pr IN-)..... V_{DD} to V_{SS}
Voltage Reference Input:
(REF_1+, REF_1–, REF_2+)..... V_{DD} to V_{SS}
Logic Input Voltage.....V_{DD} + 0.3V to GND – 0.3V
Current Into Any Pin.....10mA
While Operating 100µA
Ambient Operating Temperature Range
C Device.....0°C to +70°C
I Device.....-25°C to +85°C
Package Power Dissipation ($T_A \leq 70°C$)
CerDIP 2.29Ω
Plastic DIP.....1.23Ω
Plastic PLCC 1.23Ω

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC850 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_S = ±5V; F_{CLK} = 61.44kHz, V_{FS} = 3.2768V, T_A = 25°C, Figure 1-1, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
	Zero Scale Error		±0.25	±0.5	LSB	V_{IN} = 0V
	End Point Linearity Error	—	±1	±2	LSB	$-V_{FS} \leq V_{IN} \leq +V_{FS}$
	Differential Nonlinearity	—	±0.1	±0.5	LSB	
I_{IN}	Input Leakage Current	—	30	75	pA	V_{IN} = 0V, T_A = 25°C
		—	1.1	3	nA	$-25° \leq T_A \leq +85°C$
V_{CMR}	Common Mode Voltage Range	V_{SS} + 1.5	—	V_{SS} – 1.5	V	Over Operating Temperature Range
CMRR	Common Mode Rejection Ratio	—	80	—	dB	V_{IN} = 0V, V_{CM} = ±1V
	Full Scale Gain Temperature Coefficient	—	2	5	ppm/°C	External Ref. Temperature Coefficient = 0 ppm/°C $0°C \leq T_A \leq +70°C$
	Zero Scale Error Temperature Coefficient	—	0.3	2	µV/°C	V_{IN} = 0V $0°C \leq T_A \leq +70°C$
	Full Scale Magnitude Symmetry Error	—	0.5	2	LSB	V_{IN} = ±3.275V
e_N	Input Noise	—	30	—	μV_{P-P}	Not Exceeded 95% of Time
I_S+	Positive Supply Current	—	2	3.5	mA	
I_S–	Negative Supply Current	—	2	3.5	mA	
V_{OH}	Output High Voltage	3.5	4.9	—	V	I_O = 500µA
V_{OL}	Output Low Voltage	—	0.15	0.4	V	I_O = 1.6mA
I_{OP}	Output Leakage Current	—	0.1	1	µA	Pins 8 -15, High-Impedance State
V_{IH}	Input High Voltage	3.5	2.3	—	V	Note 3
V_{IL}	Input Low Voltage	—	2.1	1	V	Note 3
I_{PU}	Input Pull-Up Current	—	4	—	µA	Pins 2, 3, 4, 6, 7; V_{IN} = 0V
I_{PD}	Input Pull-Down Current	—	14	—	µA	Pins 1, 5; V_{IN} = 5V
I_{OSC}	Oscillator Output Current	—	140	—	µA	Pin 18, V_{OUT} = 2.5V
C_{IN}	Input Capacitance	—	1	—	pF	Pins 1 - 7, 17
C_{OUT}	Output Capacitance	—	15	—	pF	Pins 8 -15, High-Impedance State

Note 1: Demand mode, CONT/$\overline{\text{DEMAND}}$ = LOW. Figure 8-5 timing diagram. C_L = 100pF.
2: Continuous mode, CONT/$\overline{\text{DEMAND}}$ = HIGH. Figure 8-7 timing diagram.
3: Digital inputs have CMOS logic levels and internal pull-up/pull-down resistors. For TTL compatibility, external pull-up resistors to V_{DD} are recommended.

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TC850 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: V_S = ±5V; F_{CLK} = 61.44kHz, V_{FS} = 3.2768V, T_A = 25°C, Figure 1-1, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{CE}	Chip-Enable Access Time	—	230	450	nsec	CS or $\overline{CE}$, $\overline{RD}$ = LOW (Note 1)
T_{RE}	Read-Enable Access Time	—	190	450	nsec	CS = HIGH, $\overline{CE}$ = LOW, (Note 1)
T_{DHC}	Data Hold From CS or $\overline{CE}$	—	250	450	nsec	$\overline{RD}$ = LOW, (Note 1)
T_{DHR}	Data Hold From $\overline{RD}$	—	210	450	nsec	CS = HIGH, $\overline{CE}$ = LOW, (Note 1)
T_{OP}	OVR/$\overline{POL}$ Data Access Time	—	140	300	nsec	CS = HIGH, $\overline{CE}$ = LOW, $\overline{RD}$ = LOW, (Note 1)
T_{LH}	Low/High Byte Access Time	—	140	300	nsec	CS = HIGH, $\overline{CE}$ = LOW, RD = LOW, (Note 1)
	Clock Setup Time	100	—	—	nsec	Positive or Negative Pulse Width
T_{WRE}	$\overline{RD}$ Minimum Pulse Width	450	230	—	nsec	CS = HIGH, $\overline{CE}$ = LOW, (Note 2)
T_{WRD}	$\overline{RD}$ Minimum Delay Time	150	50	—	nsec	CS = HIGH, $\overline{CE}$ = LOW, (Note 2)
T_{WWD}	$\overline{WR}$ Minimum Pulse Width	75	25	—	nsec	CS = HIGH, $\overline{CE}$ = LOW, (Note 1)

Note 1: Demand mode, CONT/$\overline{DEMAND}$ = LOW. Figure 8-5 timing diagram. C_L = 100pF.

2: Continuous mode, CONT/$\overline{DEMAND}$ = HIGH. Figure 8-7 timing diagram.

3: Digital inputs have CMOS logic levels and internal pull-up/pull-down resistors. For TTL compatibility, external pull-up resistors to V_{DD} are recommended.

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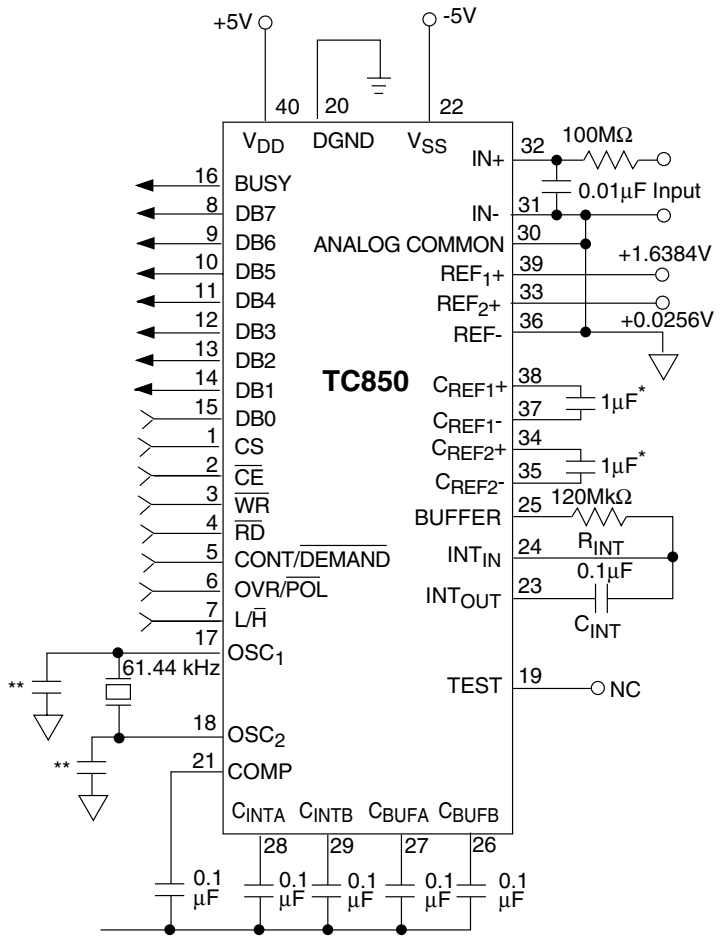
FIGURE 1-1: STANDARD TEST CIRCUIT CONFIGURATION



NOTES: Unless otherwise specified, all 0.1µF capacitors are film dielectric.
Ceramic capacitors are not recommended.
NC = No Connection
*Polypropylene capacitors.
** 100pF Mica capacitors.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table .

TABLE 2-1: PIN FUNCTION TABLE

Pin Number (40-Pin PDIP/CERDIP)	Pin Number (44-Pin PLCC)	Symbol	Description
1	2	CS	Chip select, active HIGH. Logically ANDed, with $\overline{CE}$ to enable read and write inputs (Note 1).
2	3	$\overline{CE}$	Chip enable, active LOW (Note 2).
3	4	$\overline{WR}$	Write input, active LOW. When chip is selected (CS = HIGH and $\overline{CE}$ = LOW) and in demand mode (CONT/$\overline{DEMAND}$ = LOW), a logic LOW on $\overline{WR}$ starts a conversion (Note 1).
4	5	$\overline{RD}$	Read input, active LOW. When CS = HIGH and $\overline{CE}$ = LOW, a logic LOW on $\overline{RD}$ enables the 3-state data outputs (Note 2).
5	6	CONT/ $\overline{DEMAND}$	Conversion control input. When CONT/$\overline{DEMAND}$ = LOW, conversions are initiated by the $\overline{WR}$ input. When CONT/$\overline{DEMAND}$ = HIGH, conversions are performed continuously (Note 1).
6	7	OVR/$\overline{POL}$	Overrange/polarity data-select input. When making conversions in the demand mode (CONT/$\overline{DEMAND}$ = LOW), OVR/$\overline{POL}$ controls the data output on DB7 when the high-order byte is active (Note 2).
7	8	L/$\overline{H}$	Low/high byte-select input. When CONT/$\overline{DEMAND}$ = LOW, this input controls whether low-byte or high-byte data is enabled on DB0 through DB7 (Note 2).
8	9	DB7	Most significant data bit output. When reading the A/D conversion result, the polarity, overrange and DB7 data are output on this pin.
9-15	10-17	DB6-DB0	Data outputs DB6-DB0. 3-state, bus compatible.
16	18	BUSY	A/D conversion status output. BUSY goes to a logic HIGH at the beginning of the de-integrate phase, then goes LOW when conversion is complete. The falling edge of BUSY can be used to generate a µP interrupt.
17	19	OSC_1	Crystal oscillator connection or external oscillator input.
18	20	OSC_2	Crystal oscillator connection.
19	21	TEST	For factory testing purposes only. Do not make external connection to this pin.
20	22	DGND	Digital ground connection.
21	24	COMP	Connection for comparator auto zero capacitor. Bypass to V_{SS} with 0.1µF.
22	25	V_{SS}	Negative power supply connection, typically -5V.
23	26	INT_{OUT}	Output of the integrator amplifier. Connect to C_{INT}.
24	27	INT_{IN}	Input to the integrator amplifier. Connect to summing node of R_{INT} and C_{INT}.
25	28	BUFFER	Output of the input buffer. Connect to R_{INT}.
26	29	C_{BUFB}	Connection for buffer auto zero capacitor. Bypass to V_{SS} with 0.1µF.
27	30	C_{BUFA}	Connection to buffer auto zero capacitor. Bypass to V_{SS} with 0.1µF.
28	31	C_{INTA}	Connection for integrator auto zero capacitor. Bypass to V_{SS} with 0.1µF.
29	32	C_{INTB}	Connection for integrator auto zero capacitor. Bypass to V_{SS} with 0.1µF.
30	33	ANALOG COMMON	Analog common.
31	35	IN–	Negative differential analog input.
32	36	IN+	Positive differential analog input.

Note 1: This pin incorporates a pull-down resistor to DGND.
2: This pin incorporates a pull-up resistor to V_{DD}.
3: Pins 1, 23 and 34 (44-PLCC) package are NC “No Internal connection.

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TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (40-Pin PDIP/CERDIP)	Pin Number (44-Pin PLCC)	Symbol	Description
33	37	REF_2+	Positive input for reference voltage V_{REF2}. ($V_{REF2} = V_{REF1}/64$)
34	38	$C_{REF2}+$	Positive connection for V_{REF2} reference capacitor.
35	39	$C_{REF2}-$	Negative connection for V_{REF2} reference capacitor.
36	40	REF–	Negative input for reference voltages.
37	41	$C_{REF1}-$	Negative connection for V_{REF1} reference capacitor.
38	42	$C_{REF1}+$	Positive connection for V_{REF1} reference capacitor.
39	43	REF_1+	Positive input for V_{REF1}.
40	44	V_{DD}	Positive power supply connection, typically +5V.

Note 1: This pin incorporates a pull-down resistor to DGND.
2: This pin incorporates a pull-up resistor to V_{DD}.
3: Pins 1, 23 and 34 (44-PLCC) package are NC “No Internal connection.

3.0 DETAILED DESCRIPTION

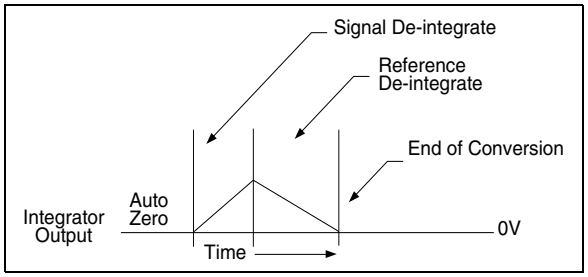
The TC850 is a multiple-slope, integrating A/D converter (ADC). The multiple-slope conversion process, combined with chopper-stabilized amplifiers, results in a significant increase in ADC speed, while maintaining very high resolution and accuracy.

3.1 Dual Slope Conversion Principles

The conventional dual slope converter measurement cycle (shown in Figure 3-1) has two distinct phases:

1. Input signal integration
2. Reference voltage integration (de-integration).

FIGURE 3-1: DUAL SLOPE ADC CYCLE



The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity constant reference voltage is then de-integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual slope converter, complete conversion requires the integrator output to "ramp-up" and "ramp-down." Most dual slope converters add a third phase, auto zero. During auto zero, offset voltages of the input buffer, integrator and comparator are nulled, thereby eliminating the need for zero offset adjustments.

Dual slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. By converting the unknown analog input voltage into an easily measured function of time, the dual slope converter reduces the need for expensive, precision passive components.

Noise immunity is an inherent benefit of the integrating conversion method. Noise spikes are integrated, or averaged, to zero during the integration period. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments.

A simple mathematical equation relates the input signal, reference voltage and integration time:

EQUATION 3-1:

$$\frac{1}{R_{INT}C_{INT}}\int_0^{T_{INT}} V_{IN}(T)DT = \frac{V_{REF}\,T_{DEINT}}{R_{INT}C_{INT}}$$

where:

V_{REF} = Reference voltage

T_{INT} = Signal integration time (fixed)

T_{DEINT} = Reference voltage integration time (variable).

3.2 Multiple Slope Conversion Principles

One limitation of the dual slope measurement technique is conversion speed. In a typical dual slope method, the auto zero and integrate times are each one-half of the de-integrate time. For a 15-bit conversion, $2^{14} + 2^{14} + 2^{15}$ (65,536) clock pulses are required for auto zero, integrate and de-integrate phases, respectively. The large number of clock cycles effectively limits the conversion rate to about 2.5 conversions per second, when a typical analog CMOS fabrication process is used.

The TC850 uses a multiple slope conversion technique to increase conversion speed (Figure 3-2). This technique makes use of a two-slope de-integration phase and permits 15-bit resolution up to 40 conversions per second.

During the TC850's de-integration phase, the integration capacitor is rapidly discharged to yield a resolution of 9 bits. At this point, some charge will remain on the capacitor. This remaining charge is then slowly de-integrated, producing an additional 6 bits of resolution. The result is 15 bits of resolution achieved with only $2^9 + 2^6$ (512 + 64, or 576) clock pulses for de-integration. A complete conversion cycle occupies only 1280 clock pulses.

In order to generate "fast-slow" de-integration phases, two voltage references are required. The primary reference (V_{REF1}) is set to one-half of the full scale voltage (typically V_{REF1} = 1.6384V, and V_{FS} = 3.2768V). The secondary voltage reference (V_{REF2}) is set to $V_{REF1}/64$ (typically 25.6 mV). To maintain 15-bit linearity, a tolerance of 0.5% for V_{REF2} is recommended.

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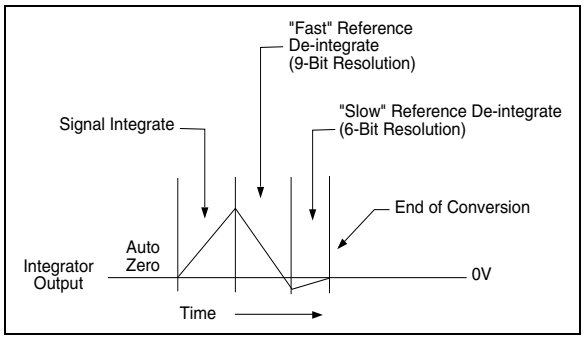
FIGURE 3-2: "FAST SLOW" REFERENCE DE-INTEGRATION CYCLE



4.0 ANALOG SECTION DESCRIPTION

The TC850 analog section consists of an input buffer amplifier, integrator amplifier, comparator and analog switches. A simplified block diagram is shown in Figure 4-1.

4.1 Conversion Timing

Each conversion consists of three phases:

1. Zero Integrator
2. Signal Integrate
3. Reference Integrate (or De-integrate)

Each conversion cycle requires 1280 internal clock cycles (Figure 4-2).

FIGURE 4-1: ANALOG SECTION SIMPLIFIED SCHEMATIC

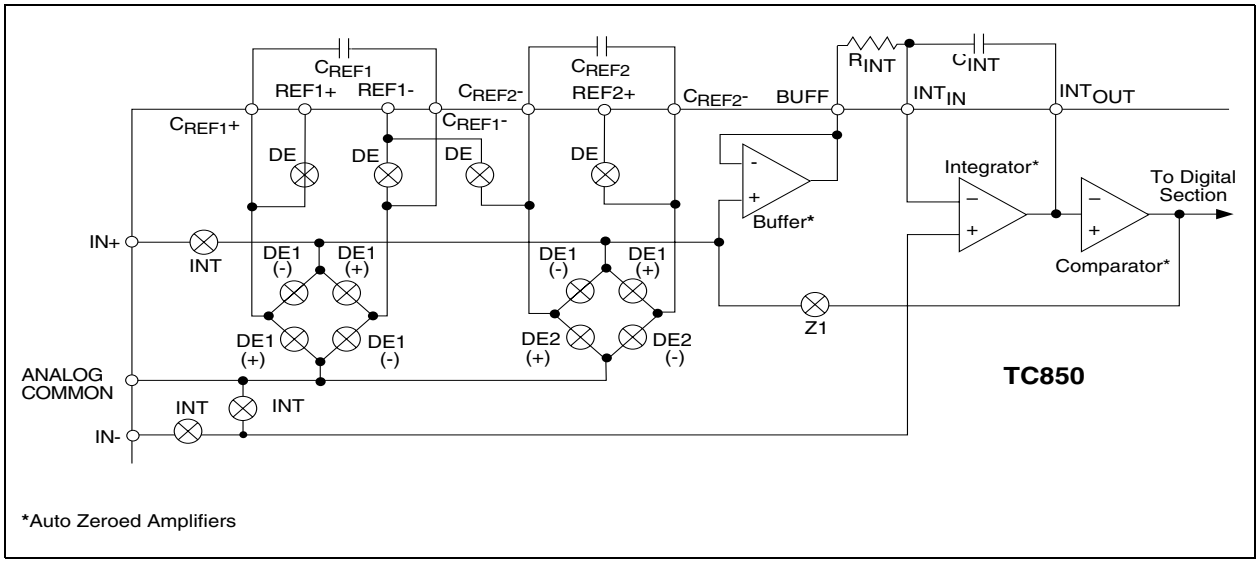
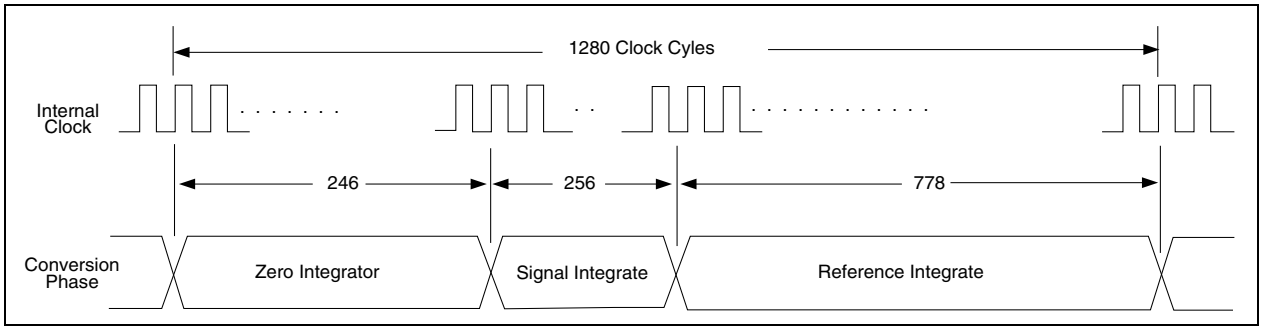


FIGURE 4-2: CONVERSION TIMING



4.2 Zero Integrator Phase

During the zero integrator phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. At the same time, a feedback loop is closed around the input buffer, integrator and comparator. The feedback loop ensures the integrator output is near 0V before the signal integrate phase begins.

During this phase, a chopper-stabilization technique is used to cancel offset errors in the input buffer, integrator and comparator. Error voltages are stored on the C_{BUFF}, C_{INT} and COMP capacitors. The zero integrate phase requires 246 clock cycles.

4.3 Signal Integrate Phase

The zero integrator loop is opened and the internal differential inputs are connected to IN+ and IN-. The differential input signal is integrated for a fixed time period. The TC850 signal integrate period is 256 clock periods, or counts. The crystal oscillator frequency is ÷4 before clocking the internal counters.

The integration time period is:

EQUATION 4-1:

$$T_{INT} = \frac{4 \times 256}{F_{OSC}}$$

4.4 Reference Integrate Phase

During reference integrate phase, the charge stored on the integrator capacitor is discharged. The time required to discharge the capacitor is proportional to the analog input voltage.

The reference integrate phase is divided into three subphases:

1. Fast
2. Slow
3. Overrange de-integrate

During fast de-integrate, V_{IN}- is internally connected to analog common and V_{IN}+ is connected across the previously-charged reference capacitor (C_{REF1}). The integrator capacitor is rapidly discharged for a maximum of 512 internal clock pulses, yielding 9 bits of resolution.

During the slow de-integrate phase, the internal V_{IN}+ node is now connected to the C_{REF2} capacitor and the residual charge on the integrator capacitor is further discharged a maximum of 64 clock pulses. At this point, the analog input voltage has been converted with 15 bits of resolution.

If the analog input is greater than full scale, the TC850 performs up to three overrange de-integrate subphases. Each subphase occupies a maximum of 64 clock pulses. The overrange feature permits analog inputs up to 192 LSBs greater than full scale to be correctly converted. This feature permits the user to digitally null up to 192 counts of input offset, while retaining full 15-bit resolution.

In addition to 512 counts of fast, 64 counts of slow and 192 counts of overrange de-integrate, the reference integrate phase uses 10 clock pulses to permit internal nodes to settle. Therefore, the reference integrate cycle occupies 778 clock pulses.

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5.0 PIN DESCRIPTION (ANALOG)

5.1 Differential Inputs (IN+ and IN–)

The analog signal to be measured is applied at the IN+ and IN– inputs. The differential input voltage must be within the Common mode range of the converter. The input Common mode range extends from V_{DD} - 1.5V to V_{SS} +1.5V. Within this Common mode voltage range, an 80 dB CMRR is typical.

The integrator output also follows the Common mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large, positive Common mode voltage, with a near full scale negative differential input voltage, is applied. The negative input signal drives the integrator positive when most of its available swing has been used up by the positive Common mode voltage. For applications where maximum Common mode range is critical, integrator swing can be reduced. The integrator output can swing within 0.4V of either supply without loss of linearity.

5.2 Differential Reference (V_{REF})

The TC850 requires two reference voltage sources in order to generate the "fast-slow" de-integrate phases. The main voltage reference (V_{REF1}) is applied between the REF_1+ and REF- pins. The secondary reference (V_{REF2}) is applied between the REF_2+ and REF- pins.

The reference voltage inputs are fully differential and the reference voltage can be generated anywhere within the power supply voltage of the converter. However, to minimize rollover error, especially at high conversion rates, keep the reference Common mode voltage (i.e., REF-) near or at the analog common potential. All voltage reference inputs are high impedance. Average reference input current is typically only 30pA.

5.3 Analog Common (ANALOG COMMON)

Analog common is used as the IN- return during the zero integrator and de-integrate phases of each conversion. If IN- is at a different potential than analog common, a Common mode voltage exists in the system. This signal is rejected by the 80dB CMRR of the converter. However, in most applications, IN- will be set at a fixed, known voltage (power supply common, for instance). In this case, analog common should be tied to the same point so that the Common mode voltage is eliminated.

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6.0 DIGITAL SECTION DESCRIPTION

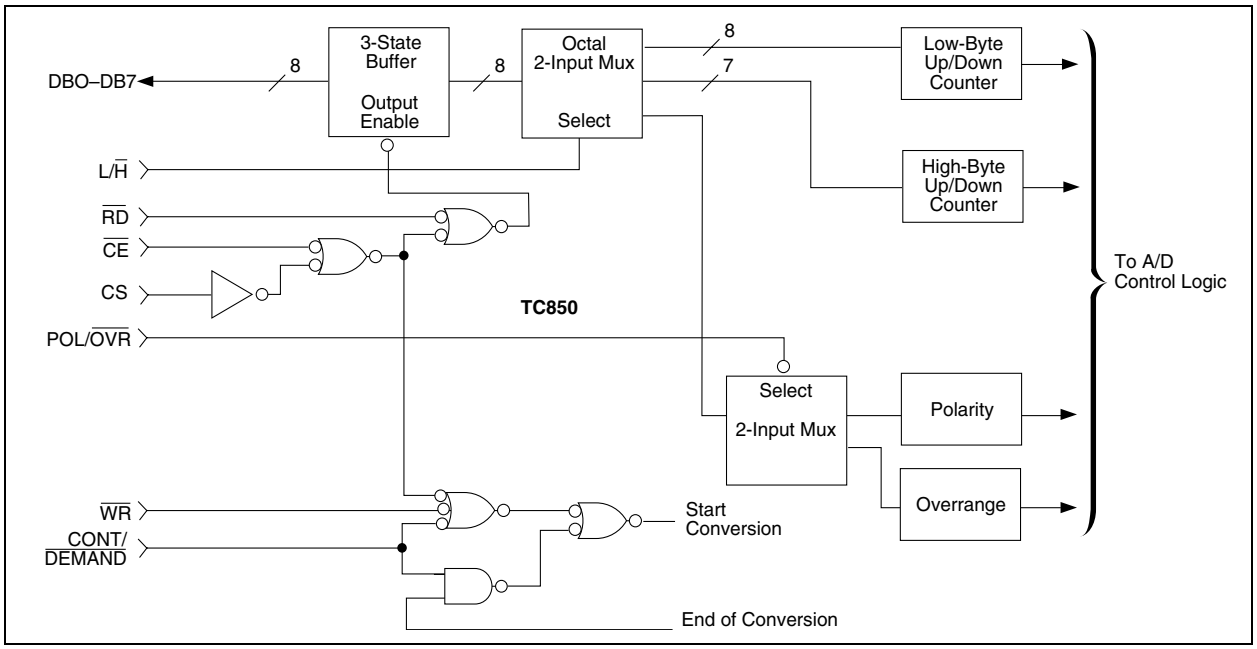
The TC850 digital section consists of two sets of conversion counters, control and sequencing logic, clock oscillator and divider, data latches and an 8-bit, 3-state interface bus. A simplified schematic of the bus interface logic is shown in Figure 6-1

6.1 Clock Oscillator

The TC850 includes a crystal oscillator on-chip. All that is required is to connect a crystal across OSC_1 and OSC_2 pins and to add two inexpensive capacitors (Figure 1-1). The oscillator output is ÷ 4 prior to clocking the A/D internal counters. For example, a 100kHz crystal produces a system clock frequency of 25kHz. Since each conversion requires 1280 clock periods, in this case the conversion rate will be 25,000/1280, or 19.5 conversions per second.

In most applications, however, an external clock is divided down from the microprocessor clock. In this case, the OSC_1 pin is used as the external oscillator input and OSC_2 is left unconnected. The external clock driver should swing from digital ground to V_{DD}. The ÷ 4 function is active for both external clock and crystal oscillator operations.

FIGURE 6-1: BUS INTERFACE SIMPLIFIED SCHEMATIC



6.2 Digital Operating Modes

Two modes of operation are available with the TC850, continuous conversions and on-demand. The operating mode is controlled by the CONT/DEMAND input. The bus interface method is different for continuous and demand modes of operation.

6.2.1 DEMAND MODE OPERATION

When CONT/DEMAND is low, the TC850 performs one conversion each time the chip is selected and the WR input is pulsed low. Data is valid on the falling edge of the BUSY output and can be accessed using the interface truth table (Table 6-1).

6.2.2 CONTINUOUS MODE OPERATION

When CONT/DEMAND is high, the TC850 continuously performs conversions. Data will be valid on the falling edge of the BUSY output and remains valid for 443-1/2 clock cycles.

The low/high (L/H) byte-select and overrange/polarity (OVR/POL) inputs are disabled during continuous mode operation. Data must be read in three consecutive bytes, as shown in Table 6-1.

Note:	In continuous mode, the conversion result must be read within 443-1/2 clock cycles of the BUSY output falling edge. After this time (i.e.,1/2 clock cycle before BUSY goes high) the internal counters are reset and the data is lost.

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TABLE 6-1: BUS INTERFACE TRUTH TABLE

$\overline{CE}$ • CS Pins 1 and 2	$\overline{RD}$ Pin 4	CONT/$\overline{DEMAND}$ Pin 5	L/$\overline{H}$ Pin 7	OVR/$\overline{POL}$ Pin 6	DB7 Pin 8	DB6–DB0 Pin 9-Pin 15 (Note 1)
0	0	0	0	0	"1" = Input Positive	Data Bits 14 - 8
0	0	0	0	1	"1" = Input Overrange (Note 2)	Data Bits 14 - 8
0	0	0	1	X	Data Bit 7	Data Bits 6 - 0
0	0	1	X	X	Note 3	
0	1	X	X	X	High-Impedance State	
1	X	X	X	X	High-Impedance State	

Note 1: Pin numbers refer to 40-pin PDIP.

2: Extended overrange operation: Although rated at 15 bits (±32,767 counts) of resolution, the TC850 provides an additional 191 counts above full scale. For example, with a full-scale input of 3.2768V, the maximum analog input voltage which will be properly converted is 3.2958V. The extended resolution is signified by the overrange bit being high and the low-order byte contents being between 0 and 190. For example, with a full-scale voltage of 3.2768V:

V_{IN}	Overrange Bit	Low Byte	Data Bits 14–8
3.2767V	Low	255_{10}	127_{10}
3.2768V	High	000_{10}	0_{10}
3.2769V	High	001_{10}	0_{10}
3.2867V	High	099_{10}	0_{10}

3: Continuous mode data transfer:

a. In continuous mode, data MUST be read in three sequential bytes after the BUSY output goes low:
   (1) The first byte read will be the high-order byte, with DB7 = polarity.
   (2) The second byte read will contain the low-order byte.
   (3) The third byte read will again be the high-order byte, but with DB7 = overrange.

b. All three data bytes must be read within 443-1/2 clock cycles after the falling edge of BUSY.

c. The $\overline{c}$ input must go high after each byte is read, so that the internal byte counter will be incremented. However, the CS and $\overline{CE}$inputs can remain enabled through the entire data transfer sequence.

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6.3 Pin Description (Digital)

6.3.1 CHIP SELECT AND CHIP ENABLE (CS AND $\overline{CE}$)

The CS and CE inputs permit easy interfacing to a variety of digital bus systems. $\overline{CE}$ is active LOW while CS is active HIGH. These inputs are logically ANDed internally and are used to enable the $\overline{RD}$ and $\overline{WR}$ inputs.

6.3.2 WRITE ENABLE INPUT ($\overline{WR}$)

The write input is used to initiate a conversion when the TC850 is in demand mode. CS and $\overline{CE}$ must be active for the $\overline{WR}$ input to be recognized. The status of the data bus is meaningless during the $\overline{WR}$ pulse, because no data is actually written into the TC850.

6.3.3 READ ENABLE INPUT ($\overline{RD}$)

The read input, combined with CS and $\overline{CE}$, enable the 3-state data bus outputs. Also, in continuous mode, the rising edge of the $\overline{RD}$ input activates an internal byte counter to sequentially read the three data bytes.

6.3.4 LOW/HIGH BYTE SELECT (L/$\overline{H}$)

The L/$\overline{H}$ input determines whether the low (least significant) byte or high (most significant) byte of data is placed on the 3-state data bus. This input is meaningful only when the TC850 is in the demand mode. In the continuous mode, data must be read in three predetermined bytes, so the L/$\overline{H}$ input is ignored.

6.3.5 OVERRANGE/POLARITY BIT SELECT (OVR/$\overline{POL}$)

The TC850 provides 15 bits of resolution, plus polarity and overrange bits. Thus, 17 bits of information must be transferred on an 8-bit data bus. To accomplish this, the overrange and polarity bits are multiplexed onto data bit DB7 of the most significant byte. When OVR/$\overline{POL}$ is HIGH, DB7 of the high byte contains the overrange status (HIGH = analog input overrange, LOW = input within full scale). When OVR/$\overline{POL}$ is LOW, DB7 is HIGH for positive analog input polarity and LOW for negative polarity. The OVR/$\overline{POL}$ input is meaningful only when CS, $\overline{CE}$ and $\overline{RD}$ are active, and L/$\overline{H}$ is LOW (i.e., the most significant byte is selected). OVR/$\overline{POL}$ is ignored when the TC850 is in continuous mode.

6.3.6 CONTINUOUS/DEMAND MODE INPUT (CONT/$\overline{DEMAND}$)

This input controls the TC850 operating mode. When CONT/$\overline{DEMAND}$ is HIGH, the TC850 performs conversions continuously. In continuous mode, data must be read in the prescribed sequence shown in Table 6-1. Also, all three data bytes must be read within 443-1/2 internal clock cycles after the BUSY output goes low. After 443-1/2 clock cycles data will be lost.

When CONT/$\overline{DEMAND}$ is LOW, the TC850 begins a conversion each time CS and $\overline{CE}$ are active and $\overline{WR}$ is being pulsed LOW. The conversion is complete and data can be read after the falling edge of the BUSY output. In demand mode, data can be read in any sequence and remains valid until $\overline{WR}$ is again pulsed LOW.

6.3.7 BUSY OUTPUT (BUSY)

The BUSY output is used to convey an end-of-conversion to external logic. BUSY goes HIGH at the beginning of the de-integrate phase and goes LOW at the end of the conversion cycle. Data is valid on the falling edge of BUSY. The output-high period is fixed at 836 clock periods, regardless of the analog input value. BUSY is active during continuous and demand mode operation.

This output can also be used to generate an end-of-conversion interrupt in µP-based systems. Noninterrupt-driven systems can poll BUSY to determine when data is valid.

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7.0 ANALOG SECTION TYPICAL APPLICATIONS

7.1 Component Selection

7.1.1 REFERENCE VOLTAGE

The typical value for reference voltage V_{REF1} is 1.6384V. This value yields a full scale voltage of 3.2768V and resolution of 100µV per step. The V_{REF2} value is derived by dividing V_{REF1} by 64. Thus, typical V_{REF2} value is 1.6384V/64, or 25.6mV. The V_{REF2} value should be adjusted within ±1% to maintain 15-bit accuracy for the total conversion process;

EQUATION 7-1: :

$$V_{REF} = \frac{V_{REF1} \pm 1\%}{64}$$

The reference voltage is not limited to exactly 1.6384V, however, because the TC850 performs a ratiometric conversion. Therefore, the conversion result will be:

EQUATION 7-2:

$$\text{Digital Counts} = \frac{V_{IN}}{V_{REF1}} \bullet 16384$$

The full scale voltage can range from 3.2V to 3.5V. Full scale voltages of less than 3.2V will result in increased noise in the least significant bits, while a full scale above 3.5V will exceed the input common-mode range.

7.1.2 INTEGRATION RESISTOR

The TC850 buffer supplies 25µA of integrator charging current with minimal linearity error. R_{INT} is easily calculated:

EQUATION 7-3:

$$R_{INT} = \frac{V_{FULLSCALE}}{25\mu A}$$

For a full scale voltage of 3.2768V, values of R_{INT} between 120kΩ and 150kΩ are acceptable.

7.1.3 INTEGRATION CAPACITOR

The integration capacitor should be selected to produce an integrator swing of ≈ 4V at full scale. The capacitor value is easily calculated:

EQUATION 7-4:

$$C = \frac{V_{FS}}{R_{INT}} \bullet \frac{4 \bullet 256}{4V\ F_{CLOCK}}$$

where:

F_{CLOCK} is the crystal or external oscillator frequency and V_{FS} is the maximum input voltage.

The integration capacitor should be selected for low dielectric absorption to prevent rollover errors. A polypropylene, polyester or polycarbonate dielectric capacitor is recommended.

7.1.4 REFERENCE CAPACITORS

The reference capacitors require a low-leakage dielectric, such as polypropylene, polyester or polycarbonate. A value of 1µF is recommended for operation over the temperature range. If high-temperature operation is not required, the C_{REF} values can be reduced.

7.1.5 AUTO ZERO CAPACITORS

Five capacitors are required to auto zero the input buffer, integrator amplifier and comparator. Recommended capacitors are 0.1µF film dielectric (such as polyester or polypropylene). Ceramic capacitors are not recommended.

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8.0 DIGITAL SECTION TYPICAL APPLICATIONS

8.1 Oscillator

The TC850 may operate with a crystal oscillator. The crystal selected should be designed for a Pierce oscillator, such as an AT-cut quartz crystal. The crystal oscillator schematic is shown in Figure 8-1.

Since low frequency crystals are very large and ceramic resonators are too lossy, the TC850 clock should be derived from an external source, such as a microprocessor clock. The clock should be input on the OSC_1 pin and no connection should be made to the OSC_2 pin. The external clock should swing between DGND and V_{DD}.

Since oscillator frequency is ÷4 internally and each conversion requires 1280 internal clock cycles, the conversion time will be:

EQUATION 8-1:

$$\text{Conversion Time} = \frac{4 \times 1280}{F_{CLOCK}}$$

An important advantage of the integrating ADC is the ability to reject periodic noise. This feature is most often used to reject line frequency (50Hz or 60Hz) noise. Noise rejection is accomplished by selecting the integration period equal to one or more line frequency cycles. The desired clock frequency is selected as follows:

EQUATION 8-2:

$$F_{CLOCK} = F_{NOISE} \times 4 \times 256$$

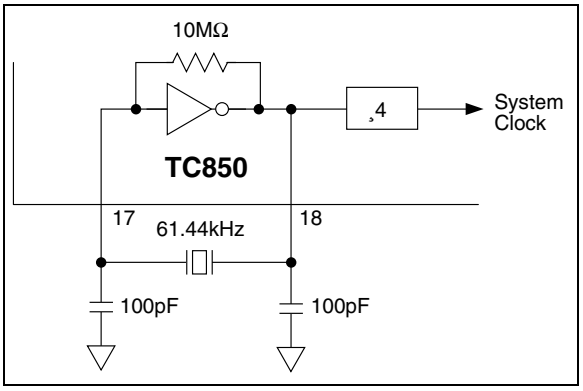
where:

F_{NOISE} is the noise frequency to be rejected,
4 represents the clock divider,
256 is the number of integrate cycles.

For example, 60Hz noise will be rejected with a clock frequency of 61.44kHz, giving a conversion rate of 12 conversions/sec. Integer submultiples of 61.44kHz (such as 30.72kHz, etc.) will also reject 60Hz noise. For 50Hz noise rejection, a 51.2kHz frequency is recommended.

If noise rejection is not important, other clock frequencies can be used. The TC850 will typically operate at conversion rates ranging from 3 to 40 conversions/sec, corresponding to oscillator frequencies from 15.36kHz to 204.8kHz.

FIGURE 8-1: CRYSTAL OSCILLATOR SCHEMATIC



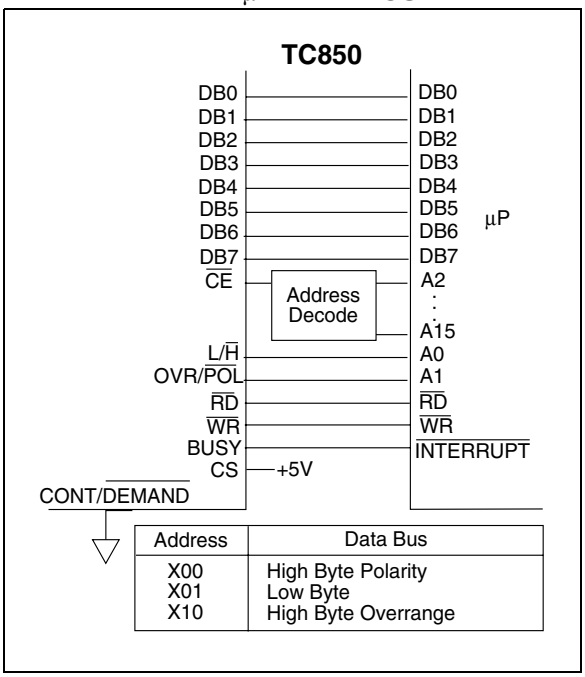
8.2 Data Bus Interfacing

The TC850 provides an easy and flexible digital interface. A 3-state data bus and six control inputs permit the TC850 to be treated as a memory device, in most applications. The conversion result can be accessed over an 8-bit bus or via a µP I/O port.

A typical µP bus interface for the TC850 is shown in Figure 8-2. In this example, the TC850 operates in the demand mode and conversion begins when a write operation is performed to any decoded address space. The BUSY output interrupts the µP at the end-of-conversion.

The A/D conversion result is read as three memory bytes. The two LSBs of the address bus select high/low byte and overrange/polarity bit data, while high-order address lines enable the $\overline{CE}$ input.

FIGURE 8-2: INTERFACE TO TYPICAL µP DATA BUS



Address	Data Bus
X00	High Byte Polarity
X01	Low Byte
X10	High Byte Overrange

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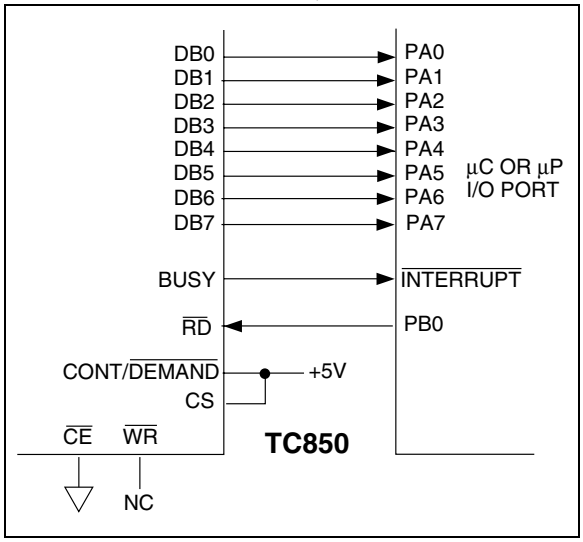
Figure 8-3 shows a typical interface to a µP I/O port or single-chip µC. The TC850 operates in the continuous mode and can either interrupt the µC/µP or be polled with an input pin.

FIGURE 8-3: INTERFACE TO TYPICAL µP I/O PORT OR SINGLE-CHIP µC



Since the PA0-PA7 inputs are dedicated to reading A/D data, the A/D CS/CE inputs can be enabled continuously. In continuous mode, data must be read in 3 bytes, as shown in Table 6-1. The required RD pulses are provided by a µC/µP output pin.

The circuit of Figure 8-3 can also operate in the demand mode, with the start-up conversion strobe generated by a µC/µP output pin. In this case, the L/H and CONT/DEMAND inputs can be controlled by I/O pins and the RD input connected to digital ground.

8.3 Demand Mode Interface Timing

When CONT/DEMAND input is LOW, the TC850 performs a conversion each time CE and CS are active and WR is strobed LOW.

The demand mode conversion timing is shown in Figure 8-4. BUSY goes LOW and data is valid 1155 clock pulses after WR goes LOW. After BUSY goes low, 125 additional clock cycles are required before the next conversion cycle will begin.

Once conversion is started, WR is ignored for 1100 internal clock cycles. After 1100 clock cycles, another WR pulse is recognized and initiates a new conversion when the present conversion is complete. A negative edge on WR is required to begin conversion. If WR is held LOW, conversions will not occur continuously.

The A/D conversion data is valid on the falling edge of BUSY and remains valid until one-half internal clock cycle before BUSY goes HIGH on the succeeding conversion. BUSY can be monitored with an I/O pin to determine end of conversion or to generate a µP interrupt.

In demand mode, the three data bytes can be read in any desired order. The TC850 is simply regarded as three bytes of memory and accessed accordingly. The bus output timing is shown in Figure 8-5.

8.4 Continuous Mode Interface Timing

When the CONT/DEMAND input is HIGH, the TC850 performs conversions continuously. Data will be valid on the falling edge of BUSY and all three bytes must be read within 443-1/2 internal clock cycles of BUSY going LOW. The timing diagram is shown in Figure 8-6.

In continuous mode, OVR/POL and L/H byte-select inputs are ignored. The TC850 automatically cycles through three data bytes, as shown in Table 6-1. Bus output timing in the continuous mode is shown in Figure 8-7.

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FIGURE 8-4: CONVERSION TIMING, DEMAND MODE

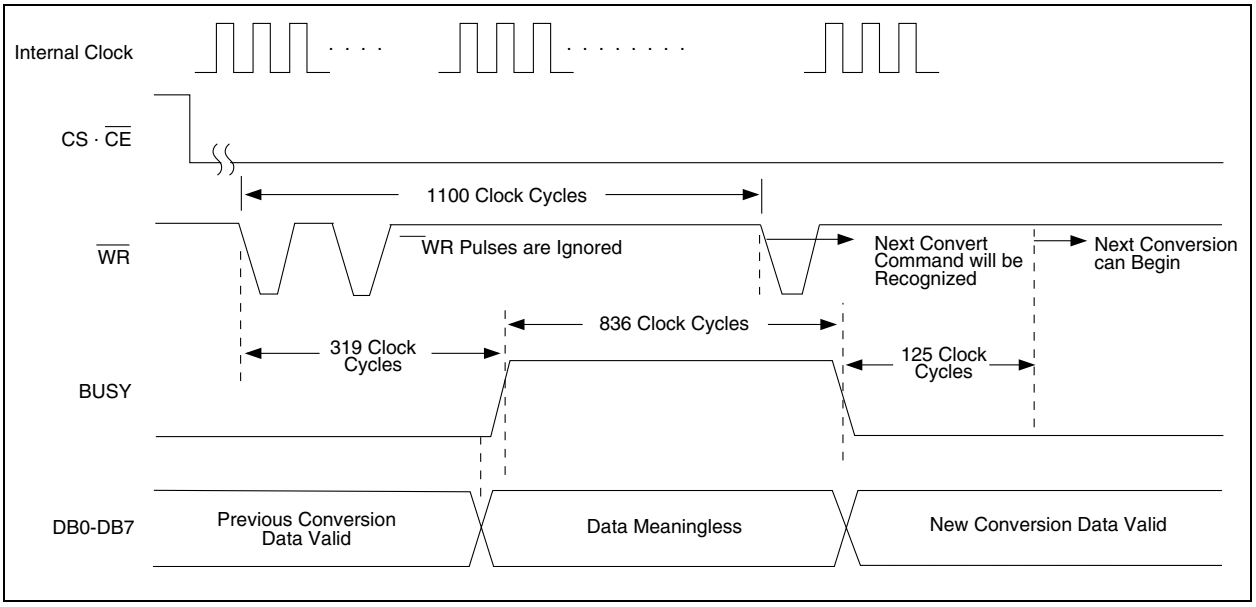
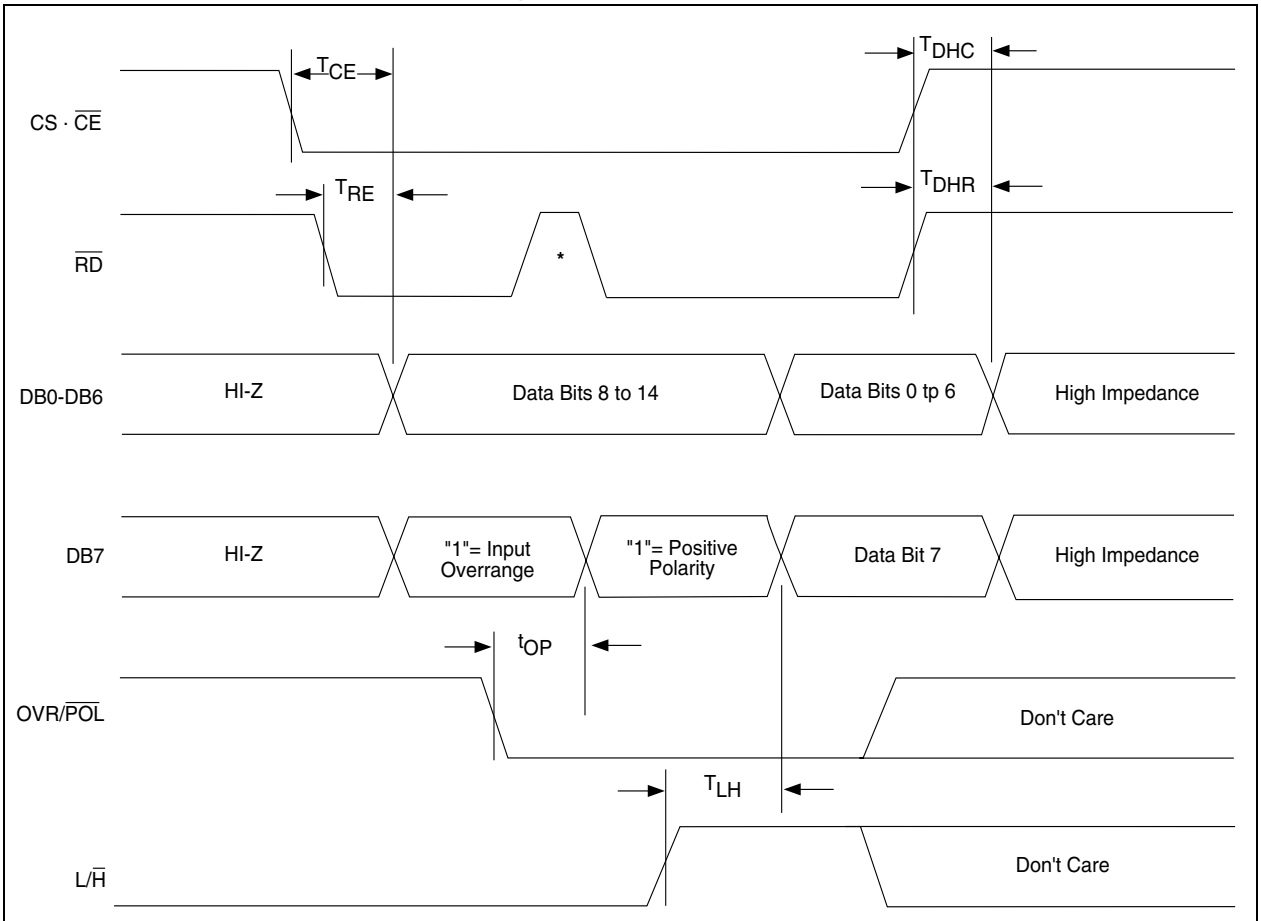


FIGURE 8-5: BUS OUTPUT TIMING, DEMAND MODE



NOTE: CONT/DEMAND = LOW

*RD (as well as CS and CE) can go HIGH after each byte is read (i.e., in a µP bus interface) or remain LOW during the entire DATA-READ sequence (i.e., µP I/O port interface).

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FIGURE 8-6: CONVERSION TIMING, CONTINUOUS MODE

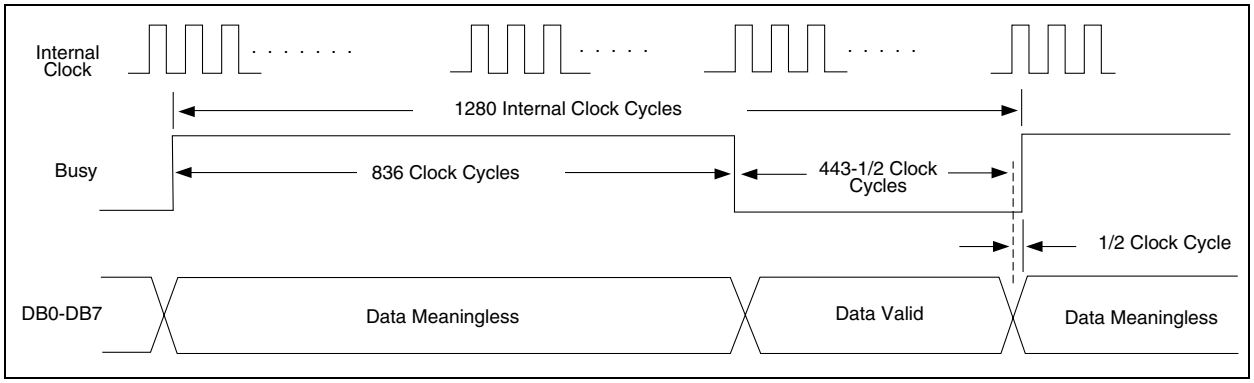
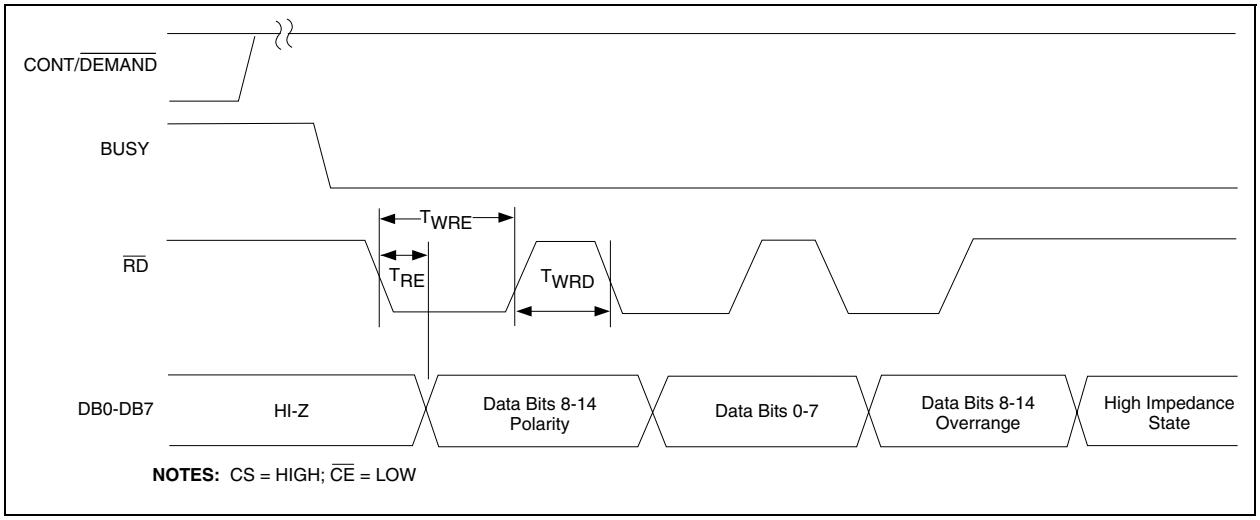


FIGURE 8-7: BUS OUTPUT TIMING, CONTINUOUS MODE



NOTES: CS = HIGH; $\overline{CE}$ = LOW

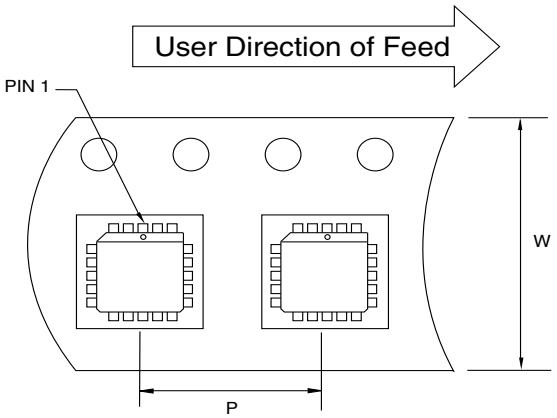
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

Package marking data not available at this time

9.2 Taping Form

Component Taping Orientation for 44-Pin PLCC Devices



Standard Reel Component Orientation
for TR Suffix Device

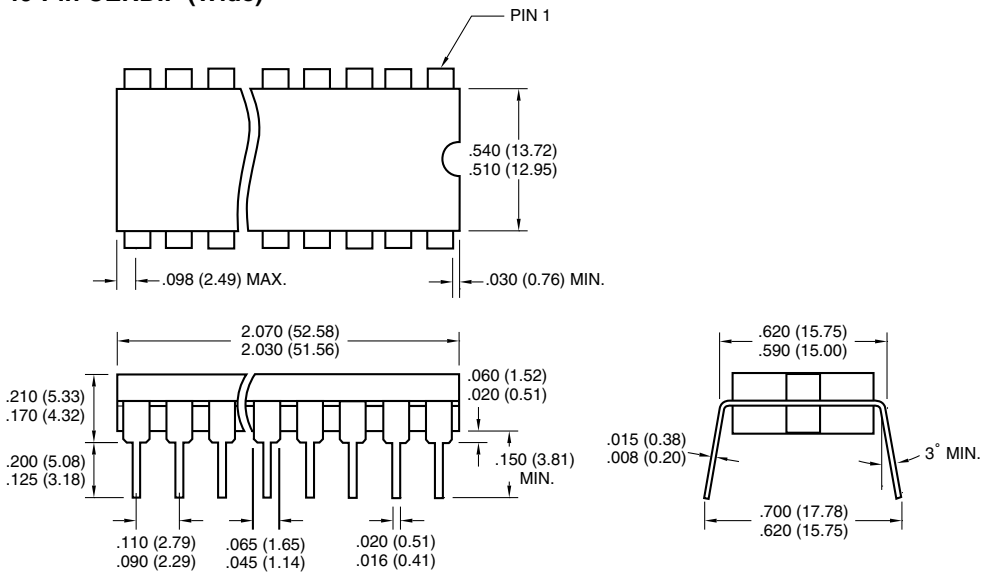
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PLCC	32 mm	24 mm	500	13 in

NOTE: Drawing does not represent total number of pins.

9.3 Package Dimensions

40-Pin CERDIP (Wide)



Dimensions: inches (mm)

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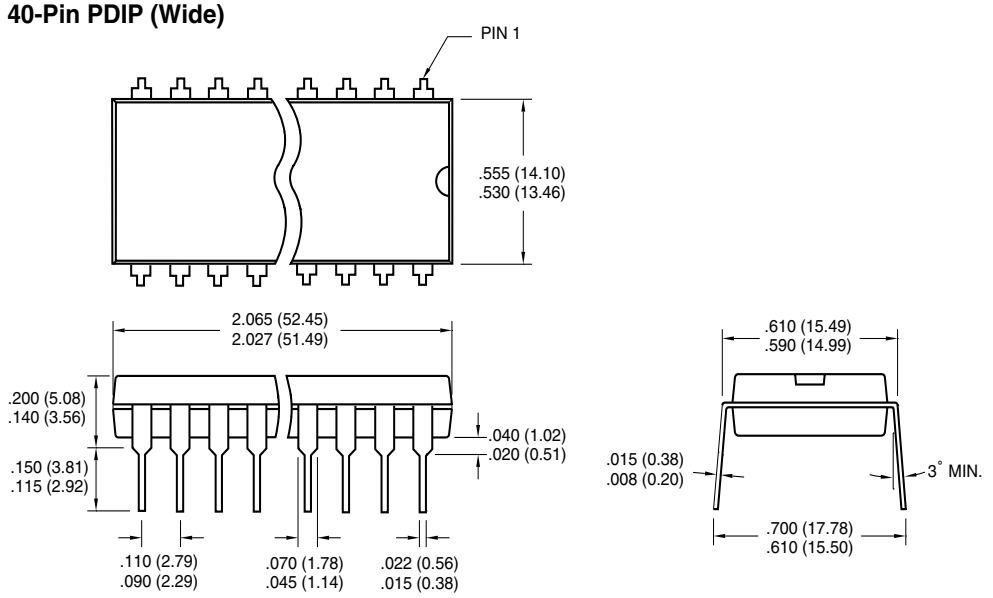
9.3 Package Dimensions (Continued)

40-Pin PDIP (Wide)



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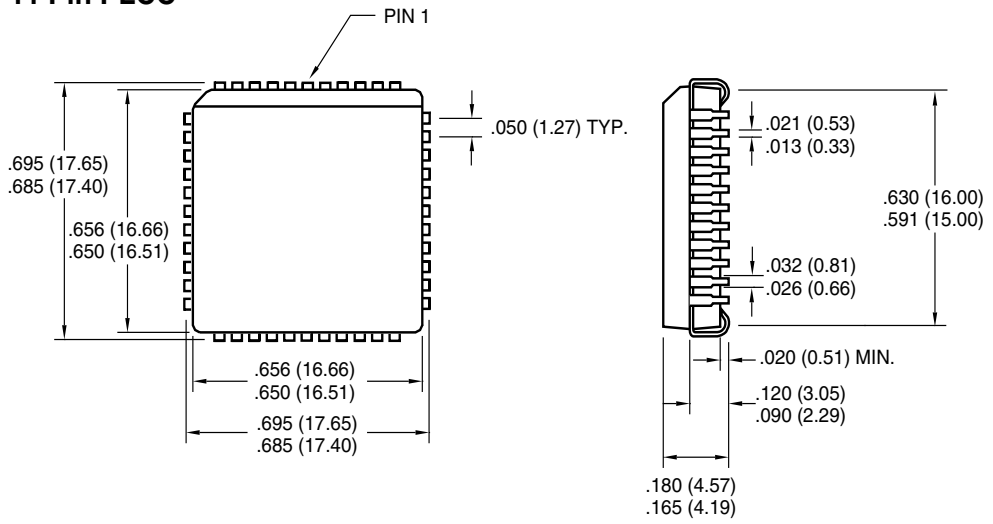
44-Pin PLCC



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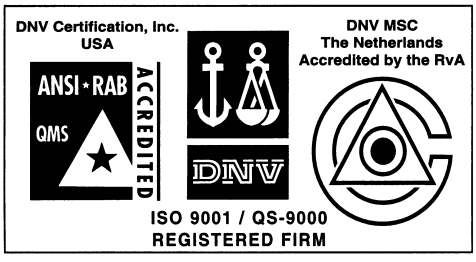

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