

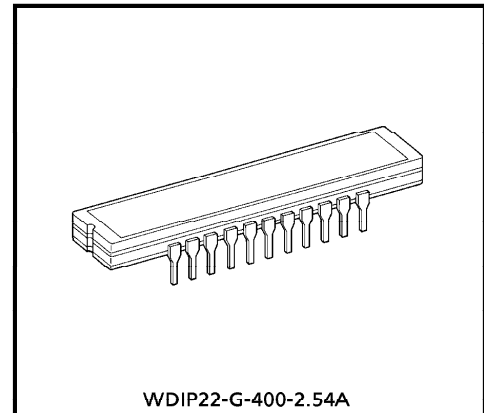
TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

TCD1300D

The TCD1300D is a high sensitive and low dark current 3648-elements linear image sensor. The sensor can be used for facsimile, imagescanner and OCR. The signal pre-processing circuit which is composed of Sample and Hold circuit and Pre-amplifier circuit. The device contains a row of 3648 photodiodes, which provide a 16 lines/mm (400DPI) across a A4 size paper.

FEATURES

- Number of Image Sensing Elements : 3648
- Image Sensing Element Size : 8 μ m by 8 μ m on 8 μ m centers
- Photo Sensing Region : High sensitive pn photodiode
- Clock : 2 phase
- Internal Circuit : S/H circuit, Pre-Amplifier circuit
- Package : 22 pin cerdip



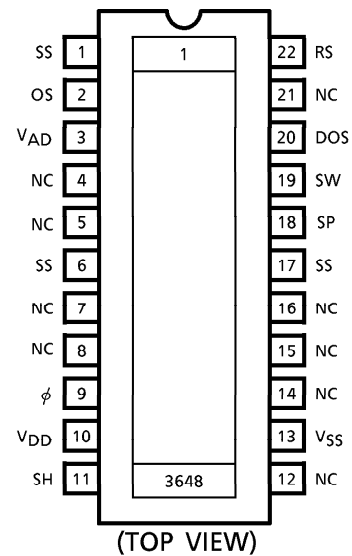
Weight : 4.4g (Typ.)

MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V_{ϕ}	- 0.3~15	V
Shift Pulse Voltage	V_{SH}		V
Reset Pulse Voltage	V_{RS}		V
Sample and Hold Pulse Voltage	V_{SP}		V
Switch Pulse Voltage	V_{SW}		V
Power Supply Voltage (Analog)	V_{AD}		V
Power Supply Voltage (Driver)	V_{DD}	V	
Operating Temperature	T_{opr}	- 25~60	°C
Storage Temperature	T_{stg}	- 40~100	°C

(Note 1) All voltage are with respect to SS and V_{SS} terminals (Ground).

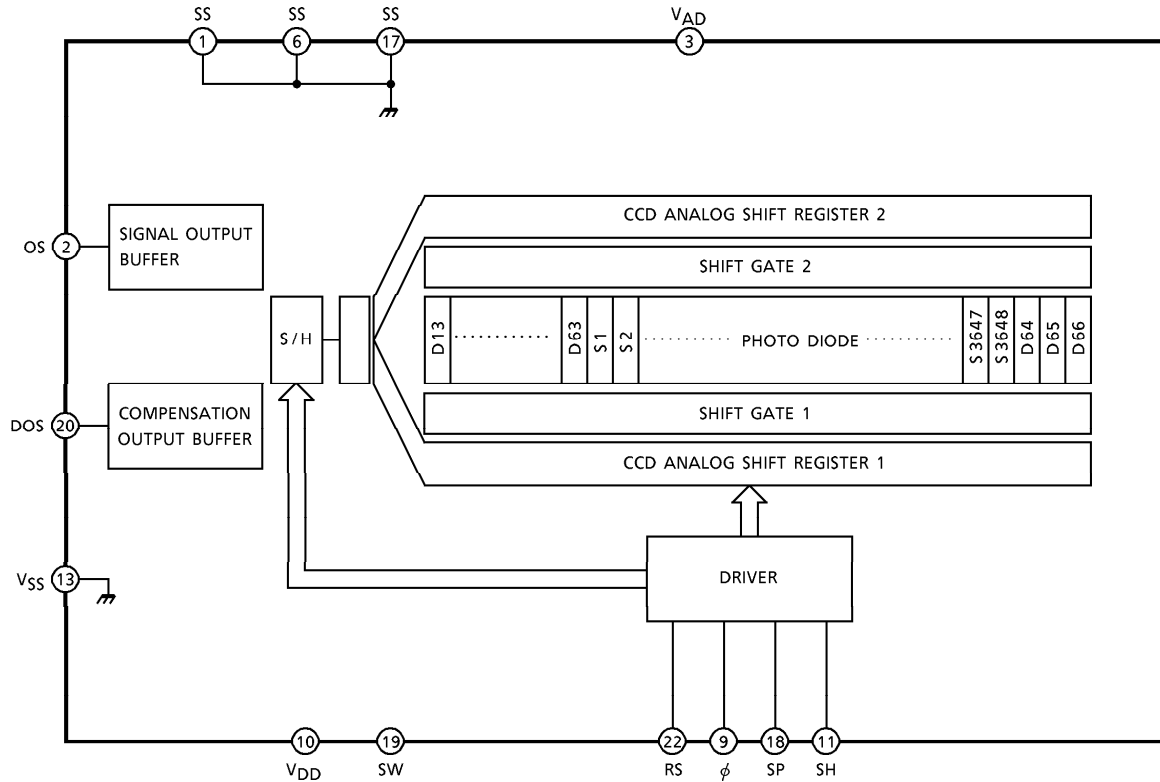
PIN CONNECTIONS



961001EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

CIRCUIT DIAGRAM



PIN NAMES

ϕ	Clock
SH	Shift Gate
RS	Reset Gate
SP	Sample Hold Gate
OS	Signal Output
DOS	Compensation Output
V _{AD}	Power (Analog)
V _{DD}	Power (Driver)
SS	Ground (Analog)
V _{SS}	Ground (Driver)
SW	Final Clock Select Switch
NC	Non Connection

961001EBA2'

● The products described in this document are subject to foreign exchange and foreign trade control laws.
 ● The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
 ● The information contained herein is subject to change without notice.

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, VAD = 12V, VDD = 12V, Vφ = VSH = VRS = 5V (PULSE), fφ = 0.5MHz, fRS = 1MHz, tINT (INTEGRATION TIME) = 10ms, LIGHT SOURCE = DAYLIGHT FLUORESCENT LAMP)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	R	4.6	5.8	7	V / lx·s	
Photo Response Non Uniformity	PRNU (1)	—	—	10	%	(Note 2)
	PRNU (3)	—	—	8	mV	(Note 3)
Register Imbalance	RI	—	—	3	%	(Note 4)
Saturation Output Voltage	VSAT	1.0	1.5	—	V	(Note 5)
Saturation Exposure	SE	—	0.3	—	lx·s	(Note 6)
Dark Signal Voltage	VDRK	—	—	3	mV	(Note 7)
Dark Signal Non Uniformity	DSNU	—	—	3	mV	(Note 7)
Analog Current Dissipation	IAD	—	16	25	mA	
Driver Current Dissipation	IDD	—	8	15	mA	
Total Transfer Efficiency	TTE	92	—	—	%	
Output Impedance	ZO	—	0.5	1	kΩ	
DC Signal Output Voltage	VOS	3.5	4.5	6	V	(Note 8)
DC Compensation Output Voltage	VDOS	3.5	4.5	6	V	(Note 8)
DC Mismatch Voltage	VOS-VDOS	—	—	100	mV	

(Note 2) Measured at 50% of SE (Typ.)

$$\text{Definition of PRNU : PRNU} = \frac{\Delta x}{\bar{x}} \times 100 (\%)$$

Where \bar{x} is average of total signal outputs and Δx is the maximum deviation from \bar{x} under uniform illumination.

(Note 3) PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.)

(Note 4) Measured at 50% of SE (Typ.)

RI is defined as follows:

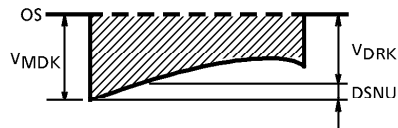
$$RI = \frac{\sum_{n=1}^{3647} |x_n - x_{n+1}|}{3647 \times \bar{x}} \times 100 (\%)$$

Where x_n and x_{n+1} are signal outputs of each pixel. \bar{x} is average of total signal outputs.

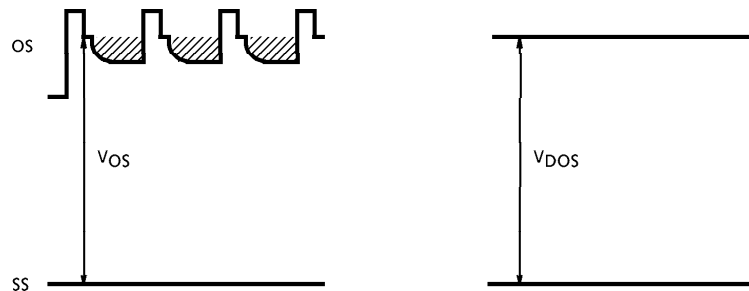
(Note 5) VSAT is defined as minimum saturation output voltage of all effective pixels.

(Note 6) Definition of SE : $SE = \frac{VSAT}{R}$ (lx·s)

(Note 7) V_{DRK} is defined as average dark signal voltage of all effective pixels.
 $DSNU$ is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



(Note 8) DC signal output voltage and DC compensation output voltage are defined as follows:



OPERATING CONDITION

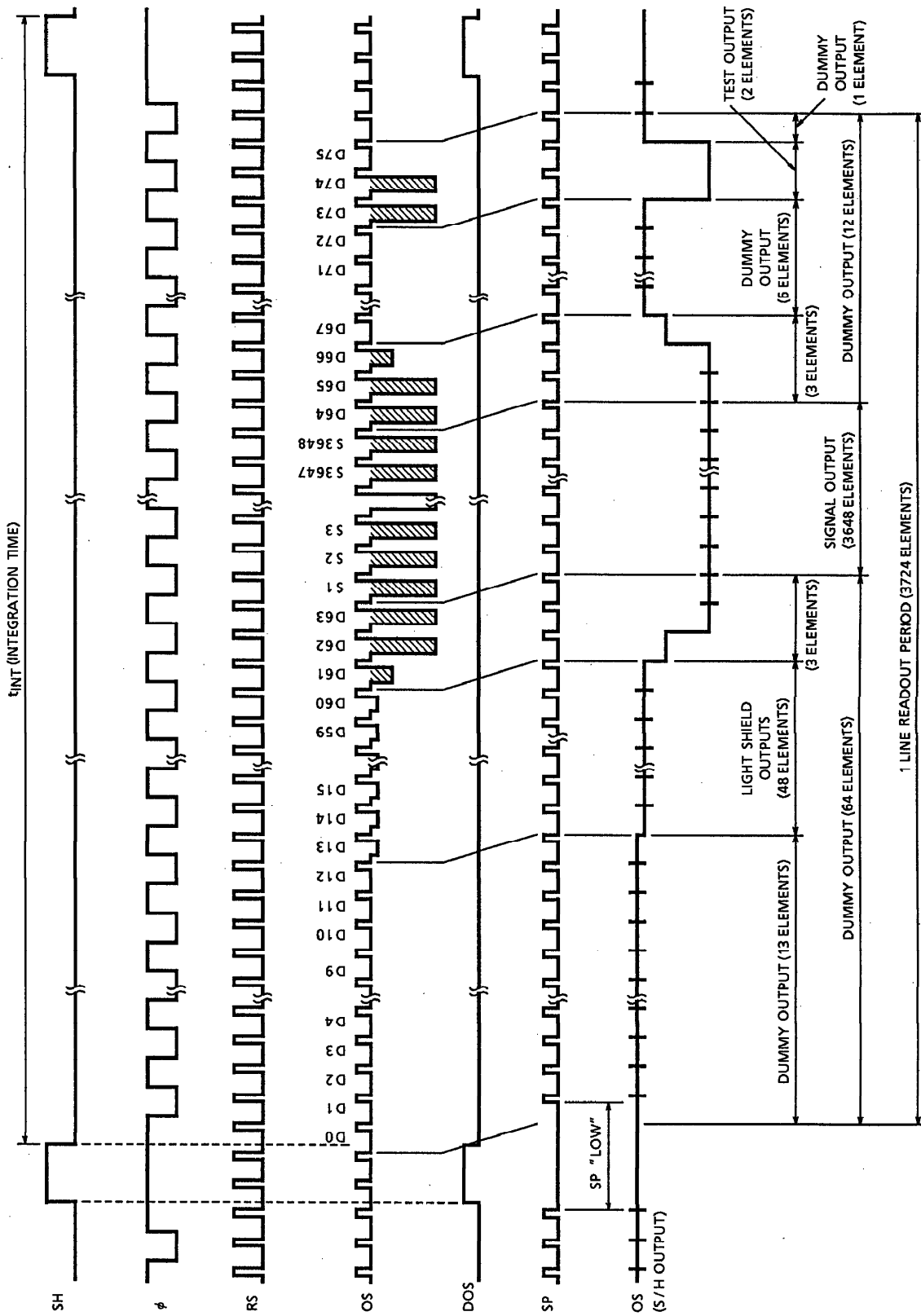
CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Voltage	"H" Level	V_{ϕ}	4.5	5.0	13	V
	"L" Level		0	—	0.5	
Shift Pulse Voltage	"H" Level	V_{SH}	4.5	5.0	13	V
	"L" Level		0	—	0.5	
Reset Pulse Voltage	"H" Level	V_{RS}	4.5	5.0	13	V
	"L" Level		0	—	0.5	
Sample and Hold Pulse Voltage (Note 9)	"H" Level	V_{SP}	4.5	5.0	13	V
	"L" Level		0	—	0.5	
Switch Pulse Voltage	"H" Level	V_{SW}	4.5	5.0	13	V
	"L" Level		0	—	0.5	
Power Supply Voltage (Analog)		V_{AD}	11.4	12	13	V
Power Supply Voltage ((Driver)		V_{DD}	11	12	13	V

(Note 9) Supply "H" level to SP terminal when sample-and-hold circuitry is not used.

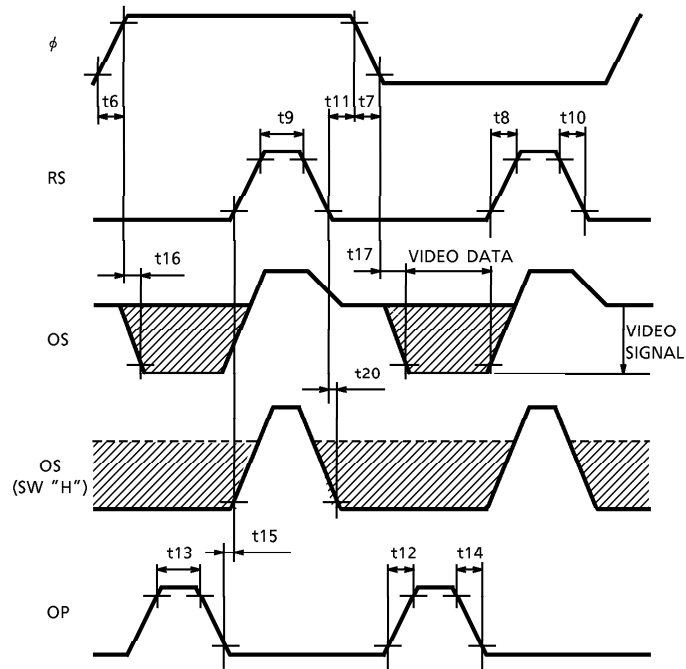
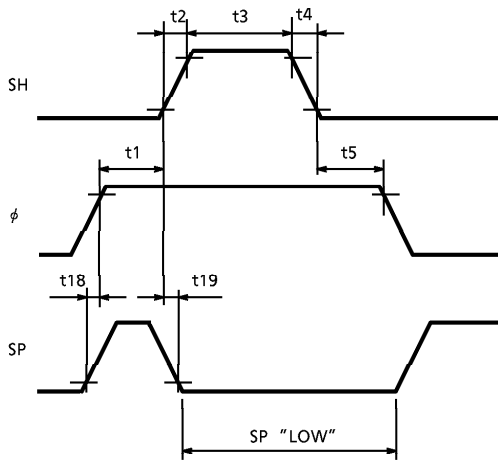
CLOCK CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	f_{ϕ}	—	0.5	1.5	MHz
Reset Pulse Frequency	f_{RS}	—	1	3	MHz
Sample and Hold Pulse Frequency	f_{SP}	—	1	3	MHz
Clock Capacitance	C_{ϕ}	—	20	40	pF
Shift Gate Capacitance	C_{SH}	—	20	40	pF
Reset Gate Capacitance	C_{RS}	—	10	20	pF
Sample and Hold Gate Capacitance	C_{SP}	—	10	20	pF
Switch Gate Capacitance	C_{SW}	—	10	20	pF

TIMING CHART



TIMING REQUIREMENTS



Video Data Delay Time (Note 9)

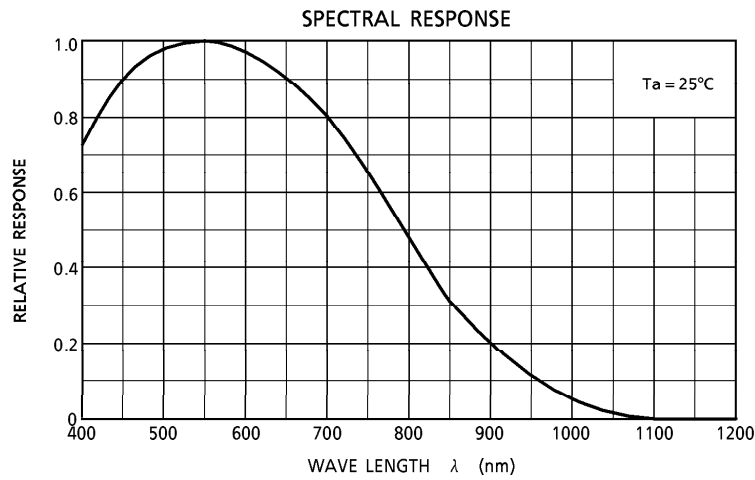
CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 10)	MAX.	UNIT
Pulse Timing of SH and ϕ	t1, t5	60 (Note 12)	1000	—	ns
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
SH Pulse Width	t3	500	1000	—	ns
ϕ Rise Time, Fall Time	t6, t7	0	50	—	ns
RS Rise Time, Fall Time	t8, t10	0	20	—	ns
RS Pulse Width	t9	20	250	—	ns
Pulse Timing of ϕ and RS	t11	0	100	—	ns
SP Rise Time, Fall Time	t12, t14	10	100	—	ns
SP Pulse Width	t13	20	100	—	ns
Pulse Timing of SP and RS	t15	0	50	—	ns
Video Data Delay Time (Note 11)	t16, t17	—	95	105	ns
	t20	—	80	90	ns
Pulse Timing of ϕ and SP	t18	0	250	—	ns
Pulse Timing of SH and SP	t19	20	450	—	ns

(Note 10) TYP. is the case of $f_{RS} = 1\text{MHz}$.

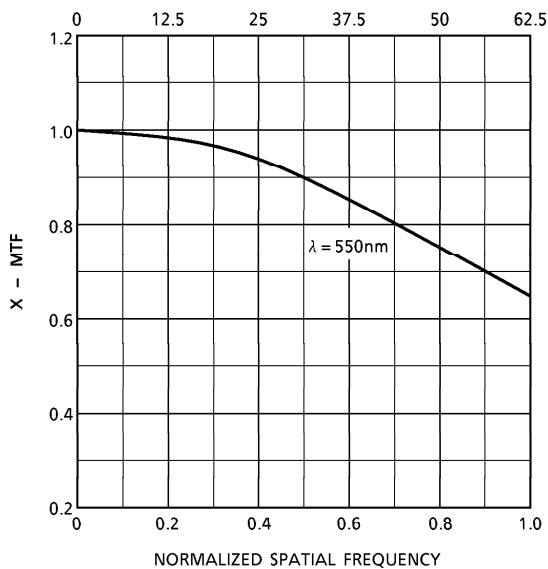
(Note 11) Load Resistance is $100\text{k}\Omega$.

(Note 12) The Case of Non Using the Dos 0ns.

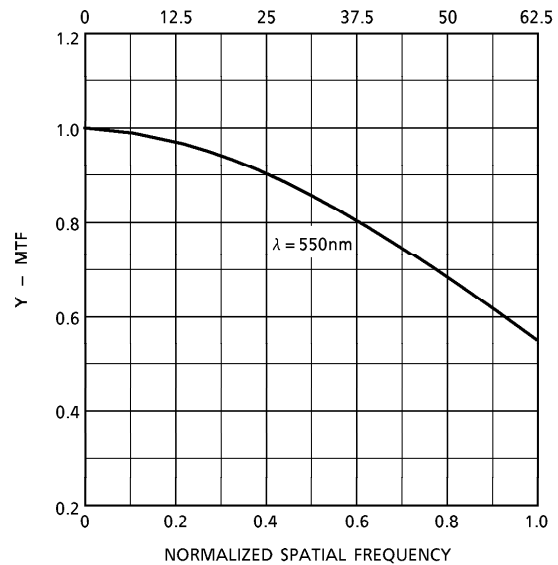
TYPICAL PERFORMANCE CURVES



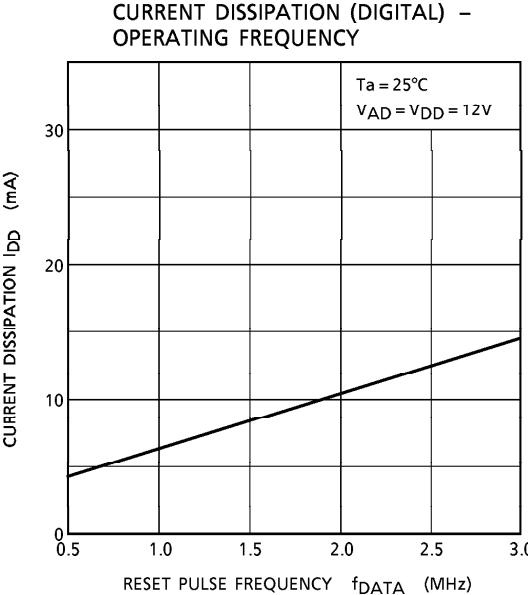
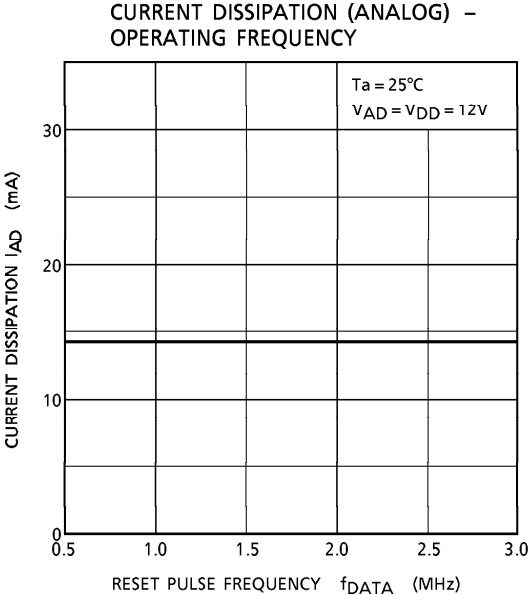
MODULATION TRANSFER FUNCTION OF X-DIRECTION
 SPATIAL FREQUENCY (Cycles / mm)



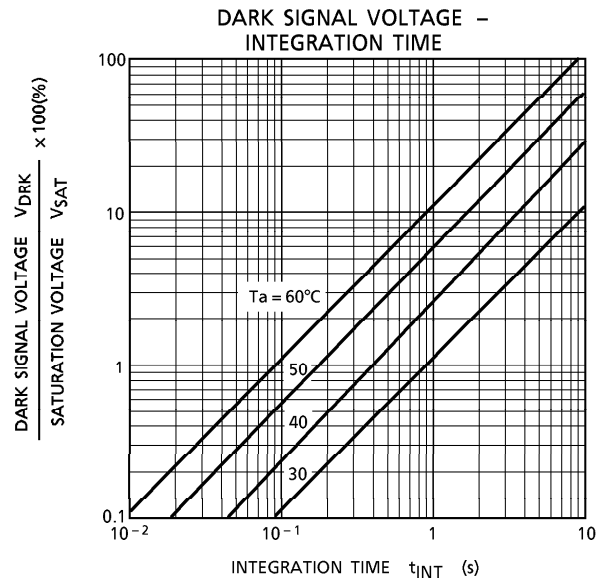
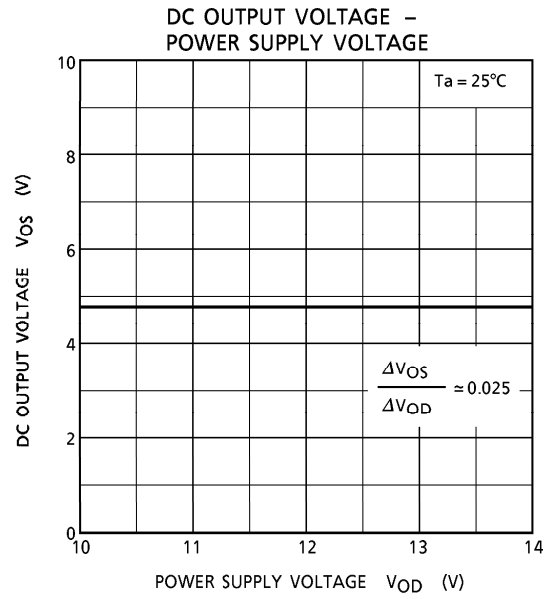
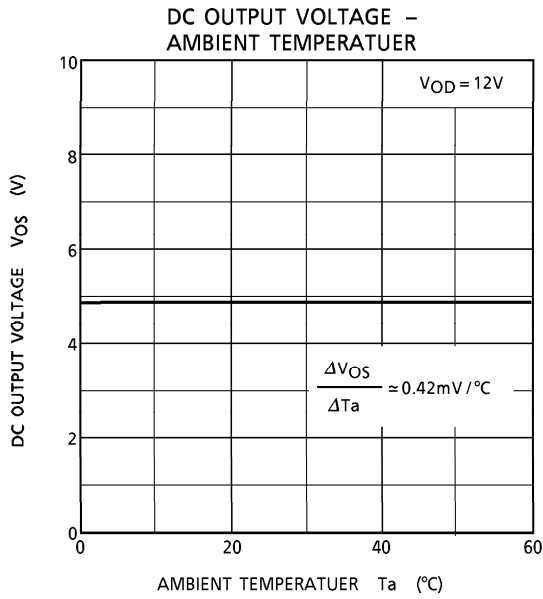
MODULATION TRANSFER FUNCTION OF Y-DIRECTION
 SPATIAL FREQUENCY (Cycles / mm)



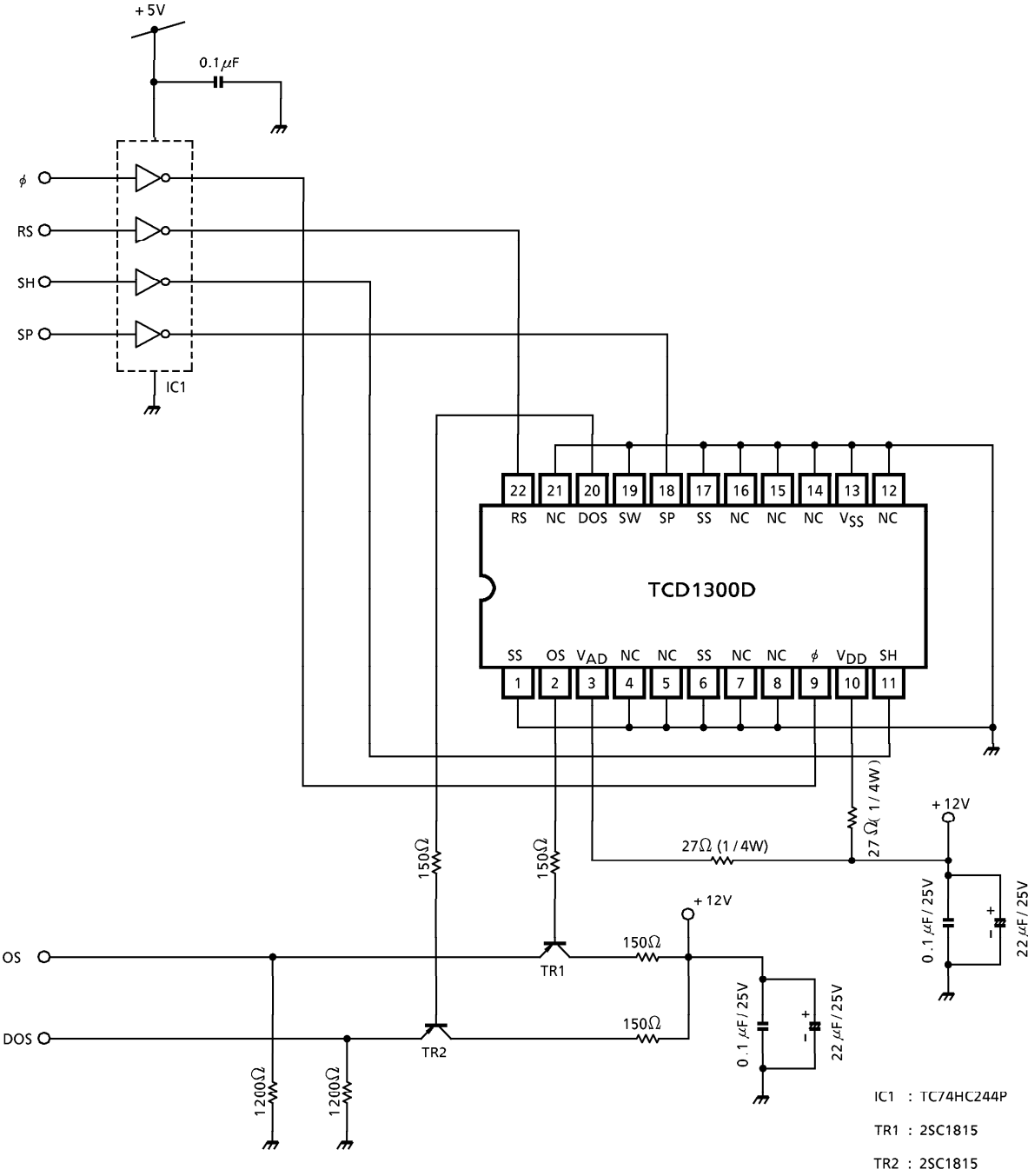
TYPICAL PERFORMANCE CURVES (Cont'd)



TYPICAL PERFORMANCE CURVES



TYPICAL DRIVE CIRCUIT



CAUTION**1. Window Glass**

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

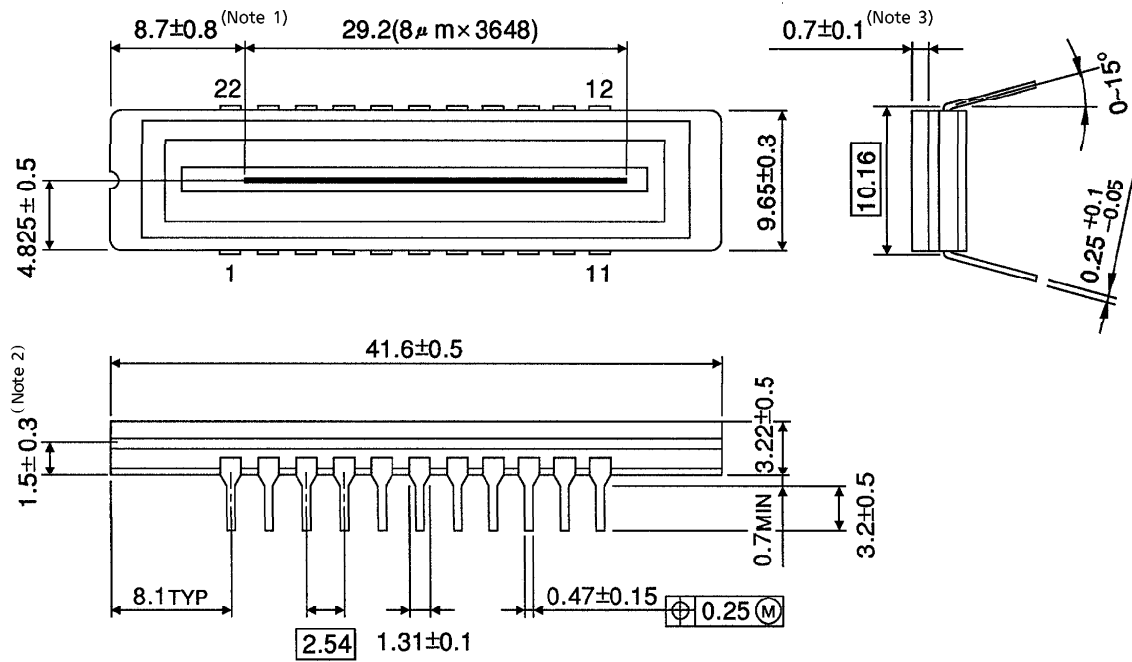
CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

OUTLINE DRAWING

WDIP22-G-400-2.54A (F)

Unit : mm



- (Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
- (Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
- (Note 3) GLASS THICKNES (n = 1.5)

Weight : 4.4g (Typ.)