

TFA9843J

2-channel audio amplifier (SE: 1 W to 20 W or BTL: 4 W to 40 W)

Rev. 02 — 19 January 2004

Preliminary data

1. General description

The TFA9843J contains two identical audio power amplifiers. The TFA9843J can be used as two Single-Ended (SE) channels with a fixed gain of 26 dB or one Bridge-Tied Load (BTL) channel with a fixed gain of 32 dB.

The TFA9843J comes in a 9-pin DIL-bent-SIL (DBS7P) power package. The TFA9843J is pin compatible with the TFA9842J and TFA9841J.

The TFA9843J contains a unique protection circuit that is solely based on multiple temperature measurements inside the chip. This gives maximum output power for all supply voltages and load conditions with no unnecessary audio holes. Almost any supply voltage and load impedance combination can be made as long as thermal boundary conditions (number of channels used, external heatsink and ambient temperature) allow it.

2. Features

- SE: 1 W to 20 W; BTL: 4 W to 40 W operation possibility
- Soft clipping
- Standby and mute mode
- No on/off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Pin compatible with the TFA9842J and TFA9841J.

3. Applications

- Television
- PC speakers
- Boom box
- Mini and micro audio receivers.



PHILIPS

4. Quick reference data

Table 1: Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---------------------------------|--|-----|------|-----|------|
| V _{CC} | supply voltage | operating | 9 | 18 | 26 | V |
| | | no signal | - | - | 28 | V |
| I _q | quiescent supply current | V _{CC} = 18 V; R _L = ∞ | - | 60 | 100 | mA |
| I _{stb} | standby supply current | | - | - | 10 | μA |
| P _o | SE output power | THD = 10 %; R _L = 4 Ω; V _{CC} = 18 V | 7 | 8.5 | - | W |
| | | THD = 10 %; R _L = 4 Ω; V _{CC} = 22 V | - | 14 | - | W |
| | BTL output power | THD = 10 %; R _L = 8 Ω; V _{CC} = 18 V | 16 | 18 | - | W |
| | | THD = 10 %; R _L = 8 Ω; V _{CC} = 22 V | - | 29 | - | W |
| THD | total harmonic distortion | SE; P _o = 1 W | - | 0.1 | 0.5 | % |
| | | BTL; P _o = 1 W | - | 0.05 | 0.5 | % |
| G _v | voltage gain | SE | 25 | 26 | 27 | dB |
| | | BTL | 31 | 32 | 33 | dB |
| SVRR | supply voltage ripple rejection | SE; f = 1 kHz | - | 60 | - | dB |
| | | BTL; f = 1 kHz | - | 65 | - | dB |

5. Ordering information

Table 2: Ordering information

| Type number | Package | | |
|-------------|---------|--|-----------|
| | Name | Description | Version |
| TFA9843J | DBS9P | plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad | SOT523 -1 |

6. Block diagram

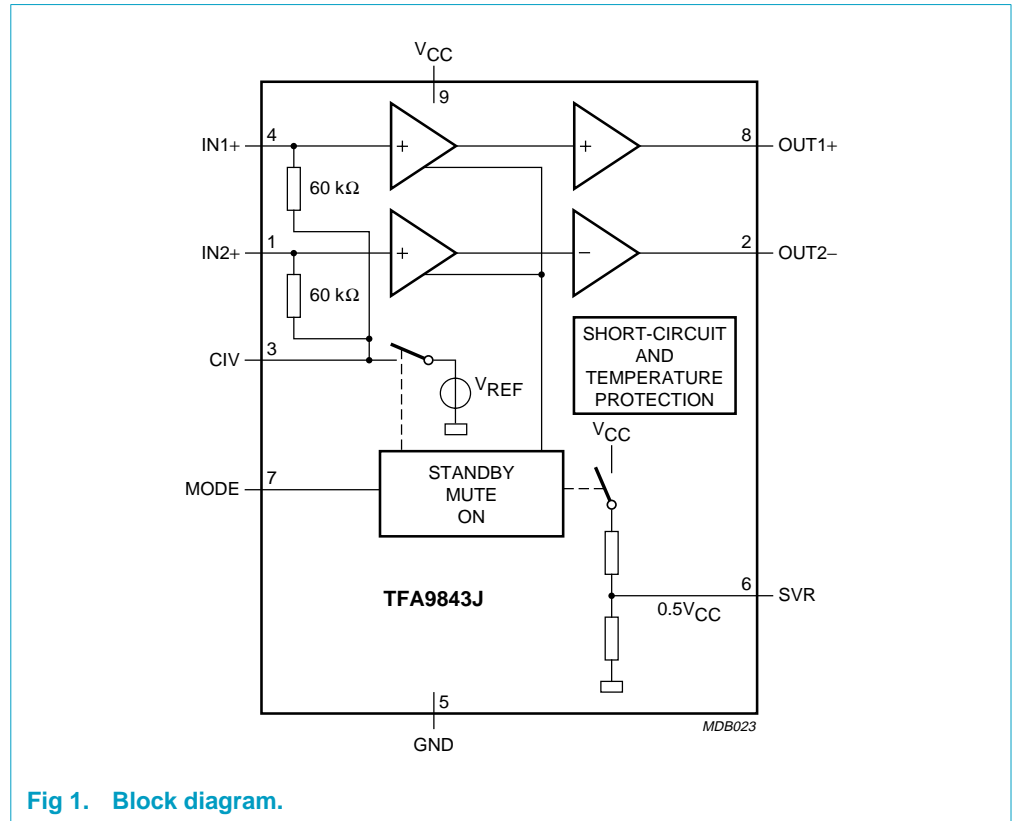


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

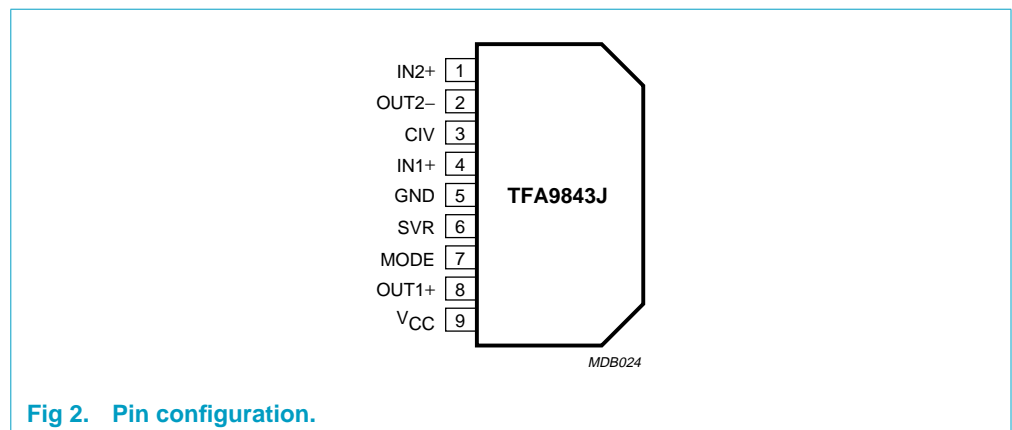


Fig 2. Pin configuration.

7.2 Pin description

Table 3: Pin description

| Symbol | Pin | Description |
|-----------------|-----|--|
| IN2+ | 1 | input 2 |
| OUT2- | 2 | inverted loudspeaker terminal 2 |
| CIV | 3 | common input voltage decoupling |
| IN1+ | 4 | input 1 |
| GND | 5 | ground |
| SVR | 6 | half supply voltage decoupling (ripple rejection) |
| MODE | 7 | mode selection input (standby, mute and operating) |
| OUT1+ | 8 | non inverted loudspeaker terminal 1 |
| V _{CC} | 9 | supply voltage |

8. Functional description

8.1 Input configuration

The input cut-off frequency is:

$$f_{i(cut-off)} = \frac{1}{2\pi(R_i \times C_i)} \quad (1)$$

Single-ended application: $R_i = 60 \text{ k}\Omega$ and $C_i = 220 \text{ nF}$:

$$f_{i(cut-off)} = \frac{1}{2\pi(60 \times 10^3 \times 220 \times 10^{-9})} = 12 \text{ Hz} \quad (2)$$

Bridge-tied load application: $R_i = 30 \text{ k}\Omega$ and $C_i = 470 \text{ nF}$:

$$f_{i(cut-off)} = \frac{1}{2\pi(30 \times 10^3 \times 470 \times 10^{-9})} = 11 \text{ Hz} \quad (3)$$

As shown in [Equation 2](#) and [Equation 3](#), large capacitor values for the inputs are not necessary; so the switch-on delay during charging of the input capacitors can be minimized. This results in a good low frequency response and good switch-on behavior.

8.2 Power amplifier

The power amplifier is a Bridge-Tied Load (BTL) or Single-Ended (SE) amplifier with an all-NPN output stage, capable of delivering a peak output current of 4 A.

Using the TFA9843J as a BTL amplifier offers the following advantages:

- Lower peak value of the supply current
- Ripple frequency on the supply voltage is twice the signal frequency

- No expensive DC-blocking capacitor
- Good low frequency performance.

8.2.1 Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10 %; see [Figure 11](#). The maximum output power is limited by the supply voltage of 26 V and the maximum available output current is 4 A repetitive peak current. A minimum load (SE) of 3 Ω is required for supply voltages > 22 V; see [Figure 5](#). A minimum load (BTL) of 6 Ω is required for supply voltages > 22 V; see [Figure 6](#).

8.2.2 Headroom

Typical CD music requires at least 12 dB (factor 15.85) dynamic headroom, compared to the average power output, for transferring the loudest parts without distortion. At $V_{CC} = 18\text{ V}$ and $P_o = 5\text{ W}$ (SE with $R_L = 4\ \Omega$) or $P_o = 10\text{ W}$ (BTL with $R_L = 8\ \Omega$) at THD = 0.2 % (see [Figure 7](#)), the Average Listening Level (ALL) music power without any distortion yields:

$$P_{o(ALL, SE)} = \frac{5 \times 10^3}{15.85} = 315\text{ mW} \quad (4)$$

$$P_{o(ALL, BTL)} = \frac{10 \times 10^3}{15.85} = 630\text{ mW} \quad (5)$$

The power dissipation can be derived from [Figure 13](#) (SE) or [Figure 14](#) (BTL) for 0 dB respectively 12 dB headroom (see [Table 4](#)).

Table 4: Power rating as function of headroom

| Headroom | Power output (THD = 0.2 %) | | Power dissipation (P_D); both channels driven |
|----------|------------------------------|------------------------------|--|
| | SE | BTL | |
| 0 dB | $P_o = 5\text{ W}$ | $P_o = 10\text{ W}$ | 8.4 W |
| 12 dB | $P_{o(ALL)} = 315\text{ mW}$ | $P_{o(ALL)} = 630\text{ mW}$ | 4.2 W |

For the average listening level a power dissipation of 4.2 W can be used for a heatsink calculation.

8.3 Mode selection

The TFA9843J has three functional modes, which can be selected by applying the proper DC voltage to pin MODE (see [Table 5](#) and [Figure 3](#)).

Table 5: Mode selection

| V_{MODE} | Amplifiers 1 and 2 |
|---|--------------------|
| 0 to 0.8 V | standby |
| 4.5 V to ($V_{CC} - 3.5\text{ V}$) | mute |
| ($V_{CC} - 2.0\text{ V}$) to V_{CC} | on |

Standby — In this mode the current consumption is very low and the outputs are floating. The device is in standby mode when $V_{\text{MODE}} < 0.8 \text{ V}$, or when pin MODE is grounded.

Mute — In this mode the amplifier is DC-biased but not operational (no audio output). This allows the input coupling capacitors to be charged to avoid pop-noise. The device is in mute mode when $4.5 \text{ V} < V_{\text{MODE}} < (V_{\text{CC}} - 3.5 \text{ V})$.

On — In this mode the amplifier is operating normally. The operating mode is activated at $V_{\text{MODE}} > (V_{\text{CC}} - 2.0 \text{ V})$.

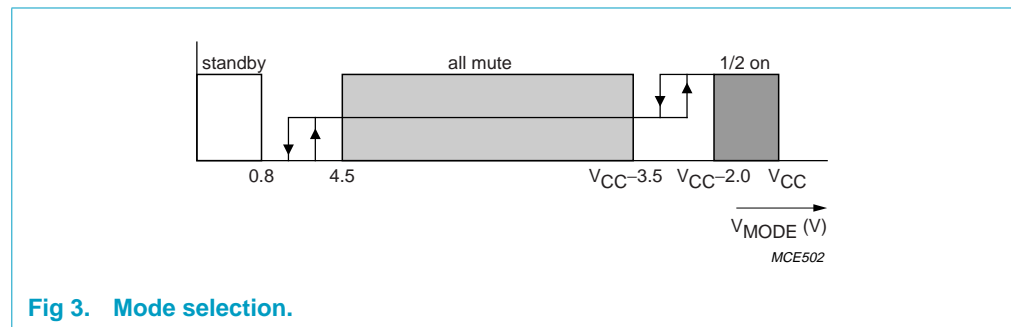


Fig 3. Mode selection.

8.4 Supply voltage ripple rejection

The supply voltage ripple rejection (SVRR) is measured with an electrolytic capacitor of $150 \mu\text{F}$ on pin SVR using a bandwidth of 20 Hz to 22 kHz. Figure 17 illustrates the SVRR as function of the frequency. A larger capacitor value on pin SVR improves the ripple rejection behavior at the lower frequencies.

8.5 Built-in protection circuits

The TFA9843J contains two types of temperature sensors; one measures local temperatures of the power stages and one measures the global chip temperature. At a local temperature of the power stage of approximately $185 \text{ }^\circ\text{C}$ or a global temperature of approximately $150 \text{ }^\circ\text{C}$ this detection circuit switches off the power stages for 2 ms. High impedance of the outputs is the result. After this time period the power stages switch on automatically and the detection will take place again; still a too high temperature switches off the power stages immediately. This protects the TFA9843J against shorts to ground, to the supply voltage, across the load and too high chip temperatures.

The protection will only be activated when necessary, so even during a short-circuit condition, a certain amount of (pulsed) current will still be flowing through the short, just as much as the power stage can handle without exceeding the critical temperature level.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|--|---------------|------|-----------------------|------|
| V _{CC} | supply voltage | operating | -0.3 | +26 | V |
| | | no signal | -0.3 | +28 | V |
| V _I | input voltage | | -0.3 | V _{CC} + 0.3 | V |
| I _{ORM} | repetitive peak output current | | - | 4 | A |
| T _{stg} | storage temperature | non-operating | -55 | +150 | °C |
| T _{amb} | ambient temperature | operating | -40 | +85 | °C |
| P _{tot} | total power dissipation | | - | 35 | W |
| V _{CC(sc)} | supply voltage to guarantee short-circuit protection | | - | 24 | V |

10. Thermal characteristics

Table 7: Thermal characteristics

| Symbol | Parameter | Conditions | Value | Unit |
|----------------------|---|----------------------|-------|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | in free air | 40 | K/W |
| R _{th(j-c)} | thermal resistance from junction to case | both channels driven | 2.0 | K/W |

11. Static characteristics

Table 8: Static characteristics

V_{CC} = 18 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = V_{CC}; V_i = 0 V; measured in test circuit *Figure 20*; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|------------------------------------|---|-----------------------|-----|-----------------------|------|
| V _{CC} | supply voltage | operating | [1] 9 | 18 | 26 | V |
| I _q | quiescent supply current | R _L = ∞ | [2] - | 60 | 100 | mA |
| I _{stb} | standby supply current | V _{MODE} = 0 | - | - | 10 | μA |
| V _O | DC output voltage | | [3] - | 9 | - | V |
| ΔV _{OUT} | differential output voltage offset | BTL mode | [4] - | - | 190 | mV |
| V _{MODE} | mode selection input voltage | on mode | V _{CC} - 2.0 | - | V _{CC} | V |
| | | mute mode | 4.5 | - | V _{CC} - 3.5 | V |
| | | standby mode | 0 | - | 0.8 | V |
| I _{MODE} | input current on pin MODE | 0 < V _{MODE} < (V _{CC} - 3.5) | - | - | 20 | μA |

[1] A minimum load (BTL) of 6 Ω is allowed at supply voltages > 22 V.

[2] With a load connected at the outputs the quiescent supply current will increase.

[3] The DC output voltage with respect to ground is approximately 0.5V_{CC}.

[4] ΔV_{OUT} = |V_{OUT1+} - V_{OUT2-}|

12. Dynamic characteristics

Table 9: Dynamic characteristics SE

$V_{CC} = 18\text{ V}$; $T_{amb} = 25\text{ °C}$; $R_L = 4\ \Omega$; $f = 1\text{ kHz}$; $V_{MODE} = V_{CC}$; measured in test circuit *Figure 19*; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|---------------------------------|---|-------|-----|-----|---------------|
| P_o | output power | THD = 10 %; $R_L = 4\ \Omega$ | 7 | 8.5 | - | W |
| | | THD = 0.5 %; $R_L = 4\ \Omega$ | - | 6.5 | - | W |
| | | $V_{CC} = 22\text{ V}$; THD = 10 %; $R_L = 4\ \Omega$ | - | 14 | - | W |
| THD | total harmonic distortion | $P_o = 1\text{ W}$ | - | 0.1 | 0.5 | % |
| G_v | SE voltage gain | | 25 | 26 | 27 | dB |
| Z_i | input impedance | | 40 | 60 | - | k Ω |
| $V_{n(o)}$ | noise output voltage | | [1] - | 150 | - | μV |
| SVRR | supply voltage ripple rejection | $f_{\text{ripple}} = 1\text{ kHz}$ | [2] - | 60 | - | dB |
| | | $f_{\text{ripple}} = 100\text{ Hz to }20\text{ kHz}$ | [2] - | 60 | - | dB |
| $V_{o(\text{mute})}$ | output voltage in mute mode | | [3] - | - | 150 | μV |
| α_{cs} | channel separation | $R_{\text{source}} = 0\ \Omega$ | 50 | 60 | - | dB |
| $ G_v $ | channel unbalance | | - | - | 1 | dB |

- [1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance $R_{\text{source}} = 0\ \Omega$ at the input.
- [2] Supply voltage ripple rejection is measured at the output, with a source impedance $R_{\text{source}} = 0\ \Omega$ at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.
- [3] Output voltage in mute mode ($V_{\text{MODE}} = 7\text{ V}$) and an input voltage of 1 V (RMS) in a bandwidth from 20 Hz to 22 kHz, so including noise.

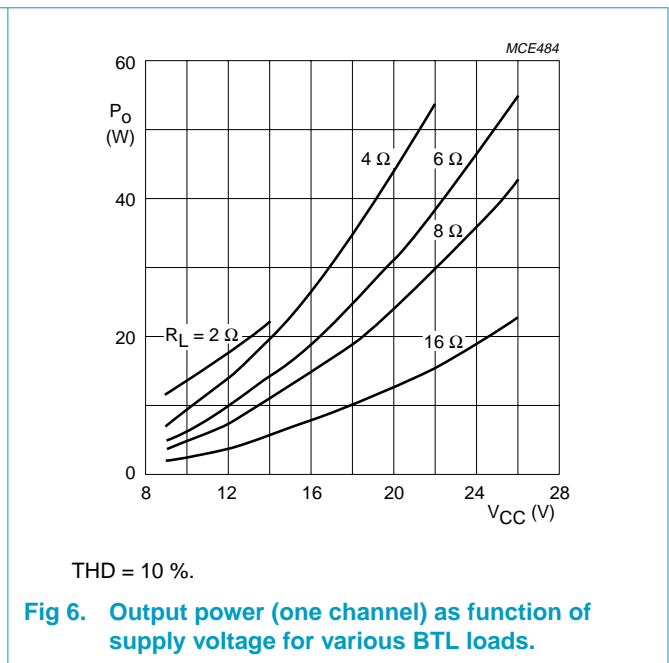
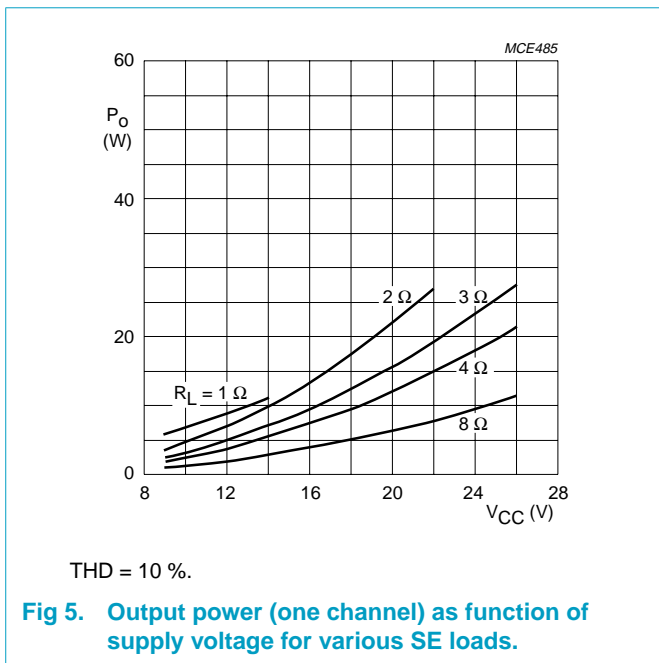
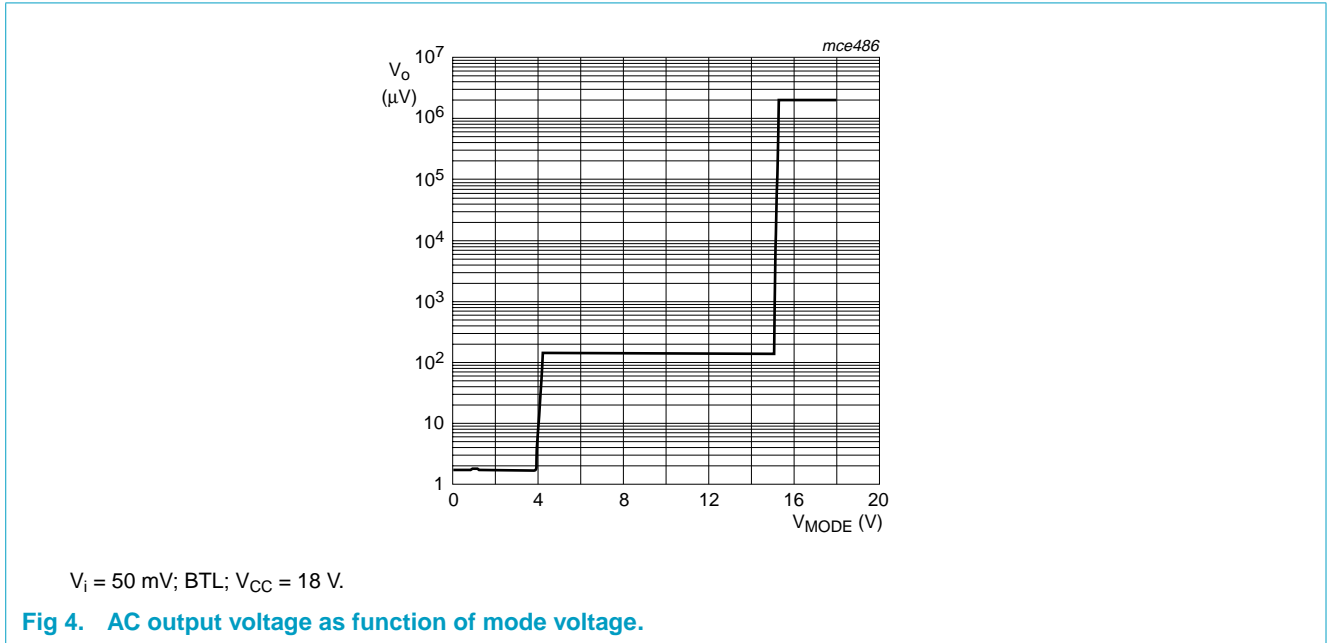
Table 10: Dynamic characteristics BTL

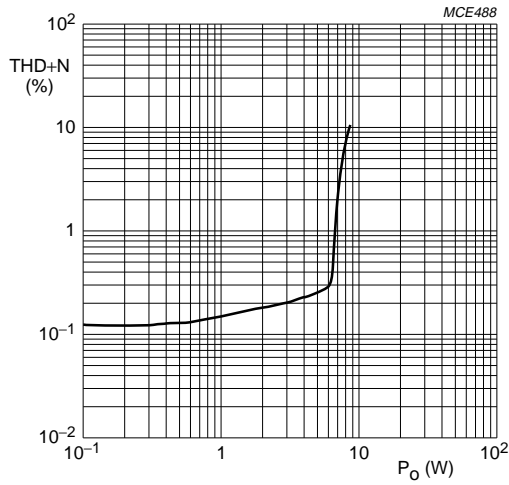
$V_{CC} = 18\text{ V}$; $T_{amb} = 25\text{ °C}$; $R_L = 8\ \Omega$; $f = 1\text{ kHz}$; $V_{MODE} = V_{CC}$; measured in test circuit *Figure 20*; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|---------------------------------|---|-------|------|-----|---------------|
| P_o | output power | THD = 10 %; $R_L = 8\ \Omega$ | 16 | 18 | - | W |
| | | THD = 0.5 %; $R_L = 8\ \Omega$ | - | 14 | - | W |
| | | $V_{CC} = 22\text{ V}$; THD = 10 %; $R_L = 8\ \Omega$ | - | 29 | - | W |
| THD | total harmonic distortion | $P_o = 1\text{ W}$ | - | 0.05 | 0.5 | % |
| G_v | BTL voltage gain | | 31 | 32 | 33 | dB |
| Z_i | input impedance | | 20 | 30 | - | k Ω |
| $V_{n(o)}$ | noise output voltage | | [1] - | 200 | - | μV |
| SVRR | supply voltage ripple rejection | $f_{\text{ripple}} = 1\text{ kHz}$ | [2] - | 65 | - | dB |
| | | $f_{\text{ripple}} = 100\text{ Hz to }20\text{ kHz}$ | [2] - | 65 | - | dB |
| $V_{o(\text{mute})}$ | output voltage in mute mode | | [3] - | - | 250 | μV |
| α_{cs} | channel separation | $R_{\text{source}} = 0\ \Omega$ | 50 | 65 | - | dB |
| $ G_v $ | channel unbalance | | - | - | 1 | dB |

- [1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance $R_{\text{source}} = 0\ \Omega$ at the input.
- [2] Supply voltage ripple rejection is measured at the output, with a source impedance $R_{\text{source}} = 0\ \Omega$ at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

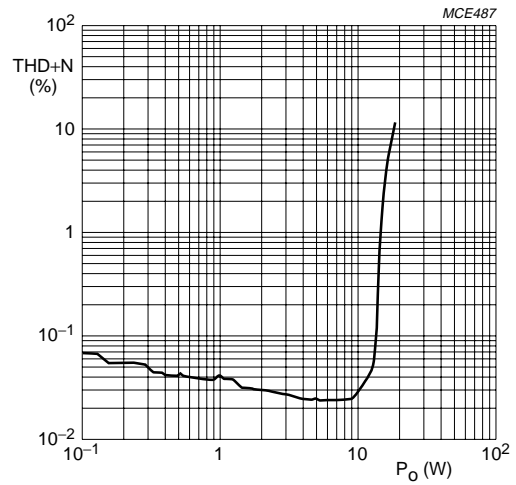
[3] Output voltage in mute mode ($V_{MODE} = 7\text{ V}$) and an input voltage of 1 V (RMS) in a bandwidth from 20 Hz to 22 kHz, so including noise.





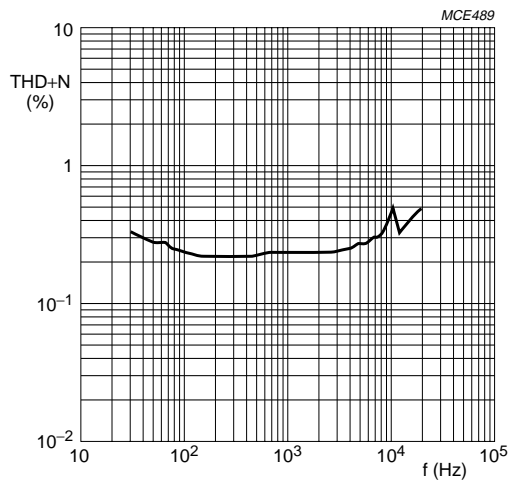
$V_{CC} = 18\text{ V}$; SE; $f = 1\text{ kHz}$; $R_L = 4\ \Omega$.

Fig 7. Total harmonic distortion as function of output power.



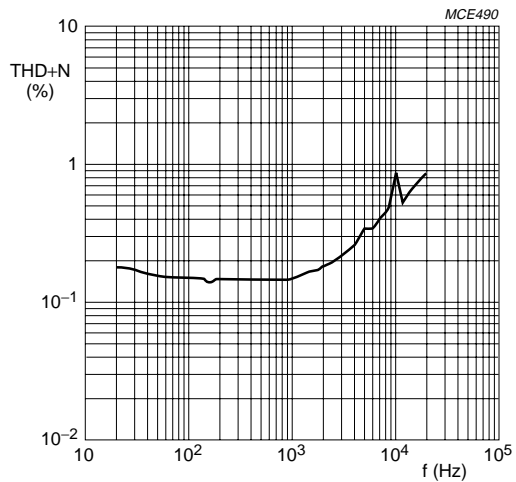
$V_{CC} = 18\text{ V}$; BTL; $f = 1\text{ kHz}$; $R_L = 8\ \Omega$.

Fig 8. Total harmonic distortion as function of output power.



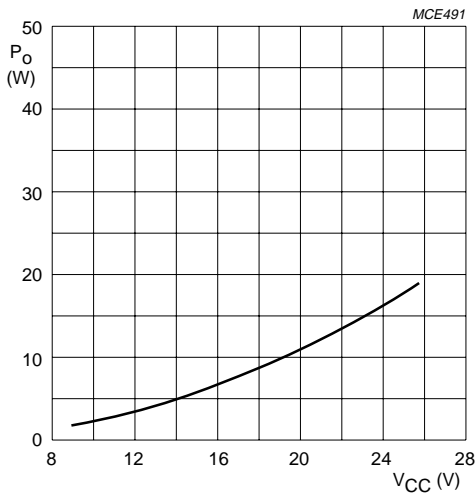
$V_{CC} = 18\text{ V}$; SE; $P_o = 1\text{ W}$; $R_L = 4\ \Omega$.

Fig 9. Total harmonic distortion as function of frequency.



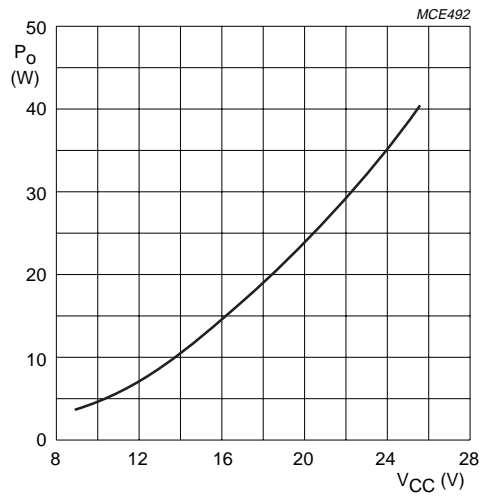
$V_{CC} = 18\text{ V}$; BTL; $P_o = 1\text{ W}$; $R_L = 8\ \Omega$.

Fig 10. Total harmonic distortion as function of frequency.



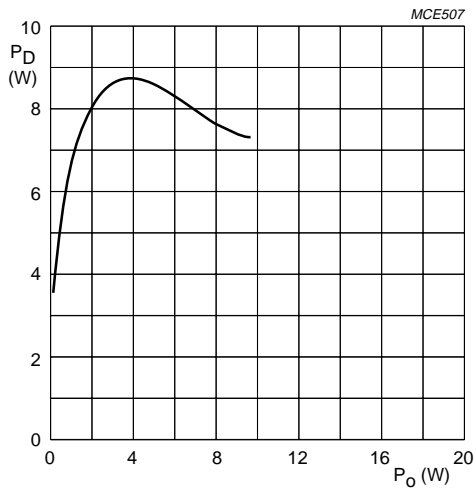
THD = 10 %; SE; R_L = 4 Ω; f = 1 kHz.

Fig 11. Output power as function of supply voltage.



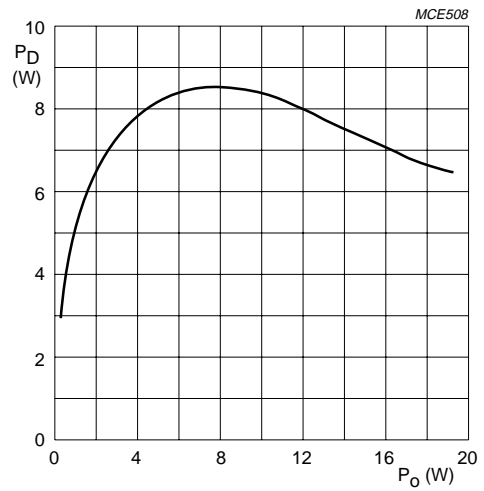
THD = 10 %; BTL; R_L = 8 Ω; f = 1 kHz.

Fig 12. Output power as function of supply voltage.



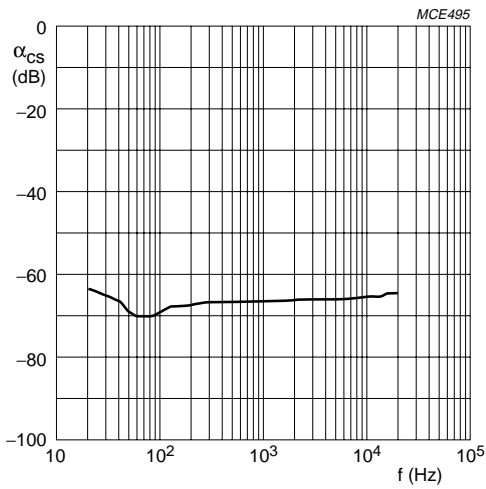
V_{CC} = 18 V; SE; R_L = 4 Ω.

Fig 13. Total (worst case, both channels driven) power dissipation as function of channel output power per channel.



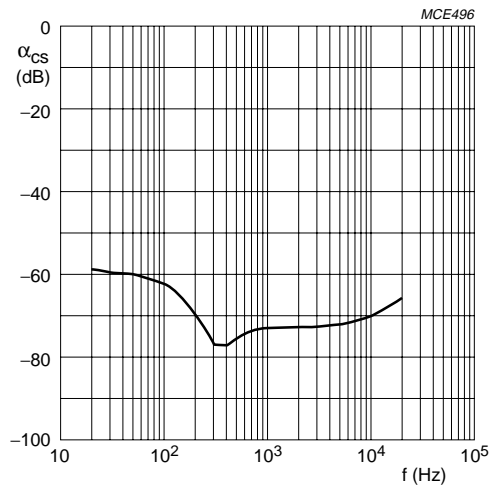
V_{CC} = 18 V; BTL; R_L = 8 Ω.

Fig 14. Total (worst case, both channels driven) power dissipation as function of channel output power per channel.



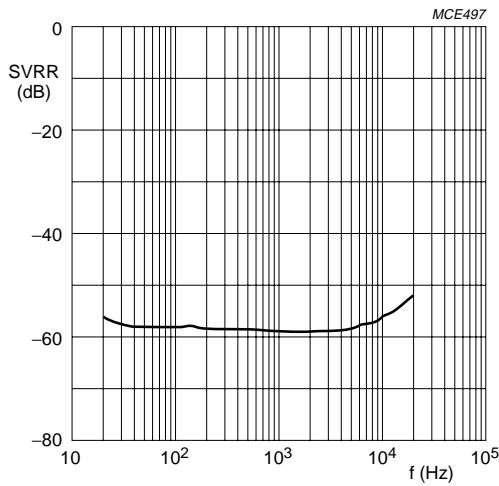
$V_{CC} = 18\text{ V}$; SE; $R_L = 4\ \Omega$.

Fig 15. Channel separation as function of frequency (no bandpass filter applied).



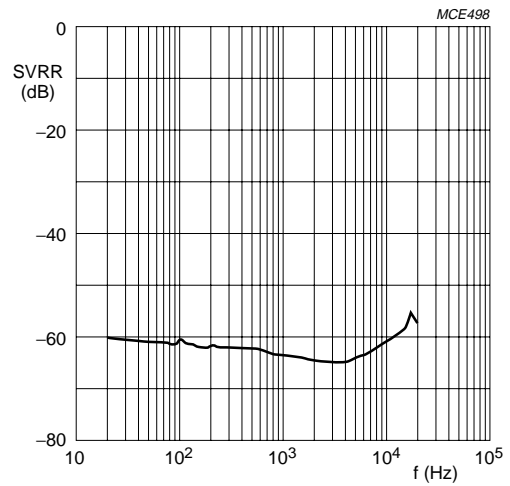
$V_{CC} = 18\text{ V}$; BTL; $R_L = 8\ \Omega$.

Fig 16. Channel separation as function of frequency (no bandpass filter applied).



$V_{CC} = 18\text{ V}$; SE; $R_{source} = 0\ \Omega$; $V_{ripple} = 300\text{ mV (RMS)}$; a bandpass filter of 20 Hz to 22 kHz has been applied; inputs short-circuited.

Fig 17. Supply voltage ripple rejection as function of frequency.



$V_{CC} = 18\text{ V}$; BTL; $R_{source} = 0\ \Omega$; $V_{ripple} = 300\text{ mV (RMS)}$; a bandpass filter of 20 Hz to 22 kHz has been applied; inputs short-circuited.

Fig 18. Supply voltage ripple rejection as function of frequency.

13. Application information

13.1 Application diagrams

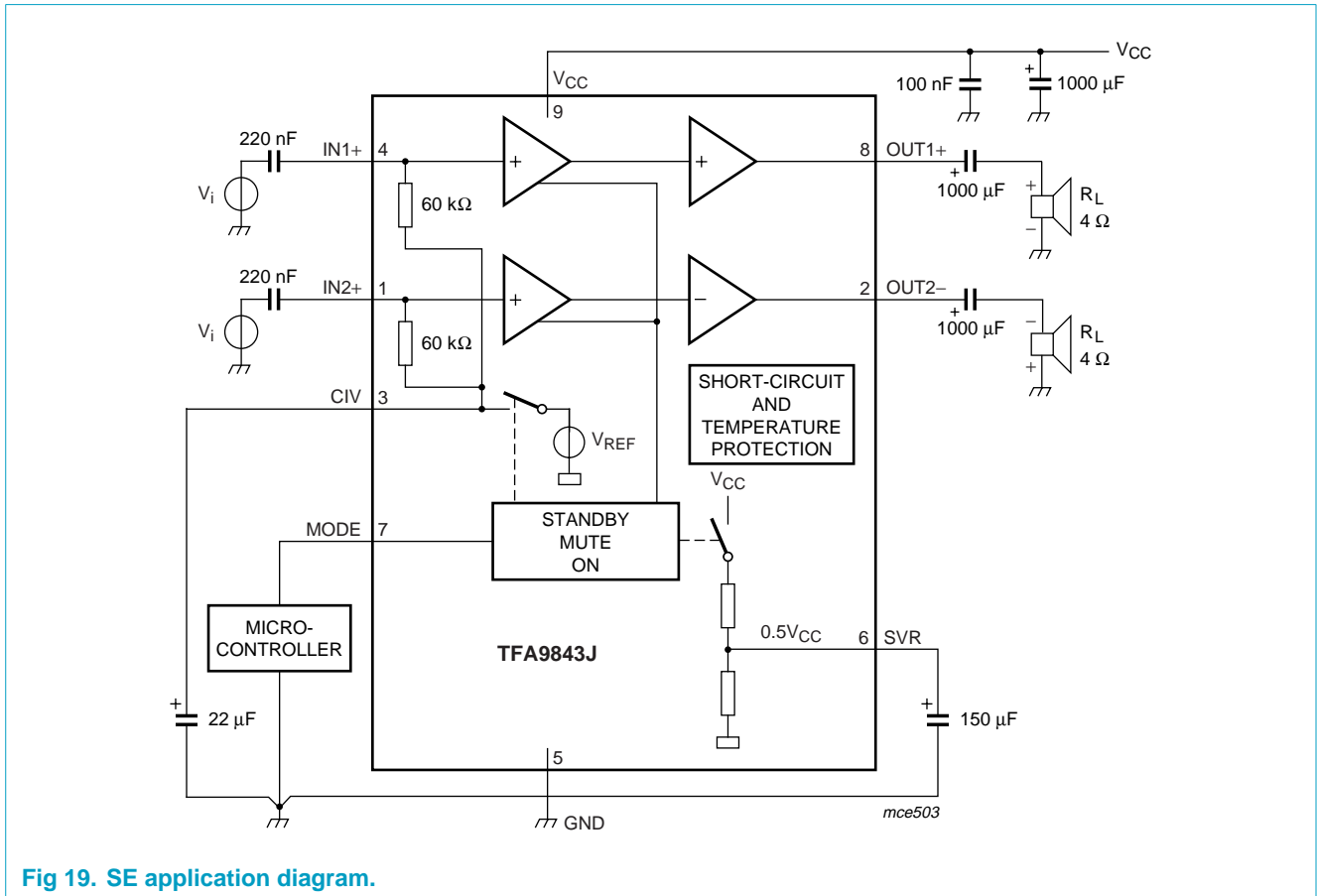


Fig 19. SE application diagram.

Remark: Switching inductive loads, the output voltage can rise beyond the maximum supply voltage of 28 V. At high supply voltage it is recommended to use (Schottky) diodes to the supply voltage and ground.

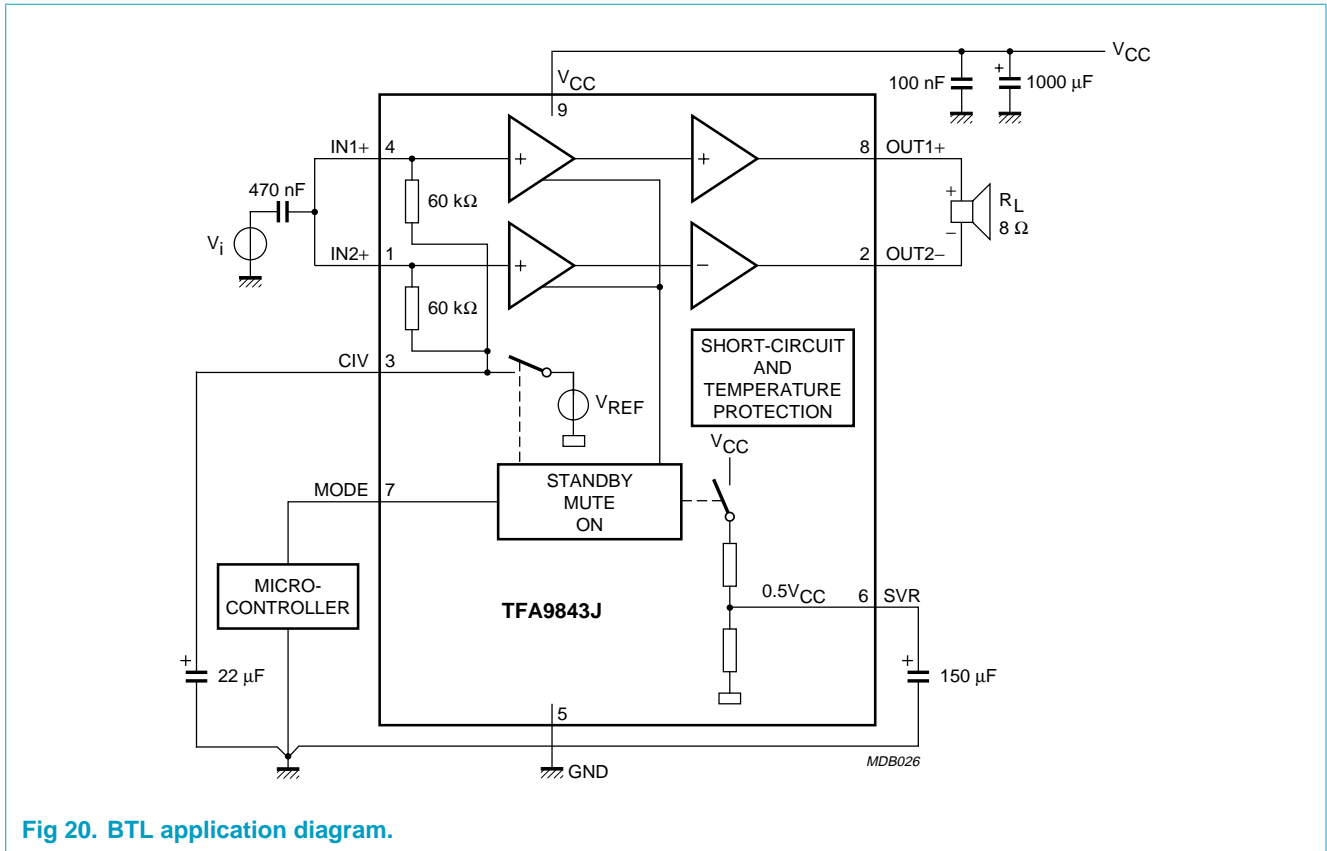


Fig 20. BTL application diagram.

Remark: Switching inductive loads, the output voltage can rise beyond the maximum supply voltage of 28 V. At high supply voltage it is recommended to use (Schottky) diodes to the supply voltage and ground.

13.2 Printed-circuit board

13.2.1 Layout and grounding

To obtain a high-level system performance, certain grounding techniques are essential. The input reference grounds have to be tied with their respective source grounds and must have separate tracks from the power ground tracks; this will prevent the large (output) signal currents from interfering with the small AC input signals. The small-signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible for delivering maximum output power.

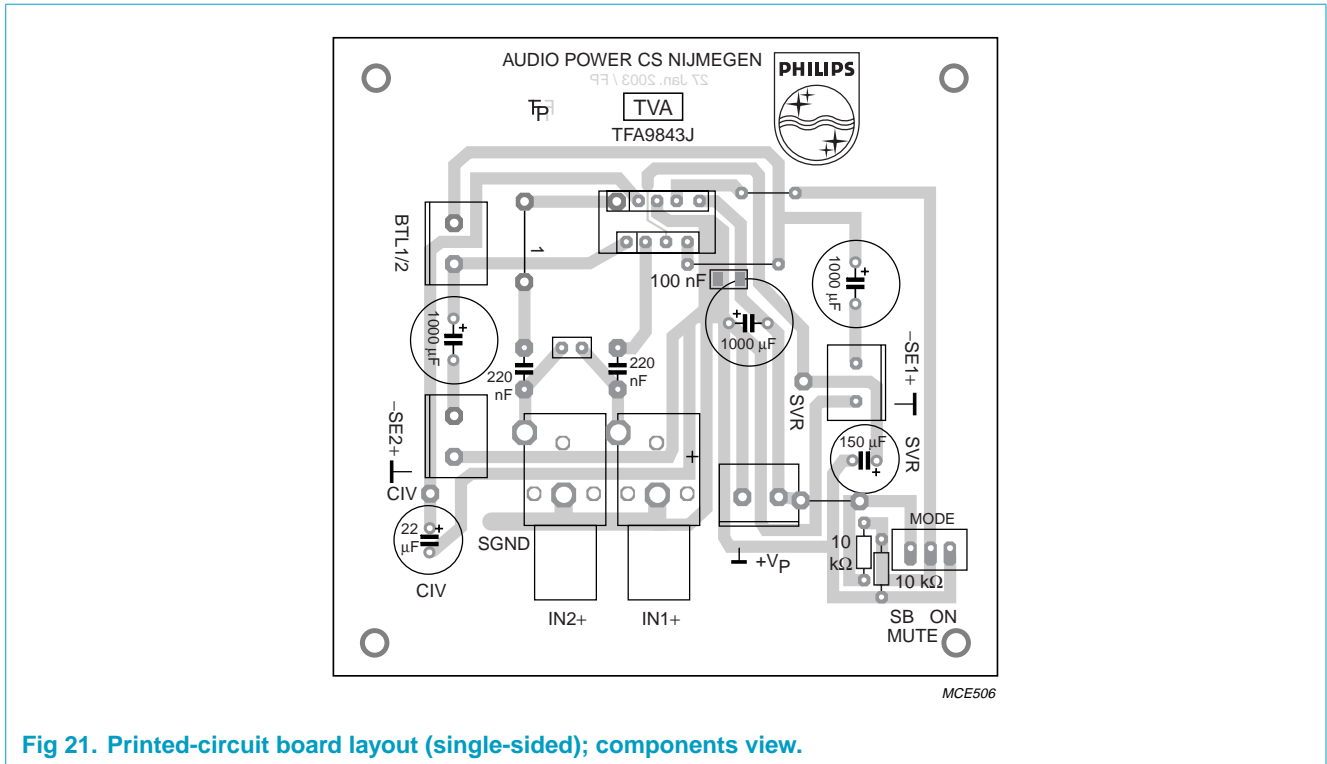


Fig 21. Printed-circuit board layout (single-sided); components view.

13.2.2 Power supply decoupling

Proper supply bypassing is critical for low-noise performance and high supply voltage ripple rejection. The respective capacitor location should be as close as possible to the device and grounded to the power ground. Proper power supply decoupling also prevents oscillations.

For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR, typical 100 nF, has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor, e.g. 1000 µF or greater, must be placed close to the device.

The bypass capacitor on pin SVR reduces the noise and ripple on the mid rail voltage. For good THD and noise performance a low ESR capacitor is recommended.

13.3 Thermal behavior and heatsink calculation

The measured maximum thermal resistance of the IC package, $R_{th(j-mb)}$, is 2.0 K/W. A calculation for the heatsink can be made, with the following parameters:

- $T_{amb(max)} = 60\text{ °C}$ (example)
- $V_{CC} = 18\text{ V}$ and $R_L = 4\ \Omega$ (SE)
- $T_{j(max)} = 150\text{ °C}$ (specification)

$R_{th(tot)}$ is the total thermal resistance between the junction and the ambient including the heatsink. This can be calculated using the maximum temperature increase divided by the power dissipation:

$$R_{th(tot)} = (T_{j(max)} - T_{amb(max)})/P_D$$

At $V_{CC} = 18\text{ V}$ and $R_L = 4\ \Omega$ (2 x SE) the measured worst-case sine-wave dissipation is 8.4 W; see Figure 13. For $T_{j(\max)} = 150\text{ }^\circ\text{C}$ the temperature raise, caused by the power dissipation, is: $150 - 60 = 90\text{ }^\circ\text{C}$:

$$P \times R_{th(\text{tot})} = 90\text{ }^\circ\text{C}$$

$$R_{th(\text{tot})} = 90/8.4 = 10.7\text{ K/W}$$

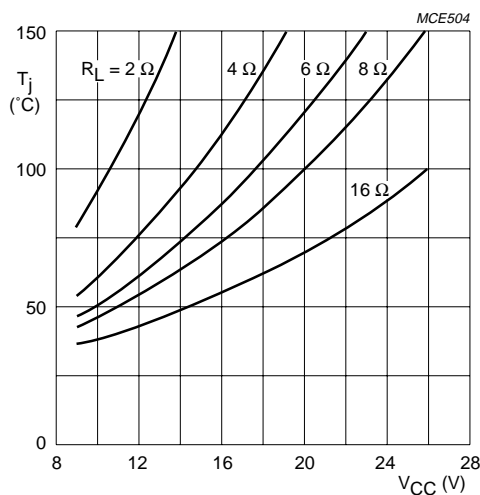
$$R_{th(\text{h-a})} = R_{th(\text{tot})} - R_{th(\text{j-mb})} = 10.7 - 2.0 = 8.7\text{ K/W}$$

This calculation is for an application at worst-case (stereo) sine-wave output signals. In practice music signals will be applied, which decreases the maximum power dissipation to approximately half of the sine-wave power dissipation (see Section 8.2.2). This allows for the use of a smaller heatsink:

$$P \times R_{th(\text{tot})} = 90\text{ }^\circ\text{C}$$

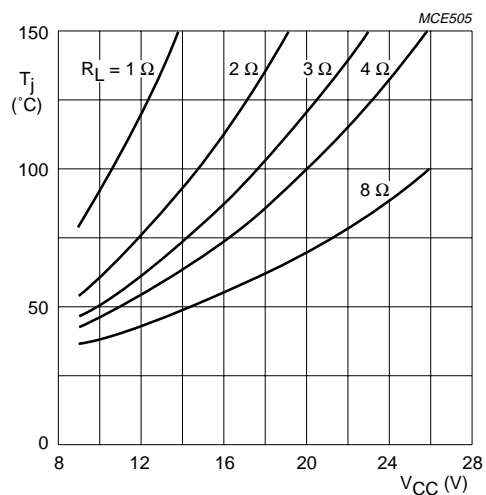
$$R_{th(\text{tot})} = 90/4.2 = 21.4\text{ K/W}$$

$$R_{th(\text{h-a})} = R_{th(\text{tot})} - R_{th(\text{j-mb})} = 21.4 - 2.0 = 19.4\text{ K/W}$$



2 x SE loads; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$; external heatsink of 10 K/W; music signals.

Fig 22. Junction temperature versus supply voltage.



BTL loads; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$; external heatsink of 10 K/W; music signals.

Fig 23. Junction temperature versus supply voltage.

14. Test information

14.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

15. Package outline

DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad SOT523-1

SOT523-1

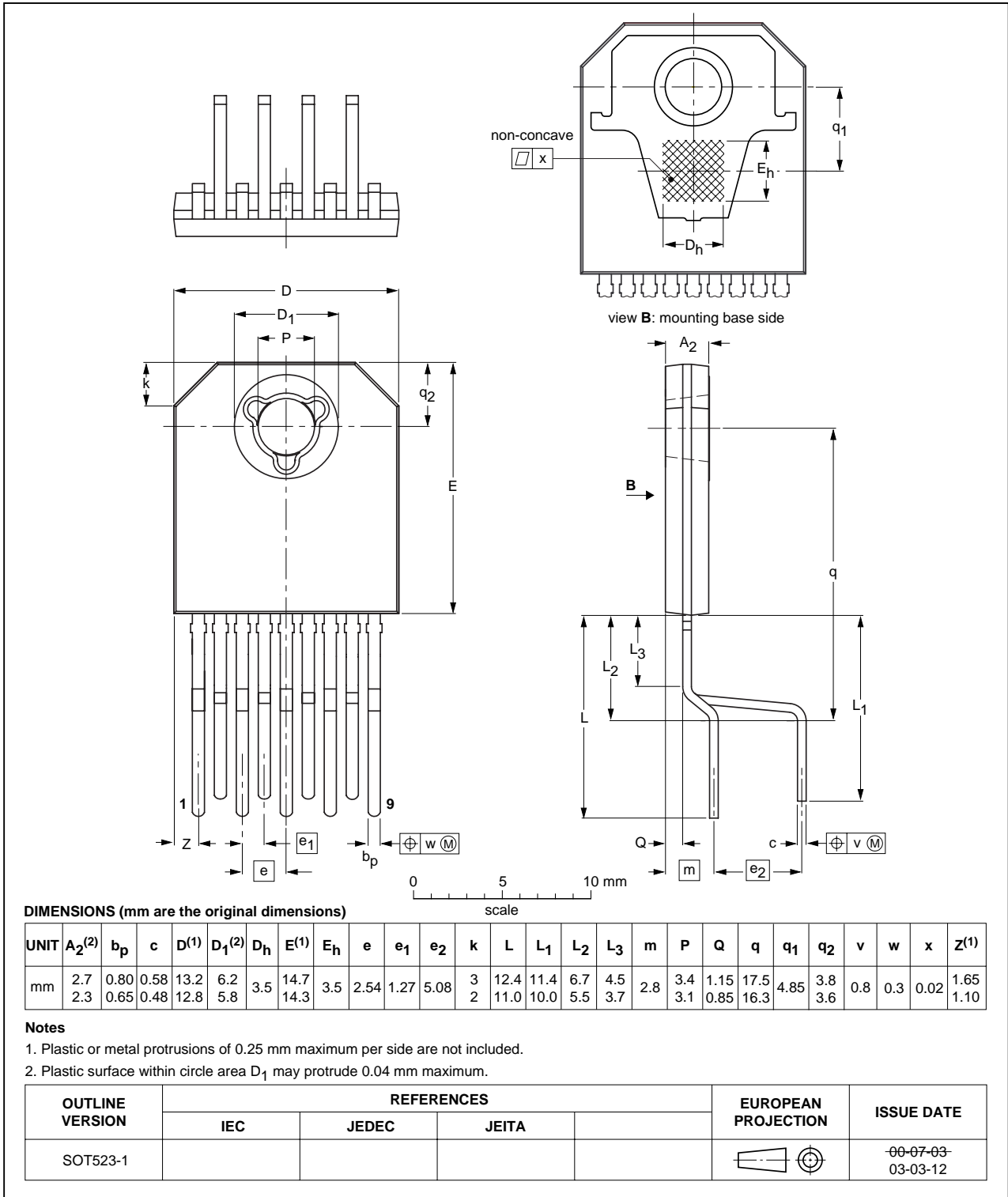


Fig 24. DBS9P package outline.

16. Soldering

16.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

16.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

16.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

16.4 Package related soldering information

Table 11: Suitability of through-hole mount IC packages for dipping and wave soldering methods

| Package | Soldering method | |
|---------------------------------|------------------|-------------------------|
| | Dipping | Wave |
| DBS, DIP, HDIP, RDBS, SDIP, SIL | suitable | suitable ^[1] |
| PMFP ^[2] | – | not suitable |

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

17. Revision history

Table 12: Revision history

| Rev | Date | CPCN | Description |
|-----|----------|------|---|
| 02 | 20040119 | - | Preliminary data (9397 750 12587) Modifications: <ul style="list-style-type: none">• Minor editorial changes. |
| 01 | 20030915 | - | Preliminary data (9397 750 10777) |

18. Data sheet status

| Level | Data sheet status ^[1] | Product status ^{[2][3]} | Definition |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

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