74FST3257

Quad 2:1 Multiplexer/ Demultiplexer Bus Switch

The ON Semiconductor 74FST3257 is a quad 2:1, high performance multiplexer/demultiplexer bus switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low R_{ON} and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

Features

- $R_{ON} < 4\ \Omega$ Typical
- Less Than 0.25 ns−Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin−For−Pin Compatible With QS3257, FST3257, CBT3257
- All Popular Packages: QSOP−16, TSSOP−16, SOIC−16
- All Devices in Package TSSOP are Inherently Pb−Free*

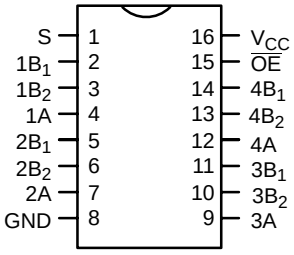

Figure 1. 16−Lead Pinout

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	A = B_1
H	L	A = B_2

Figure 2. Truth Table

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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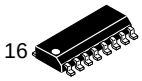
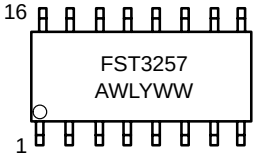
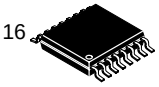
MARKING DIAGRAMS

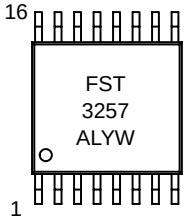


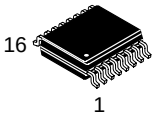
SOIC−16
D SUFFIX
CASE 751B



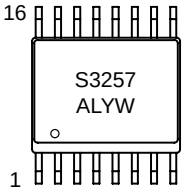


TSSOP−16
DT SUFFIX
CASE 948F





QSOP−16
QS SUFFIX
CASE 492



A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week

PIN NAMES

Pin	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
S_0, S_1	Select Inputs
A	Bus A
B_1, B_2, B_3, B_4	Bus B

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

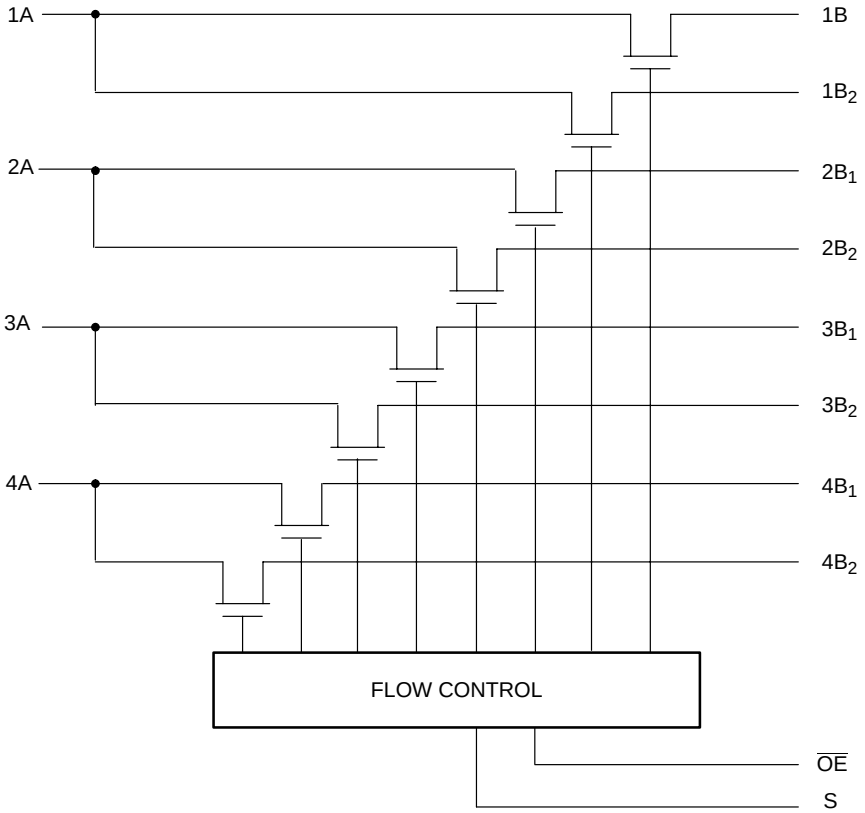


Figure 3. Logic Diagram

ORDERING INFORMATION

Device Order Number	Package	Shipping†
74FST32517D	SOIC−16	48 Units / Rail
74FST3257DR2	SOIC−16	2500 Units / Tape & Reel
74FST3257DT	TSSOP−16* (Pb−Free)	96 Units / Rail
74FST3257DTR2	TSSOP−16* (Pb−Free)	2500 Units / Tape & Reel
74FST3257QS	QSOP−16	96 Units / Rail
74FST3257QSR	QSOP−16	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		−0.5 to +7.0	V
V_O	DC Output Voltage		−0.5 to +7.0	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
I_O	DC Output Sink Current		128	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance	SOIC TSSOP QSOP	125 170 200	°C/W
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 N/A	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 4)	±500	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to JESD22−C101−A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating, Data Retention Only	4.0	5.5	V
V_I	Input Voltage	(Note 5)	0	5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0	5.5	V
T_A	Operating Free−Air Temperature		−40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate Switch I/O	Switch Control Input V_{CC} = 5.0 V ± 0.5 V	 0	DC 5	ns/V

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Typ*	Max	Unit
V_{IK}	Clamp Diode Resistance	$I_{IN} = -18mA$	4.5			−1.2	V
V_{IH}	High−Level Input Voltage		4.0 to 5.5	2.0			V
V_{IL}	Low−Level Input Voltage		4.0 to 5.5			0.8	V
I_I	Input Leakage Current	$0 \le V_{IN} \le 5.5$ V	5.5			±1.0	μA
I_{OZ}	OFF−STATE Leakage Current	$0 \le A, B \le V_{CC}$	5.5			±1.0	μA
R_{ON}	Switch On Resistance (Note 6)	V_{IN} = 0 V, I_{IN} = 64 mA	4.5		4	7	Ω
		V_{IN} = 0 V, I_{IN} = 30 mA	4.5		4	7	
		V_{IN} = 2.4 V, I_{IN} = 15 mA	4.5		8	15	
		V_{IN} = 2.4 V, I_{IN} = 15 mA	4.0		11	20	
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, I_{OUT} = 0	5.5			3	μA
ΔI_{CC}	Increase In I_{CC} per Input	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5			2.5	mA

*Typical values are at V_{CC} = 5.0 V and $T_A = 25°C$.

6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	$T_A = -40°C$ to $+85°C$, C_L = 50 pF, RU = RD = 500 Ω: V_{CC} = 4.5–5.5 V Min	Max	V_{CC} = 4.0 V Min	Max	Unit
t_{PHL}, t_{PLH}	Prop Delay Bus to Bus (Note 7)	V_I = OPEN		0.25		0.25	ns
	Prop Delay, Select to Bus A		1.0	4.7		5.2	
t_{PZH}, t_{PZL}	Output Enable Time, Select to Bus B	V_I = 7 V for t_{PZL}	1.0	5.2		5.7	ns
	Output Enable Time, I_{OE} to Bus A, B	V_I = OPEN for t_{PZH}	1.0	5.1		5.6	
t_{PHZ}, t_{PLZ}	Output Disable Time, Select to Bus B	V_I = 7 V for t_{PLZ}	1.0	5.2		5.5	ns
	Output Disable Time, I_{OE} to Bus A, B	V_I = OPEN for t_{PHZ}	1.0	5.5		5.5	

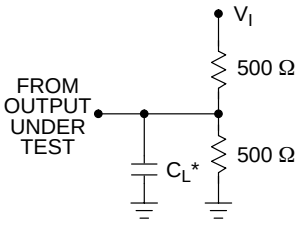
7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

CAPACITANCE (Note 8)

Symbol	Parameter	Conditions	Typ	Max	Unit
C_{IN}	Control Pin Input Capacitance	V_{CC} = 5.0 V	3		pF
$C_{I/O}$	A Port Input/Output Capacitance	V_{CC}, $\overline{OE}$ = 5.0 V	7		pF
$C_{I/O}$	B Port Input/Output Capacitance	V_{CC}, $\overline{OE}$ = 5.0 V	5		pF

8. $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



NOTES:

1. Input driven by 50 Ω source terminated in 50 Ω.
2. CL includes load and stray capacitance.

*C_L = 50 pF

Figure 4. AC Test Circuit

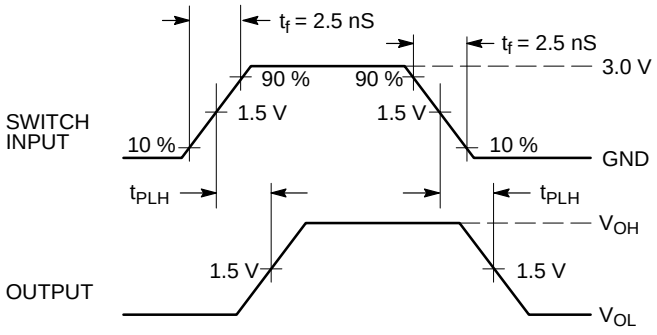


Figure 5. Propagation Delays

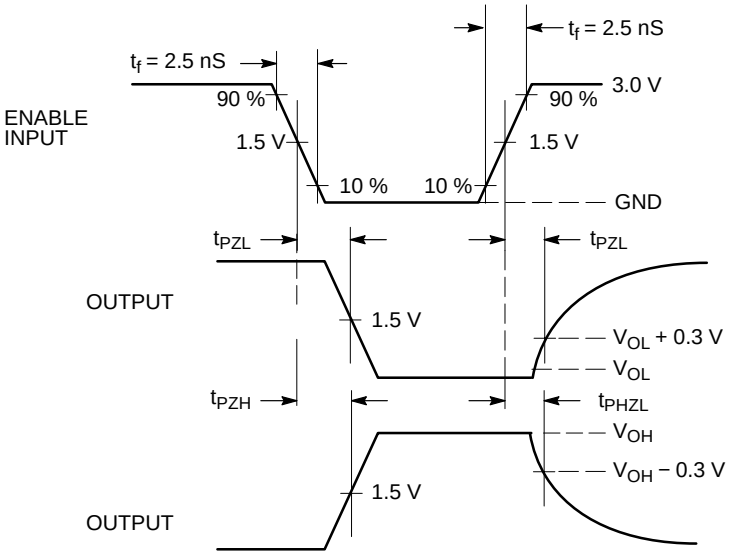
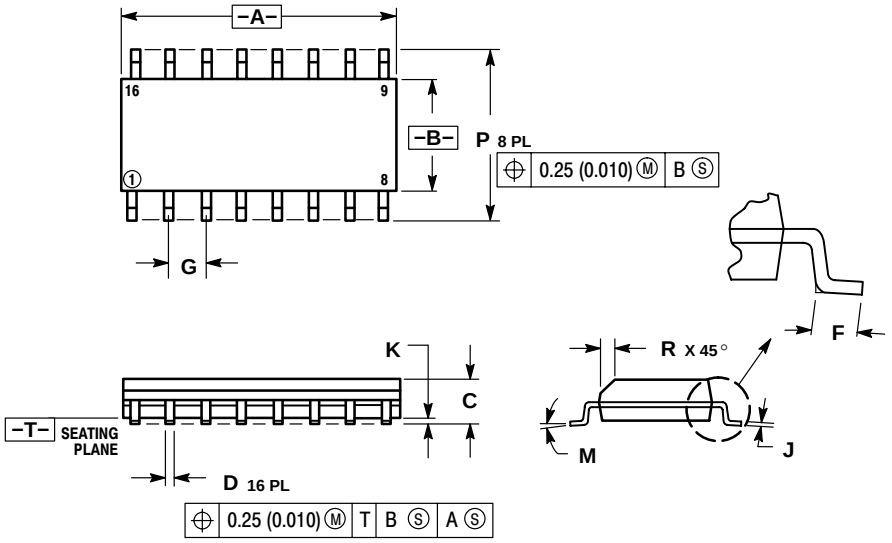


Figure 6. Enable/Disable Delays

PACKAGE DIMENSIONS

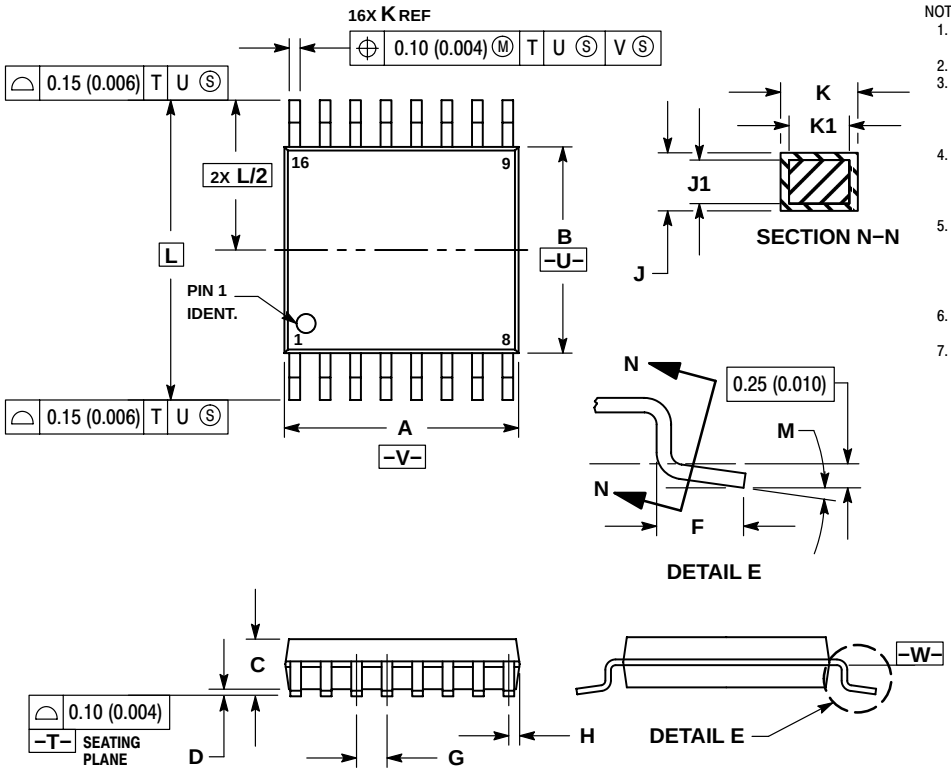
SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP−16
DT SUFFIX
CASE 948F−01
ISSUE O

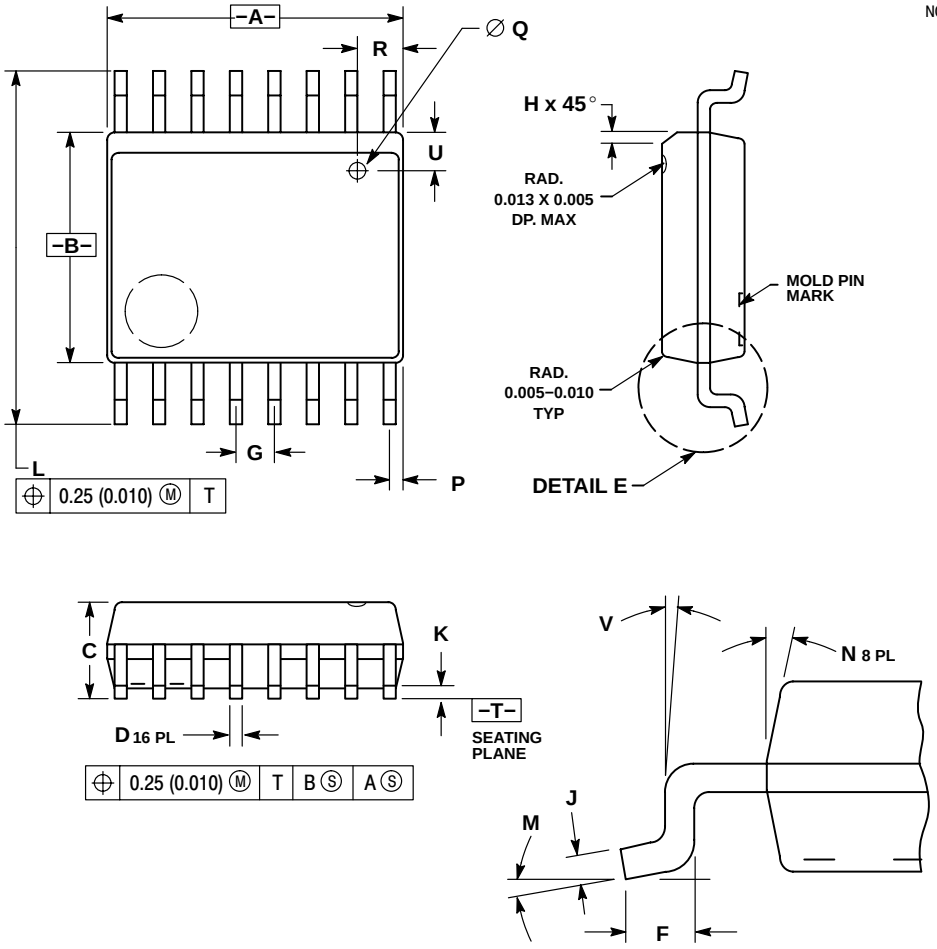


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

QSOP−16
QS SUFFIX
CASE 492−01
ISSUE O



DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.189	0.196	4.80	4.98
B	0.150	0.157	3.81	3.99
C	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.007	0.011	0.18	0.28
Q	0.020 DIA		0.51 DIA	
R	0.025	0.035	0.64	0.89
U	0.025	0.035	0.64	0.89
V	0°	8°	0°	8°

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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