# Quad 2:1 Multiplexer/ Demultiplexer Bus Switch

The ON Semiconductor 74FST3257 is a quad 2:1, high performance multiplexer/demultiplexer bus switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low  $R_{\rm ON}$  and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

#### **Features**

- $R_{ON} < 4 \Omega$  Typical
- Less Than 0.25 ns-Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible With QS3257, FST3257, CBT3257
- All Popular Packages: QSOP-16, TSSOP-16, SOIC-16
- All Devices in Package TSSOP are Inherently Pb-Free\*

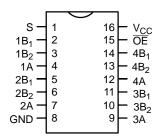


Figure 1. 16-Lead Pinout

S	ŌĒ	Function
X L H	Ι∟∟	Disconnect $A = B_1$ $A = B_2$

Figure 2. Truth Table



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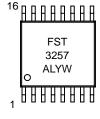
# MARKING DIAGRAMS





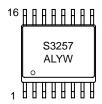


TSSOP-16 DT SUFFIX CASE 948F





QSOP-16 QS SUFFIX CASE 492



A = Assembly Location

L, WL = Wafer Lot Y = Year W, WW = Work Week

#### **PIN NAMES**

Pin	Description		
$\overline{OE}_1$ , $\overline{OE}_2$	Bus Switch Enables		
S <sub>0</sub> , S <sub>1</sub>	Select Inputs		
А	Bus A		
B <sub>1</sub> , B <sub>2</sub> , B <sub>3</sub> , B <sub>4</sub>	Bus B		

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

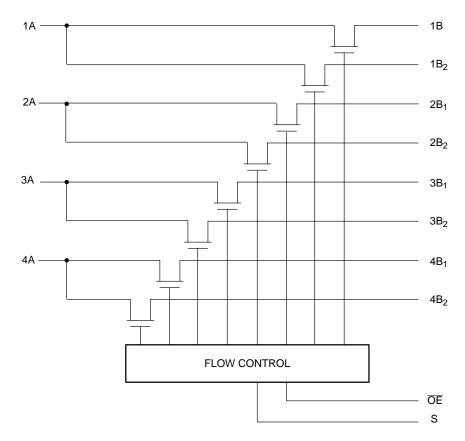


Figure 3. Logic Diagram

# **ORDERING INFORMATION**

Device Order Number	Package	Shipping <sup>†</sup>
74FST32517D	SOIC-16	48 Units / Rail
74FST3257DR2	SOIC-16	2500 Units / Tape & Reel
74FST3257DT	TSSOP-16* (Pb-Free)	96 Units / Rail
74FST3257DTR2	TSSOP-16* (Pb-Free)	2500 Units / Tape & Reel
74FST3257QS	QSOP-16	96 Units / Rail
74FST3257QSR	QSOP-16	2500 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
\*This package is inherently Pb–Free.

## **MAXIMUM RATINGS**

Symbol	Parameter		Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5  to  +7.0	V	
VI	DC Input Voltage		-0.5  to  +7.0	V
V <sub>O</sub>	DC Output Voltage		-0.5  to  +7.0	V
I <sub>IK</sub>	DC Input Diode Current	$V_I < GND$	-50	mA
I <sub>OK</sub>	DC Output Diode Current	$V_O < GND$	-50	mA
Io	DC Output Sink Current		128	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin		±100	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±100	mA	
T <sub>STG</sub>	Storage Temperature Range		-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
TJ	Junction Temperature Under Bias		+150	°C
$\theta_{\sf JA}$	Thermal Resistance	SOIC TSSOP QSOP	125 170 200	°C/W
MSL	Moisture Sensitivity		Level 1	
F <sub>R</sub>	Flammability Rating Oxygen I	ndex: 28 to 34	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage  Human Body Machine Mach	Model (Note 2)	> 2000 > 200 N/A	V
I <sub>Latchup</sub>	Latchup Performance Above V <sub>CC</sub> and Below GND at	85°C (Note 4)	±500	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- 1. Tested to EIA/JESD22-A114-A.
- 2. Tested to EIA/JESD22-A115-A.
- 3. Tested to JESD22-C101-A.
- 4. Tested to EIA/JESD78.

# **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter			Max	Unit
V <sub>CC</sub>	Supply Voltage	Operating, Data Retention Only	4.0	5.5	V
VI	Input Voltage	(Note 5)	0	5.5	V
Vo	Output Voltage	(HIGH or LOW State)	0	5.5	V
T <sub>A</sub>	Operating Free-Air Temperature		-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate Switch I/O	Switch Control Input $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	DC 5	ns/V

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

## DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			
Symbol	Parameter	Conditions	(V)	Min	Тур*	Max	Unit
V <sub>IK</sub>	Clamp Diode Resistance	I <sub>IN</sub> = -18mA	4.5			-1.2	V
V <sub>IH</sub>	High-Level Input Voltage		4.0 to 5.5	2.0			V
V <sub>IL</sub>	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I <sub>I</sub>	Input Leakage Current	$0 \le V_{IN} \le 5.5 V$	5.5			±1.0	μΑ
I <sub>OZ</sub>	OFF-STATE Leakage Current	$0 \le A, B \le V_{CC}$	5.5			±1.0	μΑ
R <sub>ON</sub>	Switch On Resistance (Note 6)	V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 64 mA	4.5		4	7	Ω
		V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 30 mA	4.5		4	7	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.5		8	15	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.0		11	20	
Icc	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0	5.5			3	μΑ
$\Delta I_{CC}$	Increase In I <sub>CC</sub> per Input	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5			2.5	mA

## **AC ELECTRICAL CHARACTERISTICS**

			$T_A = -40$ °C to $+85$ °C $C_L = 50$ pF, RU = RD = $500$ $\Omega$				
			V <sub>CC</sub> = 4	4.5–5.5 V	V <sub>CC</sub> =	4.0 V	Ī
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t <sub>PHL</sub> , t <sub>PLH</sub>	Prop Delay Bus to Bus (Note 7)	V <sub>I</sub> = OPEN		0.25		0.25	ns
	Prop Delay, Select to Bus A		1.0	4.7		5.2	1
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time, Select to Bus B	$V_I = 7 \text{ V for } t_{PZL}$	1.0	5.2		5.7	ns
	Output Enable Time, I <sub>OE</sub> to Bus A, B	V <sub>I</sub> = OPEN for t <sub>PZH</sub>	1.0	5.1		5.6	1
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time, Select to Bus B	$V_I = 7 \text{ V for } t_{PLZ}$	1.0	5.2		5.5	ns
	Output Disable Time, I <sub>OE</sub> to Bus A, B	V <sub>I</sub> = OPEN for t <sub>PHZ</sub>	1.0	5.5		5.5	1

<sup>7.</sup> This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

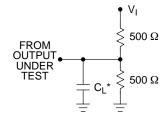
# **CAPACITANCE** (Note 8)

Symbol	Parameter	Conditions	Тур	Max	Unit
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> = 5.0 V	3		pF
C <sub>I/O</sub>	A Port Input/Output Capacitance	$V_{CC}$ , $\overline{OE} = 5.0 \text{ V}$	7		pF
C <sub>I/O</sub>	B Port Input/Output Capacitance	V <sub>CC</sub> , <del>OE</del> = 5.0 V	5		pF

<sup>8.</sup>  $T_A = +25$ °C, f = 1 MHz, Capacitance is characterized but not tested.

<sup>\*</sup>Typical values are at V<sub>CC</sub> = 5.0 V and T<sub>A</sub> = 25°C.
6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

# **AC Loading and Waveforms**



## NOTES:

- 1. Input driven by 50  $\Omega$  source terminated in 50  $\Omega.$
- 2. CL includes load and stray capacitance.
- ${}^{*}C_{L} = 50 pF$

Figure 4. AC Test Circuit

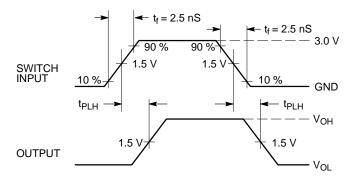


Figure 5. Propagation Delays

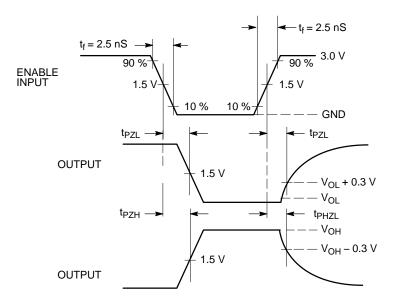
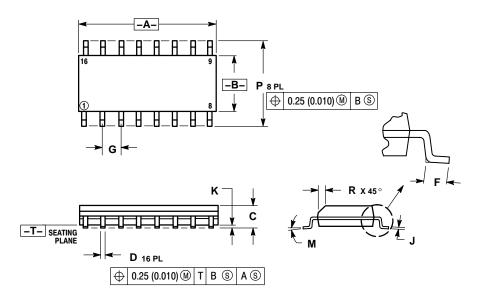


Figure 6. Enable/Disable Delays

#### PACKAGE DIMENSIONS

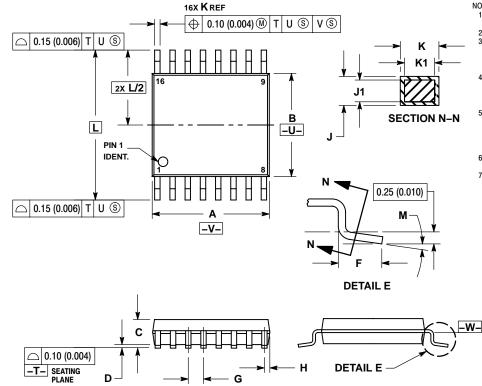
# SOIC-16 **D SUFFIX** CASE 751B-05 **ISSUE J**



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
O	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050 BSC	
_	0.19	0.25	0.008	0.009
Κ	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
Р	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

# TSSOP-16 **DT SUFFIX** CASE 948F-01 **ISSUE O**



#### NOTES:

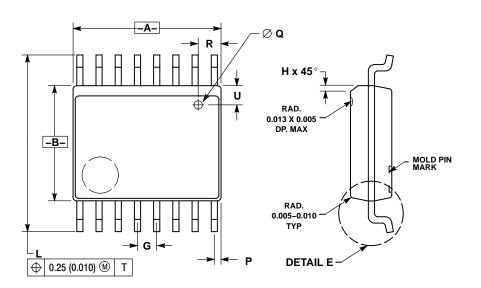
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
  DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15
- OR GATE BURRS SHALL NOT EXCEED 0.15
  (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD
  FLASH OR PROTRUSION. INTERLEAD FLASH OR
  PROTRUSION SHALL NOT EXCEED
  0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR
  PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
  EXCESS OF THE K DIMENSION AT MAXIMUM
  MATERIAL CONDITION MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

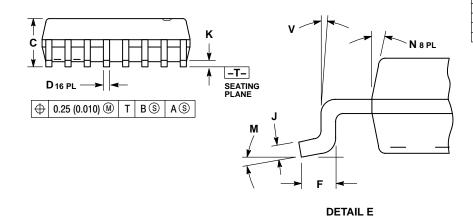
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

	MILLIMETERS		INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.18	0.28	0.007	0.011	
7	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40	BSC	0.252 BSC		
BA.	0.0	0.0	0.0	0.0	

## **PACKAGE DIMENSIONS**

# QSOP-16 **QS SUFFIX** CASE 492-01 ISSUE O





- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: INCH.

  3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.

  4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD.
- PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER
- 5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.189	0.196	4.80	4.98
В	0.150	0.157	3.81	3.99
С	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025	BSC	0.64	BSC
Н	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8 °	0°	8°
N	0°	7°	0°	7°
Р	0.007	0.011	0.18	0.28
Q	0.020	DIA	0.51 DIA	
R	0.025	0.035	0.64	0.89
U	0.025	0.035	0.64	0.89
٧	0°	8 °	0°	8°

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