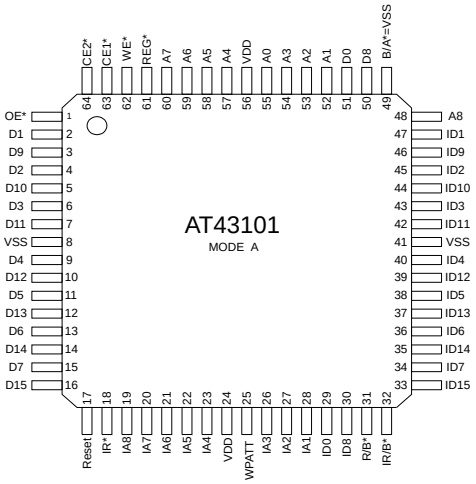
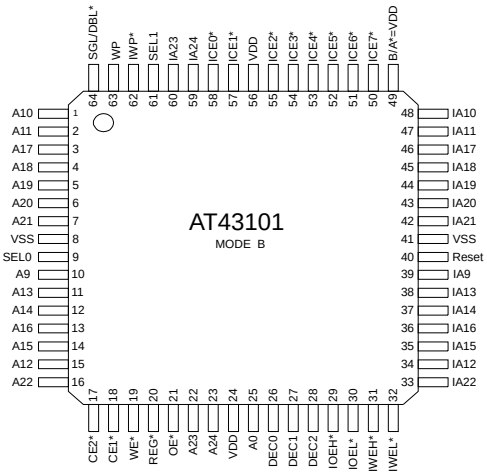
Features

- **Supports PCMCIA PC Card Standard - Release 2.1**
- **Directly connects to PCMCIA Connector**
- **No Additional Circuits Required**
- **256 x 8 Internal Parallel E^2PROM for CIS**
  - **Endurance: 10,000 Write Cycles**
  - **Data Retention: 10 Years**
  - **Internally Controlled Write Algorithm**
- **Operates over VCC = 4.5 to 5.5 Volts**
- **64 Pin TQFP, Max. Height = 1.2 mm Mounted**
- **Usage is Two Devices Per Card**
- **Dual Mode Device with Mode Select Pin**
- **Supports Up to 64 Mbytes of:**
  - **Flash E^2PROM SRAM**
  - **ROM OTP**

Description

The AT43101 is a low power, high integration PCMCIA interface chip set for memory cards. It provides a complete PCMCIA PC Card Standard Release 2.1 compliant interface with no other support devices. Two AT43101's are used on each memory card. A mode select pin configures the device for operation as a low order address and data buffer when low and as the high order address buffer/decoder when high. The two devices together form a complete address and data buffer, address decoder, memory device selection logic, read and write control logic and a Card Information Structure (CIS). Eight chip enable outputs are provided, supporting 16 memory devices. The device is pinned out for direct connection to the PCMCIA connector without PC trace cross-overs. Its 1.0 mm thick body allows population of both sides of a Type 1 PCMCIA card.





PCMCIA Card Memory Interface Circuit with 256 Bytes of Internal Attribute Memory EEPROM

AT43101

Pin Configuration

AT43101 pins are defined by the following two tables. The Pin Descriptions Table lists and describes the function of each signal used in the chip set. The Pin Assignment Table lists the signals connected to each pin for each mode and the buffer type implemented for the corresponding pin. The buffer type listed in the Pin Assignment Table does not always agree with the signal type listed in the Pin Description Table because the chip implements buffer types that support both modes of each pin. The pullup resistors included on chip as shown in the table have a nominal value of 375K ohms. An asterisk, "*", appended to a signal name indicates the signal is active low.

AT43101 Logical Pin Descriptions

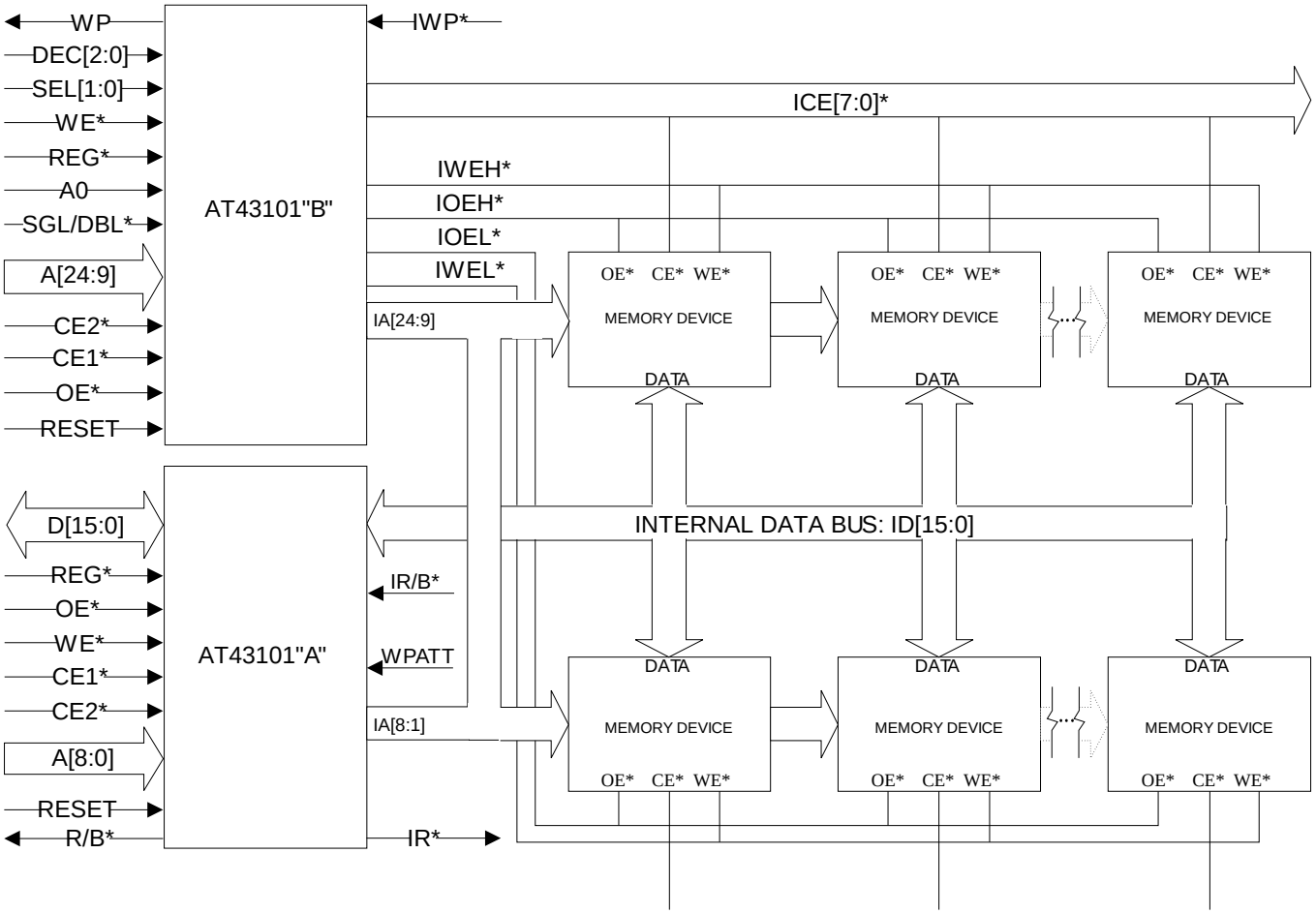
Name	Type	Description
D[15:0]	Bidir	PCMCIA Data Bus
A[24:0]	Input	PCMCIA Address Bus
CE2*	Input	Active low, PCMCIA byte enable for odd byte
CE1*	Input	Active low, PCMCIA byte enable for even byte
OE*	Input	Active low, PCMCIA output enable signal
WE*	Input	Active low, PCMCIA write enable signal
REG*	Input	PCMCIA signal high for common memory, low for attribute memory
ID[15:0]	Bidir	Memory data bus
IA[24:1]	Output	Memory address bus
SGL/DBL*	Input	Address decoder mode control input per function table
SEL[1:0]	Input	Address decoder selection inputs per function table
B/A*	Input	Mode select input. Low selects mode A, High selects mode B.
DEC[2:0]	Input	Address Inputs decoded to generate ICE[7:0]* outputs
IOEH*	Output	Active low output enable for upper byte of memory
IOEL*	Output	Active low output enable for lower byte of memory
IWEH*	Output	Active low write enable for upper byte of memory
IWEL*	Output	Active low write enable for lower byte of memory
IWP*	Input	Input from write protect switch
WP	Output	Output to PCMCIA write protect signal
ICE[7:0]*	Output	Active low chip enable outputs for 8 pairs of memory devices
Reset	Input	Active high reset
IR*	Output	Output of inverted reset
WPATT	Input	Active high attribute memory protect signal
R/B*	Output	Output from IR/B* and attribute memory Ready/Busy*
IR/B*	Input	Active low Ready/Busy* input for common memory

AT43101 Physical Pin Assignments

Pkg Pin	Mode A	Mode B	Type		Mode A	Mode B	Type	Pkg Pin
1	OE*	A10	Input		ID15	IA22	Bidir	33
2	D1	A11	Bidir		ID7	IA12	Bidir	34
3	D9	A17	Bidir		ID14	IA15	Bidir	35
4	D2	A18	Bidir		ID6	IA16	Bidir	36
5	D10	A19	Bidir		ID13	IA14	Bidir	37
6	D3	A20	Bidir		ID5	IA13	Bidir	38
7	D11	A21	Bidir		ID12	IA9	Bidir	39
8	VSS	VSS			ID4	Reset pd	Bidir	40
9	D4	SEL0 pu	Bidir		VSS	VSS		41
10	D12	A9	Bidir		ID11	IA21	Bidir	42
11	D5	A13	Bidir		ID3	IA20	Bidir	43
12	D13	A14	Bidir		ID10	IA19	Bidir	44
13	D6	A16	Bidir		ID2	IA18	Bidir	45
14	D14	A15	Bidir		ID9	IA17	Bidir	46
15	D7	A12	Bidir		ID1	IA11	Bidir	47
16	D15	A22	Bidir		A8	IA10	Bidir	48
17	Reset pd	CE2* pu	Input		B/A*	B/A*	Input	49
18	IR*	CE1* pu	Bidir		D8	ICE7*	Bidir	50
19	IA8	WE* pu	Bidir		D0	ICE6*	Bidir	51
20	IA7	REG* pu	Bidir		A1	ICE5*	Bidir	52
21	IA6	OE* pu	Bidir		A2	ICE4*	Bidir	53
22	IA5	A23	Bidir		A3	ICE3*	Bidir	54
23	IA4	A24	Bidir		A0	ICE2*	Bidir	55
24	VDD	VDD			VDD	VDD		56
25	WPATT pd	A0	Input		A4	ICE1*	Bidir	57
26	IA3	DEC0	Bidir		A5	ICE0*	Bidir	58
27	IA2	DEC1	Bidir		A6	IA24	Bidir	59
28	IA1	DEC2	Bidir		A7	IA23	Bidir	60
29	ID0	IOEH*	Bidir		REG* pu	SEL1 pu	Input	61
30	ID8	IOEL*	Bidir		WE* pu	IWP*	Input	62
31	R/B*	IWEH*	Output		CE1* pu	WP	Bidir	63
32	IR/B* pu	IWEL*	Bidir		CE2* pu	SGL/DBL* pu	Input	64

Note: pu after a pin name indicates a pull up.
pd after a pin name indicates a pull down.

System Block Diagram



Operation

The AT43101 is used in pairs to implement PCMCIA Release 2.1 compatible memory cards as shown in the system block diagram and in the internal chip block diagrams. Both PCMCIA signals and memory devices connect directly to the AT43101 with no additional components required. The AT43101 acts as a data and address buffer and address and control signal decoder for both an external memory array and an internal 256x8 E2PROM which contains the Card Information Structure.

The memory card is mapped into the Common Memory Address Space of PCMCIA according to the address signals connected to the DEC[2:0], SEL[1:0], and SGL/DBL* inputs. In a typical configuration, SGL/DBL* and SEL[1:0] are tied high or left floating since they are pulled up internally. Then DEC[2:0] function as direct inputs to the address/chip enable decoder.

For example, A[25:23] are connected to DEC[2:0] and IA[22:1] are connected to A[21:0] of sixteen 4 Mbyte devices. Note that A0 is used in conjunction with CE1* and CE2* to decode the data access and is not used as a common memory address. A[25:23] then determine which ICE[7:0] line is active.

Mixed memory size applications can use SGL/DBL* pulled low to enable a mixed mode decoding. This then enables either DEC[2:0] or SEL[1:0] as inputs to the address/chip enable decoder based on the state of SEL[1:0].

For example, the common memory space contains eight 1 Mbyte SRAM devices and six 4 Mbyte Flash devices. A[22:21] are connected to DEC[1:0] (DEC[2] is a don't care) and A[24:23] are connected to SEL[1:0]. Then IA[22:1] are used to connect to A[19:0] of the SRAM and A[21:0] of the Flash devices. ICE[3:0]* are connected to the four SRAM banks and ICE[7:5] to the three Flash banks. The SRAM is then memory mapped to the lower 4 M words of addressing and the Flash to the next 12 M words. All addressing is contiguous. Notice that ICE4* can not be used with this decoding scheme.

Address Decoder Operation

SGL/DBL* = H			SGL/DBL* = L		
SEL[1:0]	**DEC[2:0]**	**ICE[7:0]***	**SEL[1:0]**	**DEC[2:0]**	**ICE[7:0]***
XX	LLL	HHHHHHHL	LL	XLL	HHHHHHHL
XX	LLH	HHHHHHLH	LL	XLH	HHHHHHLH
XX	LHL	HHHHHLHH	LL	XHL	HHHHHLHH
XX	LHH	HHHHLHHH	LL	XHH	HHHHLHHH
XX	HLL	HHHLHHHH			
XX	HLH	HHLHHHHH	LH	XXX	HHLHHHHH
XX	HHL	HLHHHHHH	HL	XXX	HLHHHHHH
XX	HHH	LHHHHHHH	HH	XXX	LHHHHHHH

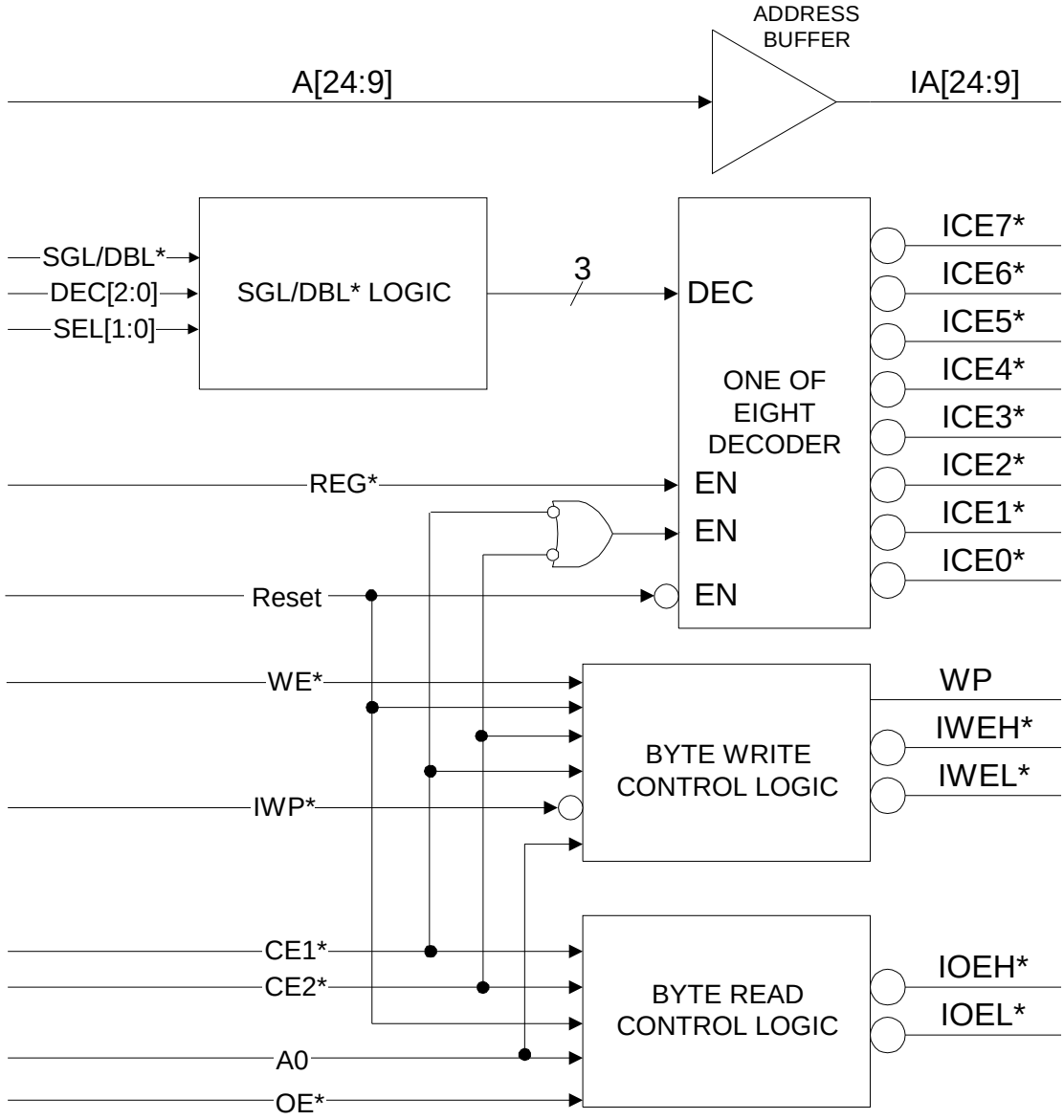
The AT43101 provides separate output and write enables for the upper and lower bytes of the memory array to implement byte addressing. The assertion of these outputs under the control of A0, CE2*, CE1*, OE* and WE* is given by the following table when REG* is high.

Byte Control Logic Operation

OE*	WE*	CE2*	CE1*	A0	IOEL*	IOEH*	IWEL*	IWEH*
H	H	X	X	X	H	H	H	H
L	H	H	H	X	H	H	H	H
L	H	H	L	L	L	H	H	H
L	H	H	L	H	H	L	H	H
L	H	L	H	X	H	L	H	H
L	H	L	L	X	L	L	H	H
H	L	H	H	X	H	H	H	H
H	L	H	L	L	H	H	L	H
H	L	H	L	H	H	H	H	L
H	L	L	H	X	H	H	H	L
H	L	L	L	X	H	H	L	L

The IWP* input provides write protection for common memory. When IWP* is low, assertion of IWEL* and IWEH* is inhibited. The WPATT input provides write protection for the attribute memory when high. This signal is pulled down internally for applications not requiring write protection. In addition, the AT43101 is disabled for 3 milliseconds during power up to prevent writes from occurring to either attribute or common memory. The state of the A*/B pin is also latched at this time. The AT43101 does not support the optional PCMCIA WAIT* signal.

Block Diagram for Mode B Operation



The AT43101 supports both Common and Attribute Memory read and write cycles of word and byte width. Common memory, the external memory devices on the PC card, is selected when REG* is high and can be accessed in either byte or word mode. Attribute memory, the internal 256x8 E2PROM, is selected when REG* is low and can only be accessed as the even byte of it's 512 byte address space. Byte/word addressing is controlled by CE1*, CE2* and A0. OE* functions as an active low output enable. WE* functions as an active low write enable.

Memory access functionality is defined by the following table. When Attribute Memory is selected by the assertion of REG*, only the lower data bus, D[7:0] is valid and only even numbered addresses may be accessed. Accordingly, an entry of "H or L" in the REG* of the function table means the access is supported for both Common Memory and Attribute Memory. An entry of "H only" means the access is supported for Common Memory accesses but not for Attribute Memory accesses.

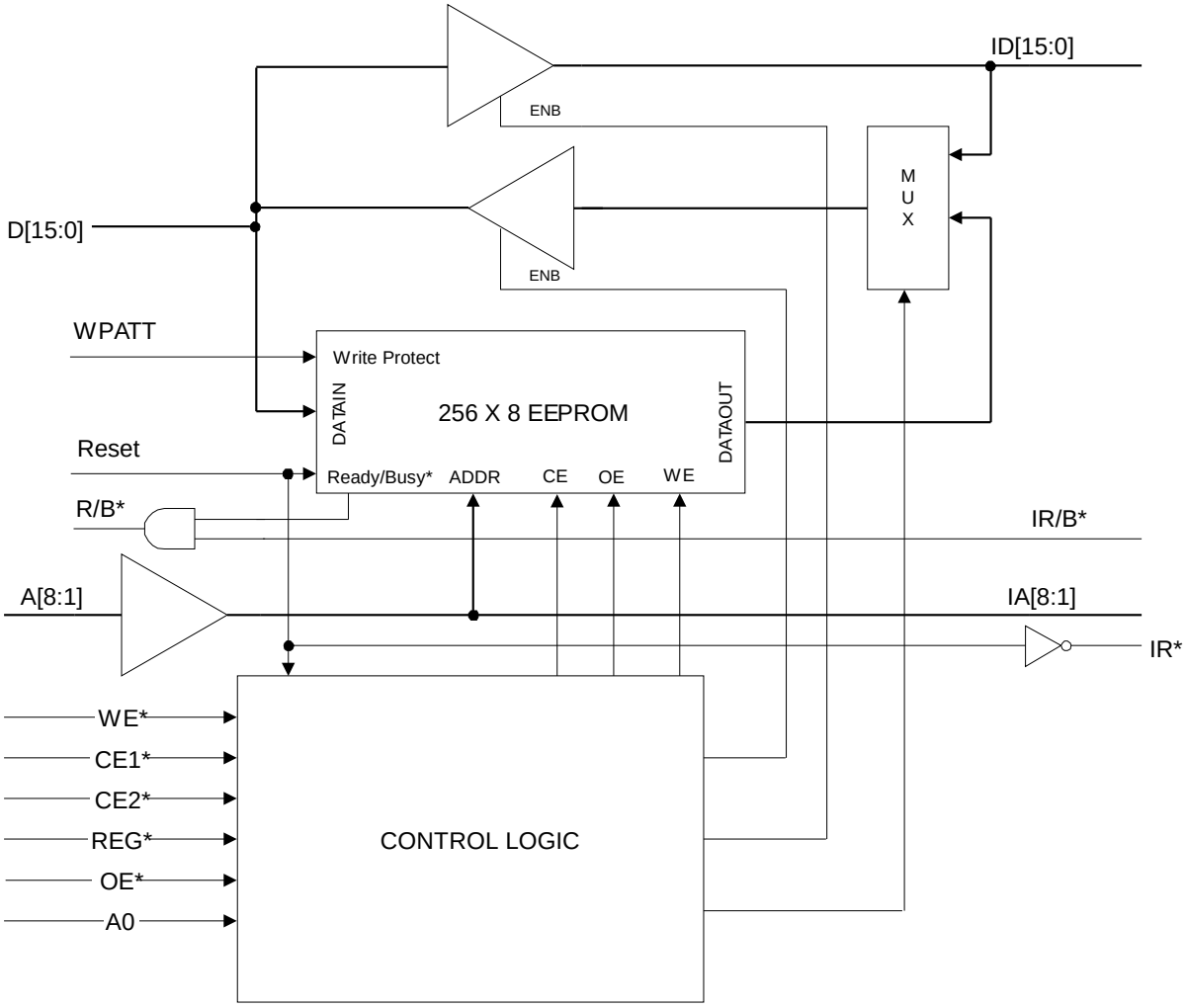
During word accesses of Common Memory, D[15:0] and ID[15:0] are active. During byte accesses (other than Odd Byte Only accesses), the PCMCIA transfers take place on D[7:0] and the AT43101 performs the required byte lane swapping based on A0 to and from D[15:8] or D[7:0]

Memory Access Functions

Mode	REG*	CE2*	CE1*	A0	OE*	WE*	D[15:8]	D[7:0]
Standby	X	H	H	X	X	X	High Z	High Z
Byte Read, Even	H or L	H	L	L	L	H	High Z	D(Even)
Byte Read, Odd	H only	H	L	H	L	H	High Z	D(Odd)
Word Read	H only	L	L	X	L	H	D(Odd)	D(Even)
Odd byte only Read	H only	L	H	X	L	H	D(Odd)	High Z
Byte Write, Even	H or L	H	L	L	H	L	X	D(Even)
Byte Wrtite, Odd	H only	H	L	H	H	L	X	D(Odd)
Word Write	H only	L	L	X	H	L	D(Odd)	D(Even)
Odd byte only Write	H only	L	H	X	H	L	D(Odd)	X

The E^2PROM includes address and data latches which are clocked at the leading edge of the effective write pulse that results from the gating of the PCMCIA control signals. The Tsu(CE), Tsu(REG), Tsu(WE) timing parameters shown in the AC Write Characteristics guarantee adequate pulse width for the latch clock signals. The actual write is triggered by the rising edge of the first of WE* or CE1* to go high. Writes to the E2PROM Attribute Memory must observe either a 10 ms. write recovery/cycle time or wait until R/B* goes inactive before another write can be initiated.

Block Diagram for Mode A Operation



Absolute Maximum Ratings*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to VSS	-0.6 V to Vcc +0.6 V
Maximum Operating Voltage	6.1 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stess rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (F = 1 MHz, T = 25°C) [1]

	Max	Units	Conditions
Cin	12	pf	Vin = 0 V
Cout	12	pf	Vout = 0 V

Note: 1. These parameters are characterized and not 100% tested.

DC and AC Operating Range

	AT43101
Operating Temperature (Case)	0°C to 70°C
V_{CC} Power Supply	4.5 V to 5.5 V

DC Characteristics

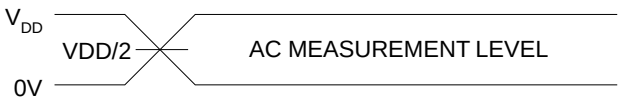
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	Vin = 0 V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	Vin = 0 V to V_{CC}	-10	10	µA
I_{LIP}	Input Load Current	Inputs with pullups/downs	-150	+150	µA
I_{SB}	Standby Current	V_{CC}=5.5 V Inputs=0 or V_{CC} I out=0mA		200	µA
I_{CCA}	Operating Current	V_{CC} =5.5 V Inputs=0 or V_{CC}, I out=0mA		5	mA
I_{CCP}	E^2PROM Write Current	V_{CC} =5.5 V Inputs=0 or V_{CC}, I out=0mA		5	mA
V_{IL}	Input Low Voltage			0.3V_{CC}	V
V_{IH}	Input High Voltage		.7V_{CC}		V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA V_{CC} = 4.5 V		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA, V_{CC} = 4.5 V	2.4		V

AC Read Characteristics

Symbol	Parameter	Min	Max	Notes
tia(A)	Delay to IA[24:0], from A[24:0]	0 ns	30 ns	
tda(A)	Data access time, from A[8:0] to D[7:0]		250 ns	3
ten(CE)	Output enable time from CE*	5 ns	36 ns	1
ten(OE)	Output enable time from OE*	5 ns	36 ns	
ten(REG)	Output enable time from REG*		36 ns	2
tdis(CE)	Output disable time from CE*		58 ns	1
tdis(OE)	Output disable time from OE*		58 ns	
tdis(REG)	Output disable time from REG*		58 ns	
tioel(A0)	Delay to IOEL*, IOEH* assertion from A0		28 ns	
tioel(CE)	Delay to IOEL*, IOEH* assertion from CE*		28 ns	1
tioel(OE)	Delay to IOEL*, IOEH* assertion from OE*		25 ns	
tioel(REG)	Delay to IOEL*, IOEH* assertion from REG*		28 ns	2
tioeh(A0)	Delay to IOEL*, IOEH* de-assertion from A0		28 ns	
tioeh(CE)	Delay to IOEL*, IOEH* de-assertion from CE*		28 ns	1
tioeh(OE)	Delay to IOEL*, IOEH* de-assertion from OE*		25 ns	
tioeh(REG)	Delay to IOEL*, IOEH* de-assertion from REG*		28 ns	2
tv(A)	Delay to data change, from change of address	0 ns		
td(ID)	Delay from ID[15:0] to D[15:0]		27 ns	
tice(A)	Delay to ICE[7:0]* from DEC[2:0], SEL[1:0], SGL/DBL*		38 ns	4
tice(REG)	Delay to ICE[7:0]* from REG*		38 ns	4
tice(CE)	Delay to ICE[7:0]* from CE1*, CE2*		30 ns	4
Ten (reset)	Chip active enable time from reset		50 ns	5
Tdis (reset)	Chip active disable time from reset		50 ns	5

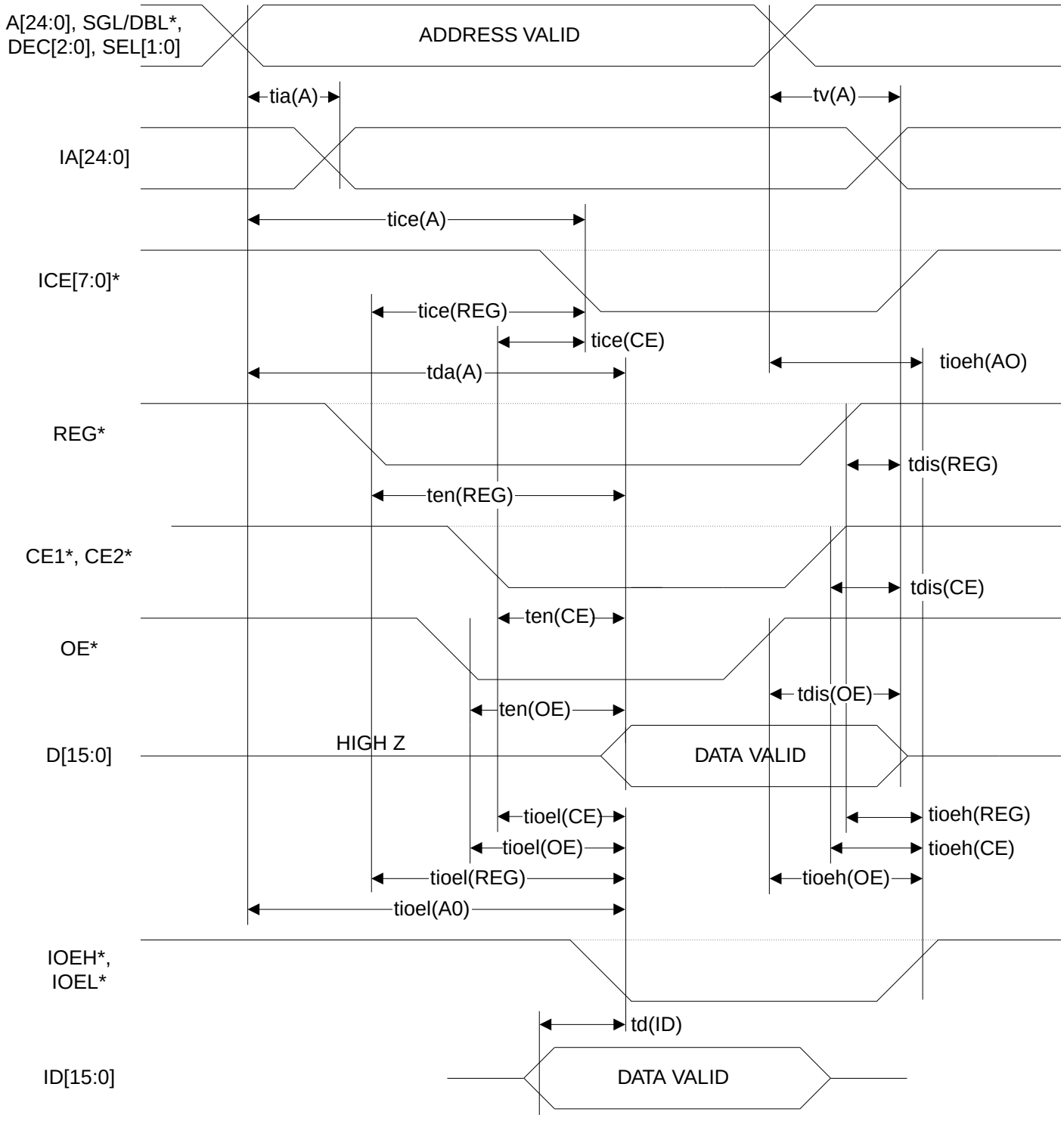
Notes:
1. Either or both of CE1*, CE2* assert according to function truth table.
2. REG* asserted only for Attribute Memory read.
3. tda(A) applies to Attribute Memory read. Access time for Common Memory read is derived from tia(A), td(ID), and external device access time.
4. Symmetrical for assertion and de-assertion. Also applies to write cycles.
5. Not shown in timing diagram.

Input Test Waveforms and Measurement Level



$t_{R1}t_f$<5 ns, test load capacitance is ≥ 50pf

AC Read Waveforms

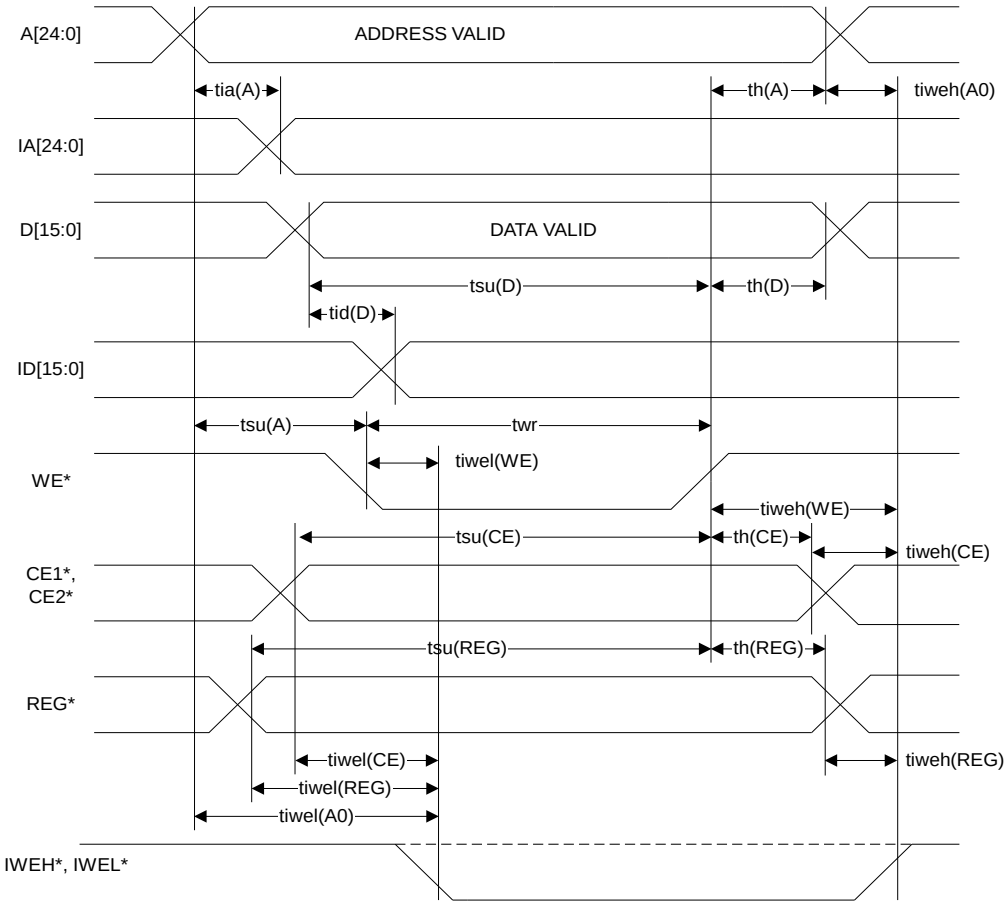


AC Write Characteristics

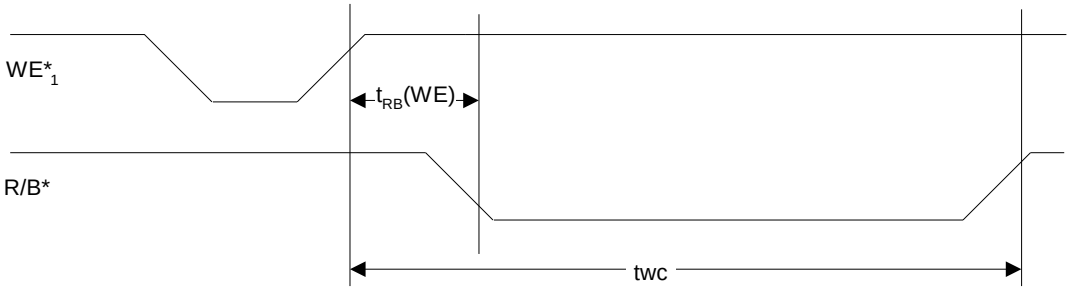
Symbol	Parameter	Min	Max	Note
tia(A)	Delay to IA[24:0], from A[24:0]	0	30 ns	
tid(D)	Delay to ID[15:0], from D[15:0]	0	31 ns	
tsu(A)	Setup time, A[24:0] valid before WE* assertion	26 ns		1
th(A)	Hold time, A[24:0] after WE* de-assertion	11 ns		1
tsu(D)	Setup time, D[15:0] valid before WE* de-assertion	10 ns		1
th(D)	Hold time, D[15:0] after WE* de-assertion	10 ns		1
tsu(CE)	Setup time, CE*, CE* before WE* de-assertion	190 ns		2
th(CE)	Hold time, CE*, CE* after WE* de-assertion	0		2
twc	Write cycle time		10 ms	1
twr	Minimum active pulse of WE*, CE1*	190 ns		1
tsu(REG)	Setup time, REG* to WE*	190 ns		
th(REG)	Hold time, REG* after WE* de-assertion	0		
tiwel(A0)	Delay to IWEL*, IWEH* assertion from A0	0	25 ns	4
tiwel(CE)	Delay to IWEL*, IWEH* assertion from CE*	0	25 ns	4
tiwel(WE)	Delay to IWEL*, IWEH* assertion from WE*	0	25 ns	4
tiwel(REG)	Delay to IWEL*, IWEH* assertion from REG*	0	25 ns	4
tiweh(A0)	Delay to IWEL*, IWEH* de-assertion from A0	0	25 ns	
tiweh(CE)	Delay to IWEL*, IWEH* de-assertion from CE*	0	25 ns	2
tiweh(WE)	Delay to IWEL*, IWEH* de-assertion from WE*	0	25 ns	
tiweh(REG)	Delay to IWEL*, IWEH* de-assertion from REG*	0	25 ns	3
twp(IWP)	Delay to WP, from IWP*	0	25 ns	5
twe(IWP)	Delay to IWEH*, IWEL* from IWP*	0	25 ns	5
tRB(WE)	Delay to R/B* from start of E^2PROM write		50 ns	1
tRB(IRB)	Delay to R/B* from IR/B*		40 ns	

Notes:
1. Parameter applies to writes of internal E^2PROM.
2. Either or both of CE1*, CE2* assert according to function truth table.
3. REG* asserted only for Attribute Memory write. REG* must be stable during the write at the level appropriate to the memory type being accessed.
4. One or both of IWEH*, IWEL* assert per A0, CE1*, CE2*, provided REG* is high.
5. Not shown in timing diagrams.

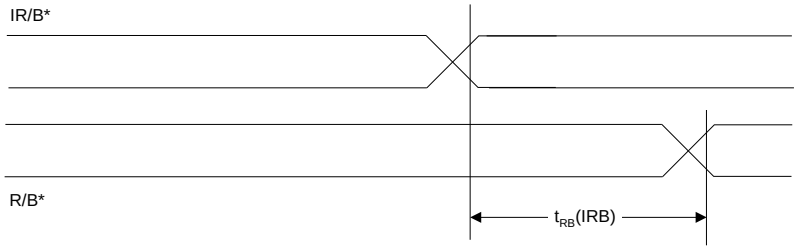
A. C. Write Waveforms - WE* Control



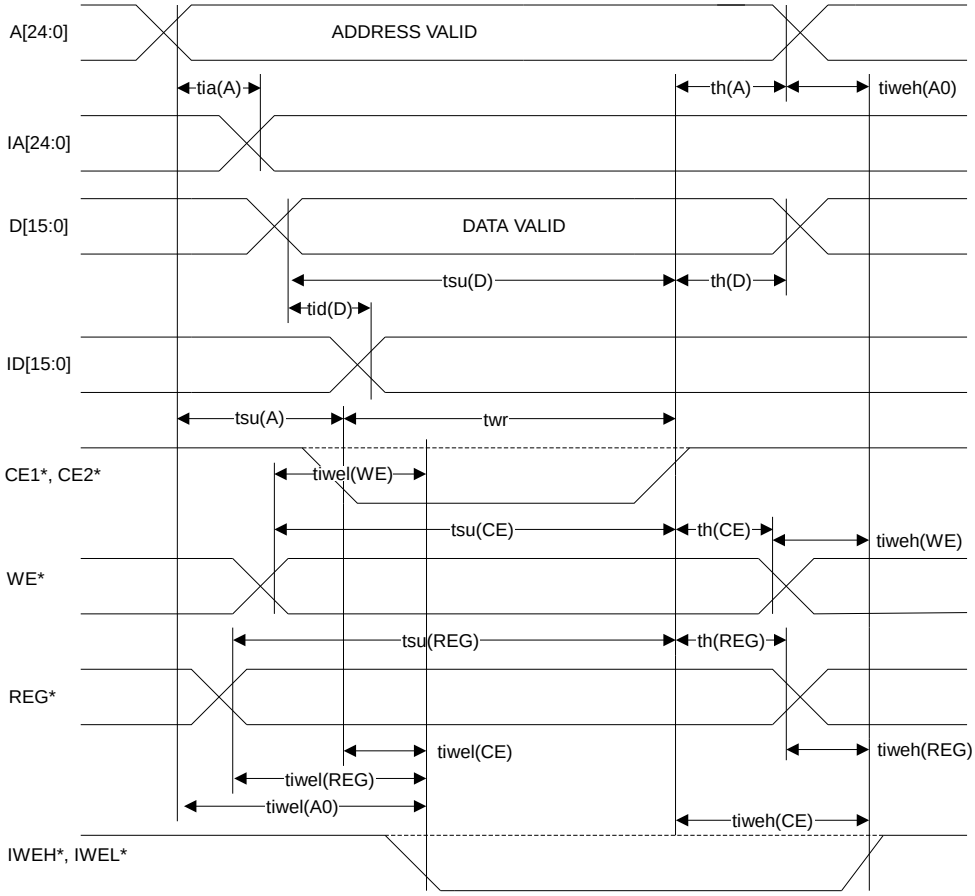
Ready/Busy* Waveforms



1) CE* or WE* dependant on controlling signal



AC Write Waveforms - CE Control



Packaging and Ordering Information

Package Type	Pin Count, Dimensions	Part Number
TQFP	64 pins, 1 mm thick	AT43101