

DATA SHEET

BST74A N-channel vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

N-channel vertical D-MOS transistor

BST74A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	P_{tot}	max.	1 W
Drain-source ON-resistance $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ.	6 Ω
		max.	12 Ω
Transfer admittance $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$	$ Y_{fs} $	typ.	250 mS

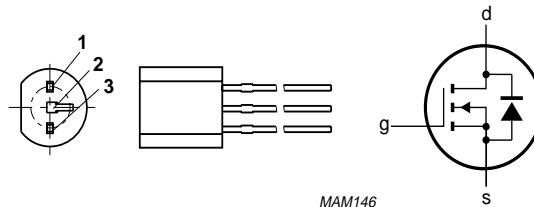
FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

PINNING - TO-92 VARIANT

- 1 = source
- 2 = gate
- 3 = drain

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to $T_{amb} = 25\text{ °C}$ (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		-65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	125 K/W
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Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm × 10 mm.

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CHARACTERISTICS $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Drain-source breakdown voltage

$I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$

$V_{(BR)DS}$ min. 200 V

Drain-source leakage current

$V_{DS} = 160\text{ V}; V_{GS} = 0$

I_{DSS} max. 10 μA

Gate-source leakage current

$V_{GS} = 20\text{ V}; V_{DS} = 0$

I_{GSS} max. 100 nA

Gate threshold voltage

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

$V_{GS(th)}$ min. 0.8 V
max. 2.8 V

Drain-source ON-resistance (see Fig.4)

$I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$

$R_{DS(on)}$ typ. 6 Ω
max. 12 Ω

Transfer admittance

$I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$

$|Y_{fs}|$ typ. 250 mS

Input capacitance at $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{iss} typ. 70 pF
max. 90 pF

Output capacitance at $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{oss} typ. 20 pF
max. 30 pF

Feedback capacitance at $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{rss} typ. 5 pF
max. 10 pF

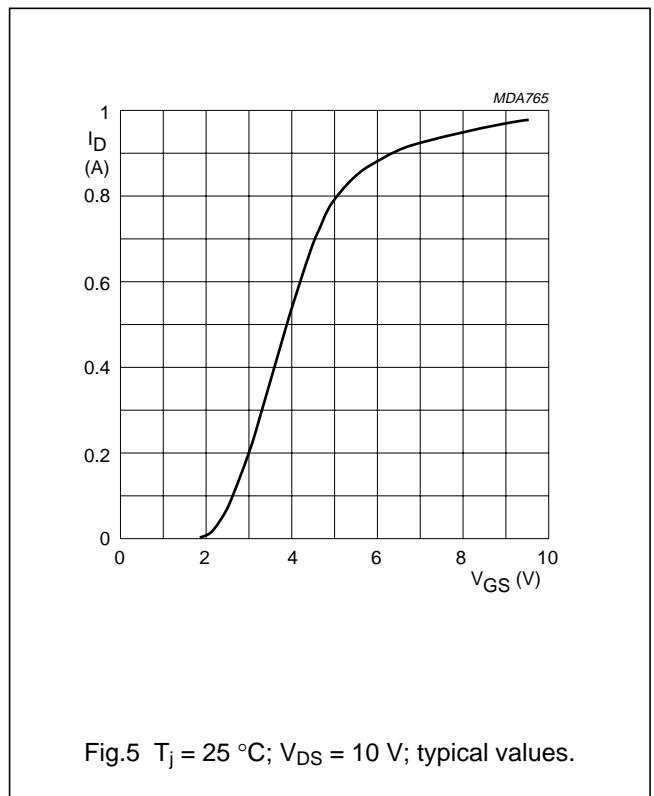
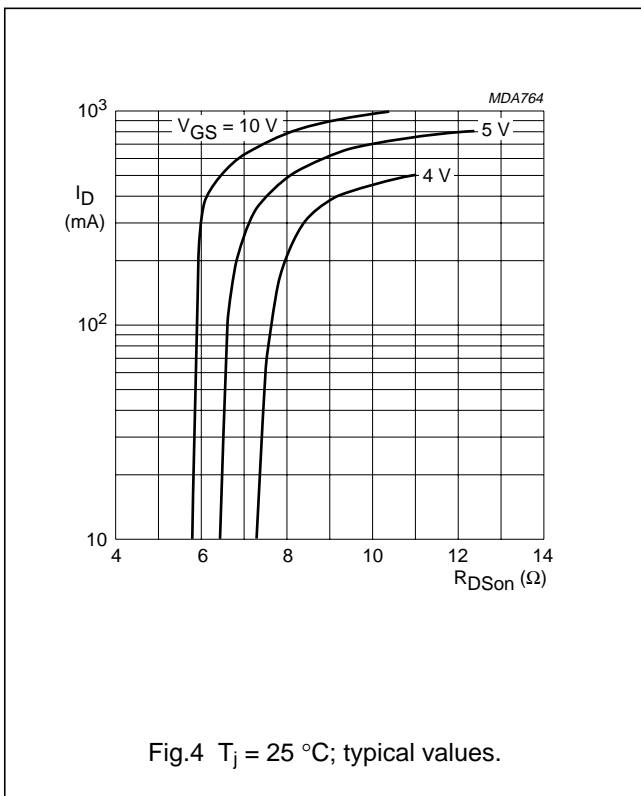
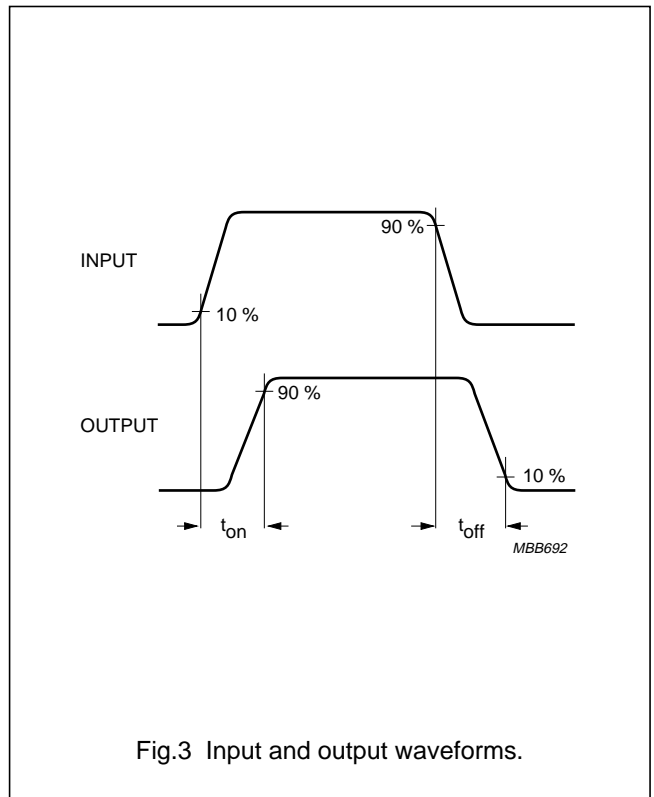
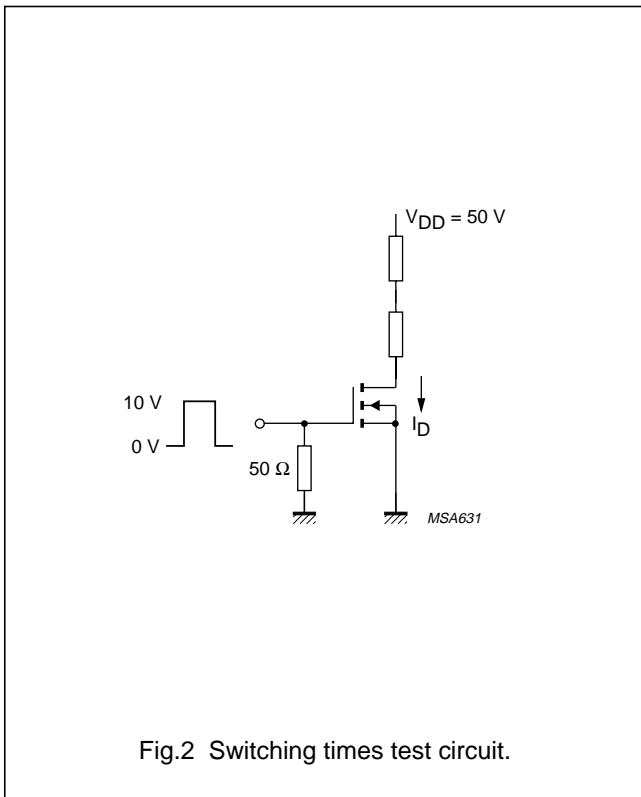
Switching times (see Figs 2 and 3)

$I_D = 250\text{ mA}; V_{DS} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$

t_{on} typ. 4 ns
max. 10 ns
 t_{off} typ. 15 ns
max. 25 ns

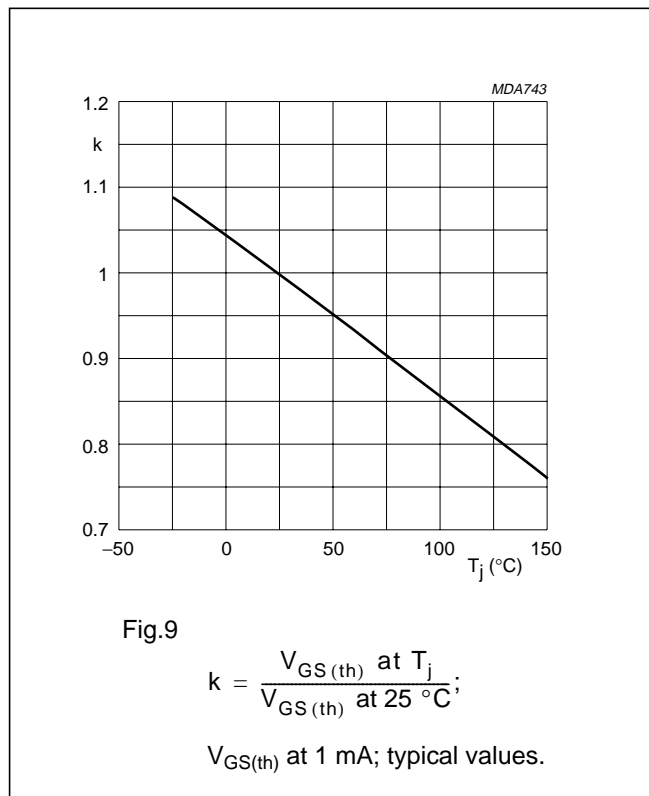
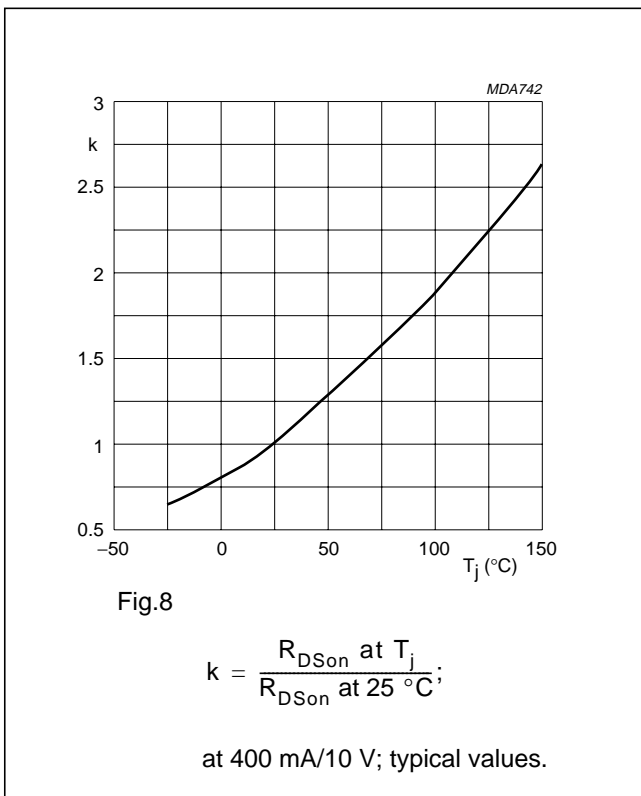
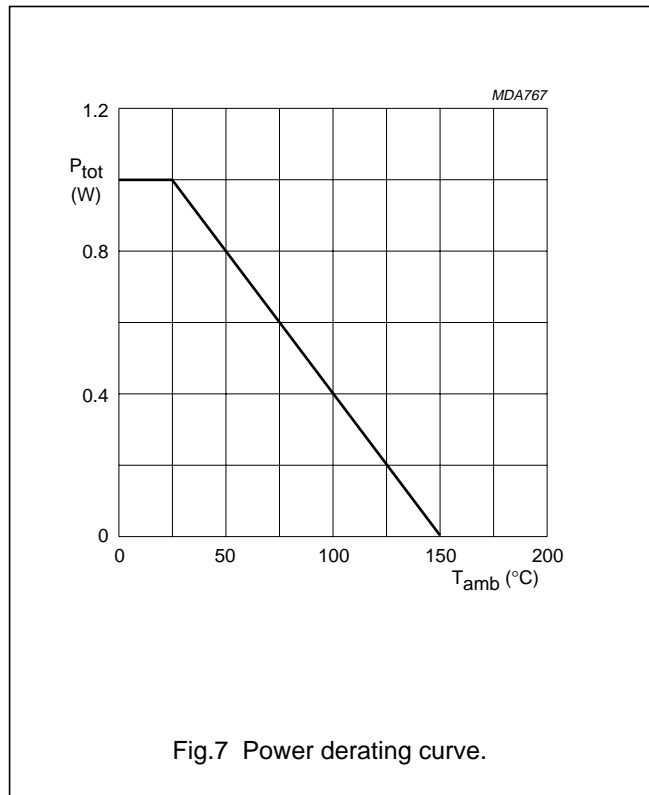
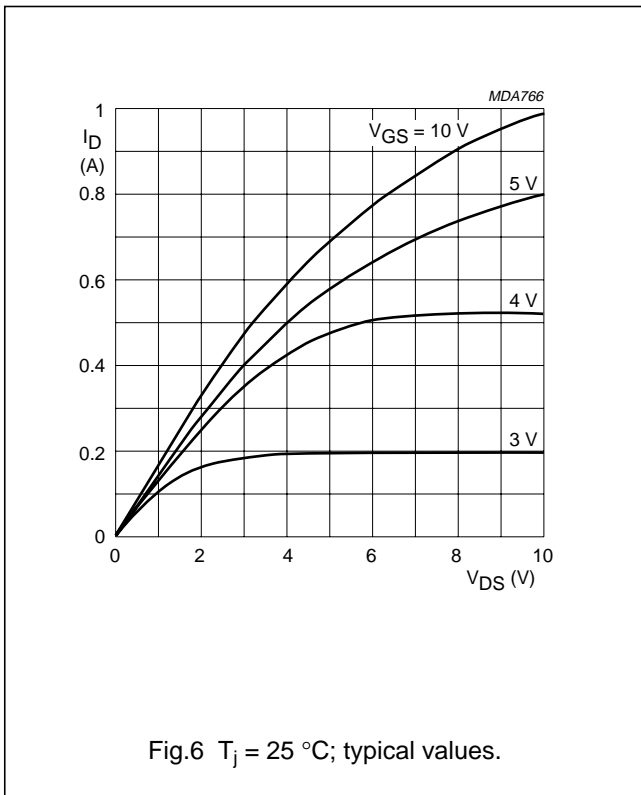
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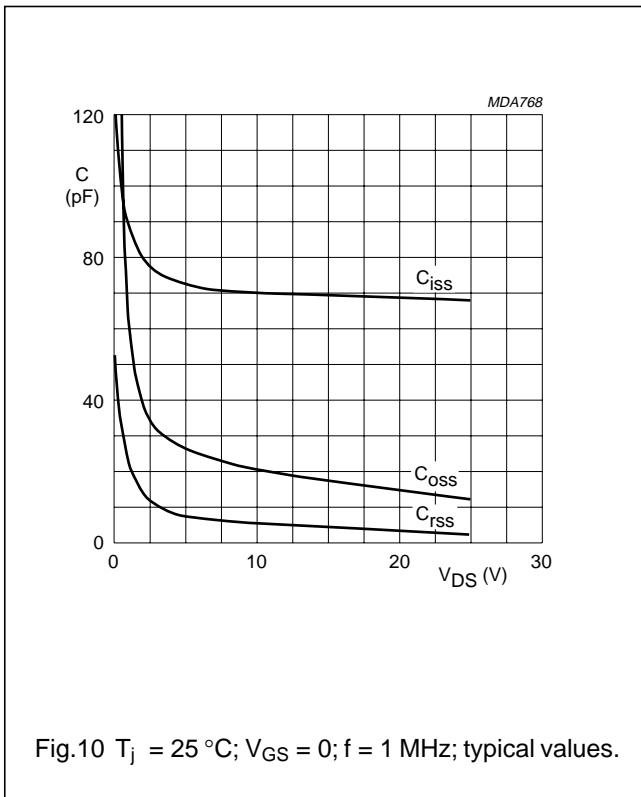
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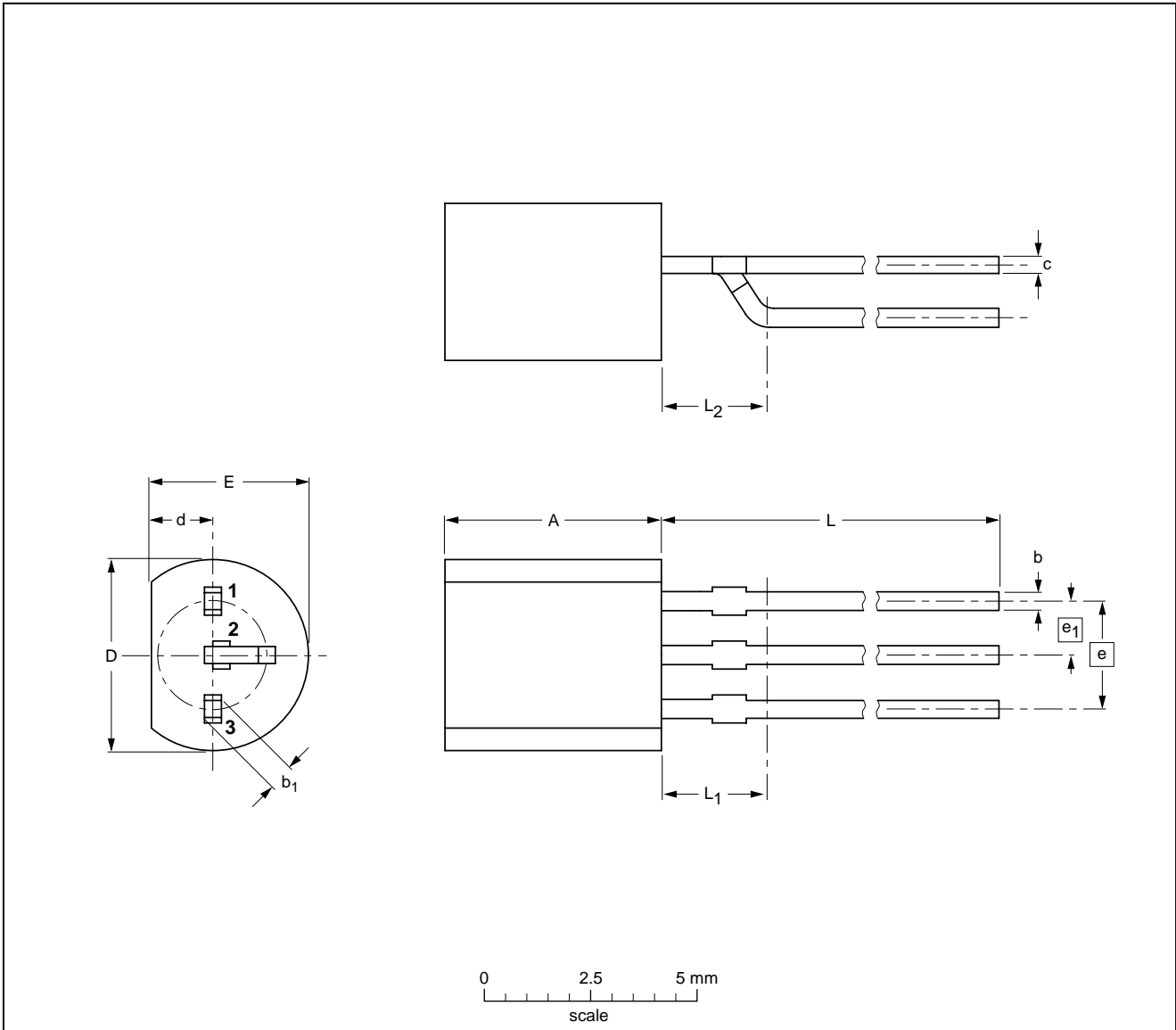
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PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max	L ₂ max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54 variant		TO-92	SC-43		97-04-14

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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