HA16113FPJ

Dual Watchdog Timers

HITACHI

The HA16113FPJ is a multifunction device that provides microprocessor systems with the necessary regulated power supply, monitors the supply voltage, and generates power-on reset and watchdog reset signals. It is ideally suited for battery-operated systems such as instrumentation systems.

Functions

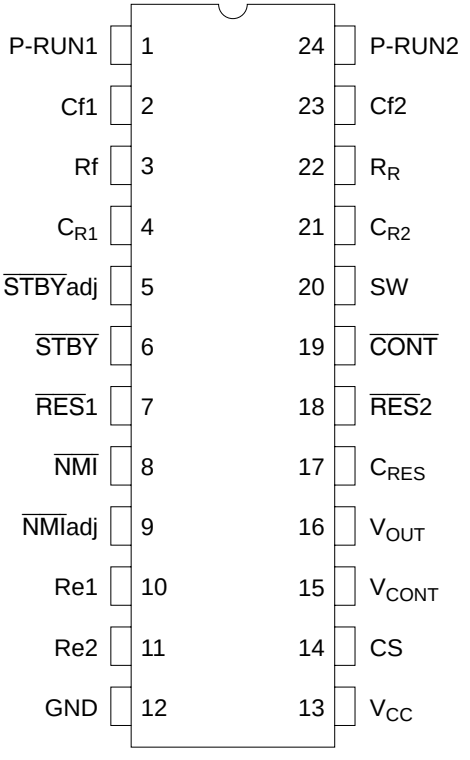
- Regulated power supply
- Power-on reset
- Two built-in auto-reset circuits
- Two built-in watchdog timer circuits (WDT)
- Output voltage monitoring (LVI)

Features

- Simultaneous or independent control of auto-reset outputs.
- Precisely regulated output voltage and accurate $\overline{\text{NMI}}$ trigger voltage (both ±2%).
- Low-voltage control with $\overline{\text{NMI}}$, simultaneous $\overline{\text{RES1}}$ and $\overline{\text{RES2}}$, and $\overline{\text{STBY}}$ outputs.
- Independently selectable durations for power-on reset and auto-reset: power-on duration is common to both reset outputs; auto-reset durations can be selected independently.
- Reset command input pin ($\overline{\text{CONT}}$) for second reset output ($\overline{\text{RES2}}$).
- WDT filter function detects minimum pulse width and maximum period of P-RUN input pulses.

Hitachi semiconductor

Pin Arrangement



(Top view)

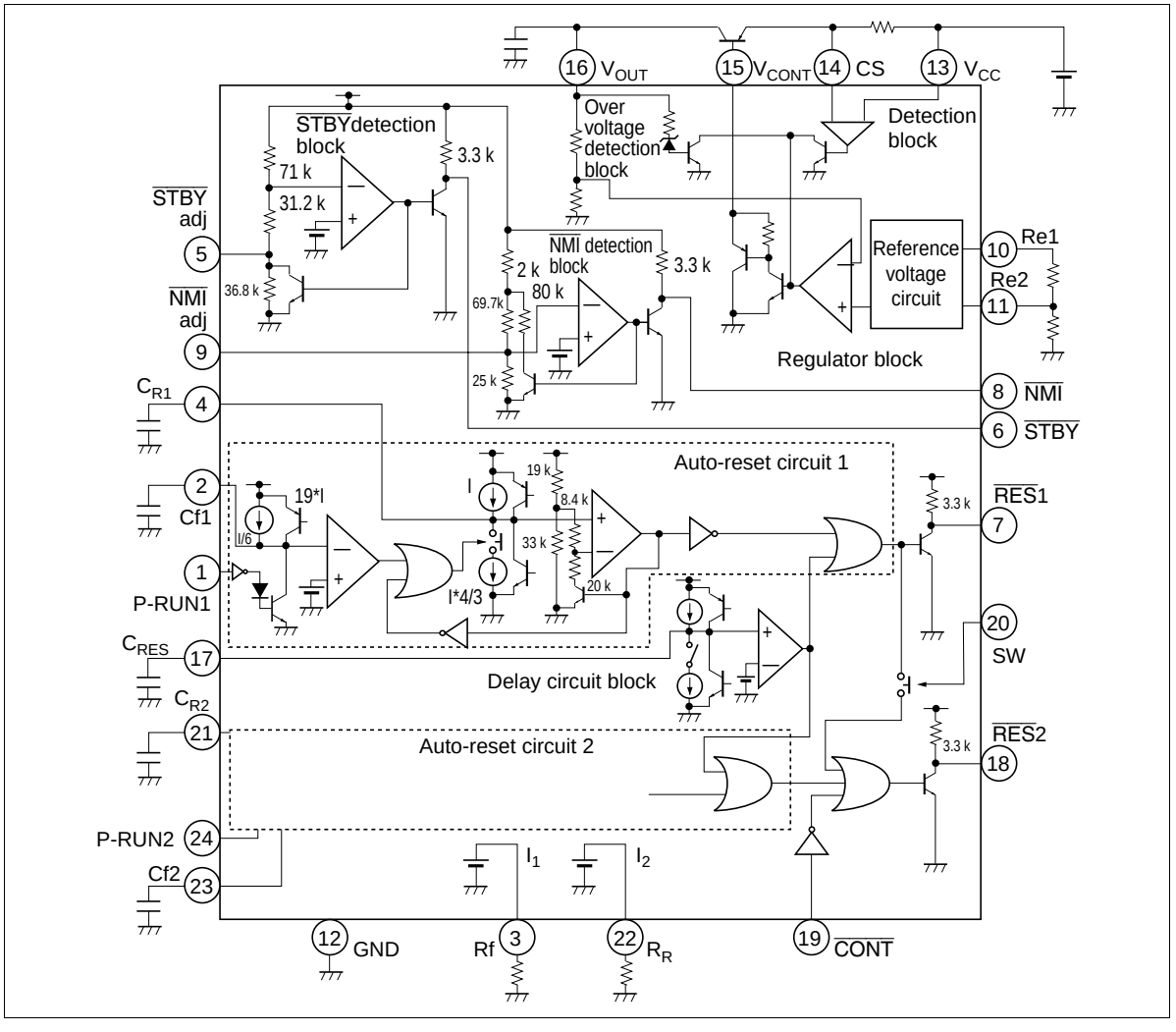
Pin Description

Pin No.	Symbol	Function
1	P-RUN1	Input from main CPU to watchdog timer 1 (WDT1)
2	Cf1	For connecting capacitor Cf1 to determine WDT1 filter characteristic (frequency band)
3	Rf	For connecting common bias resistor Rf to determine WDT1 and WDT2 filter characteristics (frequency band), power-on reset time (t_{on}, common to $\overline{RES1}$ and $\overline{RES2}$), clock-off time of auto-reset circuits 1 and 2, reset high time (t_{RH1} and t_{RH2}),reset low time (t_{RL1} and t_{RL2}), and reset pulse delay at voltage drop and recovery. Use the resistor value from 100 kΩ to 500 kΩ.
4	C_{R1}	For connecting capacitor C_{R1} to determine t_{on} for power-on reset and t_{off1}, t_{RH1}, and t_{RL1} of auto-reset circuit 1.
5	$\overline{STBY}$ adj	For adjusting standby trigger voltage (insert a resistor between this pin and ground) Recommended range: V_{H2} = 2.8 to 4.0 V
6	$\overline{STBY}$	Standby signal output
7	$\overline{RES1}$	Reset signal output to main CPU
8	$\overline{NMI}$	Low-voltage interrupt signal output for memory backup

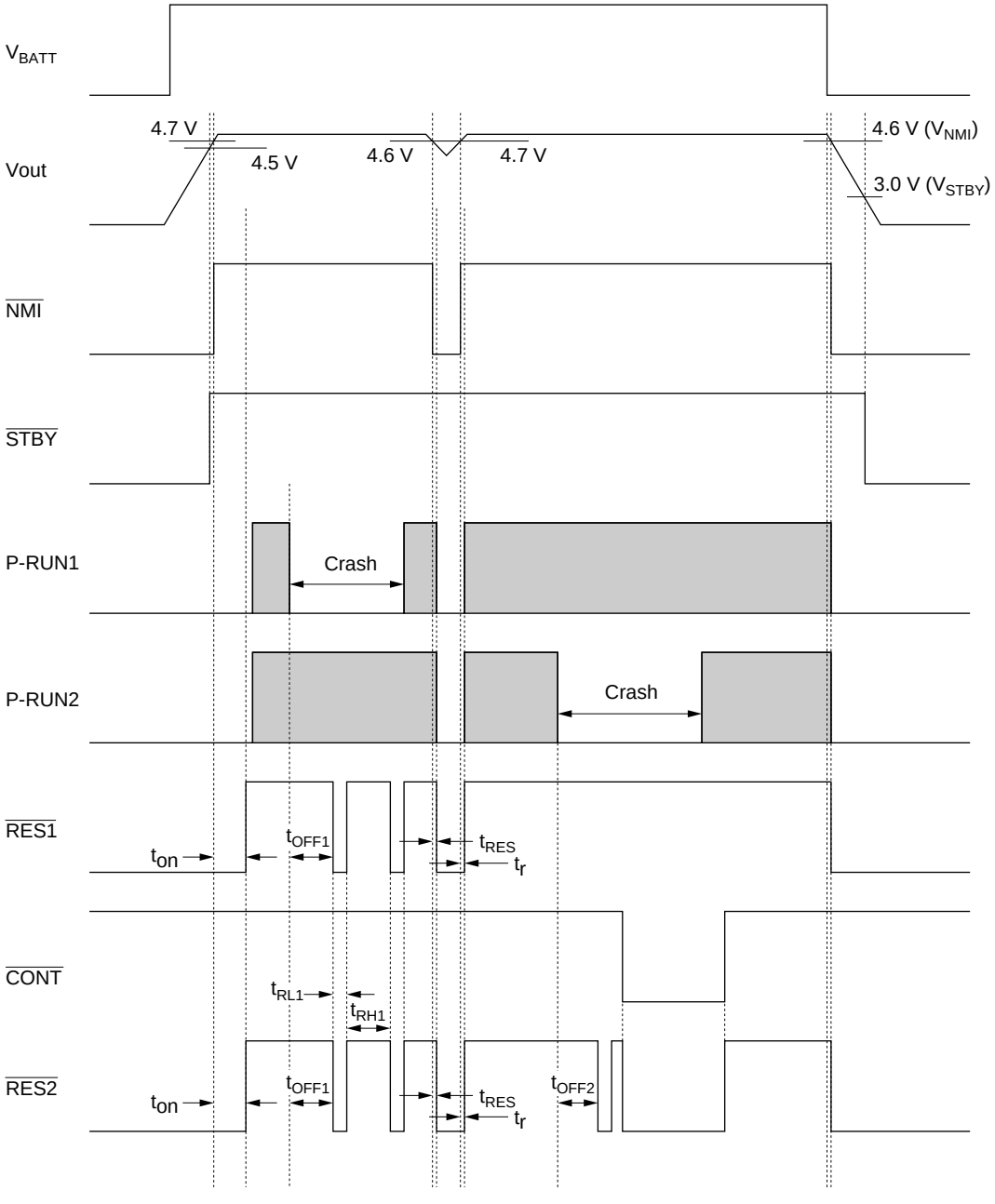
Pin Description (cont)

Pin No.	Symbol	Function
9	$\overline{\text{NMI}}$ adj	For fine adjustment of Vout trigger level for $\overline{\text{NMI}}$ signal (insert a resistor between this pin and Vout or ground) Recommended range: V_{H1} = 4.4 to 5.2 V
10	Re1	For connecting resistor Re1 to determine voltage Vout for microprocessor and IC internal circuits (insert between this pin and Re2)
11	Re2	For connecting resistor Re2 to determine voltage Vout for microprocessor and IC internal circuits (insert between this pin and ground)
12	GND	Ground
13	V_{CC}	Power supply input pin (operating range: 6 to 40 V)
14	CS	Input for detecting power supply current
15	V_C	For base control of external pnp transistor
16	Vout	Regulated voltage supplied to microprocessor and IC internal circuits Connect to collector of external pnp transistor
17	C_{RES}	Determines reset pulse delay at voltage drop and recovery. $\overline{\text{NMI}}$ output goes low as soon as Vout drops below $\overline{\text{NMI}}$ trigger level. If Vout remains below this level for time t_{RES}, both reset outputs also go low. When Vout recovers above $\overline{\text{NMI}}$ trigger level, first $\overline{\text{NMI}}$ output goes high, then after time t_r both reset outputs also go high. Times t_{RES} and t_r are adjusted by capacitor C_{RES} inserted between this pin and ground.
18	$\overline{\text{RES2}}$	Reset signal output to sub CPU
19	$\overline{\text{CONT}}$	Input pin for resetting sub CPU on command, or when sub CPU crashes Low input at $\overline{\text{CONT}}$ causes low output at $\overline{\text{RES2}}$
20	SW	Selects simultaneous control, in which main and sub CPUs are both reset when main CPU crashes, or independent control, in which sub CPU is reset independently of main CPU Open—independent control; connected to ground—simultaneous control
21	C_{R2}	For connecting capacitor C_{R2} to determine t_{off2}, t_{RH2}, and t_{RL2} of auto-reset circuit 2
22	R_R	For connecting bias resistor R_R to determine t_{off1}, t_{off2}, t_{RH1}, t_{RH2}, t_{RL1}, and t_{RL2}. Use the resistor value from 100 kΩ to 500 kΩ.
23	Cf2	For connecting capacitor Cf2 to determine WDT2 filter characteristic (frequency band)
24	P-RUN2	Input from sub CPU to watchdog timer 2 (WDT2)

Block Diagram



Timing Waveforms



Note: SW pin is connected to ground.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Value	Unit
V_{CC} power supply voltage	V_{CC}	40	V
CS voltage	V_{CS}	40	V
Control pin voltage	V_C	40	V
Control pin current	I_C	20	mA
Vout voltage	Vout	10	V
P-RUN voltage	V_{PRUN}	Vout	V
SW voltage	V_{SW}	Vout	V
$\overline{\text{CONT}}$ voltage	V_{CONT}	Vout	V
$\overline{\text{RES}}$ current	I_{RES}	5	mA
$\overline{\text{NMI}}$ current	I_{NMI}	5	mA
$\overline{\text{STBY}}$ current	I_{STBY}	5	mA
Power dissipation[Note]	P_T	600	mW
Operating temperature	Topr	–40 to +85	°C
Storage temperature	Tstg	–50 to +125	°C

Note: At ambient temperatures up to Ta = 60°C. Derated by 9.8 mW/°C above this point.

Electrical Characteristics (Ta = 25°C, Rf = 180 k , Cf1 = Cf2 = 0.01 µF, C_{R1} = C_{R2} = 0.1 µF)

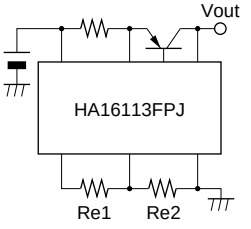
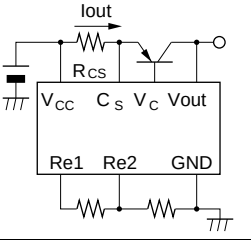
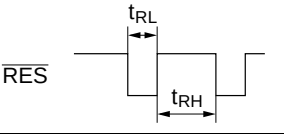
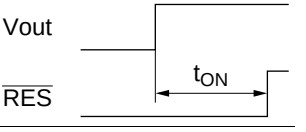
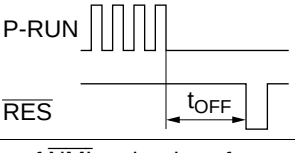
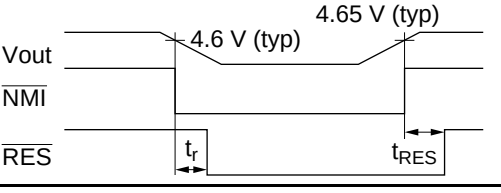
Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Chip	Power supply current		I_{CC}	—	10	15	mA	
Regulator	Output voltage		Vo1	4.875	5.00	5.125	V	V_{CC} = 6 to 17.5 V V_C current = 5 mA
			Vo2	4.80	5.00	5.20	V	V_{CC} = 6 to 17.5 V V_C current = 10 mA
	Stability with respect to line voltage		Voline	–50	—	50	mV	V_{CC} = 6 to 17.5 V V_C current = 10 mA
	Stability with respect to load current		Voload	–100	—	100	mV	V_C current = 0.1 to 15 mA
	Ripple rejection		RREJ	45	75	—	dB	Vi = 0.5 Vrms fi = 1 kHz
	Short-circuit detection voltage		Vos	0.08	0.14	0.20	V	
	Temperature coeffi-cient of output voltage		σVo/σT	—	–40	—	ppm/°C	
	Maximum adjustable output voltage		Vomax	—	—	7.0	V	
P-RUN1/2 input section	Low input voltage		$V_{IL1, 2}$	—	—	0.8	V	
	High input voltage		$V_{IH1, 2}$	2.0	—	—	V	
	High input current		$I_{IH1, 2}$	—	0.3	0.5	mA	V_{IH} = V_{OL}
Watchdog section (both $\overline{RES1}$ and $\overline{RES2}$ outputs)	Power-on time		t_{on}	25	40	60	ms	
	Clock-off time (1)		t_{off1}	80	130	190	ms	R_R: open
	Reset low time (1)		t_{RL1}	15	20	30	ms	R_R: open
	Reset high time (1)		t_{RH1}	40	60	90	ms	R_R: open
	Clock-off time (2)		t_{off2}	25	40	60	ms	R_R: = 75 kΩ
	Reset low time (2)		t_{RL2}	4	6	9	ms	R_R: = 75 kΩ
	Reset high time (2)		t_{RH2}	15	20	30	ms	R_R: = 75 kΩ
LVI section	$\overline{NMI}$ trigger voltage		V_{NMI}	4.45	4.60	4.75	V	
	Hysteresis width of above		V_{HYSN}	25	50	100	mV	
	$\overline{STBY}$ trigger voltage		V_{STBY}	2.70	3.00	3.30	V	
	Hysteresis width of above		V_{HYSS}	1.35	1.50	1.65	V	
	$\overline{RES}$ pulse delay time	Drop	t_{RES}	—	200	—	µs	C_{RES} = 1500 pF
		Recovery	t_r	—	200	—	µs	C_{RES} = 1500 pF

Electrical Characteristics (Ta = 25°C, Rf = 180 k , Cf1 = Cf2 = 0.01 µF, C_{R1} = C_{R2} = 0.1 µF) (cont)

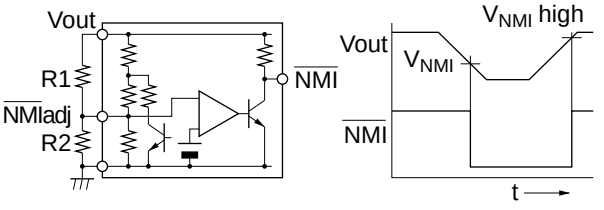
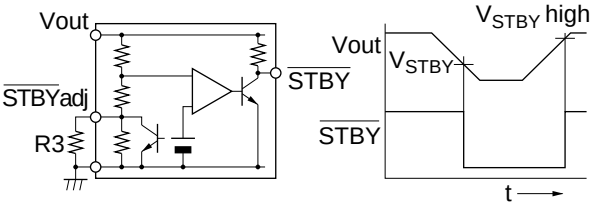
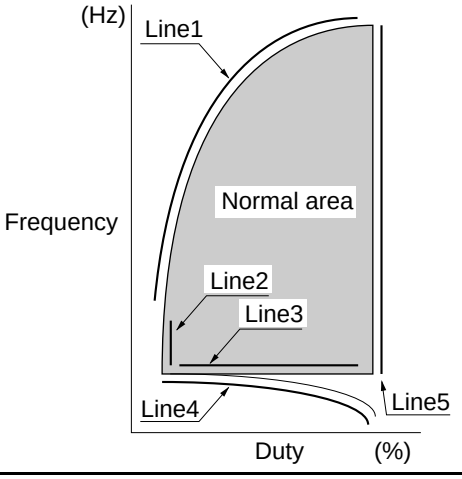
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
$\overline{\text{NMI}}$ output section	$\overline{\text{NMI}}$ low voltage	V_{OL1}	—	—	0.4	V	I_{OL1} = 2 mA
	$\overline{\text{NMI}}$ high voltage	V_{OH1}	—	V_{O1}	—	V	
	$\overline{\text{NMI}}$ function initial voltage	V_{STN}	—	0.7	1.0	V	
$\overline{\text{STBY}}$ output section	$\overline{\text{STBY}}$ low voltage	V_{OL2}	—	—	0.4	V	I_{OL2} = 2 mA
	$\overline{\text{STBY}}$ high voltage	V_{OH2}	—	V_{O1}	—	V	
	$\overline{\text{STBY}}$ function initial voltage	V_{STS}	—	0.7	1.0	V	
$\overline{\text{RES}}$1/2 output section	$\overline{\text{RES}}$1/2 low voltage	V_{OL3}	—	—	0.4	V	$I_{OL3, 4}$ = 2 mA
	$\overline{\text{RES}}$1/2 high voltage	V_{OH3}	—	V_{O1}	—	V	
	$\overline{\text{RES}}$1/2 function initial voltage	V_{STR}	—	0.7	1.0	V	
$\overline{\text{CONT}}$ and SW input section	Low input voltage	V_{IL3}	—	—	0.8	V	
	High input voltage	V_{IH3}	2.0	—	—	V	
	Low input current	I_{IL3}	–120	–60	—	µA	V_{IL3} = 0 V
	High input current	I_{IH3}	—	0.3	0.5	mA	V_{IH3} = V_{OL}
LVI section	Temperature coefficient of NMI trigger voltage	$\delta V_{H1}/\delta T$	—	100	—	ppm/°C	
	Temperature coefficient of STBY trigger voltage	$\delta V_{H2}/\delta T$	—	200	—	ppm/°C	

External Circuit Constant Calculations

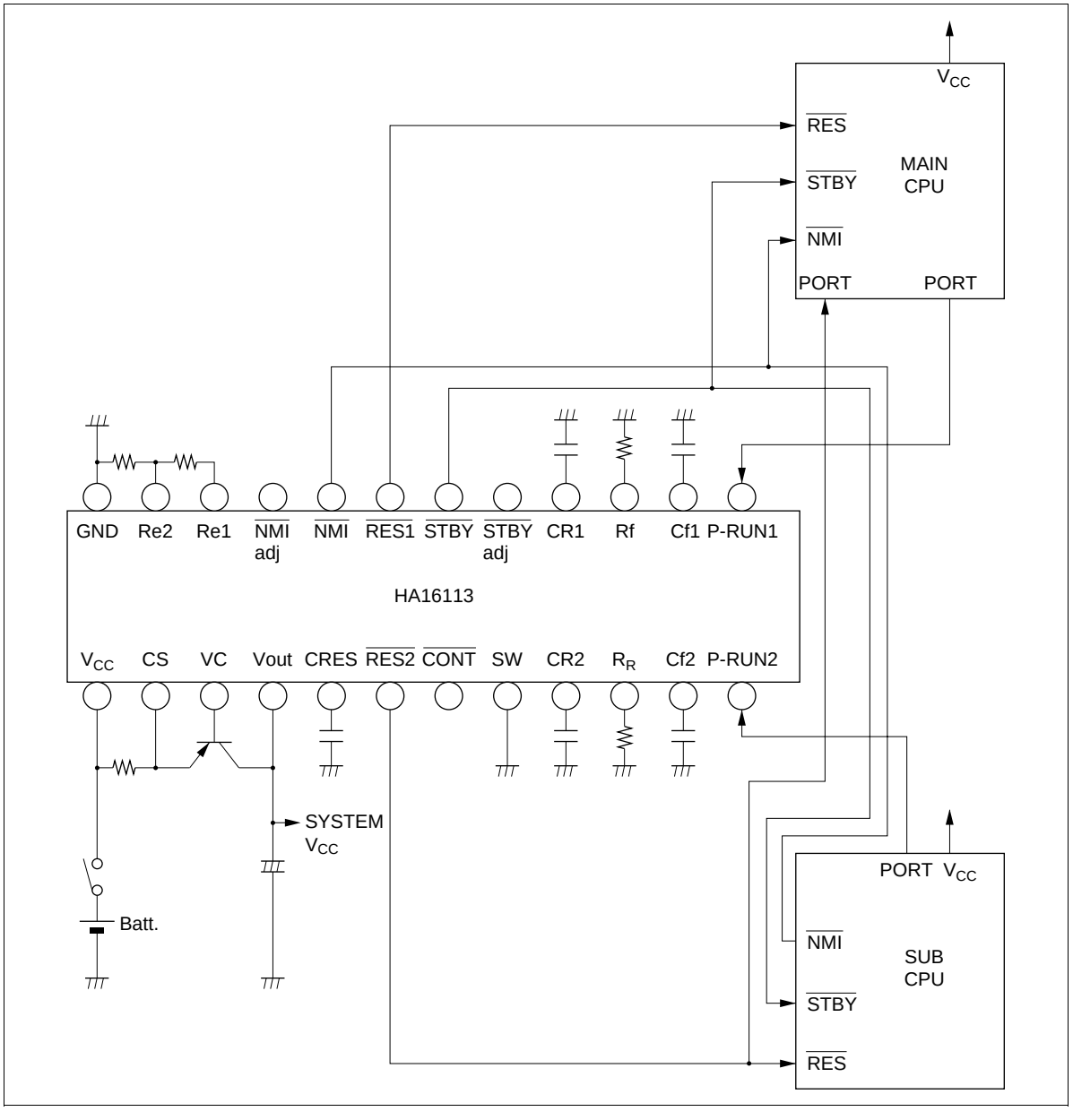
Equations for the various functions are given below. C_{R1} and Cf1 are for $\overline{RES1}$. C_{R2} and Cf2 are for $\overline{RES2}$. (Values given in equations are for reference.)

Item	Equation	Remarks
Regulated output voltage	$Vout = 0.388 \times \frac{Re2}{Re1} + 2.63$	If the desired Vout is 5 V ± 2.5%, recommended values are Re1 = 1.5 kΩ and Re2 = 9.1 kΩ 
Short-circuit detection voltage	$V_{CS} < Iout \times R_{CS}$	When this function operates, V_{CONT} stops drawing current from the base of the external transistor, so Vout output stops 
Maximum output voltage	Vout Max < 7.0 V	Prevents microprocessor damage that would result if the output voltage were raised too high by mistake. The maximum output voltage is fixed.
t_{RH}, t_{RL} (for both $\overline{RES1}$ and $\overline{RES2}$)	$t_{RH} = 3.2 \times C_R \times R'$ $t_{RL} = 1.1 \times C_R \times R'$ $\left(R' = \frac{1}{\frac{1}{Rf} + \frac{1}{R_R}} \right)$	Determines the frequency and duty cycle of the reset pulse 
t_{ON} (for both $\overline{RES1}$ and $\overline{RES2}$)	$t_{ON} = 2.2 \times C_R \times Rf$	Sets the time from the rise of Vout to the clearing of $\overline{RES}$ output 
t_{OFF} (for both $\overline{RES1}$ and $\overline{RES2}$)	$t_{OFF} = 6.1 \times C_R \times R' \left(R' = \frac{1}{\frac{1}{Rf} + \frac{1}{R_R}} \right)$	Sets the time from when P-RUN pulses stop until the reset pulse is output 
tr, t_{RES} (for both $\overline{RES1}$ and $\overline{RES2}$)	$t_r = 0.75 \times C_{RES} \times Rf$ $t_{RES} = 0.625 \times C_{RES} \times Rf$	tr sets the time from the rise of $\overline{NMI}$ to the rise of $\overline{RES}$, when Vout drops by more than the $\overline{STBY}$ trigger voltage, then recovers. t_{RES} is the time from the fall of $\overline{NMI}$ to the fall of $\overline{RES}$. 

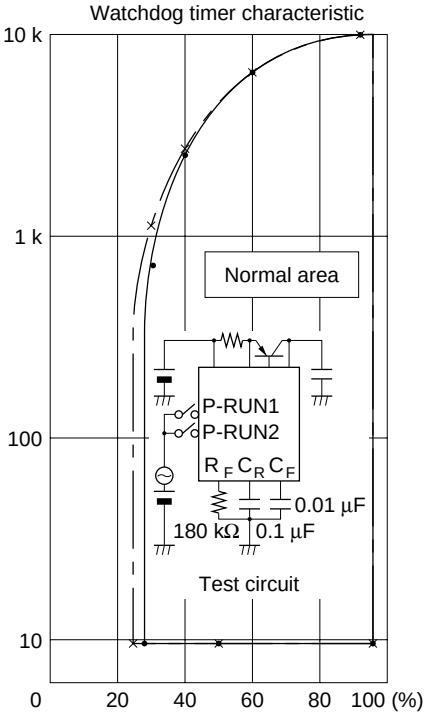
External Circuit Constant Calculations (cont)

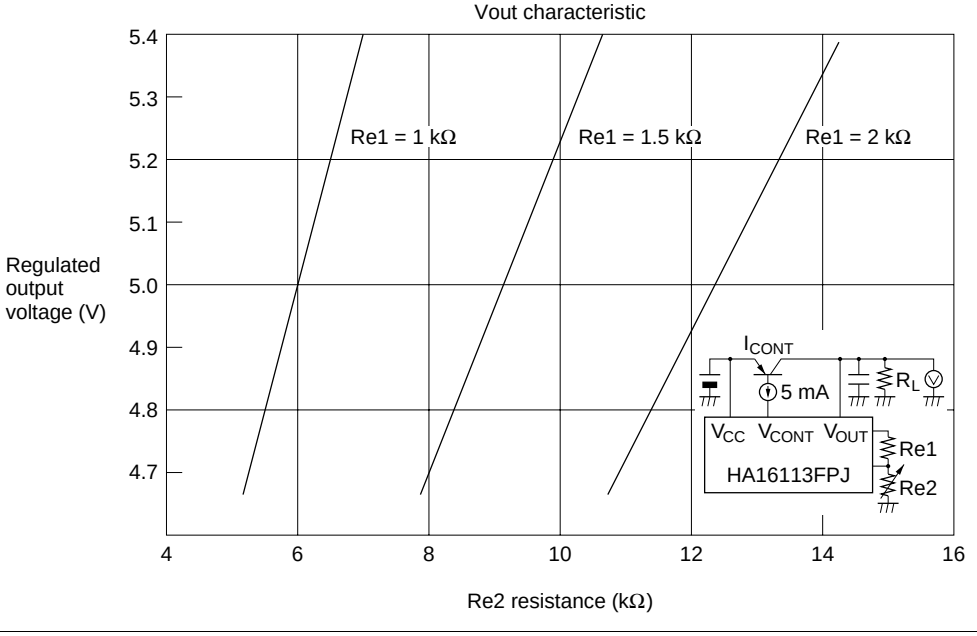
Item	Equation	Remarks
V_{NMI}	$V_{NMI} = 1.2 \times \left\{1 + \frac{(R1 \,//\, 71.7)}{(R2 \,//\, 25)}\right\}$ $\overline{NMI}$ recovery voltage (V_{NMI} high) is: V_{NMI} high = $\left(\frac{86.65}{R1} + \frac{86.65}{R2 \,//\, 25} + 1.2\right)\left(1 + \frac{73.8}{R1}\right)$ (R1 and R2 are in kΩ)	Voltage at which the $\overline{NMI}$ signal is output when Vout drops. The $\overline{NMI}$ trigger voltage and $\overline{NMI}$ recovery voltage can be trimmed by connecting resistors between the $\overline{NMI}$adj pin and Vout (R1), and between $\overline{NMI}$adj and GND (R2). 
V_{STBY}	$V_{STBY} = 1.47 \times \left\{1 + \frac{71}{31.2 + (36.8 \,//\, R3)}\right\}$ (R3 is in kΩ)	Voltage at which the $\overline{STBY}$ signal is output when Vout drops. The $\overline{STBY}$ trigger voltage can be adjusted by connecting a resistor (R3) between the $\overline{STBY}$adj pin and GND. The $\overline{STBY}$ recovery voltage cannot be adjusted. 
WDT.	Line1 = $\frac{0.31 \times (Du - 24)}{Cf \times Rf}$ Line2 = Du (= 25%)* Line3 = $\frac{0.015}{Cf \times Rf}$ Line4 = $\frac{1 - Du}{2.1 \times t_{RH}}$ Line5 = 99%* Du is the duty cycle of the P-RUN pulse. Du = $\frac{t_{RH}}{t_{RL} + t_{RH}}$ Note: Line2 and Line5 are fixed.	The watchdog timer function determines whether the P-RUN pulse is normal or not. A reset pulse is output if P-RUN is determined to be abnormal. The normal region is the part bounded by Line1 to Line3 (or Line4) in the diagram. Line4 applies in certain cases, depending on C_R, Cf, and the state of P-RUN. 

Operating Interconnections (example)

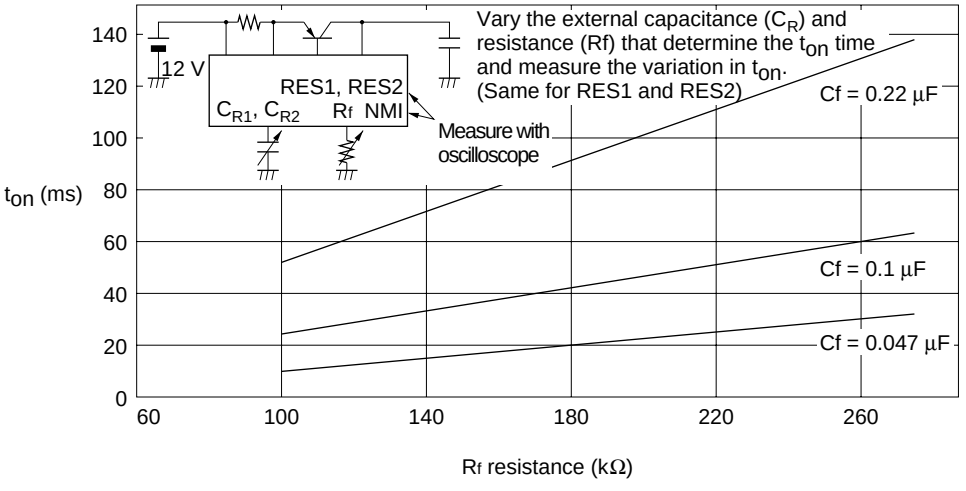


Characteristic Curves

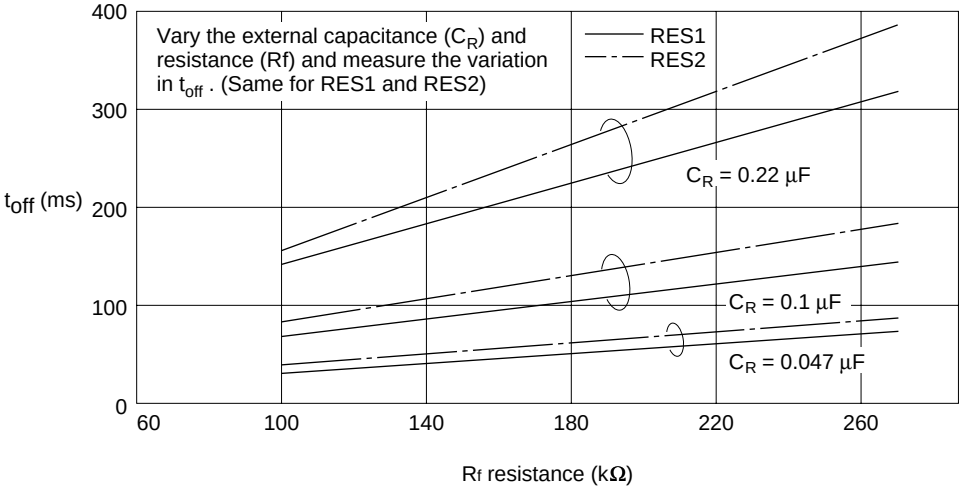




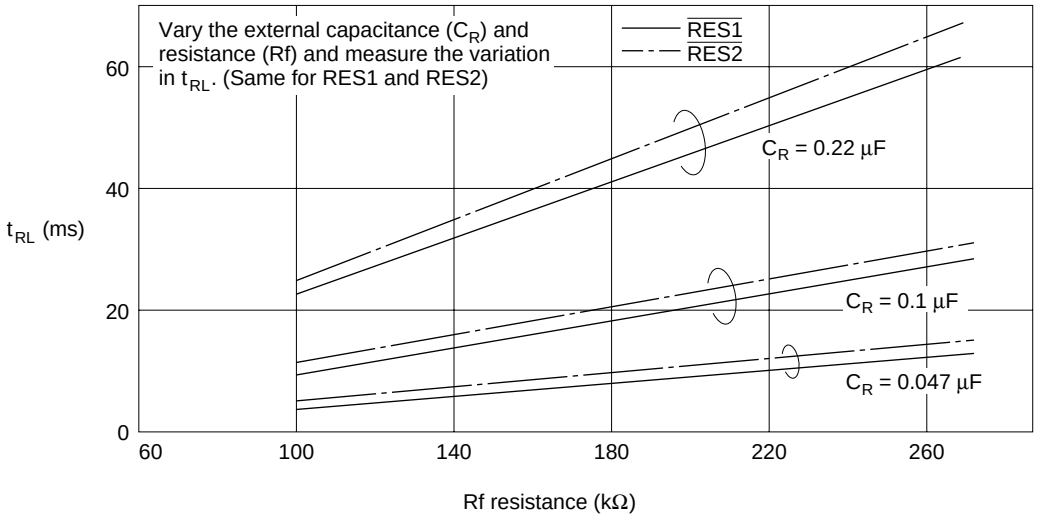
t_{on} characteristic



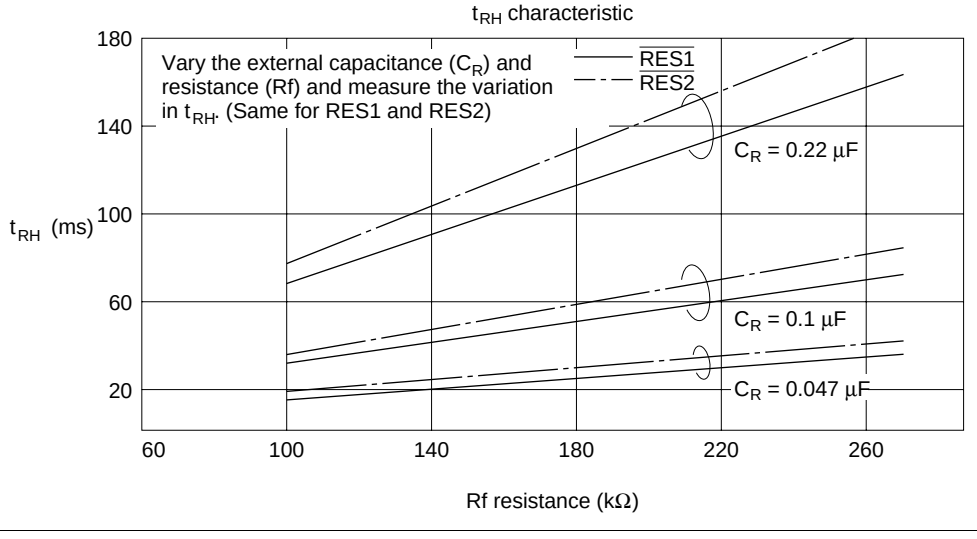
t_{off} characteristic



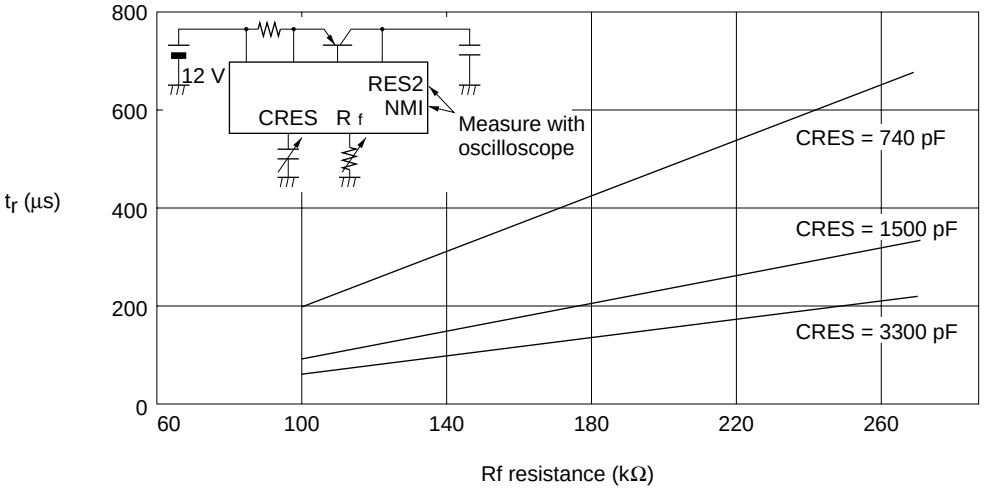
t_{RL} characteristic



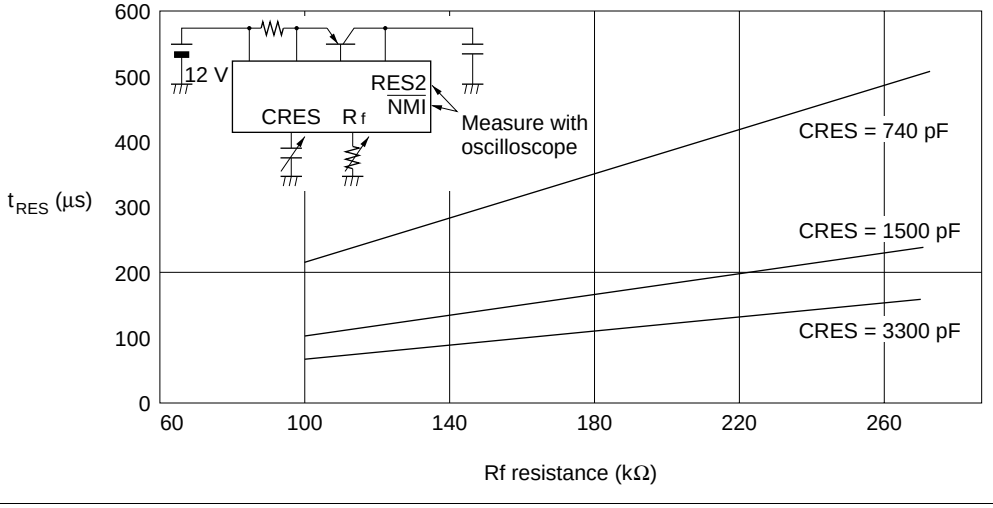
t_{RH} characteristic



t_r characteristic (for both $\overline{RES1}$ and $\overline{RES2}$)



t_{RES} characteristic (for both $\overline{RES1}$ and $\overline{RES2}$)



Precautions

If the IC's ground potential varies suddenly by several volts due to wiring impedance (see figure 7), a false $\overline{RES}$ pulse may be output. The reason for this is that potentials in the $\overline{RES}$ pulse generating circuit change together with the Vout-GND potential. The reference potential of the comparator in figure 8 and the potential of the external capacitor have different impedances as seen from the comparator, causing a momentary inversion. The solution is to stabilize the ground potential. Two ways of stabilizing the IC's ground line are:

- Separate the IC's ground line from high-current ground lines.
- Increase the capacitance (Co) used to smooth the Vout output.

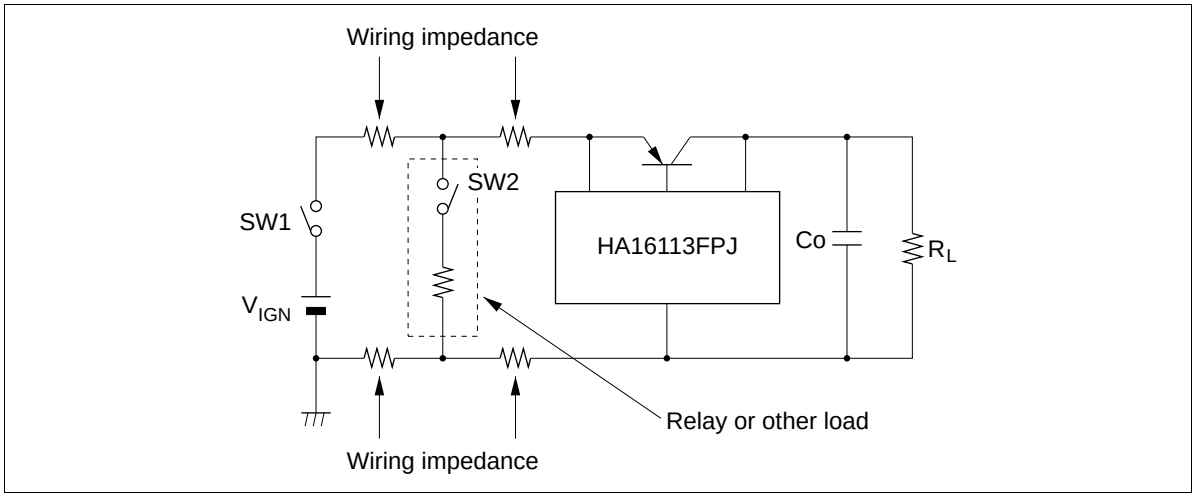


Figure 1 Typical Circuit

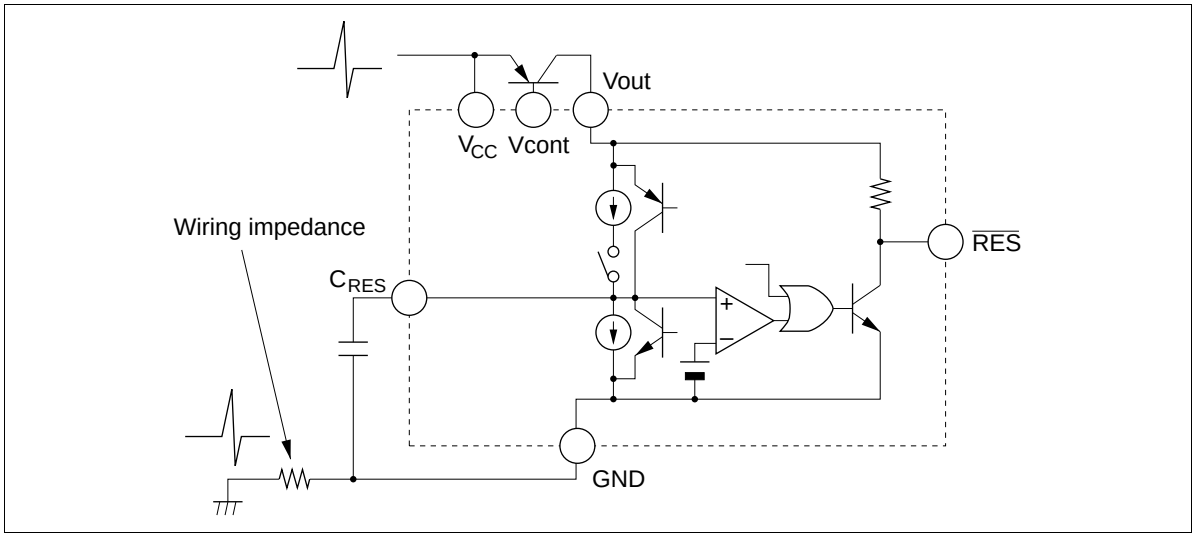
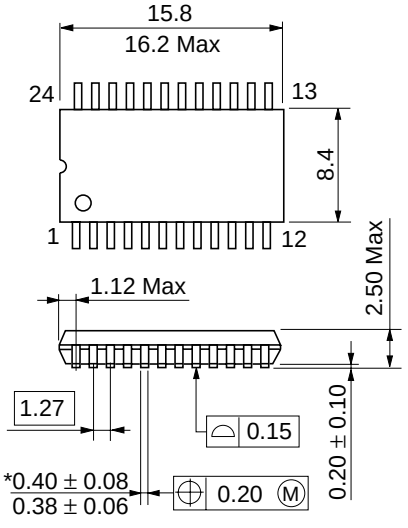
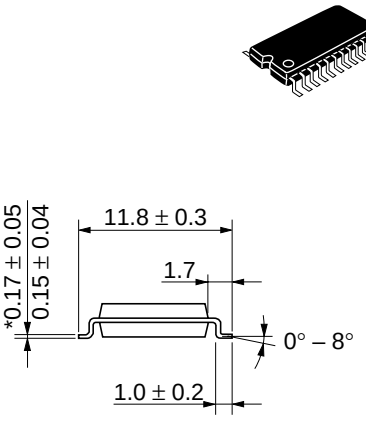


Figure 2 $\overline{RES}$ Comparator

Package Dimensions

Unit: mm





*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-24D
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.6 g

Cautions

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