Ordering number : ENN*6728

CMOS IC

LC651154N, 651154F, 651154L, LC651152N, 651152F, 651152L

Four-Bit CMOS Microcontrollers for Small-Scale Control Applications

Preliminary

Overview

The LC651154N/F/L and the LC651152N/F/L are the small-scale control application versions of Sanyo's LC6500 series of 4-bit single-chip CMOS microcontrollers, and feature the same basic architecture and instruction set. These microcontrollers include an 8-input 8-bit A/D converter and are appropriate for use in a wide range of applications, from applications with a small number of circuits and controls that were previously implemented in standard logic to applications with a larger scale such as home appliances, automotive equipment, communications equipment, office equipment, and audio equipment such as decks and players. Also note that since these ICs provide the same basic functions (certain functions and specifications do differ) as, and are pin compatible with the earlier LC651104N/F/L and LC651102N/F/L, they can replace those ICs in most cases.

Features

- Fabricated in a CMOS process for low power (A standby function that can be invoked under program control is also provided.)
- ROM/RAM
  LC651154N/F/L — ROM: 4K × 8 bits, RAM: 256 × 4 bits
  LC651152N/F/L — ROM: 2K × 8 bits, RAM: 256 × 4 bits
- Instruction set: The 80-instruction set common to the LC6500 family
- Wide operating supply voltage range: 2.2 to 6.0 V (L versions)
- Instruction cycle time: 0.92 µs (F versions)
- On-chip serial I/O function
- Flexible I/O ports
  — Number of ports: 6 ports with a total of 22 pins
  — All ports:
    · Are I/O ports
    · I/O voltage handling capacity: 15 V (maximum) (Open-drain specification C, D, E, and F ports only)
    · Output current: 20 mA (maximum) sink current (Are capable of directly driving an LED.)
  — Support options to match application system specifications
    A. Open-drain output, internal pull-up resistor specification: All ports, in bit units
    B. Output level at reset specification: Ports C and D can be specified to go to the high or low level in 4-bit units.
- Interrupt function
  — Timer interrupts through an interrupt vector (Can be tested under program control)
  — $\overline{\text{INT}}$ pin and serial I/O full/empty interrupts through an interrupt vector (Can be tested under program control)
- Stack levels: 8 (Shared with the interrupt system.)
- Timers: 4-bit variable prescaler and 8-bit programmable timers
- Clock oscillator options that match a wide range of system specifications
  — Oscillator circuit options:
    Two-pin RC oscillator (N and L versions)
    Two-pin ceramic oscillator (N, F, and L versions)
  — Clock divider circuit options:
    No divider, built-in divide-by-3, built-in divide-by-4 (N and L versions)
- Continuous square wave output (with a period 64 times the cycle time)
- A/D converter (successive approximation)
  — 8-bit precision with 8 input channels
- Watchdog timer

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— RC circuit time constant
— Optional watchdog timer reset function from an external pin

Function Table

Parameter		LC651154N/1152N	LC651154F/1152F	LC651154L/1152L
Memory	ROM	4096 × 8 bits (1154N) 2048 × 8 bits (1152N)	4096 × 8 bits (1154F) 2048 × 8 bits (1152F)	4096 × 8 bits (1154L) 2048 × 8 bits (1152L)
	RAM	256 × 4 bits (1154/1152N)	256 × 4 bits (1154/1152F)	256 × 4 bits (1154/1152L)
Instructions	Instruction set	80	80	80
	Table reference	Supported	Supported	Supported
On-chip functions	Interrupts	1 external, 1 internal	1 external, 1 internal	1 external, 1 internal
	Timers	4-bit variable prescaler + 8-bit timers	4-bit variable prescaler + 8-bit timers	4-bit variable prescaler + 8-bit timers
	Stack levels	8	8	8
	Standby function	Standby mode entered by the HALT instruction supported	Standby mode entered by the HALT instruction supported	Standby mode entered by the HALT instruction supported
I/O ports	Number of ports	22 I/O port pins	22 I/O port pins	22 I/O port pins
	Serial port	Input and output in 4 or 8 bit units	Input and output in 4 or 8 bit units	Input and output in 4 or 8 bit units
	I/O voltage handling capability	15 V max.	15 V max.	15 V max.
	Output current	10 mA typ. 20 mA max.	10 mA typ. 20 mA max.	10 mA typ. 20 mA max.
	I/O circuit types	Open drain (n-channel) and pull-up resistor output options can be specified in 1-bit units		
	Output level at reset	A high or low level output can be selected in port units (ports C and D only)		
	Square wave output	Supported	Supported	Supported
Characteristics	Minimum cycle time	2.77 µs (V_{DD} ≥ 3 V)	0.92 µs (V_{DD} ≥ 2.5 V)	3.84 µs (V_{DD} ≥ 2.2 V)
	Supply voltage	3 to 6 V	2.5 to 6 V	2.2 to 6 V
	Current drain	1.5 mA typ.	2 mA typ.	1.5 mA typ.
Oscillator	Oscillator element	RC (800/400 kHz typ.) Ceramic (400 k, 800 k, 1 MHz, 4 MHz)	Ceramic 4 MHz	RC (400 kHz typ.) Ceramic (400 k, 800 k, 1 MHz, 4 MHz)
	Divider circuit option	1/1, 1/3, 1/4	1/1	1/1, 1/3, 1/4
Other items	Package	DIP30S-D, MFP30S, SSOP30	DIP30S-D, MFP30S, SSOP30	DIP30S-D, MFP30S, SSOP30

Note: Recommendations for oscillator elements and oscillator circuit constants will be announced as the recommended circuits for these ICs are determined. Verify the progress of these developments periodically.

Differences between the LC651154N/1152N and the LC651104N/1102N.

The table below lists the points that require care when converting an existing product that uses the LC651104N/1102N to use the LC651154N/1152N.

Parameter		LC651154N/1152N	LC651104N/1102N
Allowable power dissipation	Pdmax (1) : DIP	310 mW	250 mW
	Pdmax (2) : MFP	220 mW	150 mW
	Pdmax (3) : SSOP	160 mW	(No corresponding package)
Oscillator characteristics Ceramic oscillator Oscillator frequency	f_{CFOSC} [OSC1, OSC2]	Oscillator frequency precision: within ±2% Changes in the recommended oscillator constants (See table 1.)	Oscillator frequency precision: within ±4%
2-pin RC oscillator Oscillator frequency	f_{MOSC} [OSC1, OSC2]	800 kHz typ. (V_{DD} = 3 to 6 V) Constants changed: Rext = 5.6 kΩ ±1 % Frequency variability (sample to sample): 587 to 1298 kHz	900 kHz typ. (V_{DD} = 4 to 6 V) Constants changed: Rext = 4.7 kΩ ±1 % Frequency variability (sample to sample): 634 to 1278 kHz
		400 kHz typ. (V_{DD} = 3 to 6 V) Frequency variability (sample to sample): 290 to 616 kHz	400 kHz typ. (V_{DD} = 3 to 6 V) Frequency variability (sample to sample): 276 to 742 kHz
Pull-up resistors	Ru [$\overline{RES}$]	200 to 800 kΩ (500 kΩ typ.)	300 to 700 kΩ (500 kΩ typ.)
Serial clock input clock cycle time	t_{CKCY} (1) [$\overline{SCK}$]	min. 2.0 µs	min. 3.0 µs
A/D converter characteristics	Operating voltage	V_{DD} = 3 to 6 V	V_{DD} = 4 to 6 V
AV+ = V_{DD} AV– = V_{SS}	Reference input current IRIF [AV+, AV–]	200 to 800 µA (500 µA typ.)	75 to 300 µA (150 µA typ.)
Watchdog timer Cw = 0.047 ±5% µF Rw = 680 ±1% kΩ RI = 100 ±1% Ω		V_{DD} = 3 to 6 V	V_{DD} = 4 to 6 V
Package		DIP30S-D, MFP30S An SSOP30 version was added.	DIP30S-D, MFP30S

Differences between the LC651154F/1152F and the LC651104F/1102F.

The table below lists the points that require care when converting an existing product that uses the LC651104F/1102F to use the LC651154F/1152F.

Parameter		LC651154F/1152F	LC651104F/1102F
Allowable power dissipation	Pdmax (1) : DIP	310 mW	250 mW
	Pdmax (2) : MFP	220 mW	150 mW
	Pdmax (3) : SSOP	160 mW	(No corresponding package)
Operating supply voltage	V_{DD}	2.5 to 6 V	4 to 6 V
Low-level input voltage	V_{IL}(n)	Specifications for V_{DD} = 4 to 6 V The specifications for V_{DD} = 2.5 to 6 V were added.	Specifications for V_{DD} = 4 to 6 V
Oscillator characteristics Ceramic oscillator Oscillator frequency	f_{CFOSC} [OSC1, OSC2]	Oscillator frequency precision: within ±2 %	Oscillator frequency precision: within ±4 %
Pull-up resistors	Ru [$\overline{RES}$]	200 to 800 kΩ (500 kΩ typ.)	300 to 700 kΩ (500 kΩ typ.)
A/D converter characteristics AV+ = V_{DD} AV– = V_{SS}	Operating voltage	AD speed 1/1 : V_{DD} = 3.5 to 6 V AD speed 1/2 : V_{DD} = 3 to 6 V	AD speed 1/1 : V_{DD} = 4.5 to 6 V AD speed 1/2 : V_{DD} = 4 to 6 V
	Reference input current IRIF [AV+, AV–]	200 to 800 µA (500 µA typ.)	75 to 300 µA (150 µA typ.)
Package		DIP30S-D, MFP30S An SSOP30 version was added.	DIP30S-D, MFP30S

Differences between the LC651154L/1152L and the LC651104L/1102L.

The table below lists the points that require care when converting an existing product that uses the LC651104L/1102L to use the LC651154L/1152L.

Parameter		LC651154L/1152L	LC651104L/1102L
Allowable power dissipation	Pdmax (1) : DIP	310 mW	250 mW
	Pdmax (2) : MFP	220 mW	150 mW
	Pdmax (3) : SSOP	160 mW	(No corresponding package)
Operating supply voltage	V_{DD}	2.2 to 6 V	2.5 to 6 V
Oscillator characteristics Ceramic oscillator Oscillator frequency	f_{CFOSC} [OSC1, OSC2]	Oscillator frequency precision: within ±2% Changes in the recommended oscillator constants (See table 1.)	Oscillator frequency precision: within ±4%
2-pin RC oscillator Oscillator frequency	f_{MOSC} [OSC1, OSC2]	400 kHz typ. (V_{DD} = 2.2 to 6 V) Frequency variability (sample to sample): 290 to 841 kHz	400 kHz typ. (V_{DD} = 2.5 to 6 V) Frequency variability (sample to sample): 276 to 742 kHz
Pull-up resistors	Ru [$\overline{RES}$]	200 to 800 kΩ (500 kΩ typ.)	300 to 700 kΩ (500 kΩ typ.)
Serial clock input clock cycle time	t_{CKCY} (1) [$\overline{SCK}$]	min. 2.0 µs	min. 6.0 µs
A/D converter characteristics	Operating voltage	V_{DD} = 3 to 6 V	V_{DD} = 4 to 6 V
AV+ = V_{DD} AV– = V_{SS}	Reference input current IRIF [AV+, AV–]	200 to 800 µA (500 µA typ.)	75 to 300 µA (150 µA typ.)
Watchdog timer		V_{DD} = 2.2 to 6.0 V	V_{DD} = 2.5 to 6.0 V
Package		DIP30S-D, MFP30S An SSOP30 version was added.	DIP30S-D, MFP30S

Caution: Perform a full system evaluation and inspection after replacing the microcontroller.

Pin Assignment

The pin assignment is the same for the DIP, MFP, and SSOP packages.

Pin Functions

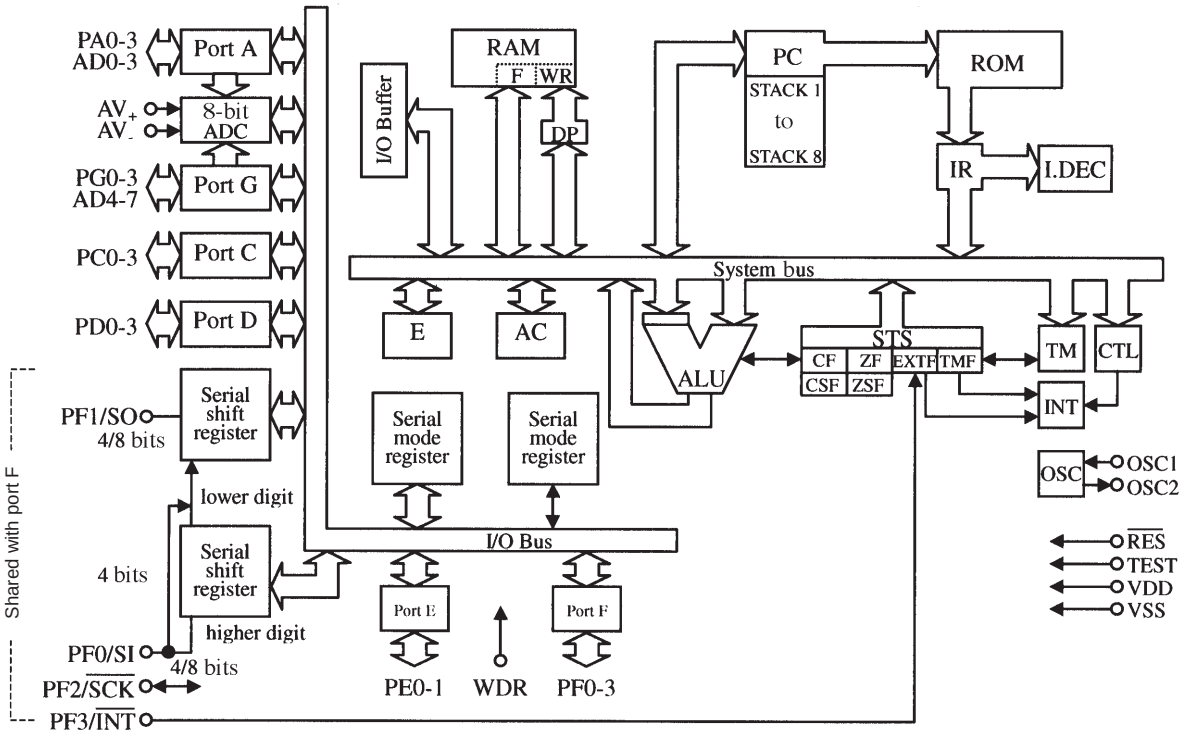
OSC1, OSC2:	Connections for the oscillator capacitor and resistor or ceramic element
$\overline{\text{RES}}$:	Reset
PA0 to PA3:	Common I/O ports A0 to A3
PC0 to PC3:	Common I/O ports C0 to C3
PD0 to PD3:	Common I/O ports D0 to D3
PE0 to PE3:	Common I/O ports E0 to E3
PF0 to PF3:	Common I/O ports F0 to F3
PG0 to PG3:	Common I/O ports G0 to G3

TEST:	IC testing.
$\overline{\text{INT}}$:	Interrupt request input
SI:	Serial input
SO:	Serial output
$\overline{\text{SCK}}$:	Serial clock input output
AD0 to AD7:	A/D converter analog inputs
AV_+, AV_-:	A/D converter reference voltage inputs
WDR:	Watchdog timer reset input

Note: Pins SI, SO, $\overline{\text{SCK}}$, and $\overline{\text{INT}}$ are shared function pins also used as PF0:3.

System Block Diagram

LC651154N/F/L, LC651152N/F/L



RAM:	Data memory
F:	Flag
WR:	Working register
AC:	Accumulator
ALU:	Arithmetic and logic unit
DP:	Data pointer
E:	E register
CTL:	Control register
OSC:	Oscillator circuit
TM:	Timer
STS:	Status register

ROM:	Program memory
PC:	Program counter
INT:	Interrupt control
IR:	Instruction register
I.DEC:	Instruction decoder
CF, CSF:	Carry flag and carry save flag
ZF, ZSF:	Zero flag and zero save flag
EXTF:	External interrupt request flag
TMF:	Internal interrupt request flag

Development Support

The following are provided for development with the LC651154 and LC651152.

- User's manual
  See the "LC651104/1102 User's Manual."
- Development tools manual
  See the "Four-Bit Microcontroller EVA86000 Development Tools Manual."
- Software manual
  "LC65/66 Series Software Manual"
- Development tools
  — Program development (EVA86000 System)
  — On-chip EPROM microcontroller <LC65E1104> for program evaluation

Pin Functions

Symbol	Number of pins	I/O	Function	Option	At reset	Handling when unused
V_{DD} V_{SS}	1	— —	Power supply	—	—	—
OSC1	1	Input	• Connection for the RC circuit or ceramic oscillator element used for the system clock oscillator • Leave OSC2 open when an external clock input is used.	(1) Two-pin RC oscillator or external clock (2) Two-pin ceramic oscillator (3) Divider option 1. No divider 2. Divide-by-3 3. Divide-by-4	—	—
OSC2	1	Output				
PA0 to PA3/ AD0 to AD3	4	I/O	• I/O port A0 to A3 Input in 4-bit units (IP instruction) Output in 4-bit units (OP instruction) Testing in 1-bit units (BP and BNP instructions) Set and reset in 1-bit units (SPB and RPB instructions) • PA3 is used for standby mode control • Application must assure that chattering does not occur on the PA3 input during HALT instruction execution. • All four pins have shared functions PA0/AD0 - A/D converter input AD0 PA1/AD1 - A/D converter input AD1 PA2/AD2 - A/D converter input AD2 PA3/AD3 - A/D converter input AD3	(1) Open-drain output (2) Pull-up resistor Options (1) and (2) can be specified in bit units	High-level output (The output n-channel transistors in the off state.)	Select the open-drain output option and connect to V_{SS}.
PC0 to PC3	4	I/O	• I/O port C0 to C3 The port functions are identical to those of PA0 to PA3. (See note.) • The output during a reset can be selected to be either high or low as an option. Note: This port has no standby mode control function.	(1) Open-drain output (2) Pull-up resistor (3) High-level output during reset (4) Low-level output during reset • Options (1) and (2) can be specified in bit units • Options (3) and (4) are specified 4 bits at a time	• High-level output • Low-level output (Depending on option selected.)	The same as for PA0 to PA3
PD0 to PD3	4	I/O	• I/O port D0 to D3 The port functions and options are identical to those of PC0 to PC3.	The same as PC0 to PC3	The same as PC0 to PC3	The same as for PA0 to PA3

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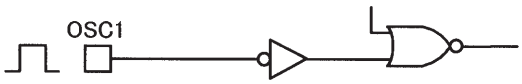
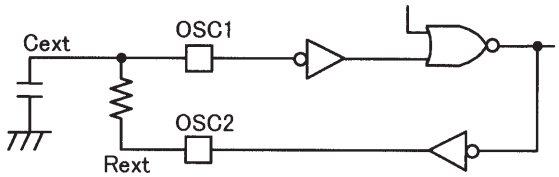
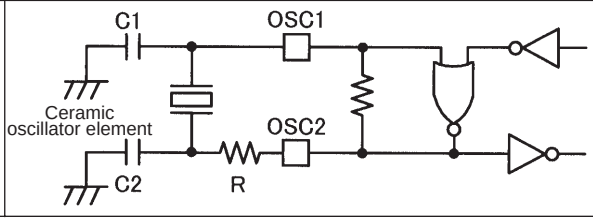
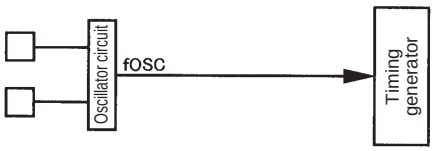
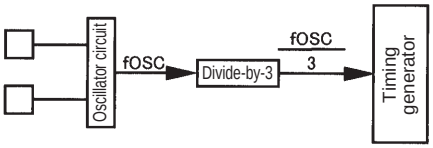
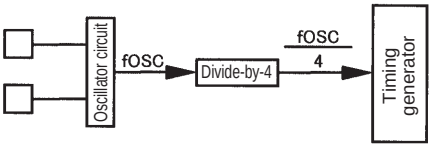
Symbol	Number of pins	I/O	Function	Option	At reset	Handling when unused
PE0-PE1/ WDR	2	I/O	• I/O port E0 to E1 Input in 4-bit units (IP instruction) Output in 4-bit units (OP instruction) Set and reset in 1-bit units (SPB and RPB instructions) Testing in 1-bit units (BP and BNP instructions) • PE0 also has a continuous pulse (64·Tcyc) output function. • PE1 becomes the watchdog reset pin WDR when selected for such as an option.	(1) Open-drain output (2) Pull-up resistor • Options (1) and (2) can be specified in bit units (3) Normal port PE1 (4) Watchdog reset WDR • Either options (3) and (4) may be specified.	High-level output (The output n-channel transistors in the off state.)	Identical to those for PA0 to PA3
PF0/SI PF1/SO PF2/$\overline{\text{SCK}}$ PF3/$\overline{\text{INT}}$	4	I/O	• I/O port F0 to F3 The port functions and options are identical to those of PE0 to PE1 (See note.) • PF0 to PF3 have shared functions as the serial interface pins and the $\overline{\text{INT}}$ input. The function can be selected under program control. SI ... Serial input pin SO ... Serial output pin $\overline{\text{SCK}}$ ... Input and output of the serial clock signal $\overline{\text{INT}}$ ... Interrupt request input The serial I/O function can be switched between 4-bit and 8-bit transfers under program control. Note: There is no continuous pulse output function.	Identical to those for PA0 to PA3	Identical to those for PA0 to PA3 The serial port functions are disabled. The interrupt source is set to $\overline{\text{INT}}$.	Identical to those for PA0 to PA3
PG0-PG3/ AD4-AD7	4	I/O	• I/O port G0 to G3 The port functions and options are identical to those of PE0 to PE1 (See note.) Note: There is no continuous pulse output function. • All four pins have shared functions. PG0/AD4 - A/D converter input AD4 PG1/AD5 - A/D converter input AD5 PG2/AD6 - A/D converter input AD6 PG3/AD7 - A/D converter input AD7	Identical to those for PA0 to PA3	Identical to those for PA0 to PA3	Identical to those for PA0 to PA3
AV_+	1	—	A/D converter reference voltage input	—	—	Connect to V_{SS}.
AV_-	1	—				
$\overline{\text{RES}}$	1	Input	• System reset input • Applications must provide an external capacitor for the power-on reset. • Apply a low level to this pin for 4 clock cycles to effect and reset start.	—	—	—
TEST	1	Input	• IC test pin This pin must be connected to V_{SS} during normal operation.	—	—	This pin must be connected to V_{SS}.

Oscillator Circuit Options

Option	Circuit	Conditions and other notes
External clock		The OSC2 pin must be left open.
Two-pin RC oscillator		
Ceramic oscillator		

Divider Circuit Options

Option	Circuit	Conditions and other notes
No divider		• This option can be used with any of the three oscillator options. • The oscillator frequency or external clock frequency must not exceed 1444 kHz. (LC651154N, LC651152N) • The oscillator frequency or external clock frequency must not exceed 4330 kHz. (LC651154F, LC651152F) • The oscillator frequency or external clock frequency must not exceed 1040 kHz. (LC651154L, LC651152L)
Built-in divide-by-three circuit		• This option can only be used with the external clock and the ceramic oscillator options. • The oscillator frequency or external clock frequency must not exceed 4330 kHz.
Built-in divide-by-four circuit		• This option can only be used with the external clock and the ceramic oscillator options. • The oscillator frequency or external clock frequency must not exceed 4330 kHz.

Caution: The following tables summarize the oscillator and divider circuit options. Use care when selecting these options.

Oscillator Options

LC651154N, LC651152N

Circuit type	Frequency	Divider option (cycle time)	V_{DD} range	Notes
Ceramic oscillator	400 kHz	1/1 (10 µs)	3 to 6 V	Cannot be used with the divide-by-three and divide-by-four options.
	800 kHz	1/1 (5 µs)	3 to 6 V	
		1/3 (15 µs)	3 to 6 V	
		1/4 (20 µs)	3 to 6 V	
	1 MHz	1/1 (4 µs)	3 to 6 V	
		1/3 (12 µs)	3 to 6 V	
		1/4 (16 µs)	3 to 6 V	
	4 MHz	1/3 (3 µs)	3 to 6 V	Cannot be used with the no divider circuit option.
		1/4 (4 µs)	3 to 6 V	
External clock used with the 2-pin RC oscillator circuit	200 k to 1444 kHz	1/1 (20 to 2.77 µs)	3 to 6 V	
	600 k to 4330 kHz	1/3 (20 to 2.77 µs)	3 to 6 V	
	800 k to 4330 kHz	1/4 (20 to 3.70 µs)	3 to 6 V	
Two-pin RC	Use the no divider circuit option and the recommended circuit constants. If using other circuit constants is unavoidable, the application must use a frequency identical to the external clock and observe the V_{DD} range specification.		3 to 6 V	
External clock used with the ceramic oscillator option	External clock drive is not possible. To use external clock drive, select the 2-pin RC oscillator option.			

LC651154F, LC651152F

Circuit type	Frequency	Divider option (cycle time)	V_{DD} range	Notes
Ceramic oscillator	4 MHz	1/1 (1 µs)	2.5 to 6 V	
External clock used with the 2-pin RC oscillator circuit	200 k to 4330 kHz	1/1 (20 to 0.92 µs)	2.5 to 6 V	
External clock used with the ceramic oscillator option	External clock drive is not possible. To use external clock drive, select the 2-pin RC oscillator option.			

LC651154L, LC651152L

Circuit type	Frequency	Divider option (cycle time)	V_{DD} range	Notes
Ceramic oscillator	400 kHz	1/1 (10 µs)	2.2 to 6 V	Cannot be used with the divide-by-three and divide-by-four options.
	800 kHz	1/1 (5 µs)	2.2 to 6 V	
		1/3 (15 µs)	2.2 to 6 V	
		1/4 (20 µs)	2.2 to 6 V	
	1 MHz	1/1 (4 µs)	2.2 to 6 V	
		1/3 (12 µs)	2.2 to 6 V	
		1/4 (16 µs)	2.2 to 6 V	
	4 MHz	1/4 (4 µs)	2.2 to 6 V	Cannot be used with either the no divider circuit option or the divide-by-three circuit option.
External clock used with the 2-pin RC oscillator circuit	200 k to 1040 kHz	1/1 (20 to 3.84 µs)	2.2 to 6 V	
	600 k to 3120 kHz	1/3 (20 to 3.84 µs)	2.2 to 6 V	
	800 k to 4160 kHz	1/4 (20 to 3.84 µs)	2.2 to 6 V	
Two-pin RC	Use the no divider circuit option and the recommended circuit constants. If using other circuit constants is unavoidable, the application must use a frequency identical to the external clock and observe the V_{DD} range specification.		2.2 to 6 V	
External clock used with the ceramic oscillator option	External clock drive is not possible. To use external clock drive, select the 2-pin RC oscillator option.			

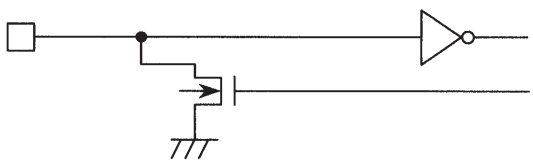
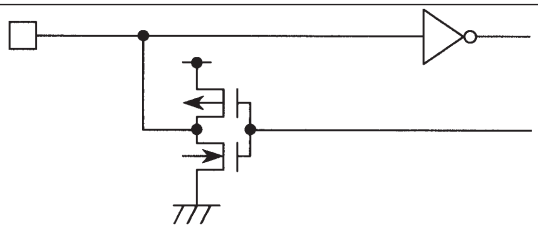
Port C and D Output Level During Reset Option

The output level during a reset can be selected from the two options below in 4-bit units for the C and D ports.

Option	Conditions and other notes
High-level output during reset	Ports C and D in 4-bit units
Low-level output during reset	Ports C and D in 4-bit units

Port Output Type Option

The following two options may be selected for the I/O ports individually (bit units).

Option	Circuit	Applicable ports
1. Open-drain output		Ports A, C, D, E, F, and G
2. Built-in pull-up resistor		

Watchdog Reset Option

This option allows the PE1/WDR pin to be selected either to be used as the normal port PE1 or to be used as the watchdog reset pin WDR.

LC651154N, 651152N

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Applicable pins and notes	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Allowed up to the generated voltage.	
Input voltage	V_I (1)		OSC1 *1	–0.3 to V_{DD} + 0.3	
	V_I (2)		TEST, $\overline{RES}$, AV_+, AV_-	–0.3 to V_{DD} + 0.3	
I/O voltage	V_{IO} (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	Open-drain specification ports	–0.3 to +15	
	V_{IO} (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	Pull-up resistor specification ports	–0.3 to V_{DD} + 0.3	
	V_{IO} (3)	PC0 to 3, PG0 to 3		–0.3 to V_{DD} + 0.3	
Peak output current	I_{OP}		I/O ports	–2 to +20	mA
Average output current	I_{OA}	Per single pin, averaged over 100 ms	I/O ports	–2 to +20	
	ΣI_{OA} (1)	The total current for PC0 to PC3, PD0 to PD3, and PE0 to PE1 *2	PC0 to 3 PD0 to 3 PE0 to 1	–15 to +100	
	ΣI_{OA} (2)	The total current for PF0 to PF3, PG0 to PG3, and PA0 to PA3 (See note 2.) *2	PF0 to 3 PG0 to 3 PA0 to 3	–15 to +100	
Allowable power dissipation	Pd max (1)	Ta = –40 to +85°C (DIP package)		310	mW
	Pd max (2)	Ta = –40 to +85°C (MFP package)		220	
	Pd max (3)	Ta = –40 to +85°C (SSOP package)		160	
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 6.0 V (Unless otherwise specified.)

Parameter	Symbol	Conditions	Applicable pins and notes	Ratings			Unit
				min	typ	max	
Operating supply voltage	V_{DD}		V_{DD}	3.0		6.0	V
Standby supply voltage	V_{ST}	RAM and register values retained*3	V_{DD}	1.8		6.0	
High-level input voltage	V_{IH} (1)	Output n-channel transistors off	Ports C, D, E, and F with open-drain specifications	0.7 V_{DD}		13.5	
	V_{IH} (2)	Output n-channel transistors off	Ports C, D, E, and F with pull-up resistor specifications	0.7 V_{DD}		V_{DD}	
	V_{IH} (3)	Output n-channel transistors off	Port A, G	0.7 V_{DD}		V_{DD}	
	V_{IH} (4)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with open-drain specifications	0.8 V_{DD}		13.5	
	V_{IH} (5)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with pull-up resistor specifications	0.8 V_{DD}		V_{DD}	
	V_{IH} (6)	V_{DD} = 1.8 to 6.0 V	$\overline{RES}$	0.8 V_{DD}		V_{DD}	
	V_{IH} (7)	External clock specifications	OSC1	0.8 V_{DD}		V_{DD}	

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Parameter	Symbol	Conditions		Applicable pins and notes	Ratings			Unit
					min	typ	max	
Low-level input voltage	V_{IL} (1)	Output n-channel transistors off	V_{DD} = 4 to 6 V	Port	V_{SS}		0.3 V_{DD}	V
	V_{IL} (2)	Output n-channel transistors off	V_{DD} = 3 to 6 V	Port	V_{SS}		0.25 V_{DD}	
	V_{IL} (3)	Output n-channel transistors off	V_{DD} = 4 to 6 V	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.25 V_{DD}	
	V_{IL} (4)	Output n-channel transistors off	V_{DD} = 3 to 6 V	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.2 V_{DD}	
	V_{IL} (5)	External clock specifications	V_{DD} = 4 to 6 V	OSC1	V_{SS}		0.25 V_{DD}	
	V_{IL} (6)	External clock specifications	V_{DD} = 3 to 6 V	OSC1	V_{SS}		0.2 V_{DD}	
	V_{IL} (7)		V_{DD} = 4 to 6 V	TEST	V_{SS}		0.3 V_{DD}	
	V_{IL} (8)		V_{DD} = 3 to 6 V	TEST	V_{SS}		0.25 V_{DD}	
	V_{IL} (9)		V_{DD} = 4 to 6 V	$\overline{RES}$	V_{SS}		0.25 V_{DD}	
	V_{IL} (10)		V_{DD} = 3 to 6 V	$\overline{RES}$	V_{SS}		0.2 V_{DD}	
Operating frequency (cycle time)	fop (Tcyc)	The clock may have a frequency up to 4.33 MHz when either the divide-by-three or divide-by-four internal divider circuit option is used.	V_{DD} = 3 to 6 V		200 (20)		1444 (2.77)	kHz (µs)
External clock conditions		Figure 1.						
Frequency	text	Either the divide-by-three or divide-by-four internal divider circuit must be used if the clock frequency exceeds 1.444 MHz.	V_{DD} = 3 to 6 V	OSC1	200		4330	kHz
Pulse width	textH, textL		V_{DD} = 3 to 6 V	OSC1	69			ns
Rise and fall times	textR, textF		V_{DD} = 3 to 6 V	OSC1			50	
Recommended oscillator circuit constants Two-pin RC oscillator	Cext Rext	Figure 2	V_{DD} = 3 to 6 V	OSC1, OSC2	270 ±5% 12 ±1%			pF kΩ
	Cext Rext	Figure 2	V_{DD} = 3 to 6 V	OSC1, OSC2	270 ±5% 5.6 ±1%			pF kΩ
Ceramic oscillator *4		Figure 3			See table 1.			

Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 6.0 V (Unless otherwise specified.)

Parameter		Symbol	Conditions	Applicable pins and notes	Ratings min	Ratings typ	Ratings max	Unit
High-level input current		I_{IH} (1)	• Output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = 13.5 V	Ports C, D, E and F with the open-drain specifications			5.0	µA
		I_{IH} (2)	• Output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = V_{DD}	Ports A and G with the open-drain specifications			1.0	
		I_{IH} (3)	When an external clock is used, V_{IN} = V_{DD}	OSC1			1.0	
Low-level input current		I_{IL} (1)	• Output n-channel transistors off • V_{IN} = V_{SS}	Ports with the open-drain specifications	–1.0			
		I_{IL} (2)	• Output n-channel transistors off • V_{IN} = V_{SS}	Ports with the pull-up resistor specifications	–1.3	–0.35		mA
		I_{IL} (3)	V_{IN} = V_{SS}	$\overline{RES}$	–45	–10		µA
		I_{IL} (4)	When an external clock is used, V_{IN} = V_{SS}	OSC1	–1.0			
High-level output voltage		V_{OH} (1)	• I_{OH} = –50 µA • V_{DD} = 4.0 to 6.0 V	Ports with the pull-up resistor specifications	V_{DD} – 1.2			V
		V_{OH} (2)	I_{OH} = –10 µA	Ports with the pull-up resistor specifications	V_{DD} – 0.5			
Low-level output voltage		V_{OL} (1)	• I_{OL} = 10 mA • V_{DD} = 4.0 to 6.0 V	Port			1.5	
		V_{OL} (2)	When I_{OL} = 1 mA and the I_{OL} for each port is 1 mA or less.	Port			0.5	
Schmitt characteristics	Hysteresis voltage	V_{HIS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, and OSC1 with Schmitt specifications*5		0.1 V_{DD}		
	High-level threshold voltage	V_{tH}			0.4 V_{DD}		0.8 V_{DD}	
	Low-level threshold voltage	V_{tL}			0.2 V_{DD}		0.6 V_{DD}	
Current drain *6 Two-pin RC oscillator		IDDOP (1)	• Operating, with the output n-channel transistors off • With the ports at V_{DD} • Figure 2, fosc = 800 kHz (typical)	V_{DD}		1.5	4	mA
Ceramic oscillator		IDDOP (2)	• Figure 3, 4 MHz, divide-by-three circuit used	V_{DD}		1.5	5	
		IDDOP (3)	• Figure 3, 4 MHz, divide-by-four circuit used	V_{DD}		1.5	4	
		IDDOP (4)	• Figure 3, 400 kHz	V_{DD}		1.0	2.5	
		IDDOP (5)	• Figure 3, 800 kHz	V_{DD}		1.5	4	
External clock		IDDOP (6)	• 200 kHz to 1444 kHz, no divider circuit • 600 kHz to 4330 kHz, divide-by-three circuit used • 800 kHz to 4330 kHz, divide-by-four circuit used	V_{DD}		1.5	5	
Standby mode		IDDst	Output n-channel transistors off, V_{DD} = 6 V	V_{DD}		0.05	10	µA
			Ports at V_{DD}, V_{DD} = 3 V	V_{DD}		0.025	5	

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Parameter	Symbol	Conditions	Applicable pins and notes	Ratings			Unit
				min	typ	max	
Oscillator characteristics Ceramic oscillator Oscillator frequency	f_{CFOSC}*7	• Figure 3, fo = 400 kHz • Figure 3, fo = 800 kHz • Figure 3, fo = 1 MHz • Figure 3, fo = 4 MHz, with the divide-by-three or divide-by-four circuit used.	OSC1, OSC2 OSC1, OSC2 OSC1, OSC2 OSC1, OSC2	392 784 980 3920	400 800 1000 4000	408 816 1020 4080	kHz
Oscillator stabilization time (note 8)	t_{CFS}	• Figure 4, fo = 400 kHz • Figure 4, fo = 800 kHz, 1 MHz, or 4 MHz, with the divide-by-three or divide-by-four circuit used.				10 10	ms
Two-pin RC oscillator Oscillator frequency	f_{MOSC}	• Figure 2, Cext = 270 pF ±5% • Figure 2, Rext = 5.6 kΩ ±1%	OSC1, OSC2	587	800	1298	kHz
		• Figure 2, Cext = 270 pF ±5% • Figure 2, Rext = 12 kΩ ±1%	OSC1, OSC2	290	400	818	
Pull-up resistor I/O ports	RPP	• Output n-channel transistors off • $V_{IN} = V_{SS}$, V_{DD} = 5 V	Pull-up resistor specification ports	8	14	30	kΩ
$\overline{RES}$	Ru	$V_{IN} = V_{SS}$, V_{DD} = 5 V	$\overline{RES}$	200	500	800	
External reset characteristics Reset time	t_{RST}				See figure 5.		
Pin capacitances	Cp	• f = 1 MHz • With all pins other than the pin being tested at $V_{IN} = V_{SS}$.			10		pF
Serial clock Input clock cycle time	t_{CKCY} (1)	Figure 6	$\overline{SCK}$	2.0			μs
Output clock cycle time	t_{CKCY} (2)	Figure 6	$\overline{SCK}$		64 × TCYC*9		
Input clock low-level pulse width	t_{CKL} (1)	Figure 6	$\overline{SCK}$	1.0			
Output clock low-level pulse width	t_{CKL} (2)	Figure 6	$\overline{SCK}$		32 × TCYC		
Input clock high-level pulse width	t_{CKH} (1)	Figure 6	$\overline{SCK}$	1.0			
Output clock high-level pulse width	t_{CKH} (2)	Figure 6	$\overline{SCK}$		32 × TCYC		
Serial input Data setup time	t_{ICK}	• Stipulated with respect to the rising edge of $\overline{SCK}$. • Figure 6	SI	0.4			
Data hold time	t_{CKI}		SI	0.4			
Serial output Output delay time	t_{CKO}	• Stipulated with respect to the falling edge of $\overline{SCK}$. • With an external resistor of 1 kΩ and an external capacitor of 50 pF on only the n-channel open-drain pins. • Figure 6	SO			0.6	

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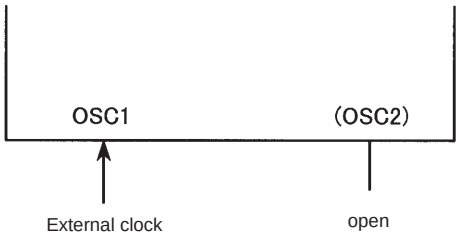
Parameter		Symbol	Conditions		Applicable pins and notes	Ratings min	Ratings typ	Ratings max	Unit
Pulse output function Period		t_{PCY}	• Figure 7 • T_{CYC} = 4 × system clock period • With an external resistor of 1 kΩ and an external capacitor of 50 pF on only the n-channel open-drain pins.		PE0		64 × T_{CYC}		µs
High-level pulse width		t_{PH}			PE0		32 × T_{CYC} ±10%		µs
Low-level pulse width		t_{PL}			PE0		32 × T_{CYC} ±10%		µs
A/D converter characteristics	Resolution			V_{DD} = 3 to 6 V			8		bit
	Absolute precision		$AV_+ = V_{DD}$ $AV_- = V_{SS}$				±1	±2	LSB
	Conversion time	TCAD	When the A/D converter speed is normal (1:1), namely 26 × T_{CYC}			72 (T_{CYC} = 2.77 µs)		312 (T_{CYC} = 12 µs)	µs
			When the A/D converter speed is one half (1:2), namely 51 × T_{CYC}			141 (T_{CYC} = 2.77 µs)		612 (T_{CYC} = 12 µs)	µs
	Input reference voltage	AV_+			AV_+	AV_-		V_{DD}	V
		AV_-			AV_-	V_{SS}		AV_+	V
	Input reference current range	IRIF	$AV_+ = V_{DD}$, $AV_- = V_{SS}$		AV_+, AV_-	200	500	800	µA
	Analog input voltage range	V_{AIN}			AD0 to AD7	AV_-		AV_+	V
	Analog port input current	I_{AIN}	Including the output off leakage current. $V_{AIN} = V_{DD}$		AD0 to AD7 (The I/O shared function ports have open-drain specifications.)			1	µA
			$V_{AIN} = V_{SS}$			–1			µA
Watchdog timer	Recommended constants*10	Cw	When PE1 has the open-drain specifications.	V_{DD} = 3 to 6 V	WDR		0.1 ±5%		µF
		Rw	When PE1 has the open-drain specifications.		WDR		680 ±1%		kΩ
		Rl	When PE1 has the open-drain specifications.		WDR		100 ±1%		Ω
	Clear time (discharge)	t_{WCT}	Figure 8		WDR	100			µs
	Clear period (charge)	t_{WCCY}	Figure 8		WDR	36			ms
	Recommended constants*10	Cw	When PE1 has the open-drain specifications.	V_{DD} = 3 to 6 V	WDR		0.047 ±5%		µF
		Rw	When PE1 has the open-drain specifications.		WDR		680 ±1%		kΩ
		Rl	When PE1 has the open-drain specifications.		WDR		100 ±1%		Ω
	Clear time (discharge)	t_{WCT}	Figure 8		WDR	40			µs
	Clear period (charge)	t_{WCCY}	Figure 8		WDR	18			ms

Notes:1. Allowed up to the amplitude generated when the oscillator shown in figure 3 is used with the recommended circuit constants and driven by the IC.
2. The average over a 100 ms period.
3. The operating V_{DD} supply voltage must be maintained from the point the HALT instruction is executed until the IC has fully entered the standby state. Applications must also assure that no chattering occurs on the PA3 pin during the HALT instruction execution cycle.
4. Recommended circuit constants that have been verified to oscillate stably according to the oscillator element manufacturer using the Sanyo-stipulated oscillator characteristics evaluation board.
5. The OSC1 pin will have Schmitt characteristics when external clock oscillator is selected with the two-pin RC oscillator option.
6. These are the results of testing using our (Sanyo's) characteristics evaluation board with the recommended circuit constants used as external components. The current flowing in the IC's output transistors and transistors that have pull-up resistors is not included.
7. f_{CFOSC} is the frequency when the recommended circuit constants from table 1 are used as external components.
8. Indicates the time required to achieve stable oscillation from the point V_{DD} rises above the lower limit of the operating voltage range.
9. TCYC = 4 × the system clock period
10. If the application could be used in an environment in which condensation is possible, extra care with respect to the leakage between PE1 and adjacent pins and leakage associated with external resistors and capacitor is required during design.



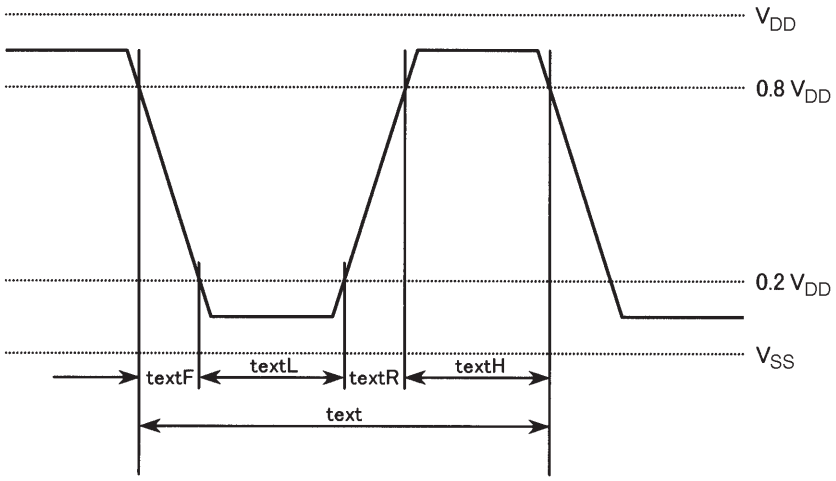


Figure 1 External Clock Input Waveform

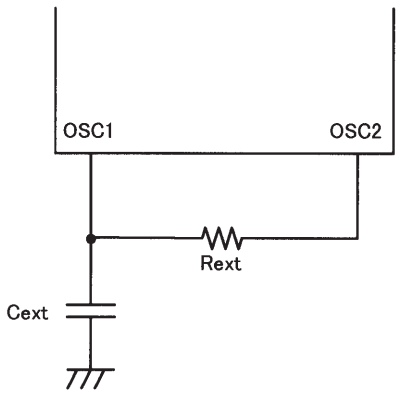


Figure 2 Two-Pin RC Oscillator Circuit

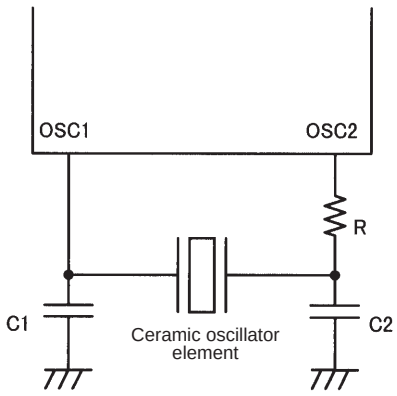


Figure 3 Ceramic Oscillator Circuit

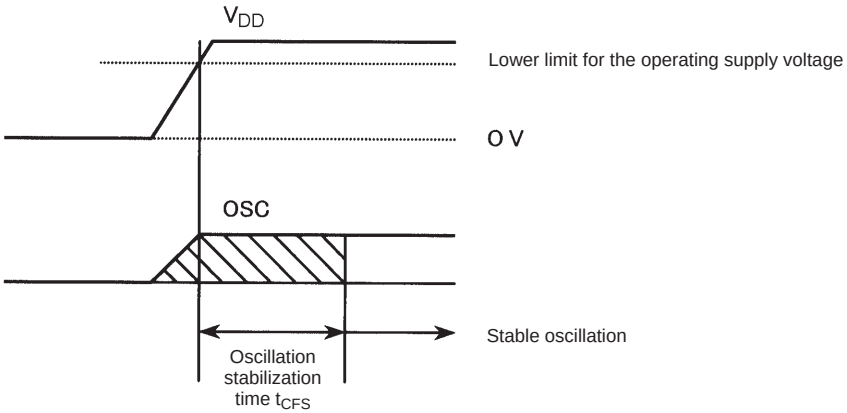


Figure 4 Oscillation Stabilization Time

Table 1 Recommended Ceramic Oscillator Circuit Constants

4 MHz (Murata Mfg. Co., Ltd.)	C1	33 pF ±10%
CSA4.00MG	C2	33 pF ±10%
CST4.00MGW (Internal capacitor)	R	0 Ω
4 MHz (Kyocera Corporation)	C1	33 pF ±10%
KBR4.0MSA	C2	33 pF ±10%
KBR4.0MKS (Internal capacitor)	R	0 Ω
1 MHz (Murata Mfg. Co., Ltd.)	C1	100 pF ±10%
CSB1000J	C2	100 pF ±10%
	R	3.3 kΩ
800 kHz (Murata Mfg. Co., Ltd.)	C1	100 pF ±10%
CSB800J	C2	100 pF ±10%
	R	3.3 kΩ
400 kHz (Murata Mfg. Co., Ltd.)	C1	220 pF ±10%
CSB400P	C2	220 pF ±10%
	R	3.3 kΩ

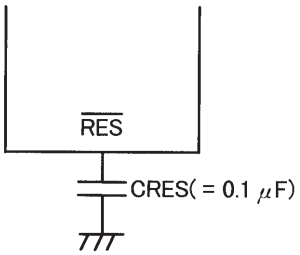


Figure 5 Reset Circuit

Note: If the power supply rise time is zero, the reset time when CRES = 0.1 μF will be between 10 and 100 ms.
If the power supply rise time is long, increase the value of CRES so that the reset time is at least 10 ms.

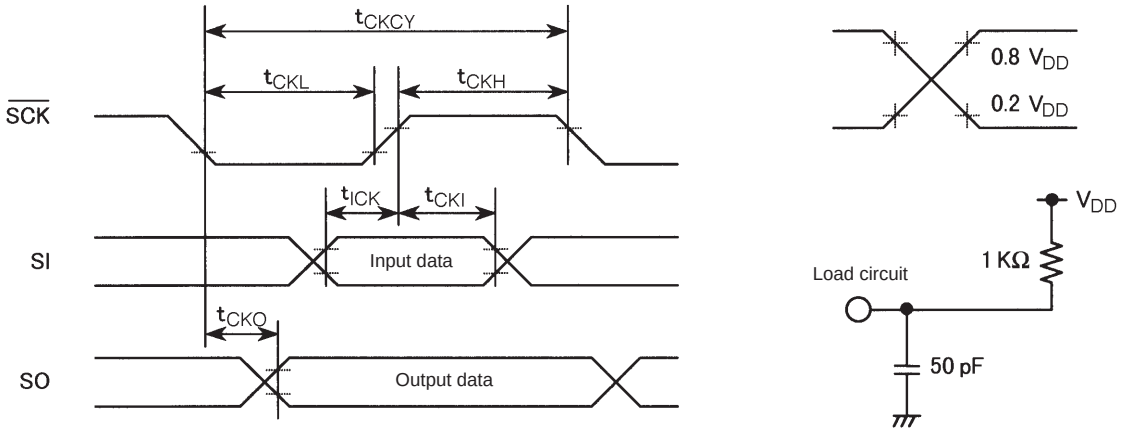
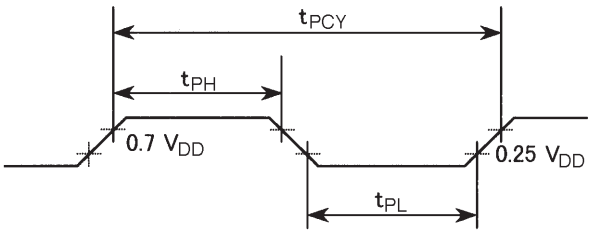
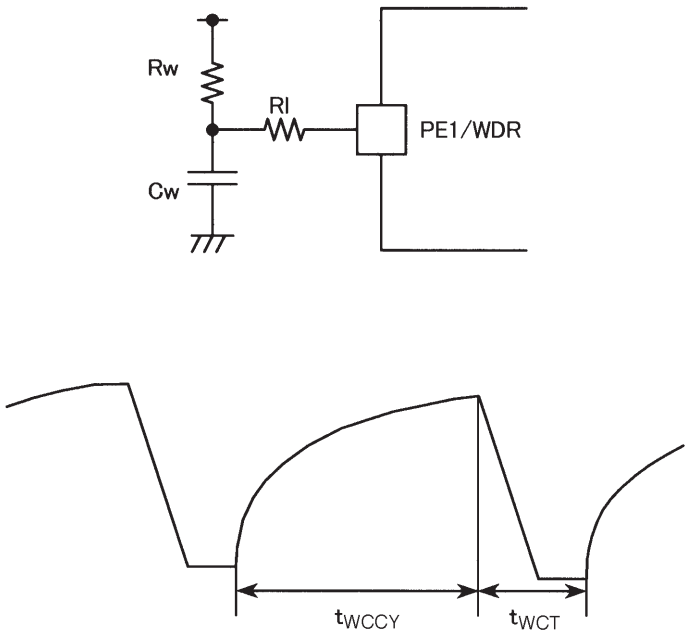


Figure 6 Serial I/O Timing



The load conditions are the same as those in figure 5.

Figure 7 Port PE0 Pulse Output Timing



t_{WCCY}: The charge time due to the time constant of the circuit consisting of the external components Cw, Rw, and Rl.
t_{WCT}: The discharge time due to software processing.

Figure 8 Watchdog Timer Waveform

RC Oscillator Characteristics for the LC651154N and LC651152N

Figure 9 shows the RC oscillator characteristics for the LC651154N and LC651152N.
However, the sample-to-sample variation in the LC651154N and LC651152N RC oscillator frequency described below does occur.

1) When:
   V_{DD} = 3.0 to 6.0 V, Ta = –40 to +85°C
   External constants: Cext = 270 pF
   Rext = 12.0 kΩ
   f_{MOSC} will be:
   290 kHz ≤ f_{MOSC} ≤ 818 kHz
2) When:
   V_{DD} = 3.0 to 6.0 V, Ta = –40 to +85°C
   External constants: Cext = 270 pF
   Rext = 5.6 kΩ
   f_{MOSC} will be:
   587 kHz ≤ f_{MOSC} ≤ 1298 kHz
   Therefore, only the above circuit constants are recommended.

   If use of circuit constants other than the above is unavoidable, they must be in the following ranges.
   Cext = 150 to 390 pF
   Rext = 3 to 20 kΩ
   (See figure 9.)

Notes • The oscillator frequency must be in the range 350 to 850 kHz when V_{DD} = 5.0 V and Ta = 25°C.
• Applications must be designed to have adequate margins so that the oscillator frequency falls in the operating clock frequency range (see the oscillator divider option table) for the voltage range V_{DD} = 3.0 to 6.0 V and for the temperature range Ta = –40 to +85°C.

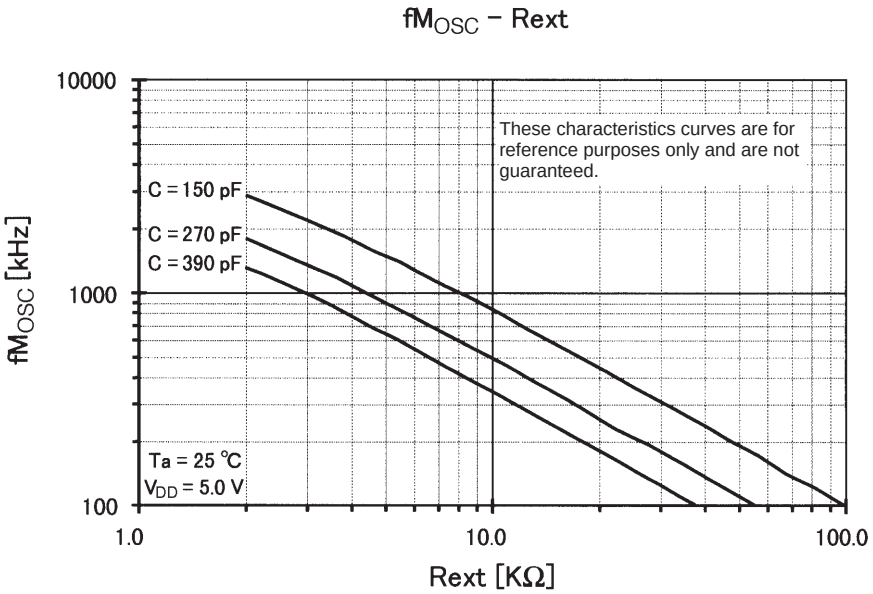


Figure 9 RC Oscillator Frequency Data (Representative Values)

LC651154F, 651152F

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Applicable pins and notes	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Allowed up to the generated voltage.	
Input voltage	V_I (1)		OSC1 *1	–0.3 to V_{DD} + 0.3	
	V_I (2)		TEST, $\overline{RES}$, AV_+, AV_-	–0.3 to V_{DD} + 0.3	
I/O voltage	V_{IO} (1)	PC0 to PC3, PD0 to PD3, PE0, 1, PF0 to PF3	Open-drain specification ports	–0.3 to +15	
	V_{IO} (2)	PC0 to PC3, PD0 to PD3, PE0, 1, PF0 to PF3	Pull-up resistor specification ports	–0.3 to V_{DD} + 0.3	
	V_{IO} (3)	PA0 to PA3, PG0 to PG3		–0.3 to V_{DD} + 0.3	
Peak output current	I_{OP}		I/O ports	–2 to +20	mA
Average output current	I_{OA}	Per single pin, averaged over 100 ms	I/O ports	–2 to +20	
	ΣI_{OA} (1)	The total current for PC0 to PC3, PD0 to PD3, and PE0 and PE1 *2	PC0 to PC3 PD0 to PD3 PE0 and PE1	–15 to +100	
	ΣI_{OA} (2)	The total current for PF0 to PF3, PG0 to PG3, and PA0 to PA3 (See note 2.) *2	PF0 to PF3 PG0 to PG3 PA0 to PA3	–15 to +100	
Allowable power dissipation	Pd max (1)	Ta = –40 to +85°C (DIP package)		310	mW
	Pd max (2)	Ta = –40 to +85°C (MFP package)		220	
	Pd max (3)	Ta = –40 to +85°C (SSOP package)		160	
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.5 to 6.0 V (Unless otherwise specified.)

Parameter	Symbol	Conditions	Applicable pins and notes	Ratings			Unit
				min	typ	max	
Operating supply voltage	V_{DD}		V_{DD}	2.5		6.0	V
Standby supply voltage	V_{ST}	RAM and register values retained*3	V_{DD}	1.8		6.0	
High-level input voltage	V_{IH} (1)	Output n-channel transistors off	Ports C, D, E, and F with open-drain specifications	0.7 V_{DD}		13.5	
	V_{IH} (2)	Output n-channel transistors off	Ports C, D, E, and F with pull-up resistor specifications	0.7 V_{DD}		V_{DD}	
	V_{IH} (3)	Output n-channel transistors off	Port A, G	0.7 V_{DD}		V_{DD}	
	V_{IH} (4)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with open-drain specifications	0.8 V_{DD}		13.5	
	V_{IH} (5)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with pull-up resistor specifications	0.8 V_{DD}		V_{DD}	
	V_{IH} (6)	V_{DD} = 1.8 to 6.0 V	$\overline{RES}$	0.8 V_{DD}		V_{DD}	
	V_{IH} (7)	External clock specifications	OSC1	0.8 V_{DD}		V_{DD}	

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Parameter	Symbol	Conditions		Applicable pins and notes	Ratings min	Ratings typ	Ratings max	Unit
Low-level input voltage	V_{IL} (1)	Output n-channel transistors off	V_{DD} = 4 to 6 V	Port	V_{SS}		0.3 V_{DD}	V
	V_{IL} (2)	Output n-channel transistors off	V_{DD} = 2.5 to 6 V	Port	V_{SS}		0.2 V_{DD}	
	V_{IL} (3)	Output n-channel transistors off	V_{DD} = 4 to 6 V	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.25 V_{DD}	
	V_{IL} (4)	Output n-channel transistors off	V_{DD} = 2.5 to 6 V	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.15 V_{DD}	
	V_{IL} (5)	External clock specifications	V_{DD} = 4 to 6 V	OSC1	V_{SS}		0.25 V_{DD}	
	V_{IL} (6)	External clock specifications	V_{DD} = 2.5 to 6 V	OSC1	V_{SS}		0.15 V_{DD}	
	V_{IL} (7)		V_{DD} = 4 to 6 V	TEST	V_{SS}		0.3 V_{DD}	
	V_{IL} (8)		V_{DD} = 2.5 to 6 V	TEST	V_{SS}		0.2 V_{DD}	
	V_{IL} (9)		V_{DD} = 4 to 6 V	$\overline{RES}$	V_{SS}		0.25 V_{DD}	
	V_{IL} (10)		V_{DD} = 2.5 to 6 V	$\overline{RES}$	V_{SS}		0.15 V_{DD}	
Operating frequency (cycle time)	fop (Tcyc)				200 (20)		4330 (0.92)	kHz (µs)
External clock conditions								
Frequency	text			OSC1	200		4330	kHz
Pulse width	textH, textL	Figure 1.		OSC1	69			ns
Rise and fall times	textR, textF			OSC1			50	ns
Recommended oscillator circuit constants		Figure 2			See table 1.			
Ceramic oscillator *4								

Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.5 to 6.0 V (Unless otherwise specified.)

Parameter		Symbol	Conditions	Applicable pins and notes	Ratings min	Ratings typ	Ratings max	Unit
High-level input current		I_{IH} (1)	• Output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = 13.5 V	Ports C, D, E and F with the open-drain specifications			5.0	µA
		I_{IH} (2)	• Output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = V_{DD}	Ports A and G with the open-drain specifications			1.0	
		I_{IH} (3)	When an external clock is used, V_{IN} = V_{DD}	OSC1			1.0	
Low-level input current		I_{IL} (1)	• Output n-channel transistors off • V_{IN} = V_{SS}	Ports with the open-drain specifications	–1.0			
		I_{IL} (2)	• Output n-channel transistors off • V_{IN} = V_{SS}	Ports with the pull-up resistor specifications	–1.3	–0.35		mA
		I_{IL} (3)	V_{IN} = V_{SS}	$\overline{RES}$	–45	–10		µA
		I_{IL} (4)	When an external clock is used, V_{IN} = V_{SS}	OSC1	–1.0			
High-level output voltage		V_{OH} (1)	• I_{OH} = –50 µA • V_{DD} = 4.0 to 6.0 V	Ports with the pull-up resistor specifications	V_{DD} – 1.2			V
		V_{OH} (2)	I_{OH} = –10 µA	Ports with the pull-up resistor specifications	V_{DD} – 0.5			
Low-level output voltage		V_{OL} (1)	• I_{OL} = 10 mA • V_{DD} = 4.0 to 6.0 V	Port			1.5	
		V_{OL} (2)	When I_{OL} = 1 mA and the I_{OL} for each port is 1 mA or less.	Port			0.5	
Schmitt characteristics	Hysteresis voltage	V_{HIS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, and OSC1 with Schmitt specifications*5		0.1 V_{DD}		
	High-level threshold voltage	V_{tH}			0.4 V_{DD}		0.8 V_{DD}	
	Low-level threshold voltage	V_{tL}			0.25 V_{DD}		0.6 V_{DD}	

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Parameter	Symbol	Conditions	Applicable pins and notes	Ratings			Unit
				min	typ	max	
Current drain*6							
Ceramic oscillator	IDDOP (1)	• Figure 2, 4 MHz • 200 kHz to 4330 kHz	V_{DD}		2	6	mA
	IDDOP (2)	• Operating, with the output n-channel transistors off and the ports at V_{DD}.	V_{DD}		2	6	
Standby mode	IDDst	• Output n-channel transistors off V_{DD} = 6 V	V_{DD}		0.05	10	µA
		• Ports at V_{DD}, V_{DD} = 2.5 V	V_{DD}		0.025	5	
Oscillator characteristics Ceramic oscillator	f_{CFOSC}*7	• Figure 2, fo = 4 MHz	OSC1, OSC2	3920	4000	4080	kHz
Oscillator frequency*8	t_{CFS}	• Figure 3, fo = 4 MHz				10	ms
Pull-up resistor I/O ports	RPP	• Output n-channel transistors off • V_{IN} = V_{SS}, V_{DD} = 5 V	Pull-up resistor specification ports	8	14	30	kΩ
$\overline{RES}$	Ru	V_{IN} = V_{SS}, V_{DD} = 5 V	$\overline{RES}$	200	500	800	
External reset characteristics Reset time	t_{RST}				See figure 4.		
Pin capacitances	Cp	• f = 1 MHz • With all pins other than the pin being tested at V_{IN} = V_{SS}.			10		pF
Serial clock Input clock cycle time	t_{CKCY} (1)	Figure 5	$\overline{SCK}$	2.0			µs
Output clock cycle time	t_{CKCY} (2)	Figure 5	$\overline{SCK}$		$64 \times T_{CYC}$*9		
Input clock low-level pulse width	t_{CKL} (1)	Figure 5	$\overline{SCK}$	0.6			
Output clock low-level pulse width	t_{CKL} (2)	Figure 5	$\overline{SCK}$		$32 \times T_{CYC}$		
Input clock high-level pulse width	t_{CKH} (1)	Figure 5	$\overline{SCK}$	0.6			
Output clock high-level pulse width	t_{CKH} (2)	Figure 5	$\overline{SCK}$		$32 \times T_{CYC}$		
Serial input Data setup time	t_{ICK}	• Stipulated with respect to the rising edge of SCK. • Figure 5	SI	0.2			
Data hold time	t_{CKI}		SI	0.2			
Serial output Output delay time	t_{CKO}	• Stipulated with respect to the falling edge of $\overline{SCK}$. • With an external resistor of 1 kΩ and an external capacitor of 50 pF on only the n-channel open-drain pins. • Figure 5	SO			0.4	
Pulse output function Period	t_{PCY}	• Figure 6 • T_{CYC} = 4 × system clock period • With an external resistor of 1 kΩ and an external capacitor of 50 pF on only the n-channel open-drain pins.	PE0		$64 \times T_{CYC}$		
High-level pulse width	t_{PH}		PE0		$32 \times T_{CYC}$ ±10%		
Low-level pulse width	t_{PL}		PE0		$32 \times T_{CYC}$ ±10%		

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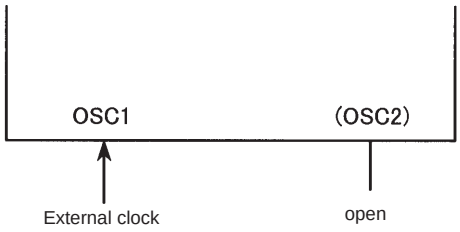
	Parameter	Symbol	Conditions			Applicable pins and notes	Ratings min	Ratings typ	Ratings max	Unit
A/D converter characteristics	Resolution				V_{DD} = 3 to 6 V			8		bit
	Absolute precision		$AV_+ = V_{DD}$	A/D converter speed 1/1	V_{DD} = 3.5 to 6 V			±1	±2	LSB
			$AV_- = V_{SS}$	A/D converter speed 1/2	V_{DD} = 3.5 to 6 V			±1	±2	
	Conversion time	TCAD	When the A/D converter speed is normal (1/1), namely 26 × T_{CYC}		V_{DD} = 3.5 to 6 V		24 (T_{CYC} = 0.92 µs)		312 (T_{CYC} = 12 µs)	µs
			When the A/D converter speed is one half (1/2), namely 51 × T_{CYC}		V_{DD} = 3 to 6 V		47 (T_{CYC} = 0.92 µs)		612 (T_{CYC} = 12 µs)	
	Input reference voltage	AV_+			V_{DD} = 3 to 6 V	AV_+	AV_-		V_{DD}	V
		AV_-				AV_-	V_{SS}		AV+	
	Input reference current range	IRIF	AV+ = V_{DD}, AV_- = V_{SS}			AV_+, AV_-	200	500	800	µA
	Analog input voltage range	VAIN				AD0 to AD7	AV_-		AV_+	V
	Analog port input current	IAIN	Including the output off leakage current. $V_{AIN} = V_{DD}$			AD0 to AD7 (The I/O shared function ports have open-drain specifications.)			1	µA
			$V_{AIN} = V_{SS}$				–1			
Watchdog timer	Recommended constants*10	Cw	When PE1 has the open drain specifications.			WDR		0.01 ±5%		µF
		Rw	When PE1 has the open drain specifications.			WDR		680 ±1%		kΩ
		RI	When PE1 has the open drain specifications.			WDR		100 ±1%		Ω
	Clear time (discharge)	t_{WCT}	Figure 7			WDR	10			µs
	Clear period (charge)	t_{WCCY}	Figure 7			WDR	4.2			ms

Notes:1. Allowed up to the amplitude generated when the oscillator shown in figure 2 is used with the recommended circuit constants and driven by the IC.
2. The average over a 100 ms period.
3. The operating V_{DD} supply voltage must be maintained from the point the HALT instruction is executed until the IC has fully entered the standby state. Applications must also assure that no chattering occurs on the PA3 pin during the HALT instruction execution cycle.
4. Recommended circuit constants that have been verified to oscillate stably according to the oscillator element manufacturer using the Sanyo-stipulated oscillator characteristics evaluation board.
5. The OSC1 pin will have Schmitt characteristics when external clock oscillator is selected with the two-pin RC oscillator option.
6. These are the results of testing using our (Sanyo's) characteristics evaluation board with the recommended circuit constants used as external components. The current flowing in the IC's output transistors and transistors that have pull-up resistors is not included.
7. f_{CFOSC} is the frequency when the recommended circuit constants from table 1 are used as external components.
8. Indicates the time required to achieve stable oscillation from the point V_{DD} rises above the lower limit of the operating voltage range (See figure 3).
9. T_{CYC} = 4 × the system clock period
10. If the application could be used in an environment in which condensation is possible, extra care with respect to the leakage between PE1 and adjacent pins and leakage associated with external resistors and capacitor is required during design.



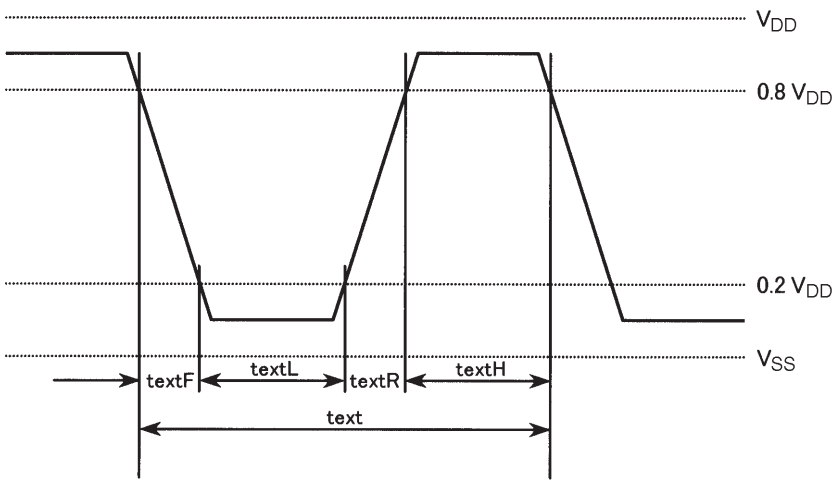


Figure 1 External Clock Input Waveform

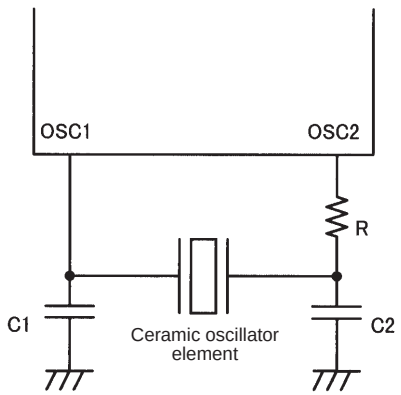


Figure 2 Ceramic Oscillator Circuit

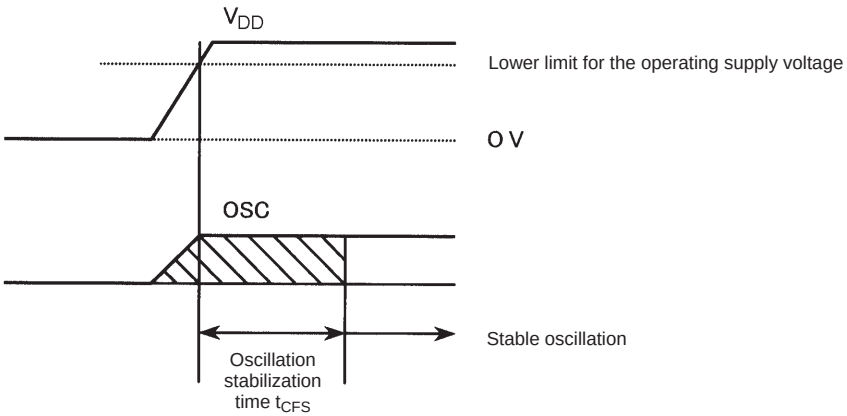


Figure 4 Oscillation Stabilization Time

Table 1 Recommended Ceramic Oscillator Circuit Constants

4 MHz (Murata Mfg. Co., Ltd.)	C1	33 pF ±10%
CSA4.00MG	C2	33 pF ±10%
CST4.00MGW (Internal capacitor)	R	0 Ω
4 MHz (Kyocera Corporation)	C1	33 pF ±10%
KBR4.0MSA	C2	33 pF ±10%
KBR4.0MKS (Internal capacitor)	R	0 Ω

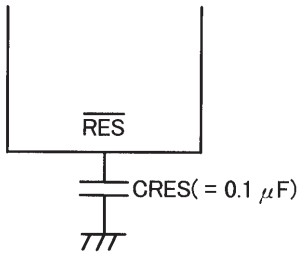


Figure 5 Reset Circuit

Note: If the power supply rise time is zero, the reset time when CRES = 0.1 µF will be between 10 and 100 ms.
If the power supply rise time is long, increase the value of CRES so that the reset time is at least 10 ms.

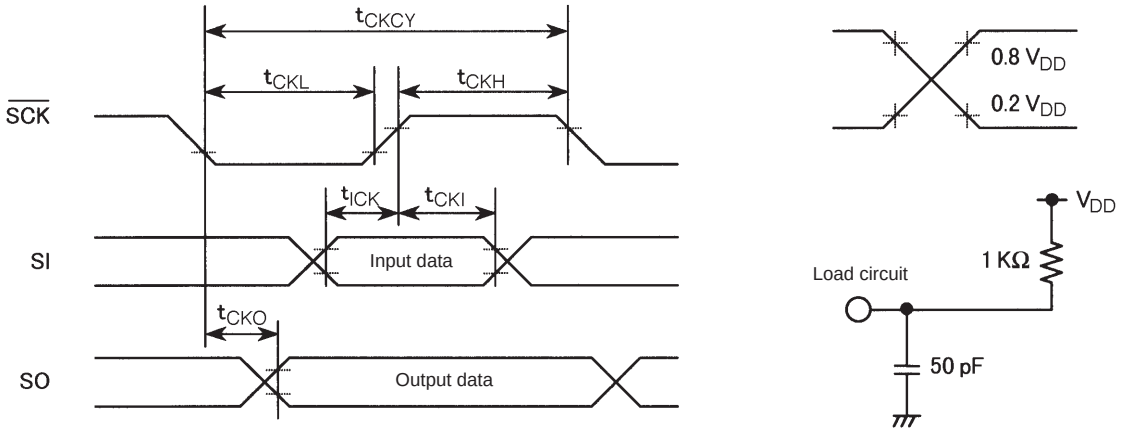
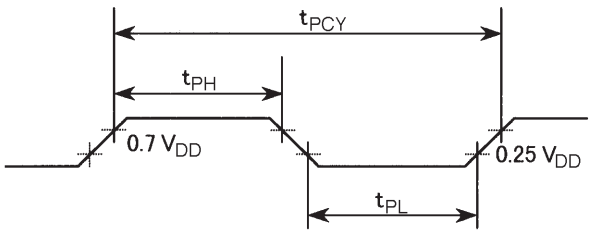
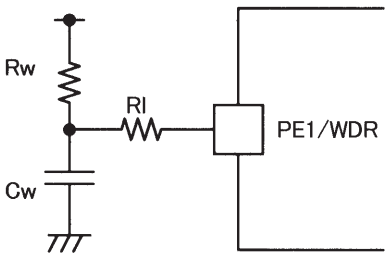


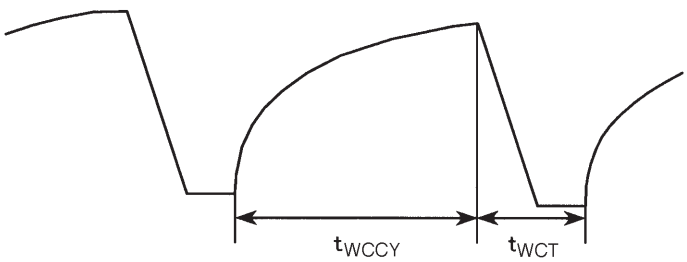
Figure 5 Serial I/O Timing



The load conditions are the same as those in figure 4.

Figure 6 Port PE0 Pulse Output Timing





t_{WCCY}: The charge time due to the time constant of the circuit consisting of the external components Cw, Rw, and RI.
t_{WCT}: The discharge time due to software processing.

Figure 7 Watchdog Timer Waveform

LC651154L, 651152L

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Applicable pins and notes	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Allowed up to the generated voltage.	
Input voltage	V_I (1)		OSC1 *1	–0.3 to V_{DD} + 0.3	
	V_I (2)		TEST, $\overline{RES}$, AV_+, AV_	–0.3 to V_{DD} + 0.3	
I/O voltage	V_{IO} (1)	PC0 to PC3, PD0 to PD3, PE0, 1, PF0 to PF3	Open-drain specification ports	–0.3 to +15	
	V_{IO} (2)	PC0 to PC3, PD0 to PD3, PE0, 1, PF0 to PF3	Pull-up resistor specification ports	–0.3 to V_{DD} + 0.3	
	V_{IO} (3)	PA0 to PA3, PG0 to PG3		–0.3 V_{DD} + 0.3	
Peak output current	I_{OP}		I/O ports	–2 to +20	mA
Average output current	I_{OA}	Per single pin, averaged over 100 ms	I/O ports	–2 to +20	
	ΣI_{OA} (1)	The total current for PC0 to PC3, PD0 to PD3, and PE0 to PE1 *2	PC0 to PC3 PD0 to PD3 PE0 to PE1	–15 to +100	
	ΣI_{OA} (2)	The total current for PF0 to PF3, PG0 to PG3, and PA0 to PA3 (See note 2.) *2	PF0 to PF3 PG0 to PG3 PA0 to PA3	–15 to +100	
Allowable power dissipation	Pd max (1)	Ta = –40 to +85°C (DIP package)		310	mW
	Pd max (2)	Ta = –40 to +85°C (MFP package)		220	
	Pd max (3)	Ta = –40 to +85°C (SSOP package)		160	
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.2 to 6.0 V (Unless otherwise specified.)

Parameter	Symbol	Conditions	Applicable pins and notes	Ratings			Unit
				min	typ	max	
Operating supply voltage	V_{DD}		V_{DD}	2.2		6.0	V
Standby supply voltage	V_{ST}	RAM and register values retained*3	V_{DD}	1.8		6.0	
High-level input voltage	V_{IH} (1)	Output n-channel transistors off	Ports C, D, E, and F with open-drain specifications	0.7 V_{DD}		13.5	
	V_{IH} (2)	Output n-channel transistors off	Ports C, D, E, and F with pull-up resistor specifications	0.7 V_{DD}		V_{DD}	
	V_{IH} (3)	Output n-channel transistors off	Port A, G	0.7 V_{DD}		V_{DD}	
	V_{IH} (4)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with open-drain specifications	0.8 V_{DD}		13.5	
	V_{IH} (5)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with pull-up resistor specifications	0.8 V_{DD}		V_{DD}	
	V_{IH} (6)	V_{DD} = 1.8 to 6.0 V	$\overline{RES}$	0.8 V_{DD}		V_{DD}	
	V_{IH} (7)	External clock specifications	OSC1	0.8 V_{DD}		V_{DD}	
Low-level input voltage	V_{IL} (1)	Output n-channel transistors off	Port	V_{SS}		0.2 V_{DD}	
	V_{IL} (2)	Output n-channel transistors off	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.15 V_{DD}	
	V_{IL} (3)	Output n-channel transistors off	OSC1	V_{SS}		0.15 V_{DD}	
	V_{IL} (4)		TEST	V_{SS}		0.2 V_{DD}	
	V_{IL} (5)		$\overline{RES}$	V_{SS}		0.15 V_{DD}	

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Parameter	Symbol	Conditions	Applicable pins and notes	Ratings			Unit
				min	typ	max	
Operating frequency (cycle time)	fop (Tcyc)	The clock may have a frequency up to 4.16 MHz when the divide-by-four internal divider circuit option is used.		200 (20)		1040 (3.84)	kHz (µs)
External clock conditions		Figure 1.					
Frequency	text	Either the divide-by-three or divide-by-four internal divider circuit must be used if the clock frequency exceeds 1.040 MHz.	OSC1	200		4160	kHz
Pulse width	textH, textL		OSC1	100			ns
Rise and fall times	textR, textF		OSC1			100	ns
Recommended oscillator circuit constants							
Two-pin RC oscillator	Cext	Figure 2	OSC1, OSC2		270 ±5%		pF
	Rext				12 ±1%		kΩ
Ceramic oscillator *4		Figure 3			See table 1.		

Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.2 to 6.0 V (Unless otherwise specified.)

Parameter	Symbol	Conditions	Applicable pins and notes	Ratings			Unit
				min	typ	max	
High-level input current	I_{IH} (1)	• Output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = 13.5 V	Ports C, D, E and F with the open-drain specifications			5.0	µA
	I_{IH} (2)	• Output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = V_{DD}	Ports A and G with the open-drain specifications			1.0	
	I_{IH} (3)	When an external clock is used, V_{IN} = V_{DD}	OSC1			1.0	
Low-level input current	I_{IL} (1)	• Output n-channel transistors off • V_{IN} = V_{SS}	Ports with the open-drain specifications	–1.0			
	I_{IL} (2)	• Output n-channel transistors off • V_{IN} = V_{SS}	Ports with the pull-up resistor specifications	–1.3	–0.35		mA
	I_{IL} (3)	V_{IN} = V_{SS}	$\overline{RES}$	–45	–10		µA
	I_{IL} (4)	When an external clock is used, V_{IN} = V_{SS}	OSC1	–1.0			
High-level output voltage	V_{OH}	• I_{OH} = –10 µA	Ports with the pull-up resistor specifications	V_{DD} – 0.5			V
Low-level output voltage	V_{OL} (1)	• I_{OL} = 3 mA	Port			1.5	
	V_{OL} (2)	When I_{OL} = 1 mA and the I_{OL} for each port is 1 mA or less.	Port			0.4	
Schmitt characteristics: Hysteresis voltage	V_{HIS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, and OSC1 with Schmitt specifications*5		0.1 V_{DD}		
Schmitt characteristics: High-level threshold voltage	V_{tH}			0.4 V_{DD}		0.8 V_{DD}	
Schmitt characteristics: Low-level threshold voltage	V_{tL}			0.2 V_{DD}		0.6 V_{DD}	
Current drain *6 Two-pin RC oscillator	IDDOP (1)	• Operating, with the output n-channel transistors off • With the ports at V_{DD} • Figure 2, fosc = 800 kHz (typical)	V_{DD}		1.0	4	mA
Ceramic oscillator	IDDOP (2)	• Figure 3, 4 MHz, divide-by-four circuit used	V_{DD}		1.5	4	
	IDDOP (3)	• Figure 3, 4 MHz, divide-by-four circuit used V_{DD} = 2.2 V	V_{DD}		0.5	1	
	IDDOP (4)	• Figure 3, 400 kHz	V_{DD}		1.0	2.5	
	IDDOP (5)	• Figure 3, 800 kHz	V_{DD}		1.5	4	
External clock	IDDOP (6)	• 200 kHz to 1024 kHz, no divider circuit • 600 kHz to 3120 kHz, divide-by-three circuit used • 800 kHz to 4160 kHz, divide-by-four circuit used	V_{DD}		1.5	4	
Standby mode	IDDst	Output n-channel transistors off, V_{DD} = 6 V	V_{DD}		0.05	10	µA
		Ports at V_{DD}, V_{DD} = 2.2 V	V_{DD}		0.020	4	

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Parameter	Symbol	Conditions	Applicable pins and notes	Ratings			Unit
				min	typ	max	
Oscillator characteristics Ceramic oscillator Oscillator frequency	f_{CFOSC}*7	• Figure 3, fo = 400 kHz • Figure 3, fo = 800 kHz • Figure 3, fo = 1 MHz • Figure 3, fo = 4 MHz, with the divide-by-four circuit used.	OSC1, OSC2 OSC1, OSC2 OSC1, OSC2 OSC1, OSC2	392 784 980 3920	400 800 1000 4000	408 816 1020 4080	kHz
Oscillator stabilization time *8	t_{CFS}	• Figure 4, fo = 400 kHz • Figure 4, fo = 800 kHz, 1 MHz, or 4 MHz, with the divide-by-four circuit used.				10 10	ms
Two-pin RC oscillator Oscillator frequency	f_{MOSC}	• Figure 2, Cext = 270 pF ±5% • Figure 2, Rext = 5.6 kΩ ±1%	OSC1, OSC2	290	400	841	kHz
Pull-up resistor I/O ports	RPP	• Output n-channel transistors off • $V_{IN} = V_{SS}$, V_{DD} = 5 V	Pull-up resistor specification ports	8	14	30	kΩ
$\overline{RES}$	Ru	$V_{IN} = V_{SS}$, V_{DD} = 5 V	$\overline{RES}$	200	500	800	
External reset characteristics Reset time	t_{RST}				See figure 5.		
Pin capacitances	Cp	• f = 1 MHz • With all pins other than the pin being tested at $V_{IN} = V_{SS}$.			10		pF
Serial clock Input clock cycle time	t_{CKCY} (1)	Figure 6	$\overline{SCK}$	2.0			µs
Output clock cycle time	t_{CKCY} (2)	Figure 6	$\overline{SCK}$		$64 \times T_{CYC}$*9		
Input clock low-level pulse width	t_{CKL} (1)	Figure 6	$\overline{SCK}$	2.0			
Output clock low-level pulse width	t_{CKL} (2)	Figure 6	$\overline{SCK}$		$32 \times T_{CYC}$		
Input clock high-level pulse width	t_{CKH} (1)	Figure 6	$\overline{SCK}$	2.0			
Output clock high-level pulse width	t_{CKH} (2)	Figure 6	$\overline{SCK}$		$32 \times T_{CYC}$		
Serial input Data setup time	t_{ICK}	• Stipulated with respect to the rising edge of $\overline{SCK}$. • Figure 6	SI	0.5			
Data hold time	t_{CKI}		SI	0.5			
Serial output Output delay time	t_{CKO}	• Stipulated with respect to the falling edge of $\overline{SCK}$. • With an external resistor of 1 kΩ and an external capacitor of 50 pF on only the n-channel open-drain pins. • Figure 6	SO			1.0	
Pulse output function Period	t_{PCY}	• Figure 7 • TCYC = 4 × system clock period • With an external resistor of 1 kΩ and an external capacitor of 50 pF on only the n-channel open-drain pins.	PE0		$64 \times T_{CYC}$		
High-level pulse width	t_{PH}		PE0		$32 \times T_{CYC}$ ±10%		
Low-level pulse width	tPL		PE0		$32 \times T_{CYC}$ ±10%		

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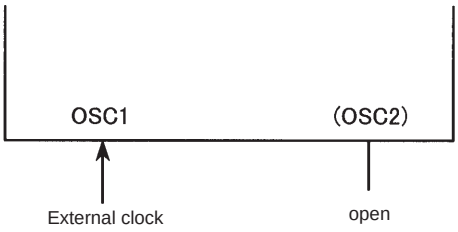
Parameter		Symbol	Conditions		Applicable pins and notes	Ratings			Unit
						min	typ	max	
A/D converter characteristics	Resolution			V_{DD} = 3 to 6 V			8		bit
	Absolute precision		$AV_+ = V_{DD}$ $AV_- = V_{SS}$				±1	±2	LSB
	Conversion time	TCAD	When the A/D converter speed is normal (1/1), namely $26 \times T_{CYC}$			99 (T_{CYC} = 3.84 µs)		312 (T_{CYC} = 12 µs)	µs
			When the A/D converter speed is one half (1/2), namely $51 \times T_{CYC}$			195 (T_{CYC} = 3.84 µs)		612 (T_{CYC} = 12 µs)	
	Input reference voltage	AV_+			AV_+	AV_-		V_{DD}	V
		AV_-			AV_-	V_{SS}		AV_+	
	Input reference current range	I_{RIF}	$AV_+ = V_{DD}$ $AV_- = V_{SS}$		AV_+, AV_-	200	500	800	µA
	Analog input voltage range	V_{AIN}			AD0 to AD7	AV_-		AV_+	V
	Analog port input current	I_{AIN}	Including the output off leakage current. $V_{AIN} = V_{DD}$		AD0 to AD7 (The I/O shared function ports have open-drain specifications.)			1	µA
			$V_{AIN} = V_{SS}$			–1			
Watchdog timer	Recommended constants*10	Cw	When PE1 has the open-drain specifications.	V_{DD} = 2.2 to 6 V	WDR		0.1 ±5%		µF
		Rw	When PE1 has the open-drain specifications.		WDR		680 ±1%		kΩ
		RI	When PE1 has the open-drain specifications.		WDR		100 ±1%		Ω
	Clear time (discharge)	t_{WCT}	Figure 8		WDR	100			µs
	Clear period (charge)	t_{WCCY}	Figure 8		WDR	31			ms
	Recommended constants*10	Cw	When PE1 has the open-drain specifications.	V_{DD} = 2.2 to 6 V	WDR		0.047 ±5%		µF
		Rw	When PE1 has the open-drain specifications.		WDR		680 ±1%		kΩ
		RI	When PE1 has the open-drain specifications.		WDR		100 ±1%		Ω
	Clear time (discharge)	t_{WCT}	Figure 8		WDR	40			µs
	Clear period (charge)	t_{WCCY}	Figure 8		WDR	14			ms

Notes:
1. Allowed up to the amplitude generated when the oscillator shown in figure 3 is used with the recommended circuit constants and driven by the IC.
2. The average over a 100 ms period.
3. The operating V_{DD} supply voltage must be maintained from the point the HALT instruction is executed until the IC has fully entered the standby state. Applications must also assure that no chattering occurs on the PA3 pin during the HALT instruction execution cycle.
4. Recommended circuit constants that have been verified to oscillate stably according to the oscillator element manufacturer using the Sanyo-stipulated oscillator characteristics evaluation board.
5. The OSC1 pin will have Schmitt characteristics when external clock oscillator is selected with the two-pin RC oscillator option.
6. These are the results of testing using our (Sanyo's) characteristics evaluation board with the recommended circuit constants used as external components. The current flowing in the IC's output transistors and transistors that have pull-up resistors is not included.
7. f_{CFOSC} is the frequency when the recommended circuit constants from table 1 are used as external components.
8. Indicates the time required to achieve stable oscillation from the point V_{DD} rises above the lower limit of the operating voltage range (See figure 4).
9. $T_{CYC} = 4 \times$ the system clock period
10. If the application could be used in an environment in which condensation is possible, extra care with respect to the leakage between PE1 and adjacent pins and leakage associated with external resistors and capacitor is required during design.



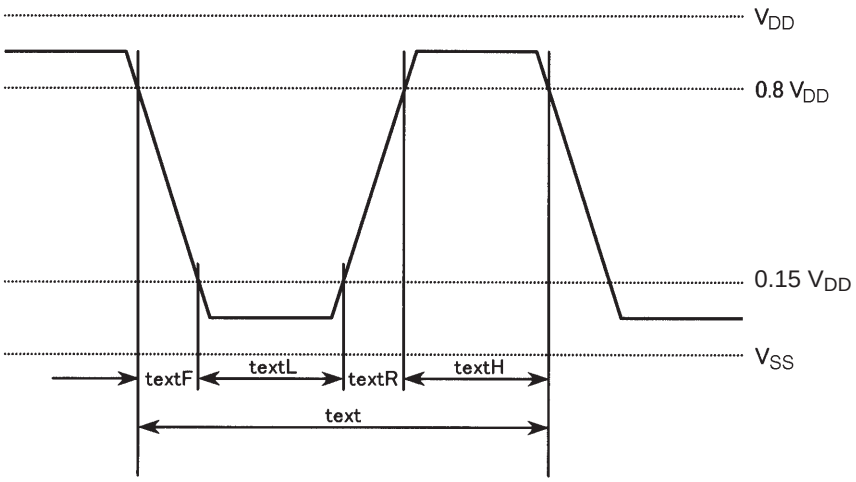


Figure 1 External Clock Input Waveform

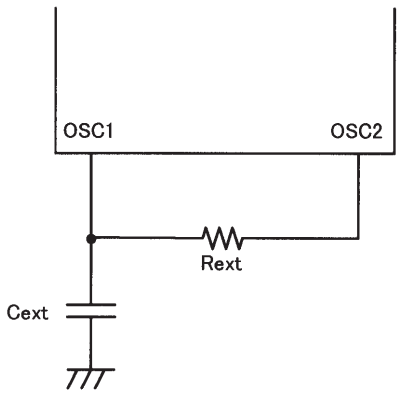


Figure 2 Two-Pin RC Oscillator Circuit

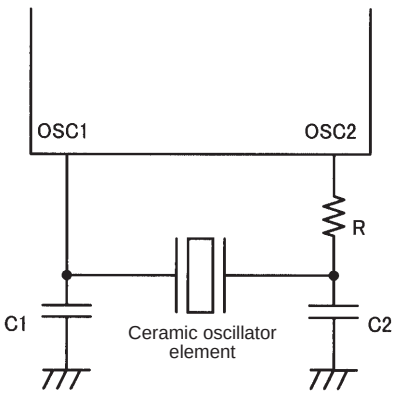


Figure 3 Ceramic Oscillator Circuit

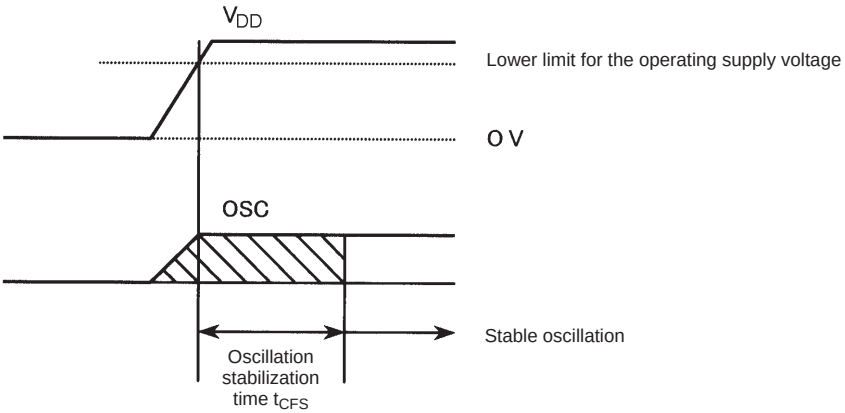


Figure 4 Oscillation Stabilization Time

Table 1 Recommended Ceramic Oscillator Circuit Constants

4 MHz (Murata Mfg. Co., Ltd.)	C1	33 pF ±10%
CSA4.00MG	C2	33 pF ±10%
CST4.00MGW (Internal capacitor)	R	0 Ω
4 MHz (Kyocera Corporation)	C1	33 pF ±10%
KBR4.0MSA	C2	33 pF ±10%
KBR4.0MKS (Internal capacitor)	R	0 Ω
1 MHz (Murata Mfg. Co., Ltd.)	C1	100 pF ±10%
CSB1000J	C2	100 pF ±10%
	R	3.3 kΩ
800 kHz (Murata Mfg. Co., Ltd.)	C1	100 pF ±10%
CSB800J	C2	100 pF ±10%
	R	3.3 kΩ
400 kHz (Murata Mfg. Co., Ltd.)	C1	220 pF ±10%
CSB400P	C2	220 pF ±10%
	R	3.3 kΩ

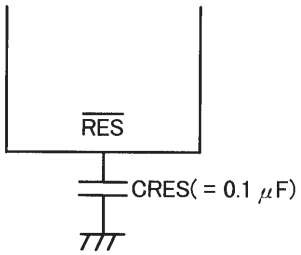


Figure 5 Reset Circuit

Note: If the power supply rise time is zero, the reset time when CRES = 0.1 μF will be between 10 and 100 ms.
If the power supply rise time is long, increase the value of CRES so that the reset time is at least 10 ms.

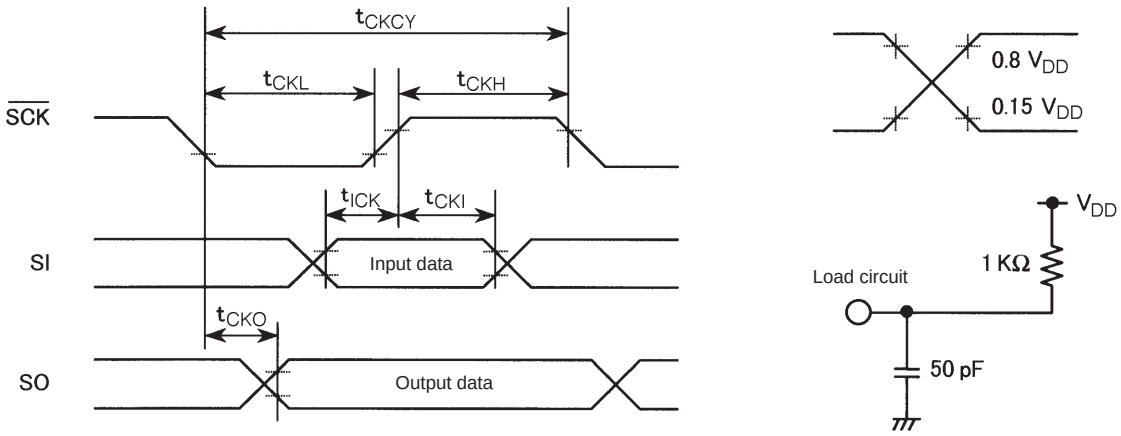
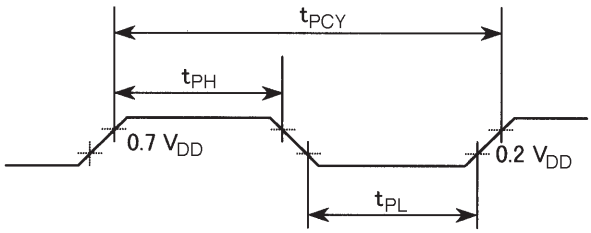
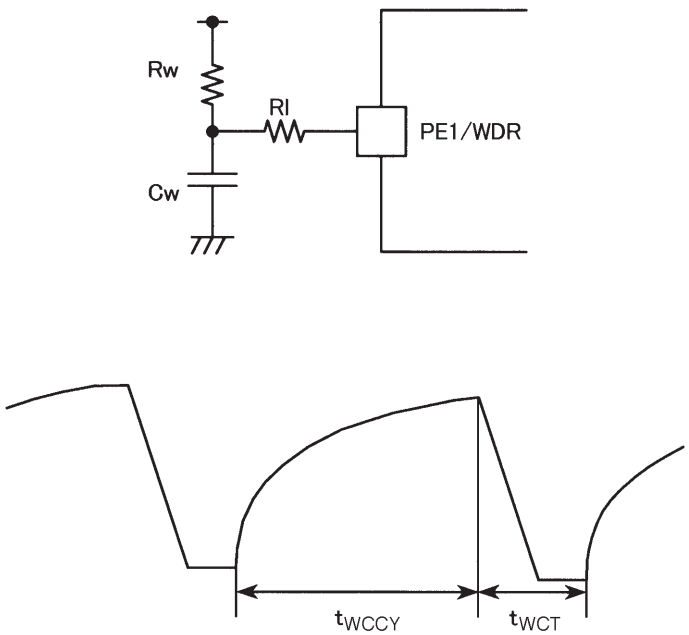


Figure 6 Serial I/O Timing



The load conditions are the same as those in figure 5.

Figure 7 Port PE0 Pulse Output Timing



t_{WCCY}: The charge time due to the time constant of the circuit consisting of the external components Cw, Rw, and Rl.
t_{WCT}: The discharge time due to software processing.

Figure 8 Watchdog Timer Waveform

RC Oscillator Characteristics for the LC651154L and LC651152L

Figure 9 shows the RC oscillator characteristics for the LC651154L and LC651152L.
However, the sample-to-sample variation in the LC651154L and LC651152L RC oscillator frequency described below does occur.

1) When:
   V_{DD} = 2.2 to 6.0 V, Ta = –40 to +85°C
   External constants: Cext = 270 pF
   Rext = 12.0 kΩ
   f_{MOSC} will be:
   290 kHz ≤ f_{MOSC} ≤ 841 kHz
   Therefore, only the above circuit constants are recommended.

   If use of circuit constants other than the above is unavoidable, they must be in the following ranges.
   Cext = 150 to 390 pF
   Rext = 3 to 20 kΩ
   (See figure 9.)

Note 8. The oscillator frequency must be in the range 350 to 850 kHz when V_{DD} = 5.0 V and Ta = 25°C.
Note 9. Applications must be designed to have adequate margins so that the oscillator frequency falls in the operating clock frequency range (see the oscillator divider option table) for the voltage range V_{DD} = 2.2 to 6.0 V and for the temperature range Ta = –40 to 85°C.

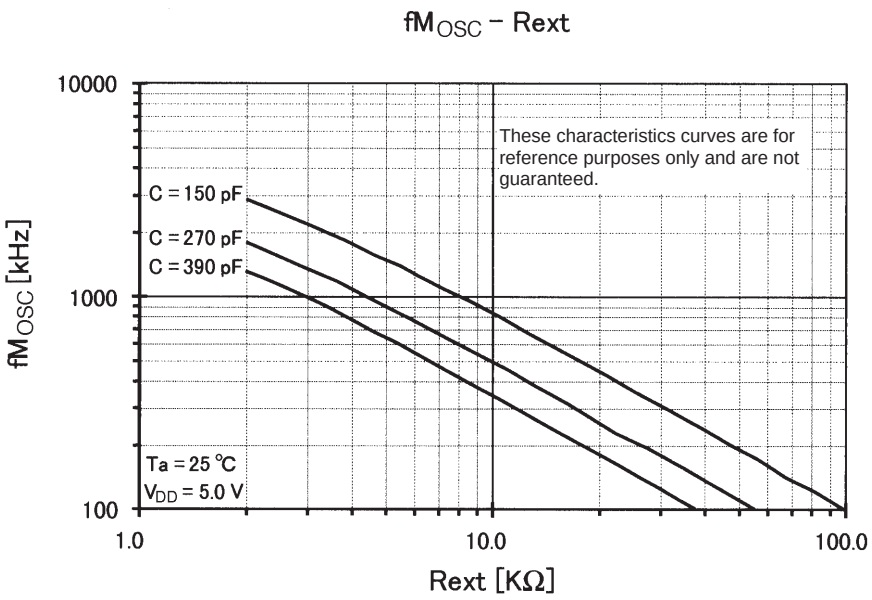
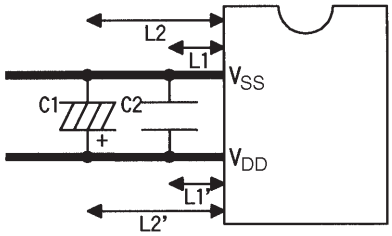


Figure 9 RC Oscillator Frequency Data (Representative Values)

Notes on Printed Circuit Board Design

This section describes points that require care concerning noise from the point of view of the microcontroller and presents means of preventing associated problems when designing a printed circuit board to use with these products in a mass produced end product. The ideas presented in this section are effective design techniques for preventing and avoiding problems (such as incorrect microcontroller operation and program failures) due to noise.

1. The V_{DD} and V_{SS} power supply pins
   Insert capacitors that meet the following conditions between the V_{DD} and V_{SS} power supply pins.
   - The lengths of the lines between the V_{DD} and V_{SS} pins and the capacitors C1 and C2 should be as close to exactly equal as possible (L1 = L1', L2 = L2'). Furthermore, these distances should be as short as possible.
   - Insert two capacitors, C1 and C2 in parallel, with C1 having a large capacitance and C2 having a small capacitance.
   - The V_{DD} and V_{SS} lines in the printed circuit board pattern should be wider than any other lines in the pattern.



2. The OSC1 and OSC2 clock I/O pins
   — If the ceramic oscillator option is selected (See figure 2-1.)
   - Keep the lines between the clock I/O pins (input: OSC1, output: OSC2) and the external components as short as possible (the distance Losc in the figure).
   - Make the length of the lines (Lvss + L1 and Lvss + L2) from the microcontroller V_{SS} pin to the V_{SS} side of the capacitors connected to the oscillator element as short as possible.
   - V_{SS} line for the oscillator circuit and other V_{SS} line should branch from a point nearest to the V_{SS} pin.
   - Due to the capacitances of the wiring on the printed circuit board, it may be necessary to modify the values of the oscillator circuit constants (including the values of the capacitors C1 and C2 and the limiting resistor Rd) from the values presented in this catalog. We recommend consulting the manufacturer of the oscillator element with regard to these circuit constants.

   — If the 2-pin RC oscillator option is selected (Figure 2-2)
   - Keep the lines between the clock I/O pins (input: OSC1, output: OSC2) and the external components (the capacitor Cext and the resistor Rext) as short as possible (the distance Losc in the figure).
   - Make the length of the lines (Lvss + Lc) from the microcontroller V_{SS} pin to the V_{SS} side of the capacitor functioning as the oscillator element as short as possible.
   - Take the V_{SS} used by the oscillator circuit (as well as other V_{SS} usages) from a point as close as possible to the V_{SS} pin.

   — If the external oscillator option is selected (Figure 2-3)
   - Keep the line between the clock input pin (OSC1) and the external oscillator circuit as short as possible (the distance Losc in the figure).
   - Leave the clock output pin (OSC2) open.
   - Make the length (Losc) of the lines to the V_{DD} and V_{SS} pins used by the external oscillator as short as possible.

   — Other points that apply to all oscillator circuits:
   - Keep all lines that carry signals that change rapidly, signals that have large amplitudes due to being connected to the medium-voltage handling capacity ports, or signals that carry large currents as far away from the oscillator circuit as possible. Also, do not allow such signal lines to cross any clock-signal related lines.

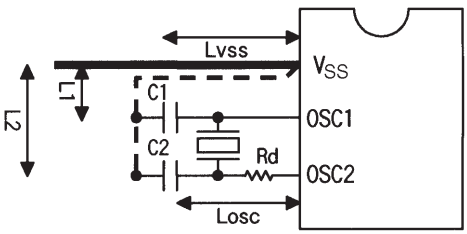


Figure 2-1 Sample Oscillator Circuit 1 (Ceramic oscillator)

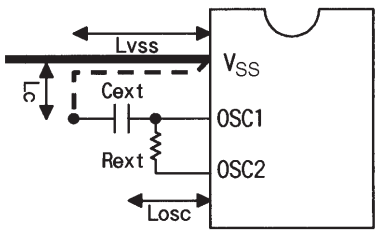


Figure 2-2 Sample Oscillator Circuit 2 (2-pin RC oscillator)

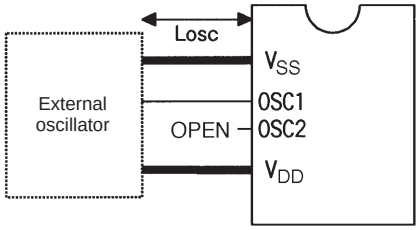


Figure 2-3 Sample Oscillator Circuit 3 (External oscillator)

3. RES: Reset pin
   - Keep the length of lines (Lres in the figure) from the $\overline{RES}$ pin to external circuits as short as possible.
   - Keep the length of the lines (L1 and L2) to the capacitor (Cres) inserted between $\overline{RES}$ and V_{SS} as short as possible.

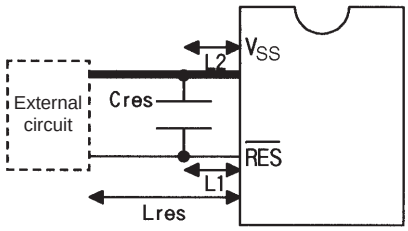


Figure 3 $\overline{RES}$ Pin Wiring

4. TEST: Test pin
   - Keep the length of the line (L) from the TEST pin to the V_{SS} pin as short as possible.
   - Run the line from the TEST pin to the V_{SS} pin as close to the V_{SS} pin as possible.

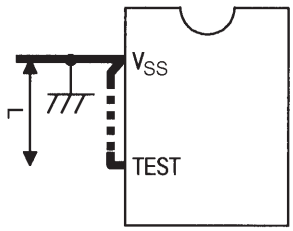


Figure 4 TEST Pin Wiring

5. AD0 to AD7: Analog input pins
   Analog input pin lines, such as those used to connect to an A/D converter input pin or a comparator input pin should be connected so as to meet the following conditions.
   - Keep the line (L1) between the limiting resistor (Rl) and the analog input pin as short as possible.
   - Locate the capacitor inserted between the analog input pins and the AV- pin (the A/D converter reference voltage input pin) as close as possible to the AV- input pin. That is, make the line length L1 + L2 as short as possible.

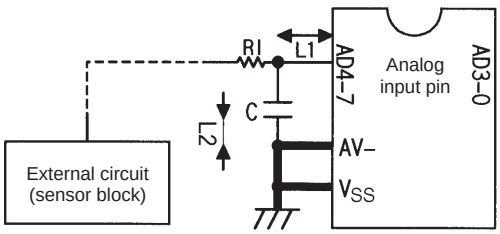


Figure 5 Analog Input Pin Wiring

6. I/O pins
   All of the pins on these products function as both input and output pins.
   - When used as an input pin, insert a limiting resistor, and keep the length of the line to that pin as short as possible.
     Supplement: This is not only useful in printed circuit board design, but is also useful in preventing and avoiding problems (such as incorrect microcontroller operation and program failures) by taking the program specifications and microcontroller option selections described below into consideration.
   - If signals are input from external sources when the microcontroller power supply is unstable, select the medium-voltage handling capacity (n-channel open drain) output as the output type option for that input pin, and also insert a limiting resistor in the input circuit.
   - Always implement key chattering exclusion measures for external signals applied to microcontroller input pins.
   - The pin output data should be re-output periodically with an output instruction (OP or SPB).

- When reading data input to a pin that can function as either input or output, set the output value for that pin to 1 every time the input is read using an output instruction (OP or SPB).

7. Unused pins
   - See the users manual for the product or refer to the pin functions as described in the semiconductor report for the device.