

LH5116S

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time: 1000 ns (MAX.)
- Low-power consumption:
 - Operating: 33 mW (MAX.)
 - Standby: 3.3 μW (MAX.)
- Fully-static operation
- Three-state outputs
- Single +3 V power supply
- Package: 24-pin, 450-mil SOP

DESCRIPTION

The LH5116S is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It operates at a low supply voltage of 3 V ±10%.

PIN CONNECTIONS

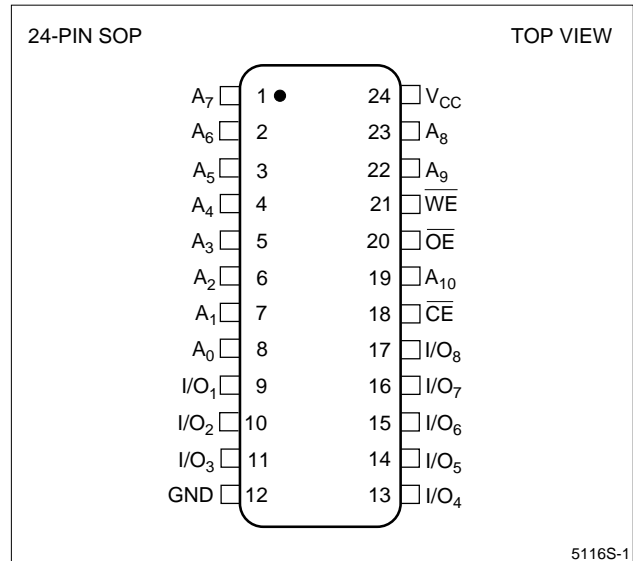


Figure 1. Pin Connections for SOP Package

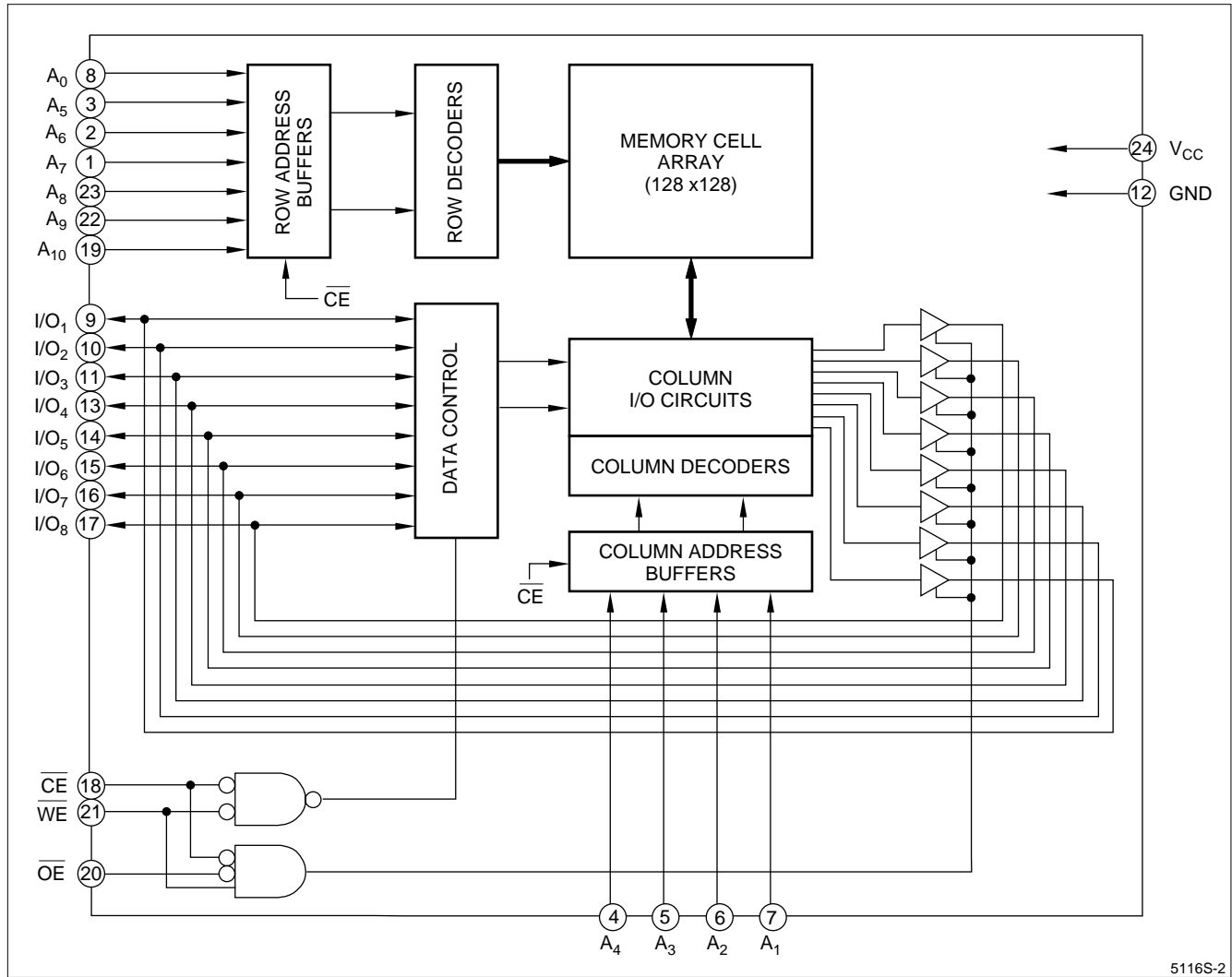


Figure 2. LH5116S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₀	Address input
CE	Chip Enable input
OE	Output Enable input
WE	Write Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data input/output
V _{CC}	Power supply
GND	Ground

TRUTH TABLE

\overline{CE}	\overline{OE}	\overline{WE}	MODE	I/O ₁ - I/O ₈	SUPPLY CURRENT	NOTE
L	X	L	Write	D _{IN}	Operating (I _{CC})	1
L	L	H	Read	D _{OUT}	Operating (I _{CC})	
H	X	X	Deselect	High-Z	Standby (I _{SB})	1
L	H	X	Output disable	High-Z	Operating (I _{CC})	1

NOTE:
 1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} +0.3	V	1
Operating temperature	T _{opr}	0 to +50	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +50°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	2.7	3.0	3.3	V
Input voltage	V _{IH}	2.2		V _{CC} + 0.3	V
	V _{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 3 V ±10%, T_A = 0 to +50°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output 'LOW' voltage	V _{OL}	I _{OL} = 2.1 mA			0.5	V	
Output 'HIGH' voltage	V _{OH}	I _{OH} = -1.0 mA	V _{CC} - 0.5			V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}	-1.0		1.0	μA	
Output leakage current	I _{LO}	CE = V _{IH} , V _{I/O} = 0 V to V _{CC}	-1.0		1.0	μA	
Operating current	I _{CC1}	Outputs open (OE = V _{CC})		8	10	mA	1
	I _{CC2}	Outputs open (OE = V _{IH})		8	10	mA	2
Standby current	I _{CCL}	CE ≥ V _{CC} - 0.2 V All other input pins = 0 V to V _{CC}			1.0	μA	

NOTES:

1. CE = 0 V; all other input pins = 0 V to V_{CC}
2. CE = V_{IL}; all other input pins = V_{IL} to V_{IH}

AC CHARACTERISTICS (V_{CC} = 3 V ±10%, T_A = 0 to +50°C)**(1) READ CYCLE**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t _{RC}	1000			ns	
Address access time	t _{AA}			1000	ns	
Chip enable access time	t _{ACE}			1000	ns	
Chip enable Low to output in Low-Z	t _{CLZ}	10			ns	1
Output enable access time	t _{OE}			100	ns	
Output enable Low to output in Low-Z	t _{OLZ}	10			ns	1
Chip disable to output in High-Z	t _{CHZ}	0		40	ns	1
Output enable to output in High-Z	t _{OHZ}	0		40	ns	1
Output hold time	t _{OH}	10			ns	

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

(2) WRITE CYCLE ($V_{CC} = 3\text{ V} \pm 10\%$, $T_A = 0$ to $+50^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	1000			ns	
Chip enable to end of write	t_{CW}	100			ns	
Address valid time	t_{AW}	100			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	100			ns	
Write recovery time	t_{WR}	20			ns	
\overline{WE} Low to output in High-Z	t_{WHZ}			30	ns	1
Data valid to end of write	t_{DW}	50			ns	
Data hold time	t_{DH}	20			ns	
Output active from end of write	t_{OW}	10			ns	1
Output enable to output in High-Z	t_{OHZ}	0		40	ns	1

NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a ± 200 mV transition from steady state levels into the test load.

AC TEST CONDITIONS

PARAMETER	MODE	NOTE
Input voltage amplitude	0 to V_{CC}	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load conditions	C_L (100 pF)	1

NOTE:

- Includes scope and jig capacitance.

DATA RETENTION CHARACTERISTICS ($T_A = 0$ to $+50^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE \geq V_{CCDR} - 0.2\text{ V}$	2.0			V	
Data retention current	I_{CCDR}	$CE \geq V_{CCDR} - 0.2\text{ V}$, $V_{CCDR} = 2.0\text{ V}$			1.0 0.2	μA	1
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	2

NOTES:

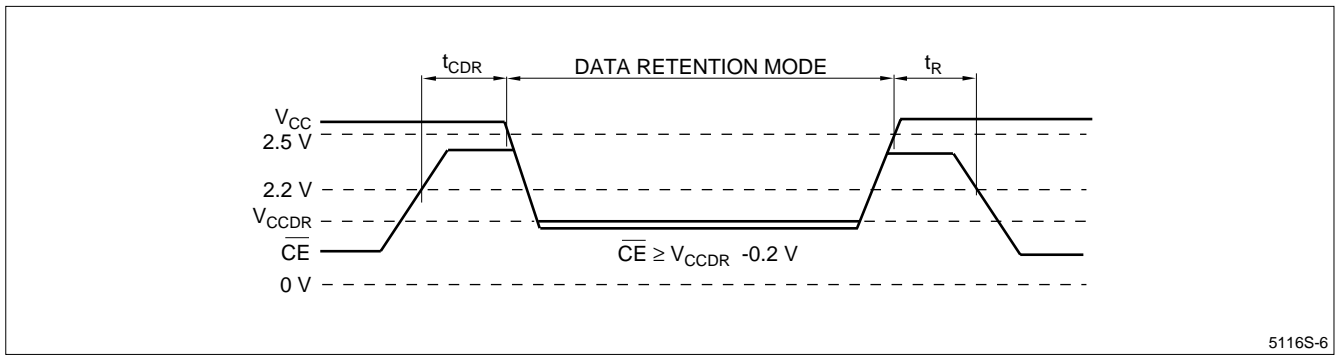
- $T_A = 25^\circ\text{C}$
- t_{RC} = Read cycle time

CAPACITANCE ¹ ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}$			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$			10	pF

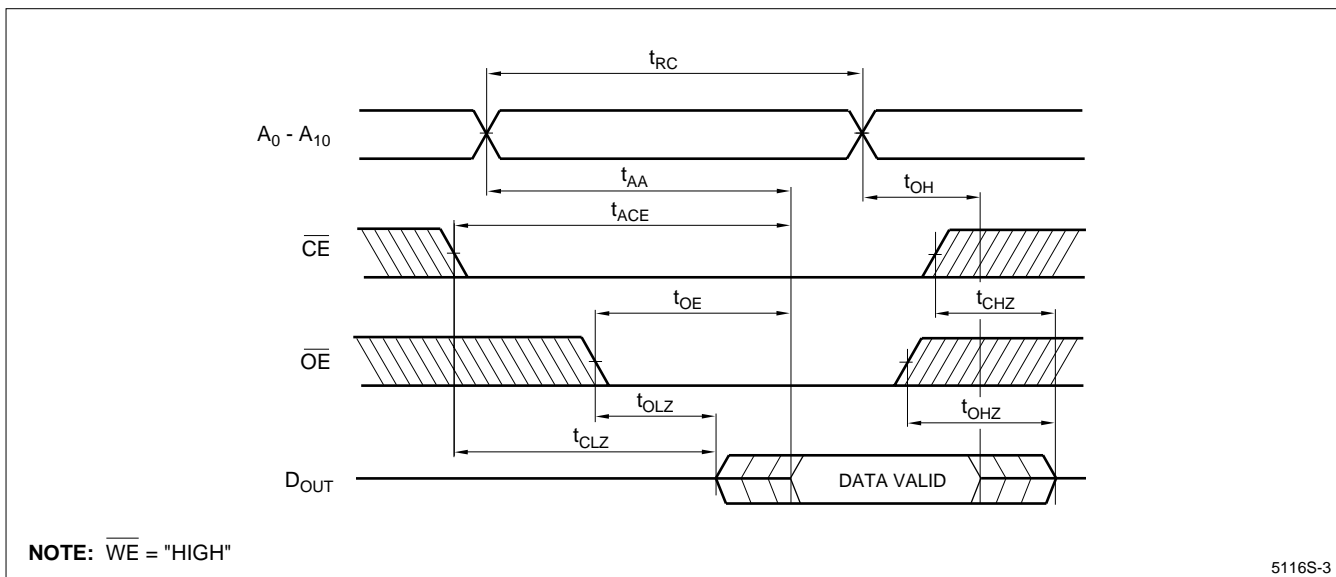
NOTE:

- This parameter is sampled and not production tested.



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Figure 3. Low Voltage Data Retention



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Figure 4. Read Cycle

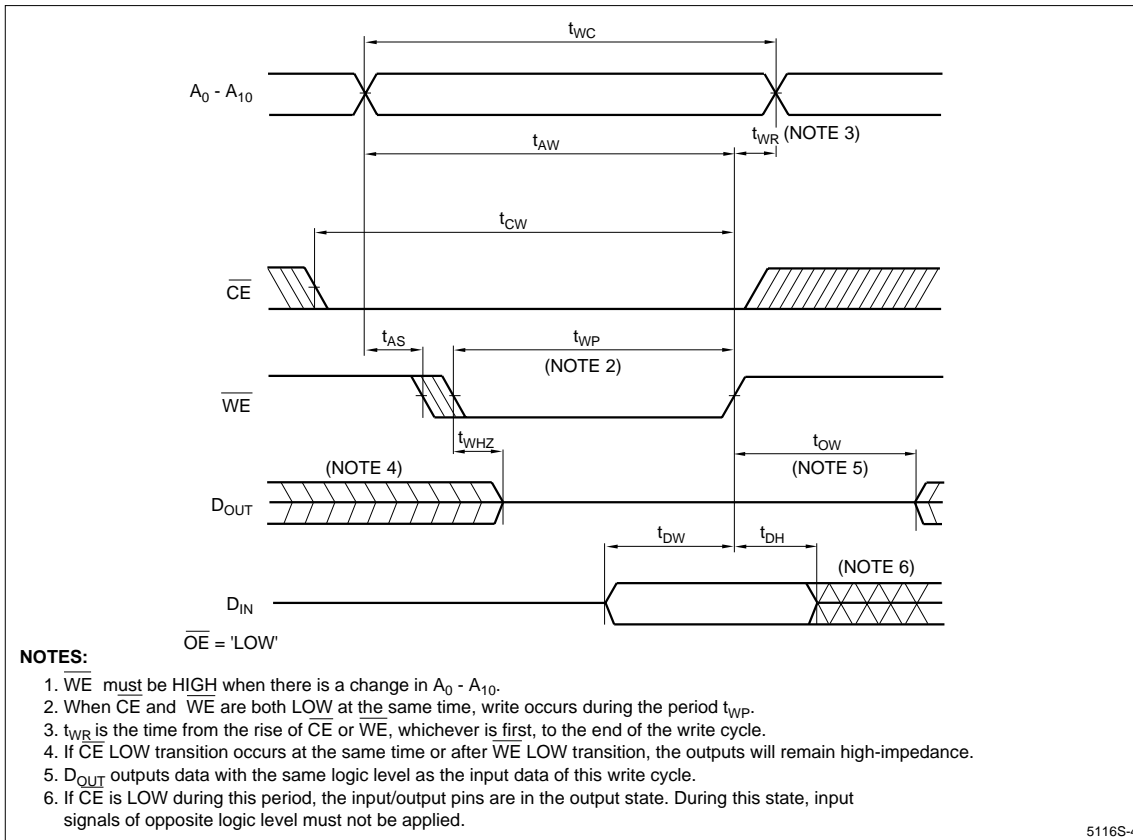


Figure 5. Write Cycle 1 (Note 1)

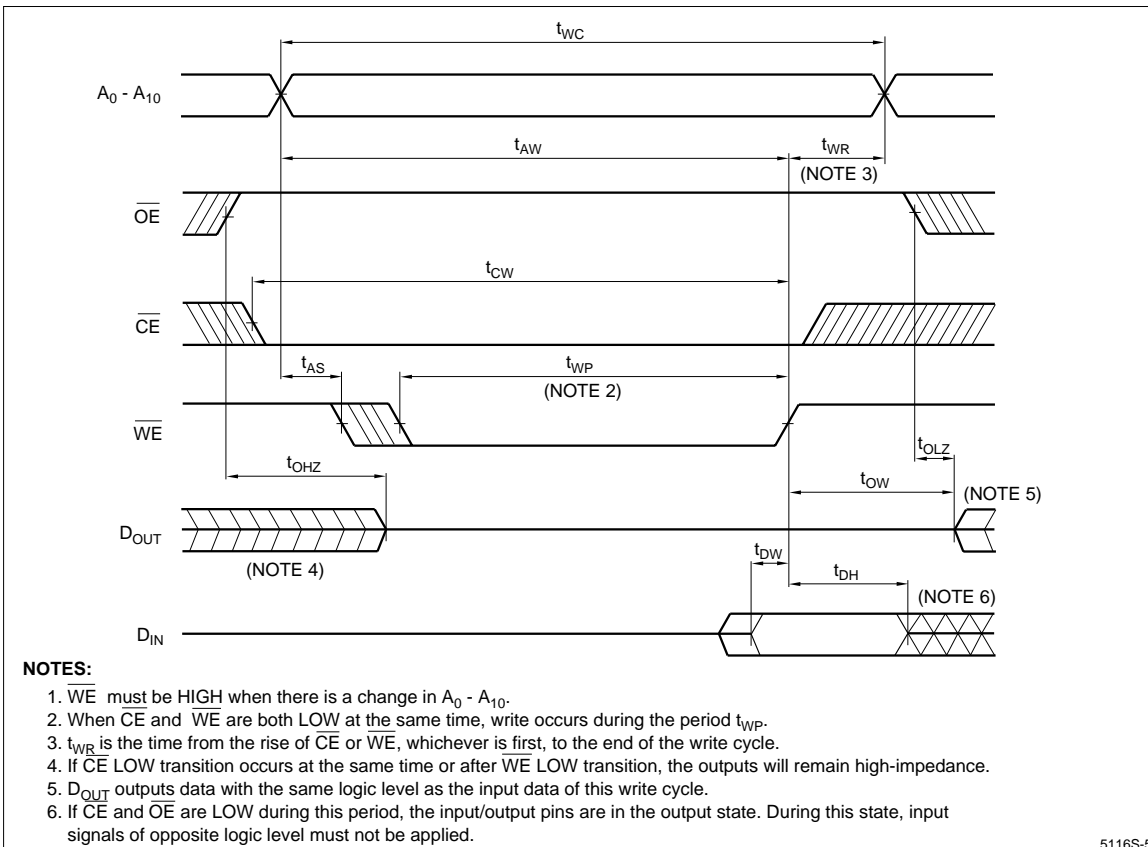
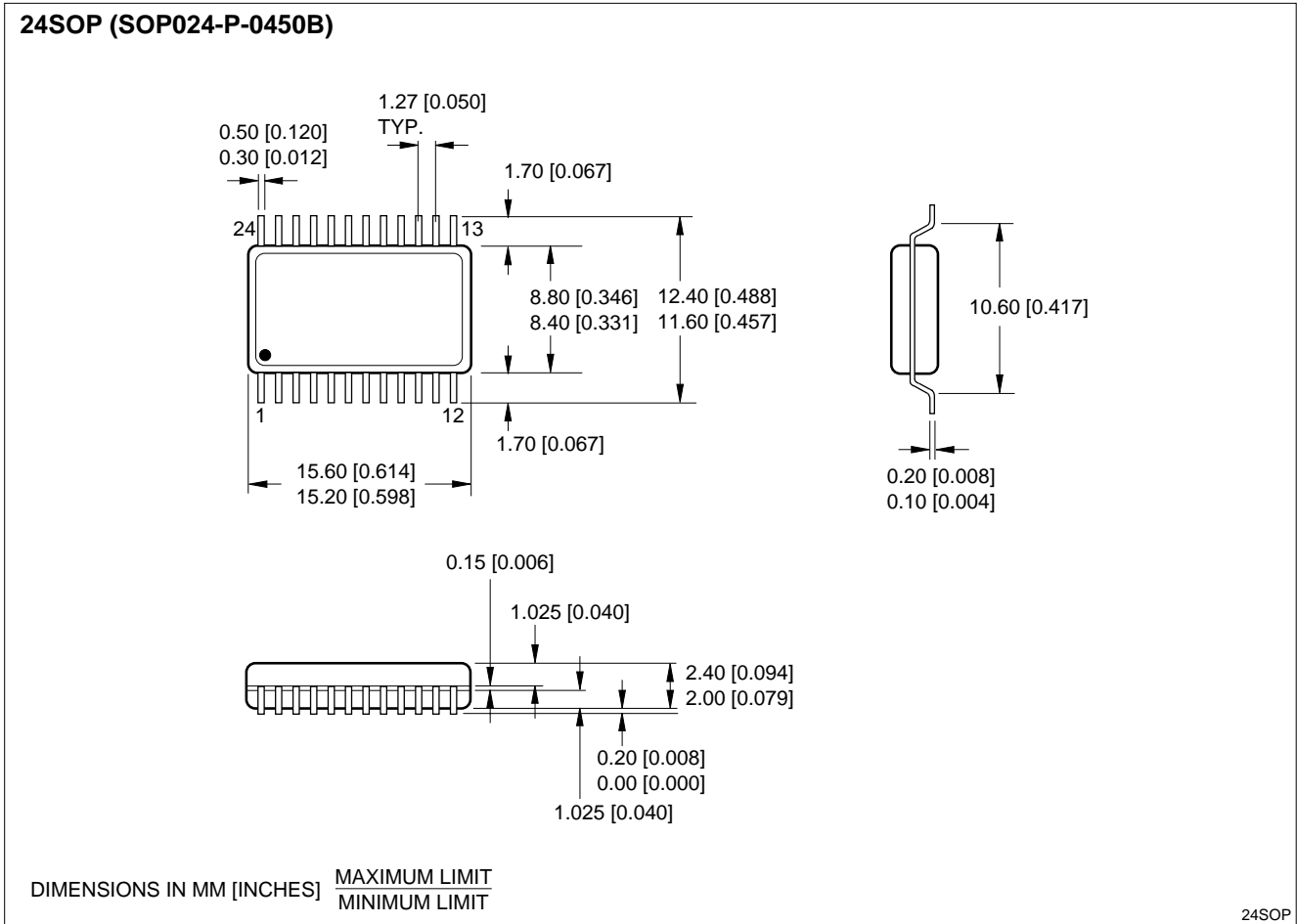


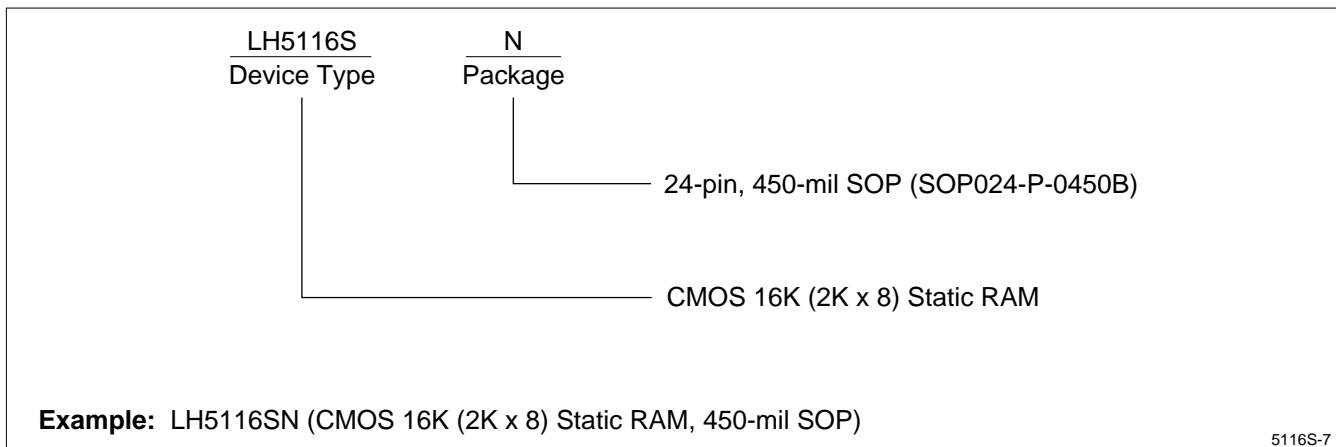
Figure 6. Write Cycle 2 (Note 1)

PACKAGE DIAGRAM



24-pin, 450-mil SOP

ORDERING INFORMATION



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