




MK74CB115 1 to 16 Buffalo™ Clock Driver

Description

The MK74CB115 Buffalo™ is a monolithic CMOS high speed clock driver. It consists of a single input to sixteen low-skew output, non-inverting clock drivers. The chip is capable of driving 16 CMOS loads up to 200 MHz with a maximum of 250 ps output to output skew. The MK74CB115 is packaged in the tiny 28 pin SSOP, which uses the same board space as the narrow 16 pin SOIC.

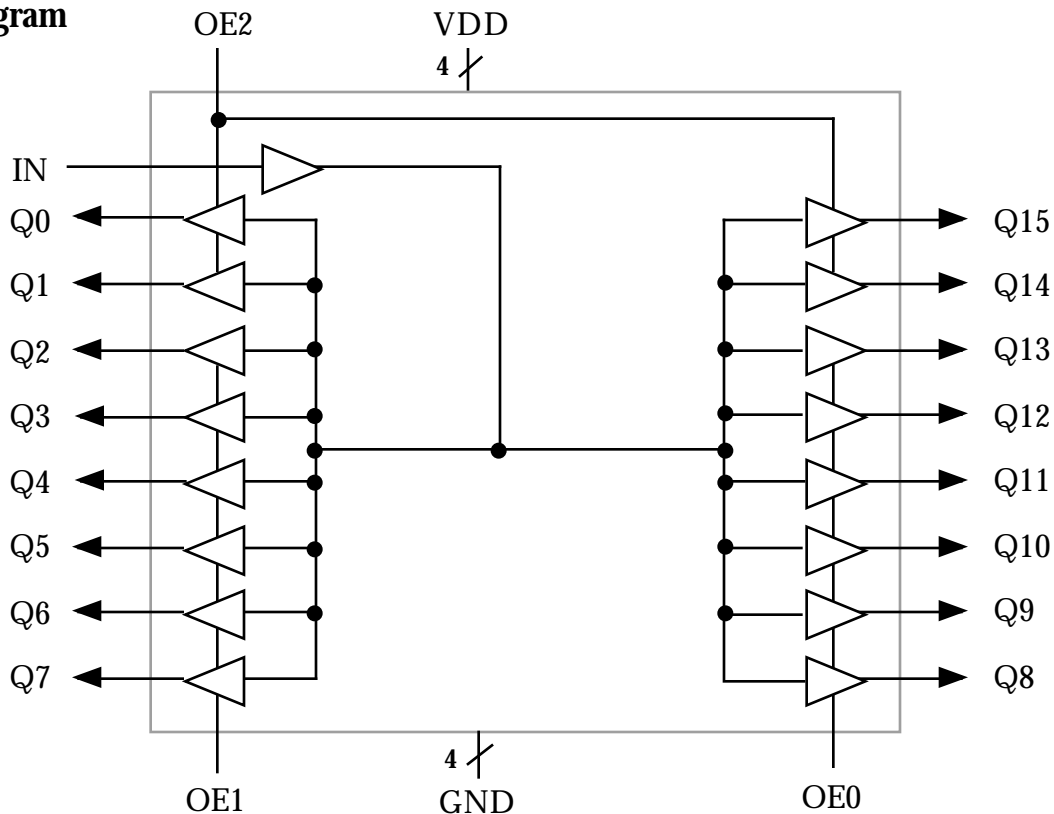
Features

- Tiny 28 pin SSOP (150 mil) package 
- One input to sixteen output clock drivers
- Outputs are skew matched to within 250 ps
- 3.3V±10% or 5V±10% supply voltage
- 3 Output Enables allow configuration as 1 to 4, 1 to 6, 1 to 10, 1 to 12 or 1 to 16 buffer
- Clock speeds up to 200 MHz

Family of ICS Parts

The MK74CB115 Buffalo™ is designed to be used with ICS's clock synthesizer devices. The inputs of the Buffalo are matched to the outputs of ICS clock synthesizers. Consult ICS for applications support.

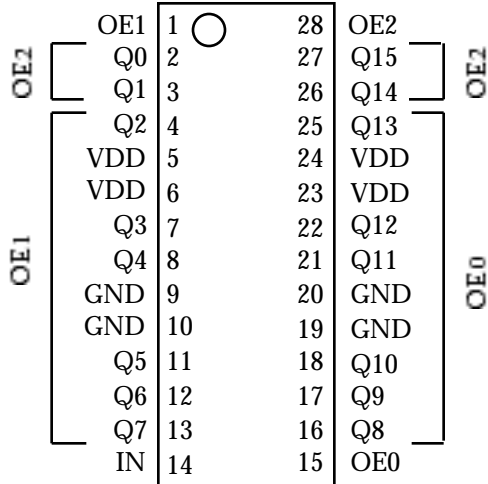
Block Diagram



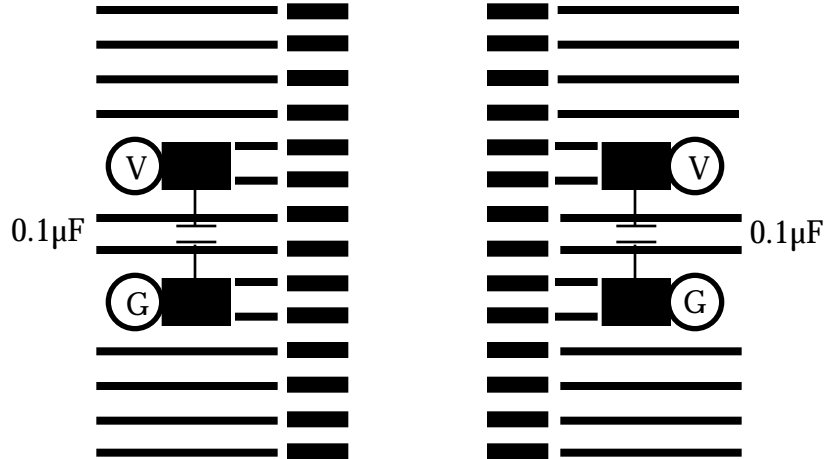


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Pin Assignment



Suggested Layout



For simplicity, series terminating resistors (required) are not shown for the outputs, but should be placed as close to the device as possible. It is most critical to have the 0.1µF decoupling capacitors closest.

Ⓧ = connect to VDD Ⓞ = connect to GND

Pin Descriptions

Number	Name	Type	Description
1	OE1	I	Output Enable. Tri-states Q2 to Q7 clock outputs when this input is low. Internal pull-up.
2, 3	Q0, Q1	O	Clock outputs.
4, 7, 8	Q2, Q3, Q4	O	Clock outputs.
5, 6	VDD	P	Power supply. Connect to +3.3 V or 5 V.
9, 10	GND	P	Connect to ground.
11, 12, 13	Q5, Q6, Q7	O	Clock outputs.
14	IN	I	Clock input for 16 buffers.
15	OE0	I	Output Enable. Tri-states Q8 to Q13 clock outputs when this input is low. Internal pull-up.
16, 17, 18	Q8, Q9, Q10	O	Clock outputs.
19, 20	GND	P	Connect to ground.
21, 22, 25	Q11, Q12, Q13	O	Clock outputs.
23, 24	VDD	P	Power supply. Connect to +3.3 V or 5 V.
26, 27	Q14, Q15	O	Clock outputs.
28	OE2	I	Output Enable. Tri-states Q0, Q1, Q15 and Q14 clock outputs when this input is low. Internal pull-up.

Type: I = Input, O = output, P = power supply connection



Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	0.5		VDD+0.5	V
Clock Outputs	Referenced to GND	0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 20 seconds			260	°C
Storage Temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Operating Voltage, VDD		3.0	3.3	5.5	V
Input High Voltage, VIH (IN pin)	Input clock	(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL (IN pin)	Input clock		VDD/2	(VDD/2)-1	V
Input High Voltage, VIH (OE pins)		2.0			V
Input Low Voltage, VIL (OE pins)				0.8	V
Output High Voltage, 3.3V	IOH=-8mA	VDD-0.4			V
Output High Voltage, 3.3V	IOH=-12mA	2.4			V
Output Low Voltage, 3.3V	IOL=12mA			0.8	V
Operating Supply Current, IDD, at 100 MHz	No Load		55		mA
Output Impedance			14		
Short Circuit Current, 3.3V	Each output		±50		mA
On-Chip Pull-up Resistor	OE0, OE1, OE2		250		k
Input Capacitance			5		pF
AC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Input Clock Frequency with load = 8 pF	Note 4, 5	0		200	MHz
Propagation Delay with load = 15pF			1.4	3	ns
Output Clock Rise Time	0.8 to 2.0V			2	ns
Output Clock Fall Time	2.0 to 0.8V			2	ns
Output Clock Rising Edge Skew	At VDD/2. Note 2		100	250	ps
Output Enable Time, OE high to output on				20	ns
Output Disable Time, OE low to tri-state				20	ns

Notes:

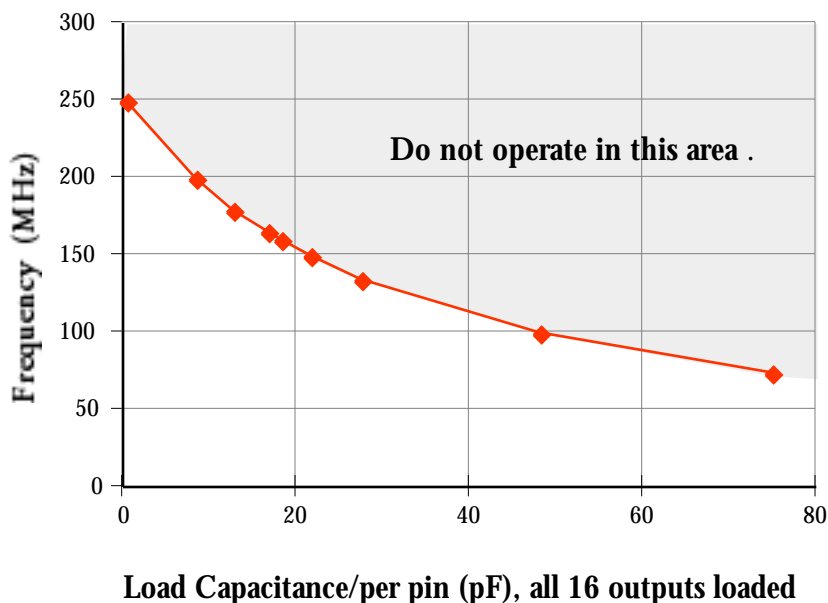
1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Between any two outputs, with equal loading.
3. At VDD = 3.3 V, 70°C, series termination of 33 Ω per pin, 8 pF load per pin.
4. See discussion and graph of speed versus load, Graph 1 on following page.



Maximum Speed/Application Notes

The maximum speed at which the chip can operate is limited by power dissipation of the package. Graph 1 shows the operating frequency plotted against load capacitance per pin for a die temperature of 125°C. This is at VDD = 3.3 V, 70°C and with 33 series termination resistor. The termination resistors are essential because they allow a large proportion of the total power to be dissipated outside the package. Reducing or eliminating the series termination will cause an increase in die temperature. It is not recommended to operate the chip at die temperature greater than 125°C. Also note that the load capacitance per pin must include PC board parasitics such as trace capacitance. ICS has other buffers specified to 250 MHz with heavier loads.

If not all outputs of the chip are used, it is possible to operate the chip faster with larger loads. Unused outputs should be left unconnected. Consult ICS for your specific requirement.



Graph 1
MK74CB115
Maximum Speed at 3.3 V

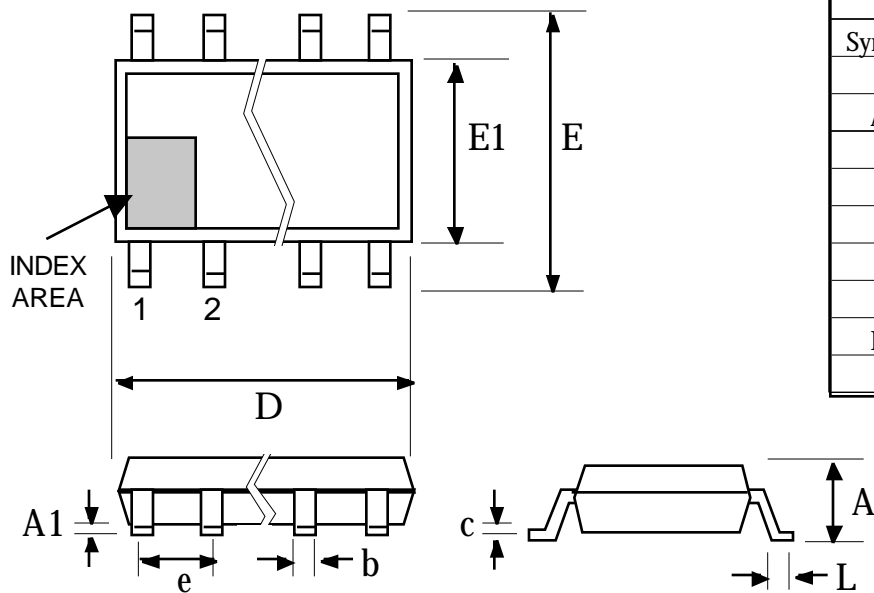


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Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)

28 pin SSOP



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.102	0.254
b	0.008	0.012	0.203	0.305
c	0.007	0.010	0.191	0.254
D	0.386	0.394	9.804	10.008
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.791	6.198
E1	0.150	0.157	3.810	3.988
L	0.016	0.050	0.406	1.270

Ordering Information

Part/Order Number	Marking	Package	Temperature
MK74CB115R	MK74CB115R	28 pin SSOP	0-70°C
MK74CB115RTR	MK74CB115R	Add Tape & Reel	0-70°C

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