DATA SHEET

OM4031T
Digital post-detection filter for FSK data receivers

Preliminary specification
File under Integrated Circuits, IC03

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Philips Semiconductors

PHILIPS

Digital post-detection filter for FSK data receivers

OM4031T

FEATURES

- External clock frequency 30 to 80 kHz (typ. 38.4 kHz)
- Supported data rates 600, 1200, 2400 and 4800 bits/s (typ.)
- Double bandwidth option (not for 4800 bits/s)
- Schmitt-triggered inputs for optimum slope tolerance
- Enable input for power-down mode
- Open-drain output (3-state in power-down mode)
- No external components required
- Single supply voltage from 1.8 to 6.0 V
- Very low operating current (1.5 μA typ.)
- Operating temperature from –10 to +70 °C.

APPLICATIONS

- Telemetry data receivers
- RF security systems
- Low-bit-rate radio data links
- Paging applications of UAA2080 and UAA2082 with software decoding.

GENERAL DESCRIPTION

The OM4031T is intended for performance enhancement of FSK data receivers that do not have a built-in post-detection filter.

It contains a digital moving average filter to remove noise from the demodulated data. When operated from a 38.4 kHz external clock it can handle data rates of 600, 1200 and 2400 bits/s at an oversampling rate of 16. The filter bandwidth can be doubled to ease the search for bit synchronization on the output data.

To allow for jitter in the input data, a 12-bit sample is taken for the majority decision. Doubling the filter bandwidth is realised by taking the majority out of 6 samples (2400 bits/s) or by doubling the sampling rate (600 and 1200 bits/s).

An input data rate of 4800 bits/s is supported at 8 times oversampling and normal bandwidth.

All inputs are Schmitt-triggered to ensure reliable operation even at signals with long rise/fall times.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.8	–	6.0	V
I_{DDPD}	power-down supply current	CE = V_{SS}	–	1.0	10.0	μA
I_{DD}	operating supply current	CE = V_{DD}; note 1	–	1.5	20.0	μA
$P_{i(ref)}$	sensitivity improvement at 3% bit error rate	note 2				
		600 bits/s, 250 μs slope	–	5.3	–	dB
		1200 bits/s, 250 μs slope	–	3.6	–	dB
		2400 bits/s, 125 μs slope	–	2.0	–	dB
T_{amb}	operating ambient temperature		–10	–	+70	°C

Notes

1. V_{DD} = 2.0 V; DOUT open-circuit; input data at 20 kHz random pattern.
2. Bench evaluated for UAA2080H at 470 MHz, not factory tested.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM4031T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Digital post-detection filter for FSK data receivers

OM4031T

BLOCK DIAGRAM

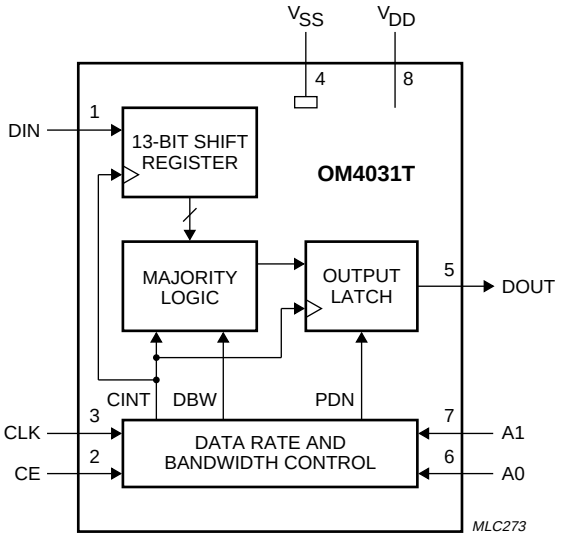


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DIN	1	data input
CE	2	chip enable input
CLK	3	external clock input
V_{SS}	4	negative supply voltage
DOUT	5	data output (open-drain)
A0	6	data rate and bandwidth control input 0 (see Table 1)
A1	7	data rate and bandwidth control input 1 (see Table 1)
V_{DD}	8	positive supply voltage

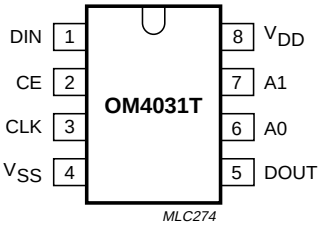


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The OM4031T digital post-detection filter oversamples the noisy binary data stream at input DIN (pin 1), and outputs a noise-reduced data stream via open-drain output DOUT (pin 5). The filter bandwidth can be doubled to ease the search for bit synchronization on the data output signal.

Input sampling takes place at 16 times the data rate. For a typical clock frequency of 38.4 kHz the nominal data rates are 600, 1200 and 2400 bits/s. A data rate of 4800 bits/s can be handled at an oversampling rate of 8 and at normal bandwidth only.

Using a different clock frequency will produce bit rates equal to the clock frequency divided by 64, 32 or 16. When the clock frequency is not an integer multiple of the data rate some edge jitter will be introduced in the output data.

The clock frequency is not very critical for the noise filtering performance: a clock frequency of 32.768 kHz could be used at 512, 1200 and 2400 bits/s without loss of performance.

Since no on-chip oscillator is available an external clock signal is required at input CLK (pin 3). Two control inputs A0 and A1 (pins 6 and 7) are used for selection of the data rate and the filter bandwidth.

A separate enable input CE (pin 2) allows the circuit to be powered down. In power-down mode (CE = LOW) the system clock is inhibited and the data output DOUT is made 3-state and remains static.

Moving average noise filter

Noise reduction is achieved by applying a moving average filter on N samples of the input data signal. In principle N can be odd or even, but in the OM4031T an even number is used (N = 12). When there is no absolute majority (equal number of ones and zeroes) the previous majority output is maintained.

An odd value for N would always produce an absolute majority and not require decision feedback. However the noise performance is worse for odd values of N, because the output can toggle at every clock (e.g. when a 101010... pattern is clocked in). For even values of N the output polarity can only change once every 3 clocks and does not toggle at all for a 101010... or a 11001100... pattern.

Using 12 out of 16 samples for the majority decision produces a filter which combines good noise reduction with a large tolerance for data jitter (maximum $\frac{1}{8}$-bit duration).

Filter implementation

The moving average filter is implemented using a 13-bit register and two state machines (COUNT and CLOCK) for the majority decision. The first stage of the shift register is used for input synchronization.

The CLOCK state machine generates the internal clock signal CINT and the bandwidth selection signal DBW in accordance with the logic levels on control lines CE, A0 and A1.

The majority decision is taken by state machine COUNT based on the contents of the input shift register and the previous decision in the output latch.

The doubled bandwidth is achieved by increasing the sampling rate by a factor of 2 for 600 and 1200 bits/s. For 2400 bits/s the number of samples for the majority decision is halved, controlled by the DBW signal. This signal is derived from the control signals as follows:

$$DBW = CE \bullet A0 \bullet \overline{A1}$$

Filter characteristic

The frequency characteristic of the moving average filter in the OM4031T is given in Fig.3 for N = 12 and N = 6.

The horizontal axis shows the normalized frequency f_N which is the ratio of the frequency f and the sampling frequency f_s. The value for f_s is given in Table 1 for the various data rates and filter bandwidths.

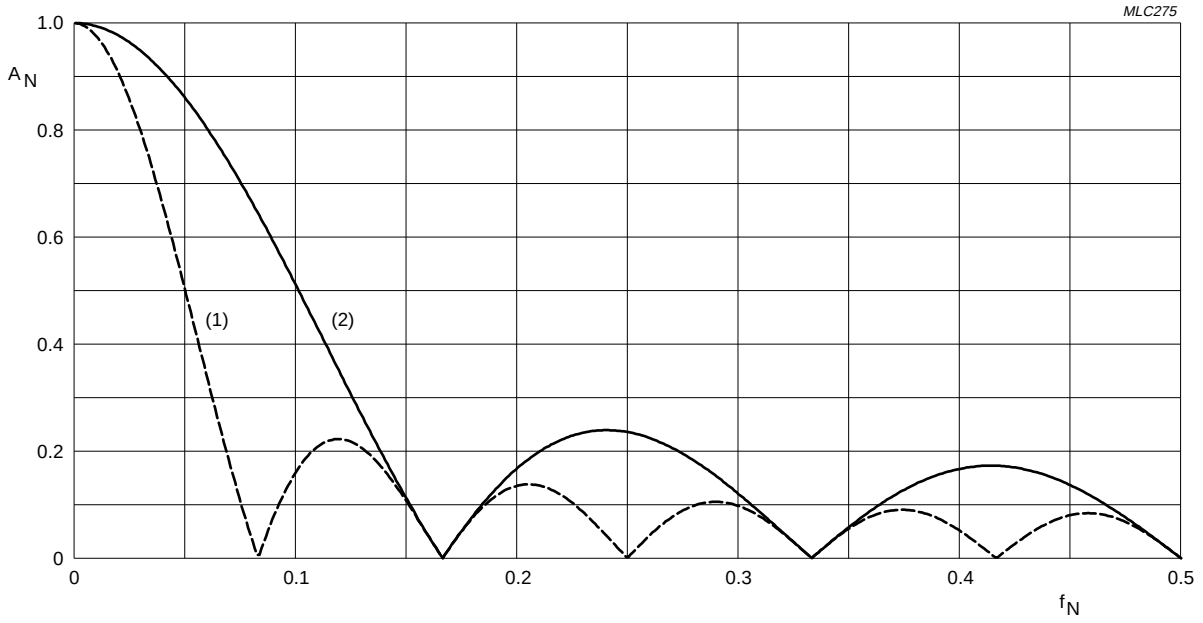
The vertical axis shows the normalized amplitude A_N.

At normal bandwidth the oversampling rate is 16, except for 4800 bits/s where it is 8. At double bandwidth the oversampling rate is 32, except for 2400 bits/s, where it is 16.

The 3 dB cut-off frequency is calculated as follows:

N = 12: $f_{co} = 0.0371 \times f_s$

N = 6: $f_{co} = 0.0748 \times f_s$



(1) N = 12.
(2) N = 6.

Fig.3 Filter transfer function of the OM4031T.

Noise reduction

The performance of the OM4031T was bench tested by measuring the sensitivity improvement (3% BER) of the UAA2080H pager receiver at various bit rates using a stand-alone pager receiver board (OM4647 at 470 MHz). The results are given in Chapter “AC Characteristics” .

The OM4031T was also tested in a POCSAG pager application using software decoding together with the UAA2080H receiver.

For 12-digit numeric messages at 1200 bits/s the typical sensitivity for 80% call success rate improved by 2.8 dB, as shown in Fig.4.

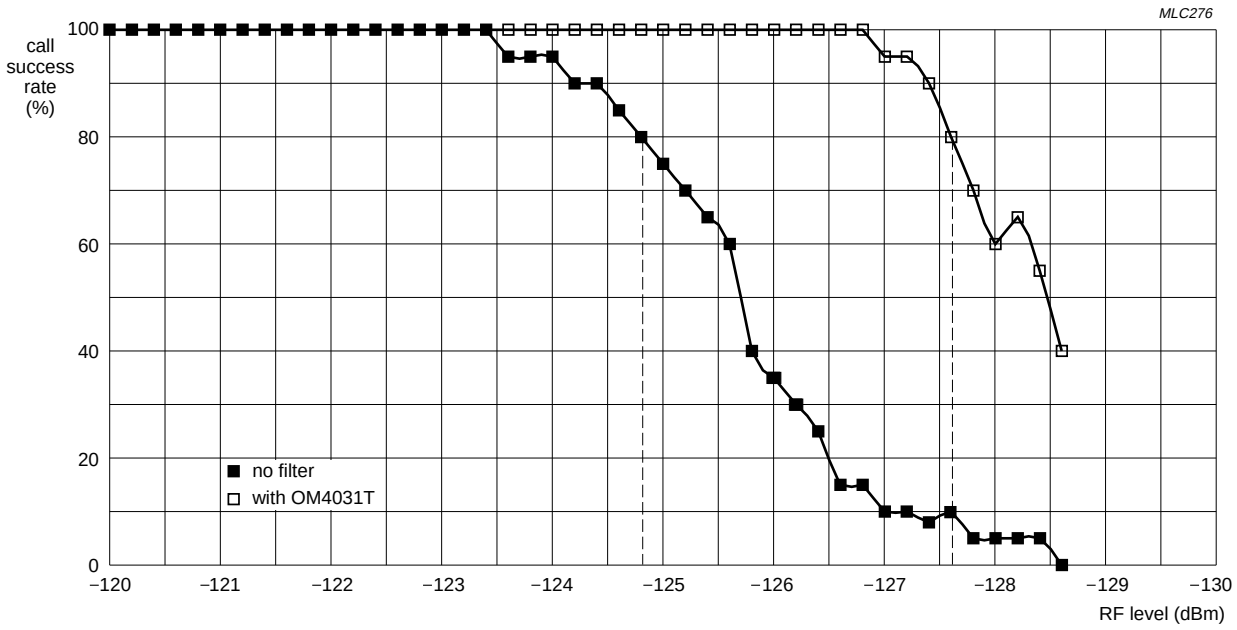


Fig.4 Paging call success rate improvement; 1200 bits/s, 12-digit numeric message.

OPERATING INSTRUCTIONS

Control signals

The operation of the OM4031T is determined by 3 control signals (CE, A0 and A1) and the clock frequency at input CLK. Table 1 shows the various possibilities for a typical clock frequency of 38.4 kHz.

The parameter N is the number of samples used in the calculation of the average bit value.

The parameter f_s is the input sampling frequency, assuming a 38.4 kHz external clock signal.

The logic levels on A0 and A1 can be changed while CE = HIGH, except to select or deselect 2400 bits/s with doubled bandwidth (A1 = LOW, A0 = HIGH). This mode must be entered or left while CE = LOW to avoid data errors on DOUT.

Table 1 Data rate and filter bandwidth selection

CE	A1	A0	N (samples)	f_s (kHz)	DATA RATE (bits/s)	
					NORMAL BANDWIDTH	DOUBLE BANDWIDTH
0	X	X	X	X	X	X
1	0	0	12	9.6	600	–
1	1	0	12	19.2	1200	600
1	0	1	6	38.4	4800(1)	2400
1	1	1	12	38.4	2400	1200

Note

1. At 4800 bits/s the oversampling rate is 8.

Power-down mode

To reduce power consumption the filter can be disabled by applying a LOW level to input CE. The result is as follows:

- The internal clock is inhibited
- Output DOUT is made 3-state and static.

Reset

The OM4031T is reset internally when power-down mode is left by applying a HIGH level to input CE. The actual reset takes place on the second falling edge on input CLK after CE = HIGH.

The status after reset is as follows:

- The shift register contains a 101010... pattern
- DOUT is made LOW.

After power-up input CE must be kept at a LOW level for at least one clock period on input CLK. This ensures a successful reset when CE is made HIGH.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	7.0	V
V_I	input voltage on any pin	–0.5	V_{DD} + 0.5	V
I_I	DC input current all pins	–	20	mA
I_O	DC output current all pins	–	20	mA
P_{tot}	total power dissipation	–	150	mW
T_{amb}	operating ambient temperature	–10	+70	°C
T_{stg}	storage temperature	–55	+125	°C

DC CHARACTERISTICS

V_{DD} = 1.8 to 6.0 V; V_{SS} = 0 V; T_{amb} = –10 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		1.8	–	6.0	V
I_{DDPD}	power-down supply voltage	CE = V_{SS}; note 1	–	1.0	10.0	µA
I_{DD}	operating supply current	CE = V_{DD}; notes 1 and 2	–	1.5	20.0	µA
Inputs A0, A1, CLK and CE						
V_{IL}	LOW level input voltage		–0.5	–	+0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = V_{DD} or V_I = V_{SS}	–	–	1.0	µA
C_I	input capacitance	tested on sample basis	–	2.0	–	pF
Output DOUT						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.0	–	–	mA
I_{LO}	output leakage current	V_{OH} = V_{DD}	–	–	1.0	µA

Notes

1. V_{DD} = 2.0 V; V_{IL} = V_{SS}; V_{IH} = V_{DD}; DOUT is open-circuit; clock signal at input CLK; f_{clk} = 38.4 kHz, amplitude: V_{SS} to V_{DD}; data signal at input DIN: random pattern at 20 kHz to simulate 2400 bits/s data with noise; t_r = t_f = 5 ns.
2. The operating current will be higher than specified when the input signal amplitude is less than 100% (equals V_{SS} to V_{DD}) or when longer rise/fall times are used. This is caused by the Schmitt-trigger circuits drawing extra current.

AC CHARACTERISTICS

V_{DD} = 1.8 to 6.0 V; V_{SS} = 0 V; T_{amb} = −10 to +70 °C; f_{clk} = 38.4 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External clock						
f_{clk}	external clock frequency		30	38.4	80	kHz
Filter bandwidth (note 1)						
f_{co}	cut-off frequency (–3 dB)	normal bandwidth				
		600 bits/s	–	356	–	Hz
		1200 bits/s	–	712	–	Hz
		2400 bits/s	–	1425	–	Hz
		4800 bits/s	–	2872	–	Hz
		double bandwidth				
		600 bits/s	–	712	–	Hz
		1200 bits/s	–	1425	–	Hz
		2400 bits/s	–	2872	–	Hz
Noise reduction (note 2)						
$P_{i(ref)}$	sensitivity improvement at 3% bit error rate	note 3				
		600 bits/s, 250 µs slope	–	5.3	–	dB
		1200 bits/s, 250 µs slope	–	3.6	–	dB
		2400 bits/s, 125 µs slope	–	2.0	–	dB

Notes

1. Filter bandwidth is guaranteed by design. Values supplied are simulation results.
2. Noise reduction is not factory tested, only bench evaluated.
3. Sensitivity improvement was bench tested on the UAA2080H demonstration board OM4747. Test signal: preamble (101010...), f_{iRF} = 469.950 MHz, deviation = ±4.0 kHz, slope = 10 to 90% of amplitude, V_P = 2.05 V, T_{amb} = 25 °C. See "*UAA2080 data sheet, AC characteristics*".

APPLICATION INFORMATION

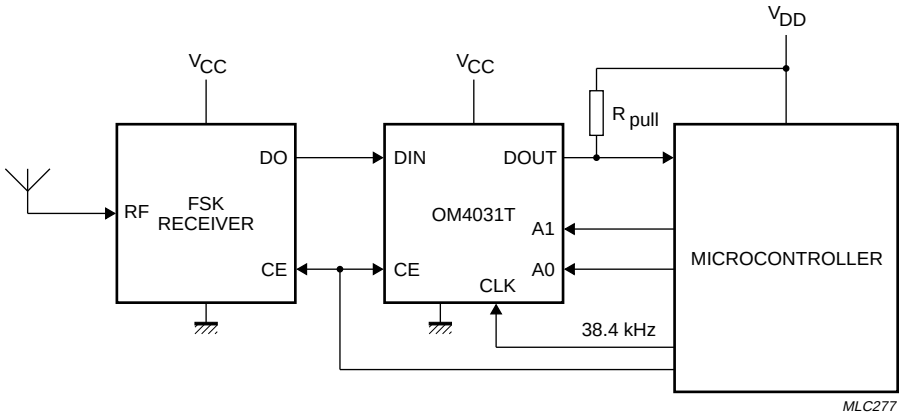


Fig.5 Typical application example.

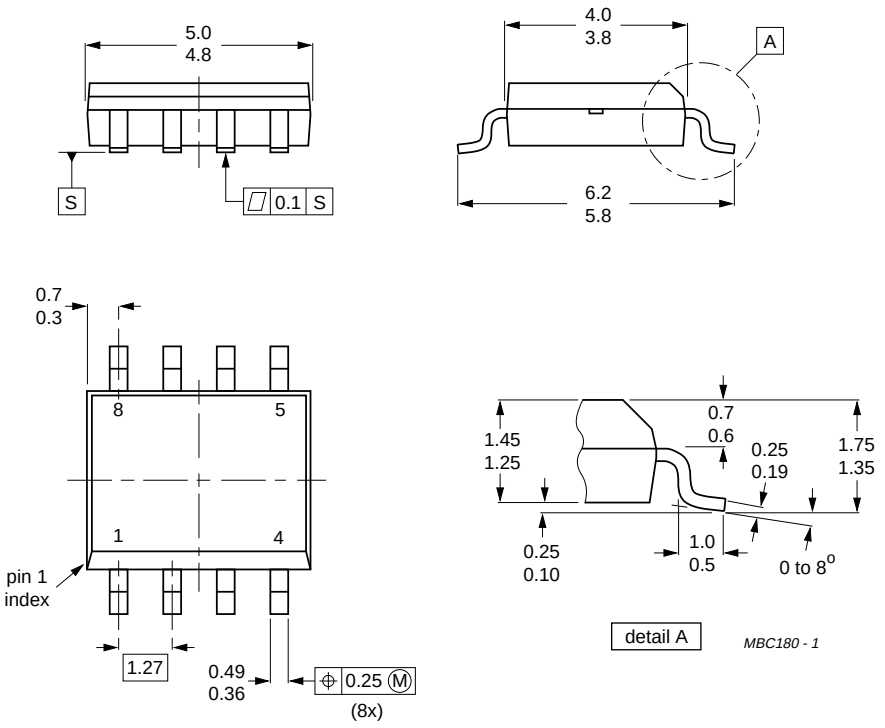
The OM4031T will generally operate from the same power supply (V_{CC}) as the FSK data receiver providing its input data. The open-drain data output allows level shifting of the data to suit a microcontroller operating at a higher power supply voltage (V_{DD}).

The value of the pull-up resistor R_{pull} on output DOUT is determined by the type and number of input circuits to be driven. The required signal rise time must be balanced against the current drawn by the pull-up.

For the highest rate (2400 bits/s) the signal rise time should preferably be below 50 μs.

For a single CMOS input with a 10 pF capacitance R_{pull} = 1 MΩ gives a rise time of approximately 30 μs ($3 \times t_{RC}$). At V_{DD} = 2.0 V this corresponds with a current of 2 μA.

PACKAGE OUTLINE



Dimensions in mm.

Fig.6 Plastic small outline package; 8 leads; body width 3.9 mm (SO8; SOT96-1).

SOLDERING

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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Argentina: IEROD, Av. Juramento 1992 - 14.b, (1428)
BUENOS AIRES, Tel. (541)786 7633, Fax. (541)786 9367

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
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Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
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