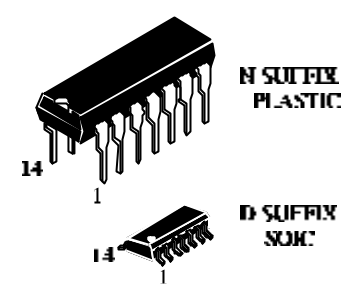


# 8-Bit Serial-Input/Parallel-Output Shift Register

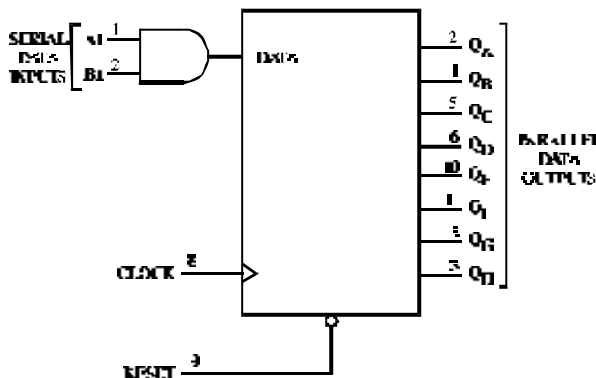
This 8-bit shift register features gated serial inputs and an asynchronous reset. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip flop to the low level at the next clock pulse. A high level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered clocking occurs or the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear



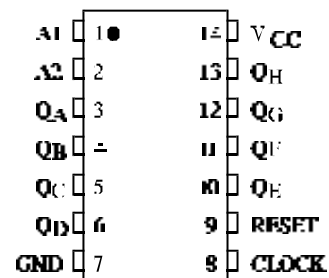
**ORDERING INFORMATION**  
 SL74LS164N Plastic  
 SL74LS164D SOIC  
 T<sub>A</sub> = 0° to 70°C  
 for all packages

## LOGIC DIAGRAM



PIN 14 = V<sub>CC</sub>  
 PIN 7 = GND

## PIN ASSIGNMENT



## FUNCTION TABLE

Inputs			Outputs			
Reset	Clock	A1 A2	Q <sub>A</sub>	Q <sub>B</sub>	... Q <sub>H</sub>	
L	X	X X	L	L	... L	
H		X X	no change			
H		H D	D	Q <sub>An</sub>	... Q <sub>Gn</sub>	
H		D H	D	Q <sub>An</sub>	... Q <sub>Gn</sub>	
H		L L	L	Q <sub>An</sub>	... Q <sub>Gn</sub>	

D = data input

X = don't care

Q<sub>An</sub> - Q<sub>Gn</sub> = data shifted from the previous stage on a rising edge at the clock input.

# SL74LS164

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	7.0	V
V <sub>IN</sub>	Input Voltage	7.0	V
V <sub>OUT</sub>	Output Voltage	5.5	V
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2.0		V
V <sub>IL</sub>	Low Level Input Voltage		0.8	V
I <sub>OH</sub>	High Level Output Current		-0.4	mA
I <sub>OL</sub>	Low Level Output Current		8.0	mA
T <sub>A</sub>	Ambient Temperature Range	0	+70	°C
f <sub>clock</sub>	Clock Frequency	0	25	MHz
t <sub>su</sub>	Setup Time, A1 or A2 to Clock	15		ns
t <sub>h</sub>	Hold Time, Clock to A1 or A2	5		ns
t <sub>w</sub>	Pulse Width, Clock	20		ns
t <sub>w</sub>	Pulse Width, Reset	20		ns
t <sub>rec</sub>	Recovery Time	5		ns

## DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V <sub>IK</sub>	Input Clamp Voltage	V <sub>CC</sub> = min, I <sub>IN</sub> = -18 mA		-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = min, I <sub>OH</sub> = -0.4 mA	2.7		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = min, I <sub>OL</sub> = 4 mA		0.4	V
		V <sub>CC</sub> = min, I <sub>OL</sub> = 8 mA		0.5	
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 2.7 V		20	mA
		V <sub>CC</sub> = max, V <sub>IN</sub> = 7.0 V		0.1	mA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 0.4 V		-0.4	mA
I <sub>O</sub>	Output Short Circuit Current	V <sub>CC</sub> = max, V <sub>O</sub> = 0 V (Noote 1)	-20	-100	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = max (Note 2)		27	mA

Note 1: Not more than one output should be shorted at a time, and duration should not exceed one second.

Note 2:  $t_{CC}$  is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied.

**AC ELECTRICAL CHARACTERISTICS** ( $T_A=25^\circ\text{C}$ ,  $V_{CC}=5.0\text{ V}$ ,  $C_L=15\text{ pF}$ ,  $R_L=2\text{ k}\Omega$ ,  $t_r=15\text{ ns}$ ,  $t_f=6.0\text{ ns}$ )

Symbol	Parameter	Min	Max	Unit
$t_{PLH}$	Propagation Delay Time, Clock to Q		27	ns
$t_{PHL}$	Propagation Delay Time, Clock to Q		32	ns
$t_{PHL}$	Propagation Delay Time, Reset to Q		36	ns
$t_{su}$	Setup Time, A1 or A2 to Clock	15		ns
$t_h$	Hold Time, Clock to A1 or A2	5		ns
$t_w$	Pulse Width, Clock	20		ns
$t_w$	Pulse Width, Reset	20		ns

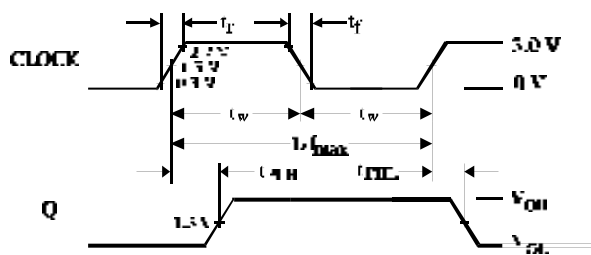


Figure 1. Switching Waveforms

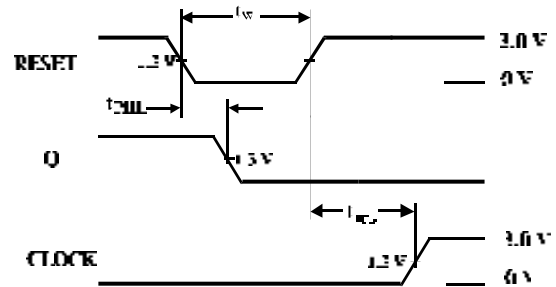


Figure 2. Switching Waveforms

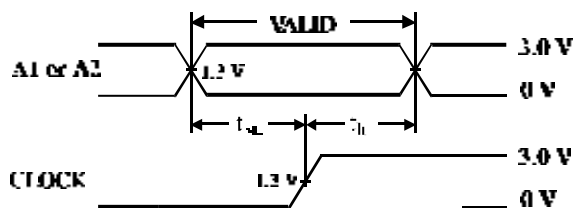
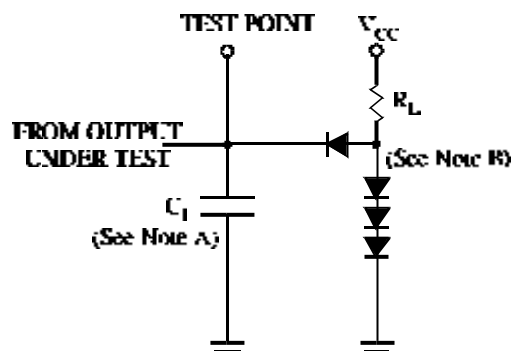


Figure 3. Switching Waveform



NOTES A.  $C_L$  includes probe and jig capacitance.  
B. All diodes are 1N916 or 1N3064.

Figure 4. Test Circuit

TIMING DIAGRAM

