NIPPON PRECISION CIRCUITS INC.

SM5841H

Audio Multi-function Digital Filter

OVERVIEW

The SM5841H is an 8-times oversampling (interpolation) digital filter for digital audio reproduction equipment. It accepts 16 or 18-bit input data, and outputs data in 16, 18 or 20-bit format, making a wide range of interfaces possible. It also features digital deemphasis for 3 sampling frequencies, a noise shaper to reduce quantization noise, a DC offset output and other circuits.

ORDERING INFOMATION

Device	Package
SM5841HP	18pin DIP
SM5841HS	22pin SOP

FEATURES

Functions

- 2-channel processing
- 8-times (8fs) oversampling (interpolation)
- Digital deemphasis (fs = 48/44.1/32 kHz)
- Serial input data
  2s complement, MSB first, 16/18-bit
- Serial output data
  2s complement, MSB first, 16/18/20-bit
- 1st-order noise shaper (for 16/18-bit output only)
- 256fs/384fs system clock selectable
- Output data DC offset (approximately 0.8%) ON/OFF control
- TTL-compatible input/outputs
- 5 V (standard) supply
- 3.2 V operating voltage
- Molybdenum-gate CMOS

Filter Characteristics

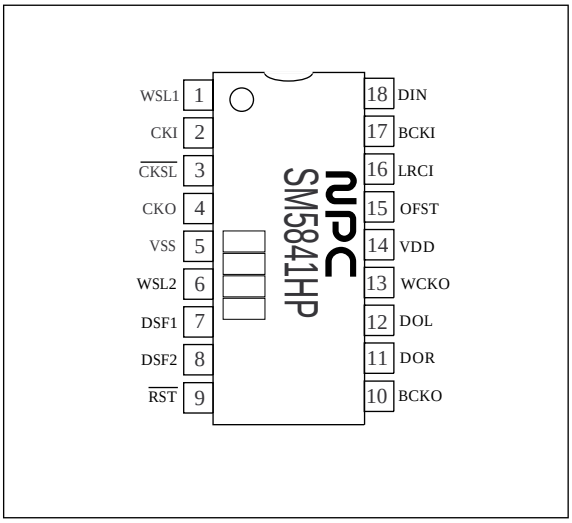
- 3-stage DC FIR interpolation filter
  1st stage (fs → 2fs), 69-tap
  2nd stage (2fs → 4fs), 13-tap
  3rd stage (4fs → 8fs), 9-tap
- IIR deemphasis filter for gain and phase characteristics close to those of analog filters
- Overflow limiter built-in

APPLICATIONS

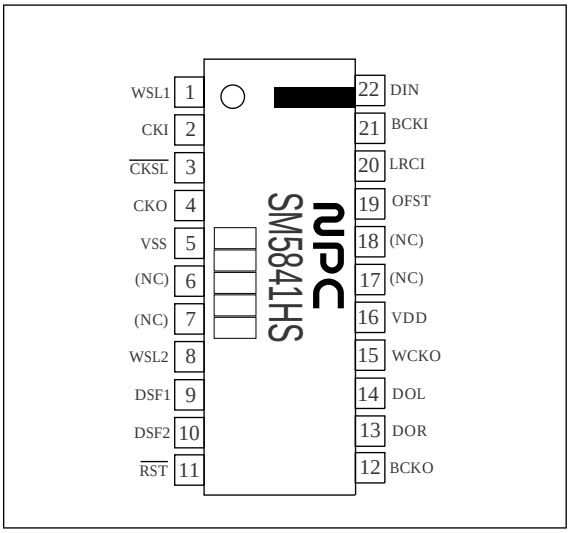
- Digital amplifiers
- CD players
- DAT players
- DBS systems
- PCM systems

PINOUT

18-pin DIP

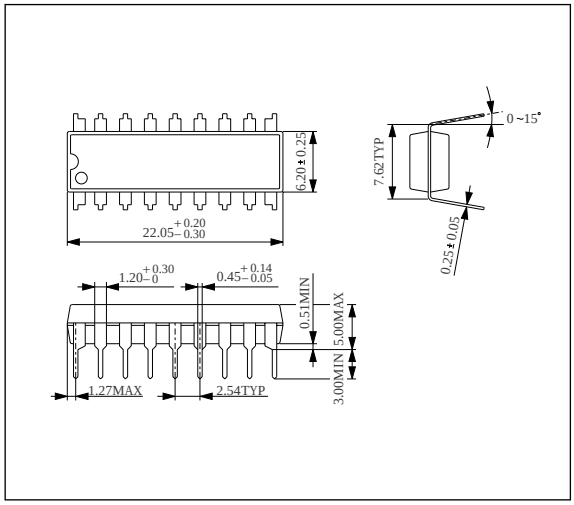


22-pin SOP

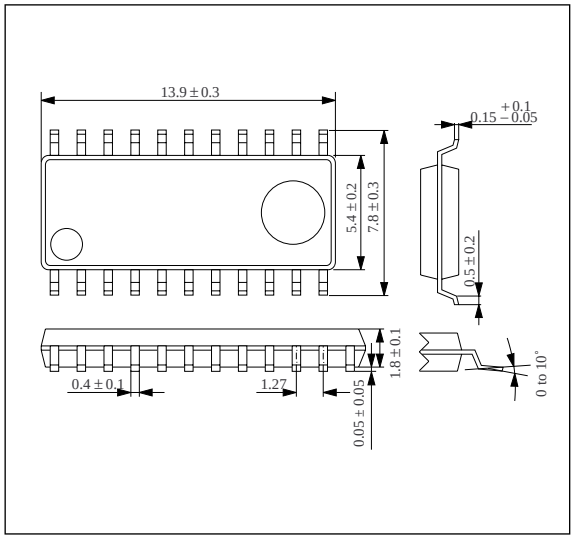


PACKAGE DIMENSIONS

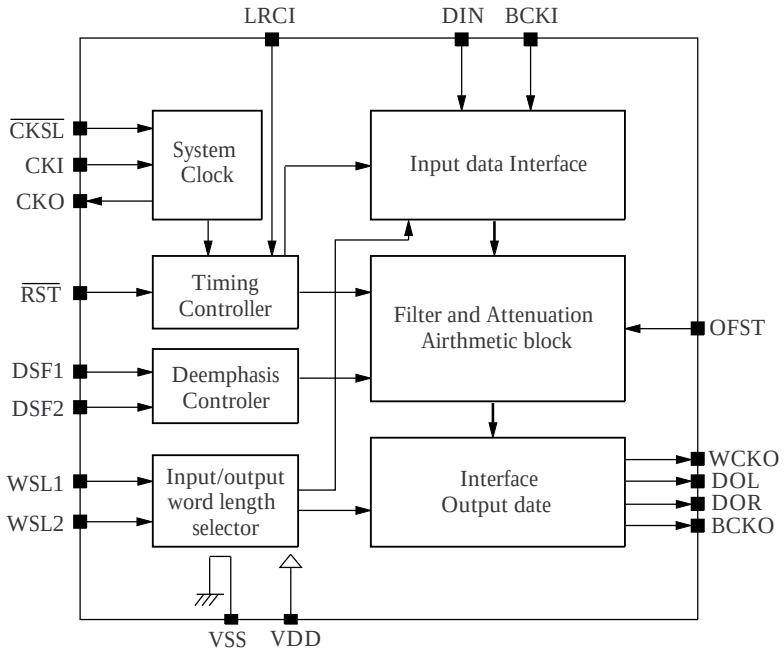
18-pin DIP (Unit: mm)



22-pin SOP (Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

SOP	DIP	Name	I/O[1]	Description
1	1	WSL1	Ip	Input/output data select pins
8	6	WSL2	Ip	
2	2	CKI	Ip	System clock input
3	3	$\overline{\text{CKSL}}$	Ip	System clock select input. 384fs when HIGH, and 256fs when LOW.
4	4	CKO	O	System clock output. The CKI is first buffered before output on CKO.
5	5	VSS	–	Ground
6	–	NC	–	No connection
7	–	NC	–	No connection
9	7	DSF1	Ip	Deemphasis select inputs
10	8	DSF2	Ip	
11	9	$\overline{\text{RST}}$	Ip	System reset. Reset and initialization when $\overline{\text{RST}}$ is LOW.
12	10	BCKO	O	Output bit clock

WSL1	WSL2	Noise shaper	Input bit length	Output bit length
HIGH	HIGH	Off	18 bits	20 bits
HIGH	LOW	On	18 bits	18 bits
LOW	HIGH	On	16 bits	18 bits
LOW	LOW	On	16 bits	16 bits

DSF1	DSF2	Deemphasis	Sampling frequency
LOW	LOW	On	44.1 kHz
LOW	HIGH	On	48.0 kHz
HIGH	LOW	Off	–
HIGH	HIGH	On	32.0 kHz

SOP	DIP	Name	I/O[1]	Description
13	11	DOR	O	Right-channel 8fs data output
14	12	DOL	O	Left-channel 8fs data output
15	13	WCKO	O	Output word clock
16	14	VDD	–	5 V supply
17	–	NC	–	No connection
18	–	NC	–	No connection
19	15	OFST	Ip	Output data DC offset select input. Summing ON when HIGH, and OFF when LOW.
20	16	LRCI	Ip	Input data sample rate (fs) clock
21	17	BCKI	Ip	Input bit clock
22	18	DIN	Ip	Input data

1. Ip = Input with pull-up resistor

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	250	mW
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	3.2 to 5.5	V
Operating temperature range	T_{opr}	–20 to 80	°C

DC Electrical Characteristics

Standard voltage: V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	V_{DD} = 5.0 V[1]	–	–	40	mA
HIGH-level input voltage[2]	V_{IH1}		0.7V_{DD}	–	–	V
LOW-level input voltage[2]	V_{IL1}		–	–	0.3V_{DD}	V
CKI AC-coupled input voltage	V_{INAC}	Sine wave input	0.3V_{DD}	–	–	V_{p-p}
HIGH-level input voltage[3]	V_{IH2}		2.4	–	–	V
LOW-level input voltage[3]	V_{IL2}		–	–	0.5	V
HIGH-level output voltage[4]	V_{OH}	I_{OH} = –0.4 mA	2.5	–	–	V
LOW-level output voltage[4]	V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	V
CKI HIGH-level input current	I_{IH1}	V_{IN} = V_{DD}	–	10	20	µA
CKI LOW-level input current	I_{IL1}	V_{IN} = 0 V	–	10	20	µA
LOW-level input current[3]	I_{IL2}	V_{IN} = 0 V	–	10	20	µA
Input leakage current[2, 3]	I_{LH}	V_{IN} = V_{DD}	–	–	1.0	µA
Input leakage current[2]	I_{LL}	V_{IN} = 0 V	–	–	1.0	µA

1. f_{SYS} = 384fs = 20 MHz, no output load
2. Pins $\overline{CKSL}$, OFST
3. Pins LRCI, DIN, BCKI, DSF1, DSF2, WSL1, WSL2, $\overline{RST}$
4. Pins CKO, DOL, DOR, BCKO, WCKO

Low voltage: V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	V_{DD} = 3.4 V[1]	–	–	20	mA
HIGH-level input voltage[2]	V_{IH1}		0.7V_{DD}	–	–	V
LOW-level input voltage[2]	V_{IL1}		–	–	0.3V_{DD}	V
CKI AC-coupled input voltage	V_{INAC}	Sine wave input	0.3V_{DD}	–	–	V_{p-p}
HIGH-level input voltage[3]	V_{IH2}		2.4	–	–	V
LOW-level input voltage[3]	V_{IL2}		–	–	0.5	V
HIGH-level output voltage[4]	V_{OH}	I_{OH} = –0.2 mA	2.5	–	–	V
LOW-level output voltage[4]	V_{OL}	I_{OL} = 0.8 mA	–	–	0.4	V
CKI HIGH-level input current	I_{IH1}	V_{IN} = V_{DD}	–	–	12	µA
CKI LOW-level input current	I_{IL1}	V_{IN} = 0 V	–	–	12	µA
LOW-level input current[3]	I_{IL2}	V_{IN} = 0 V	–	–	12	µA
Input leakage current[2, 3]	I_{LH}	V_{IN} = V_{DD}	–	–	1.0	µA
Input leakage current[2]	I_{LL}	V_{IN} = 0 V	–	–	1.0	µA

1. f_{SYS} = 384fs = 18.5 MHz, no output load
2. Pins $\overline{CKSL}$, OFST
3. Pins LRCI, DIN, BCKI, DSF1, DSF2, WSL1, WSL2, $\overline{RST}$
4. Pins CKO, DOL, DOR, BCKO, WCKO

AC Electrical Characteristics

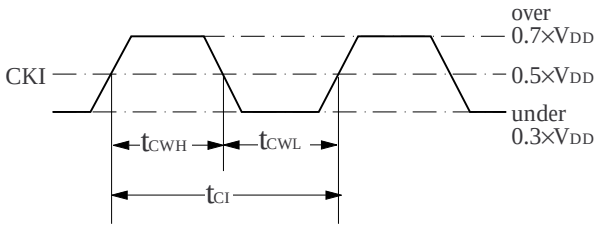
Clock (CKI)

Standard voltage: V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Condition		Rating			Unit
		$\overline{CKSL}$	System clock	min	typ	max	
HIGH-level clock pulsewidth	t_{CWH}	HIGH	384fs	23	–	250	ns
		LOW	256fs	35	–	500	
LOW-level clock pulsewidth	t_{CWL}	HIGH	384fs	23	–	250	ns
		LOW	256fs	35	–	500	
Clock pulse cycle	t_{CI}	HIGH	384fs	50	–	500	ns
		LOW	256fs	76	–	1000	

Low voltage: V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

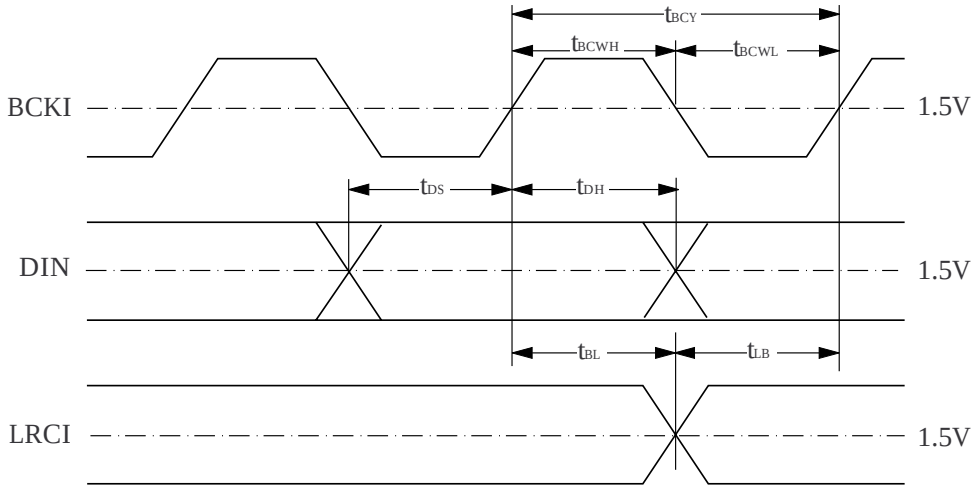
Parameter	Symbol	Condition		Rating			Unit
		$\overline{CKSL}$	System clock	min	typ	max	
HIGH-level clock pulsewidth	t_{CWH}	HIGH	384fs	25	–	250	ns
		LOW	256fs	50	–	500	
LOW-level clock pulsewidth	t_{CWL}	HIGH	384fs	25	–	250	ns
		LOW	256fs	50	–	500	
Clock pulse cycle	t_{CI}	HIGH	384fs	54	–	500	ns
		LOW	256fs	108	–	1000	



Serial input timing (BCKI, DI, LRCI)

V_{DD} = 3.2 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI pulse cycle	t_{BCY}	100	–	–	ns
DIN setup time	t_{DS}	50	–	–	ns
DIN hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	–	–	ns



Reset timing ($\overline{RST}$)

V_{DD} = 3.2 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{RST}$ LOW-level reset pulsewidth	t_{RST}	At power-ON	1	–	–	µs
		At all other times	50	–	–	ns

Control inputs (DSF1, DSF2)

V_{DD} = 3.2 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Rise time	t_r	10 to 90% level	–	–	100	ns
Fall time	t_f	90 to 10% level	–	–	100	ns

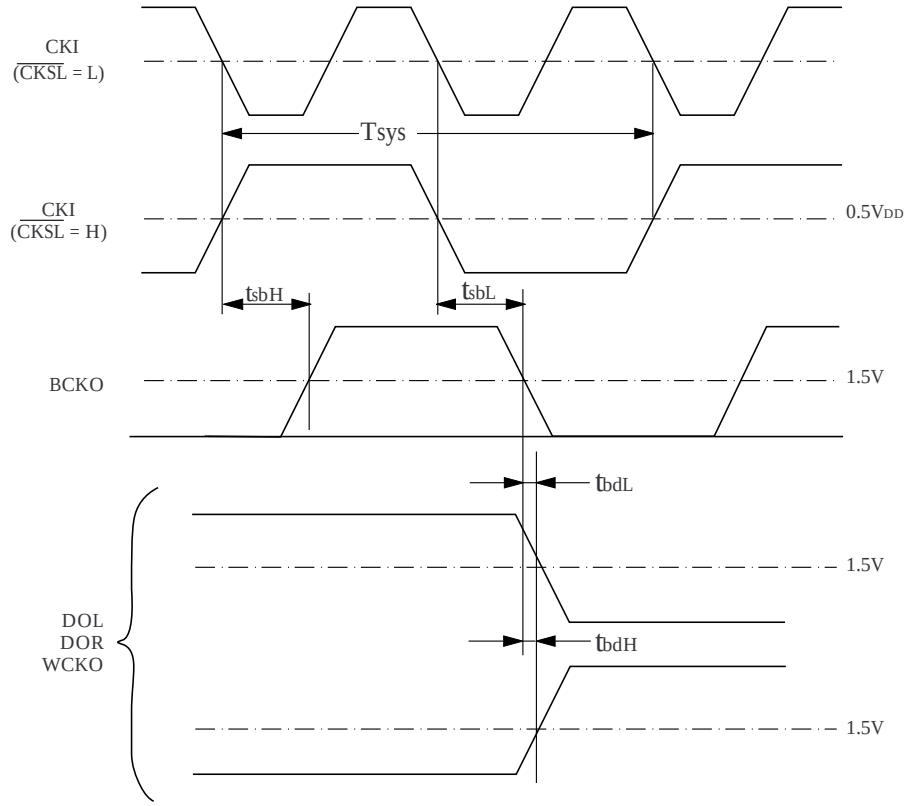
Output timing

Standard voltage: V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C, C_L = 15 pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CKI to CKO delay	t_{CKO}	CKI fall to CKO fall	–	–	30	ns
CKI to BCKO delay	t_{sbH}	CKI fall to BCKO rise	10	–	60	ns
	t_{sbL}	CKI fall to BCKO fall	10	–	60	
BCKO to DOL, DOR, WCKO delay	t_{bdH}	BCKO fall to output rise	0	–	20	ns
	t_{bdL}	BCKO fall to output fall	0	–	20	
$\overline{RST}$ to DOL, DOR delay	t_{rdH}	$\overline{RST}$ fall to output fall	–	–	40	ns
	t_{rdL}	$\overline{RST}$ rise to output rise	–	–	40	

Low voltage: V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C, C_L = 15 pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CKI to CKO delay	t_{CKO}	CKI fall to CKO fall	–	–	45	ns
CKI to BCKO delay	t_{sbH}	CKI fall to BCKO rise	10	–	100	ns
	t_{sbL}	CKI fall to BCKO fall	10	–	100	
BCKO to DOL, DOR, WCKO delay	t_{bdH}	BCKO fall to output rise	0	–	30	ns
	t_{bdL}	BCKO fall to output fall	0	–	30	
$\overline{RST}$ to DOL, DOR delay	t_{rdH}	$\overline{RST}$ fall to output fall	–	–	60	ns
	t_{rdL}	$\overline{RST}$ rise to output rise	–	–	60	

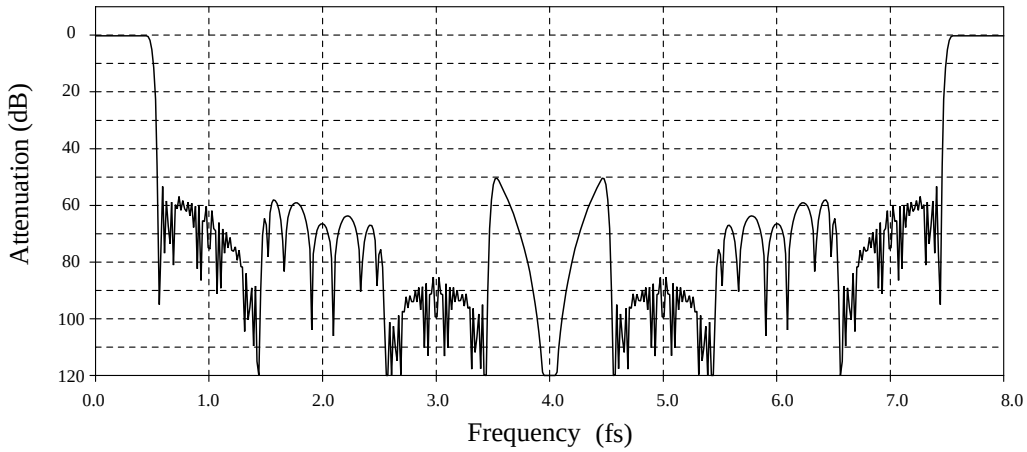


Filter Characteristics

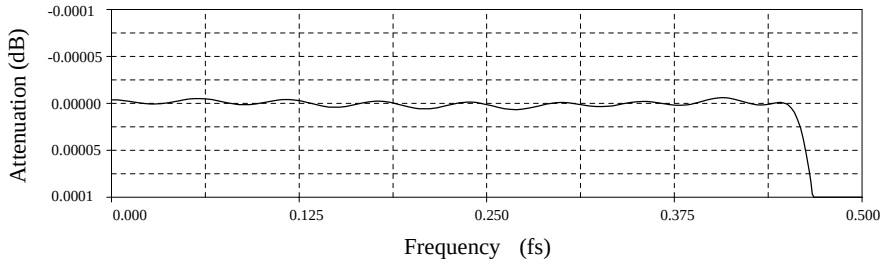
8-times interpolation filter

Parameter	Frequency		Rating (dB)		
	f	@ fs = 44.1 kHz	min	typ	max
Passband attenuation	0 to 0.4535fs	0 to 20 kHz	–	0.20	–
Passband ripple			–0.03	–	+0.03
Stopband attenuation	0.5465fs to 3.4535fs	24.1 to 152 kHz	53	–	–
	3.4535fs to 4.5465fs	152 to 201 kHz	50	–	–
	4.5465fs to 7.4535fs	201 to 328 kHz	53	–	–

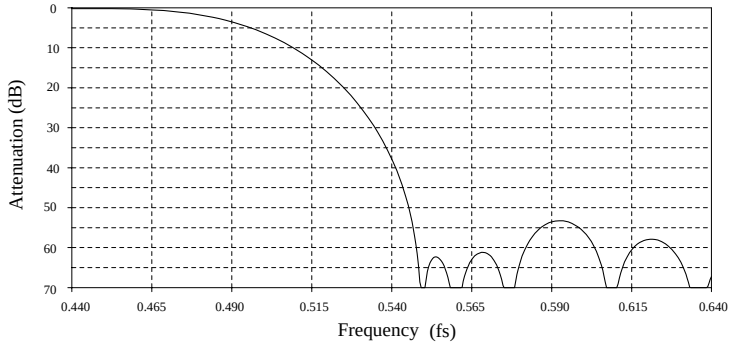
8fs filter response with deemphasis OFF



8fs filter passband response with deemphasis OFF



8fs filter band transition response with deemphasis OFF

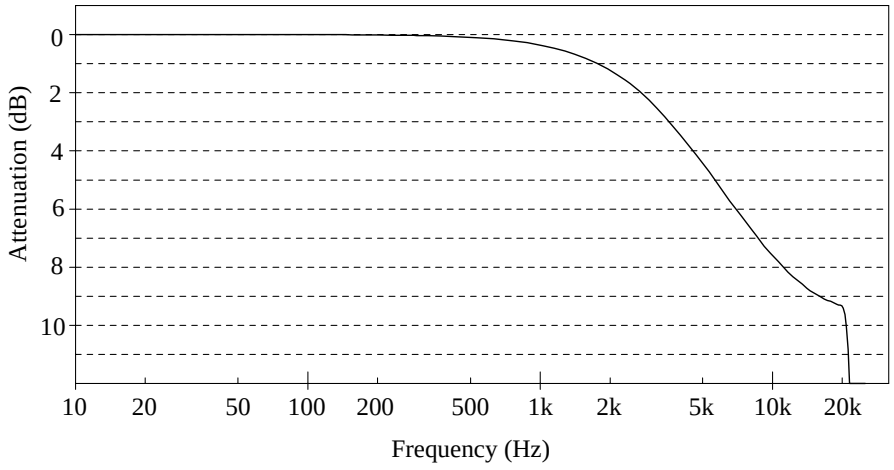


Deemphasis filter

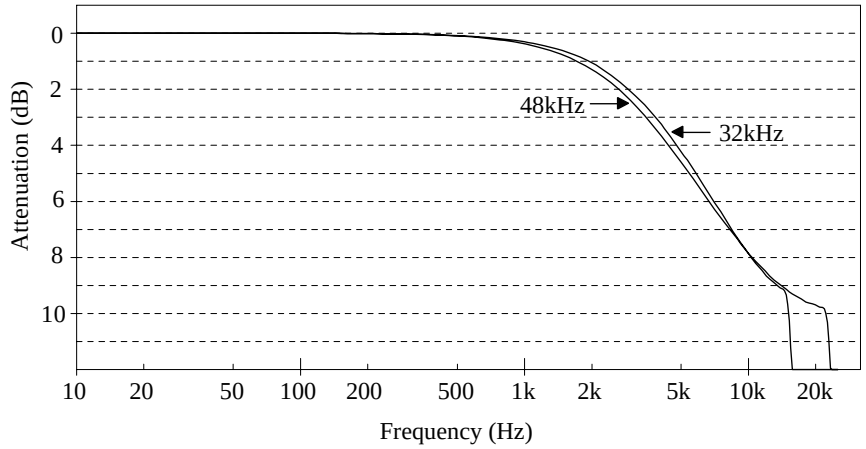
Parameter		Sampling frequency		
		32 kHz	44.1 kHz	48 kHz
Passband bandwidth (kHz)		0 to 14.5	0 to 20.0	0 to 21.7
Deviation from ideal characteristic[1]	Attenuation (dB)	–0.40 to +0.40	–0.05 to +0.15	–0.30 to +0.05
	Phase, θ (°)	–2 to 19	–1 to 15	–1 to 14

1. The maximum deviation from an ideal filter with 0 dB attenuation and 0° phase characteristics for a 1 kHz input signal.

Passband response with deemphasis ON (fs = 44.1 kHz)



Passband response with deemphasis ON (fs = 32/48 kHz)



FUNCTIONAL DESCRIPTION

The basic arithmetic block is shown in figure 1, and the function of each block is described in the following sections.

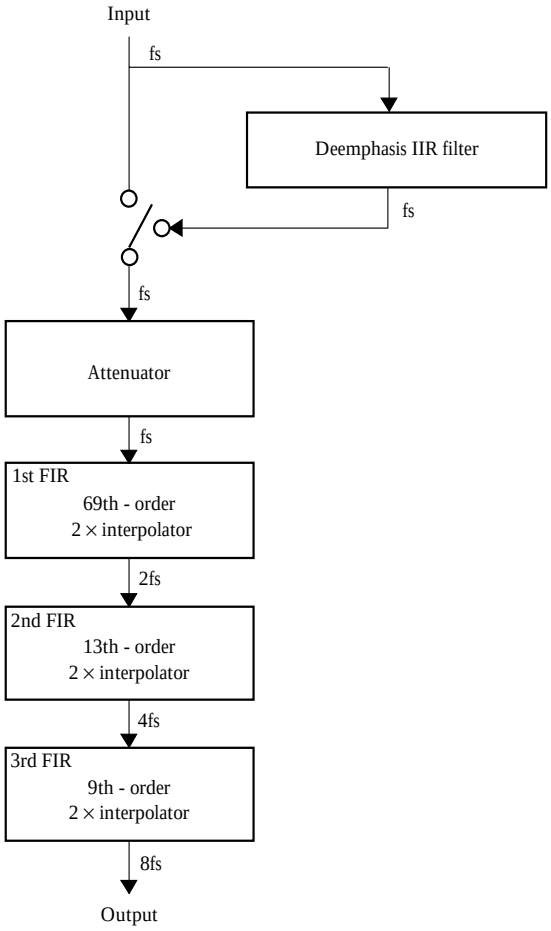


Figure 1. Arithmetic block diagram

8-times Oversampling (Interpolation)

The interpolation arithmetic block is comprised of 3 cascaded, 2-times FIR interpolation filters, as shown in figure 1.

The input signal is sampled at rate fs, and then 8-times oversampling data is output. Sampling noise in the 0.5465fs to 7.4535fs stopband is removed by the interpolation filter.

Digital Deemphasis (DSF1, DSF2)

The digital deemphasis filter has the same construction as analog filters. It is implemented as an IIR filter to faithfully reproduce the gain and phase characteristics of standard analog deemphasis filters. The filter coefficients for fs = 32.0/44.1/48.0 kHz sampling frequency are selected by DSF1 and DSF2 when the sampling frequency is specified, as shown in the following table.

DSF1	DSF2	Deemphasis	Sampling frequency
LOW	LOW	On	44.1 kHz
LOW	HIGH	On	48.0 kHz
HIGH	LOW	Off	–
HIGH	HIGH	On	32.0 kHz

System Clock (CKI, CKO, $\overline{CKSL}$)

Two system clock frequencies, 384fs and 256fs, can be used. The clock is input on CKI. The CKI input inverter has a feedback resistor to allow AC-coupled input clocks. The system clock is also buffered and then output on CKO. The system clock frequency selection and the internal clock frequency are shown in the following table.

Parameter	$\overline{CKSL}$	
	HIGH	LOW
CKI input system clock frequency (f_{SYS})	384fs	256fs
CKO clock frequency	384fs	256fs
Internal clock frequency	128fs	128fs
Serial output clock frequency	192fs	256fs

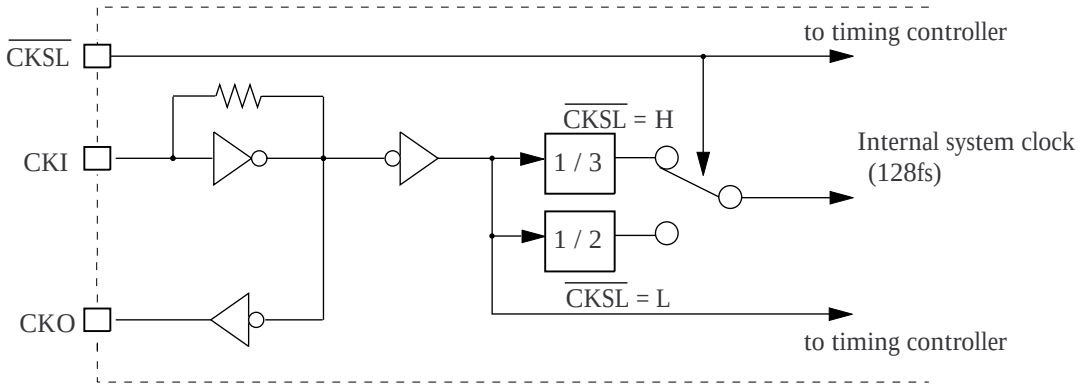


Figure 2. Clock generator circuit

Noise Shaper and I/O Data Length (WSL1, WSL2)

The SM5841H has functions that can be used to suppress the level of requantization noise due to the inherent arithmetic rounding-off that occurs in digital signal processing.

- 16/18-bit input
  The input interface accepts 16 and 18-bit input source data. That means that if 16-bit source data is digitally processed, for example in a sound field control or other DSP, the output can be input to the SM5841H without the same need for rounding-off, thereby avoiding the requantization noise that would otherwise occur.
- 16/18/20-bit output
  The output interface can support 18 and 20-bit output data, making connection to 18 or 20-bit D/A converters possible. As a result, the requantization noise generated after digital processing can be greatly reduced.
- Noise shaper function
  The 1st-order noise shaper processing occurs on the digital filter output. It reduces the requantization noise for 16 and 18-bit input signals to levels inherent in 18 and 20-bit output modes, respectively. The noise shaper does no processing on 20-bit output data.

There are 4 input data and output data length combinations possible, selected by the state of WSL1 and WSL2 as shown in the following table.

WSL1	WSL2	Noise shaper	Input bit length	Output bit length
HIGH	HIGH	Off	18 bits	20 bits
HIGH	LOW	On	18 bits	18 bits
LOW	HIGH	On	16 bits	18 bits
LOW	LOW	On	16 bits	16 bits

Audio Data Input (DIN, BCKI, LRCI)

The input data is in 16/18-bit serial, 2s complement, MSB first format.

Serial input data on DIN is clocked into an SIPO (serial in, parallel out) register on the rising edge of the BCKI bit clock, and then converted to parallel data.

SIPO output data is transferred into the left and right-channel input registers on the falling edge and rising edge, respectively, of the LRCI clock.

The internal arithmetic operation and output circuit timing is independent of the input timing. Accordingly, phase differences between LRCI, BCKI and CKI do not affect device operation, and any jitter in the data input clock does not cause jitter in the output clock.

Note that the device should be reset if either or both of the LRCI and CKI clocks stop. If the device is not reset, even though the clocks are low frequency, incorrect circuit operation may occur, generating unwanted output noise.

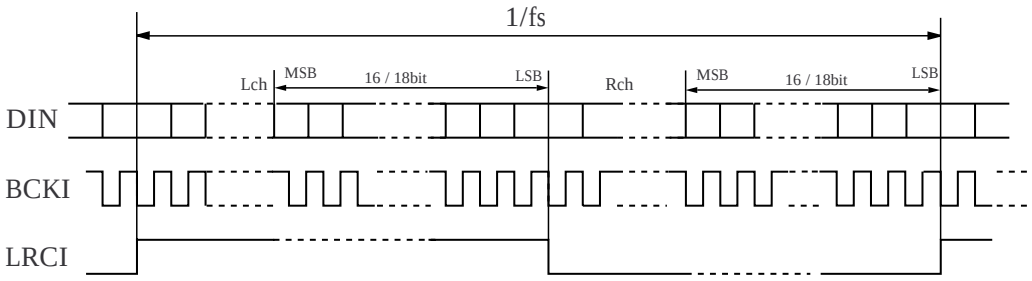


Figure 3. Audio data input timing

Audio Data Output (DOL, DOR, BCKO, WCKO, OFST)

The output data is in 16/18/20-bit serial, 8fs, simultaneous left and right-channel, 2s complement, MSB first format.

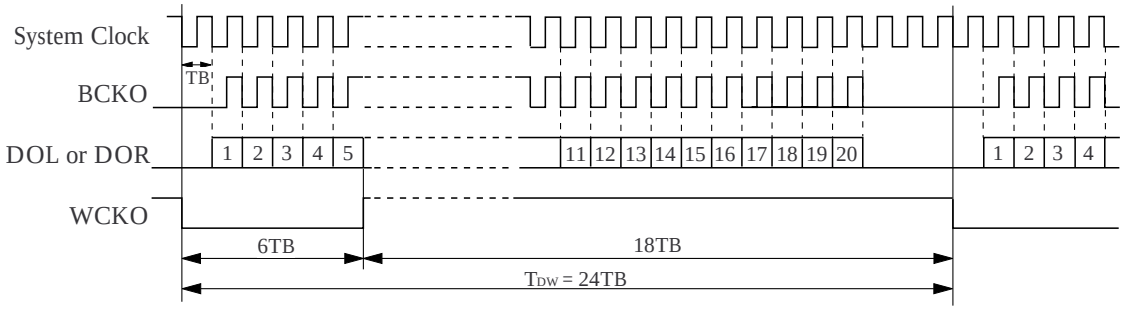
A DC offset can be added to arithmetic data before the data is output to reduce the D/A converter zero-crossing distortion for very small input signals. The offset added is approximately 0.8% of full-scale for the corresponding output bit length, as shown below.

- 512 LSB for 16-bit output
- 2048 LSB for 18-bit output
- 8192 LSB for 20-bit output

The DC offset is added to the output when OFST is HIGH. DC offset is OFF when OFST is LOW.

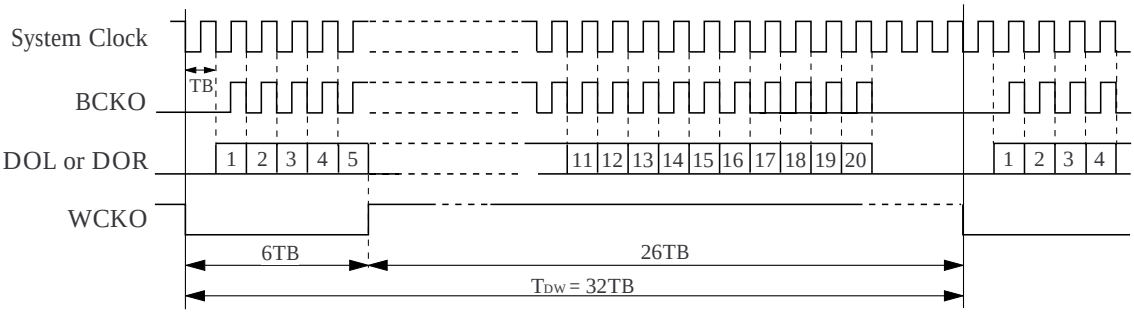
8fs serial data is output on independent DOL and DOR channels, in sync with the falling edge of the internal system clock and BCKO clock. The number of BCKO bit clock pulses per word changes depending on the output bit length selected (16/18/20 bits). Consequently, output data is latched into the D/A converter internal register on the falling of the edge of an output word clock WCKO, which has timing independent of the number of output bits as specified in the following table.

Parameter	Symbol	$\overline{CKSL}$ = HIGH	$\overline{CKSL}$ = LOW
Bit clock rate	T_B	t_{SYS} (1/192fs)	t_{SYS} (1/256fs)
Data word length	T_{DW}	$24T_B$	$32T_B$



The number of output bits is determined by the output bit length selected.

Figure 4. 8fs data output timing ($\overline{CKSL}$ = HIGH)



The number of output bits is determined by the output bit length selected.

Figure 5. 8fs data output timing ($\overline{CKSL}$ = LOW)

System Reset and Output Muting ($\overline{RST}$)

System reset

The SM5841H must be reset at power-ON by applying a LOW-level pulse on $\overline{RST}$.

At system reset, the arithmetic and output timing counters are reset on the next LRCI start edge, as long as the CKI clock has already stabilized.

The power-ON reset pulse can be applied by a microcontroller or, for systems where CKI and LRCI are stable at power-ON, by connecting a 300 pF capacitor between $\overline{RST}$ and VSS. For systems that do not use a microcontroller, the capacitor must be chosen such that the CKI and LRCI clocks fully stabilize before $\overline{RST}$ goes from LOW to HIGH.

If the system clock is interrupted or is corrupted by jitter, after power-ON reset and all internal timing is synchronized, such that a timing error greater than $\pm 3/8 \times f_{LRCI}$ occurs, the internal timing is automatically reset on the next LRCI start edge. This resynchronization affects the internal operation and can generate a momentary click noise output.

Output muting

When $\overline{RST}$ goes LOW, the DOL and DOR outputs go LOW, immediately muting the output signal, and they remain LOW for intervals in word units. Muting is released and timing is synchronized on the 3rd rising edge of LRCI after $\overline{RST}$ goes HIGH. Note that during muted output, the BCKO and WCKO clocks do not stop.

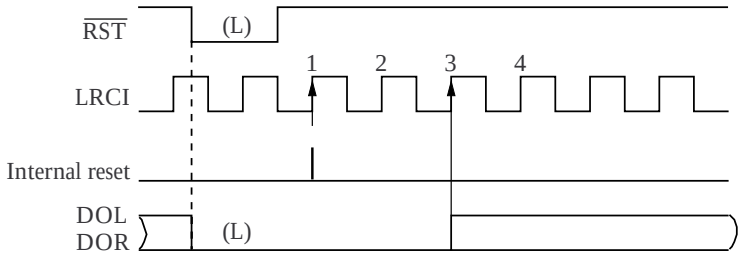


Figure 6. System reset timing and output muting

TIMING DIAGRAMS

Input Timing Examples (DIN, BCKI, LRCI)

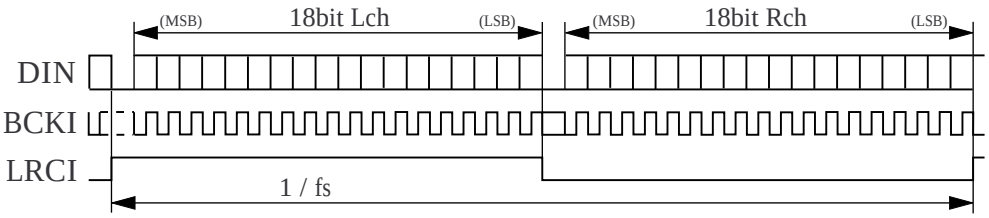


Figure 7. 18-bit input timing

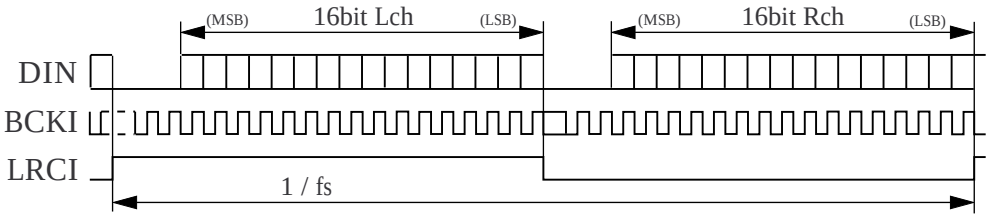
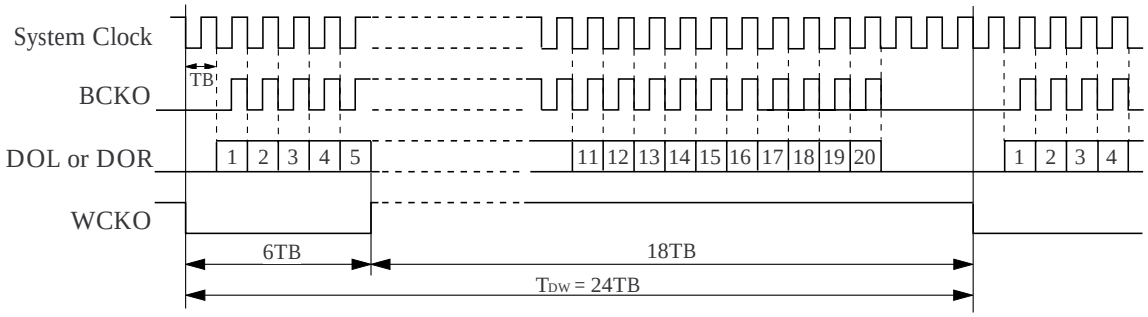


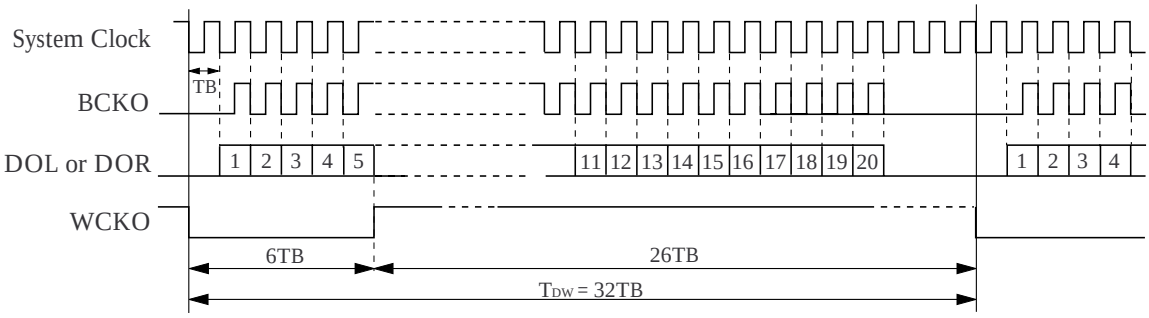
Figure 8. 16-bit input timing

Output Timing Examples (DOL, DOR, BCKO, WCKO)



The number of output bits is determined by the output bit length selected.

Figure 9. 8fs data output timing ($\overline{CKSL}$ = HIGH)

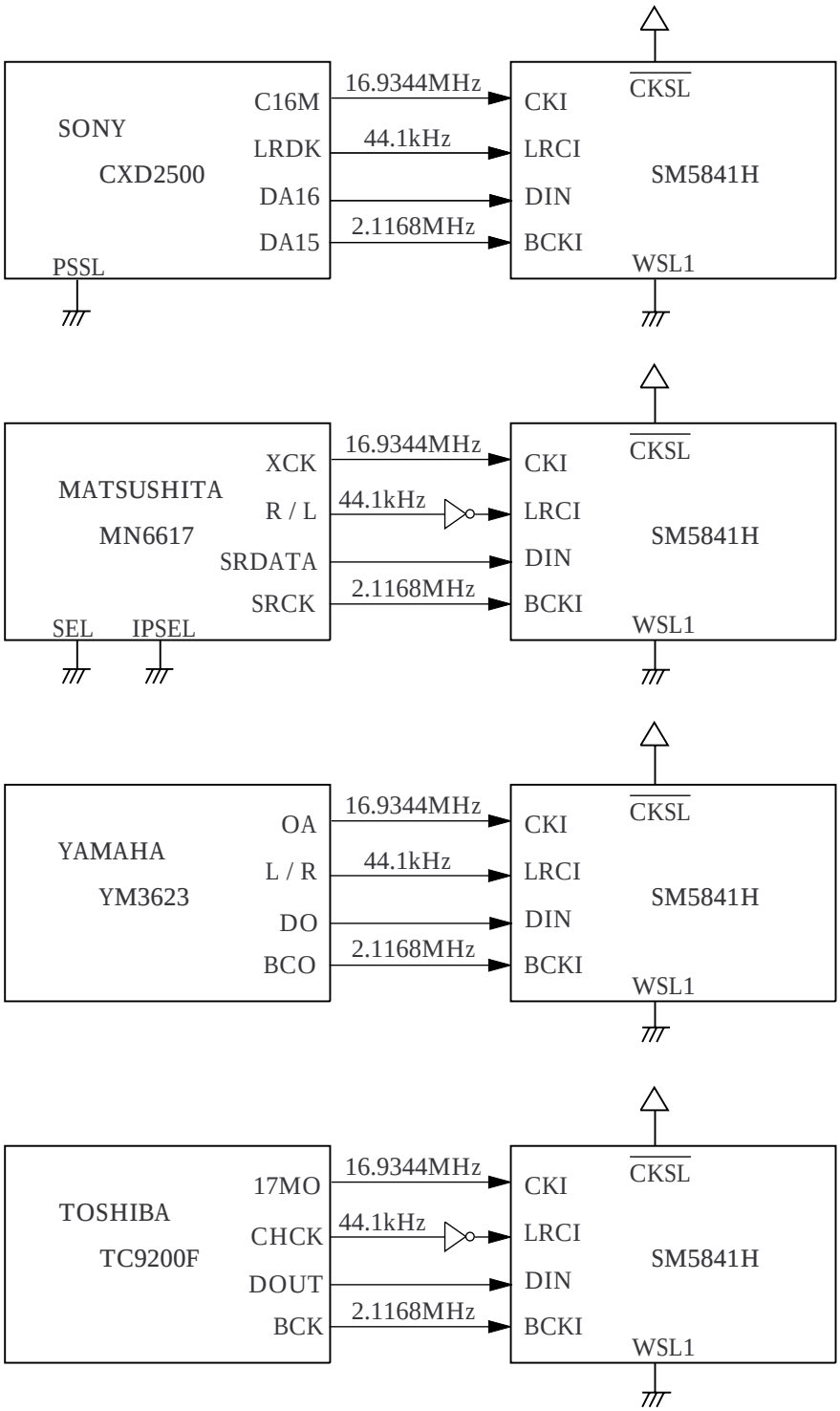


The number of output bits is determined by the output bit length selected.

Figure 10. 8fs data output timing ($\overline{CKSL}$ = LOW)

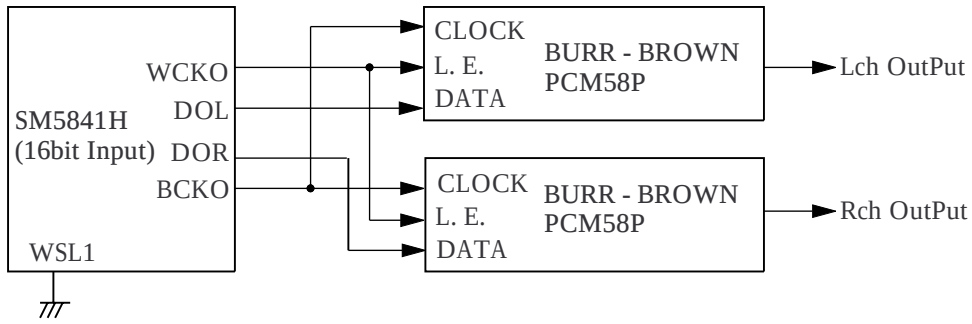
APPLICATION CIRCUITS

Input Interface Circuits



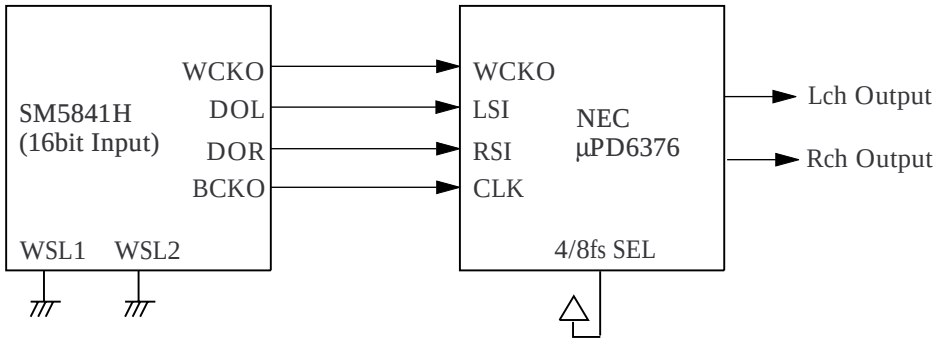
Output Interface Circuits

18-bit, 2-DAC (8fs L+R output mode)



This example is for 16-bit input mode, so WSL1 is tied HIGH. For 18-bit mode, WSL1 is tied LOW.

16-bit, 1-DAC (8fs L+R output mode)



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