



# STB55NF03L

## N-CHANNEL 30V - 0.01 $\Omega$ - 55A D<sup>2</sup>PAK STripFET™ POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB55NF03L	30 V	< 0.013 $\Omega$	55 A

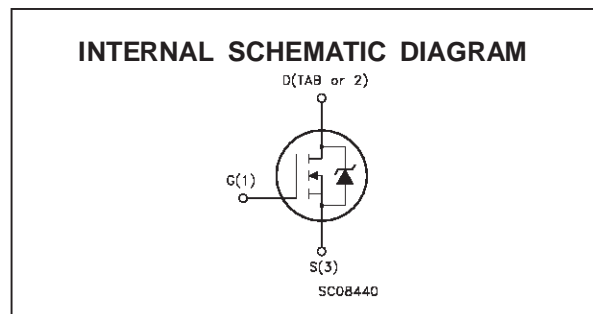
- TYPICAL R<sub>DS(on)</sub> = 0.01  $\Omega$
- OPTIMIZED FOR HIGH SWITCHING OPERATIONS
- LOW GATE CHARGE
- LOGIC LEVEL GATE DRIVE

### DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- LOW VOLTAGE DC-DC CONVERTERS
- HIGH CURRENT, HIGH SPEED SWITCHING
- HIGH EFFICIENCY SWITCHING CIRCUITS



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	30	V
V <sub>GS</sub>	Gate-source Voltage	$\pm 20$	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	55	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	39	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	220	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	80	W
	Derating Factor	0.53	W/°C
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

## STB55NF03L

### THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	1.875	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	$^{\circ}C/W$
$T_l$	Maximum Lead Temperature For Soldering Purpose		300	$^{\circ}C$

### ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$ $V_{GS} = 0$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$			$\pm 100$	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	1		2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$ $I_D = 27.5 A$ $V_{GS} = 4.5V$ $I_D = 27.5 A$		0.01 0.015	0.013 0.021	$\Omega$ $\Omega$
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	55			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 27.5 A$		40		S
$C_{iss}$	Input Capacitance	$V_{DS} = 25 V$ $f = 1 MHz$ $V_{GS} = 0$		1450		pF
$C_{oss}$	Output Capacitance			390		pF
$C_{rss}$	Reverse Transfer Capacitance			150		pF

**ELECTRICAL CHARACTERISTICS** (continued)

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 27.5\text{ A}$		25		ns
$t_r$	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		280		ns
$Q_g$	Total Gate Charge	$V_{DD} = 24\text{ V}$ $I_D = 55\text{ A}$ $V_{GS} = 4.5\text{ V}$		25	35	nC
$Q_{gs}$	Gate-Source Charge			11		nC
$Q_{gd}$	Gate-Drain Charge			12		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 27.5\text{ A}$		40		ns
$t_f$	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		60		ns

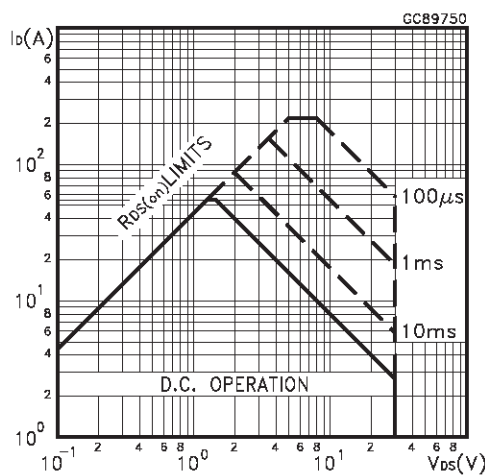
**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				55	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				220	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 55\text{ A}$ $V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 55\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		45		ns
$Q_{rr}$	Reverse Recovery Charge			52		nC
$I_{RRM}$	Reverse Recovery Current			2.3		A

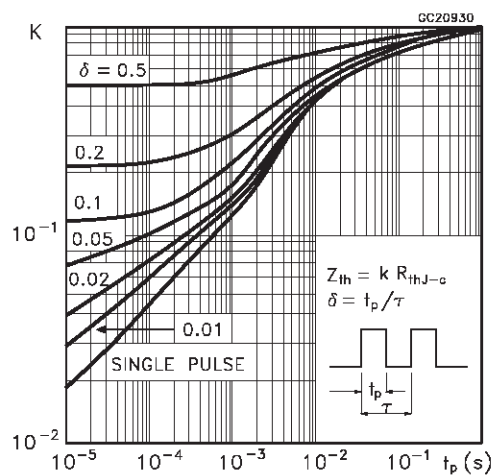
(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

(•) Pulse width limited by safe operating area

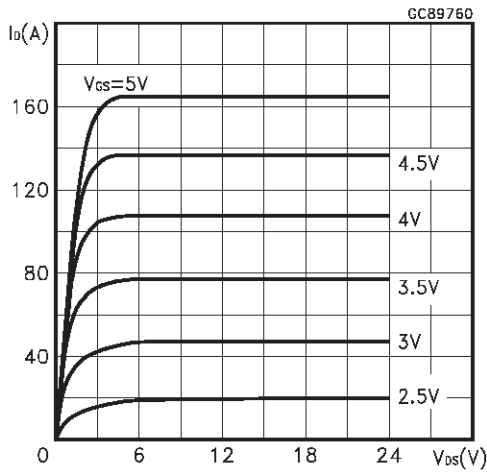
**Safe Operating Area**



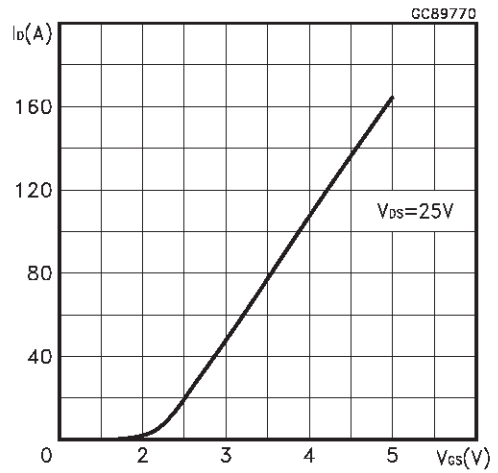
**Thermal Impedance**



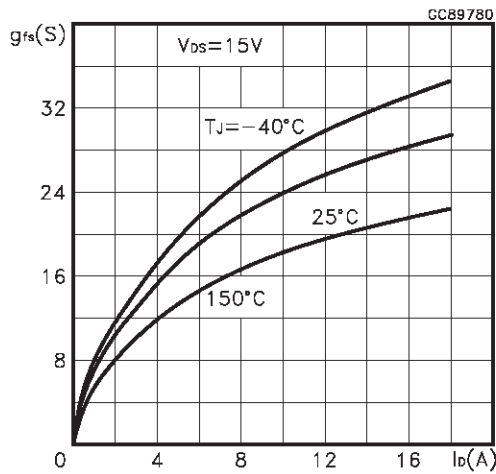
Output Characteristics



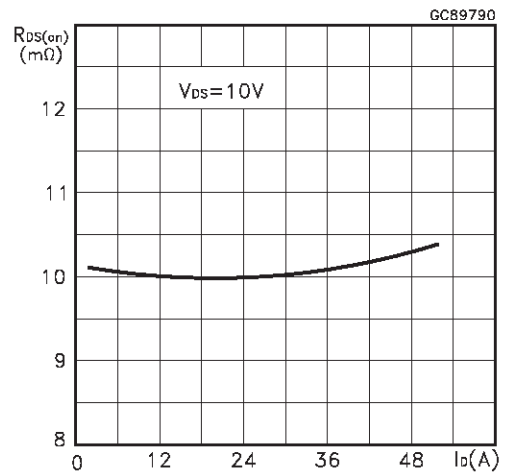
Transfer Characteristics



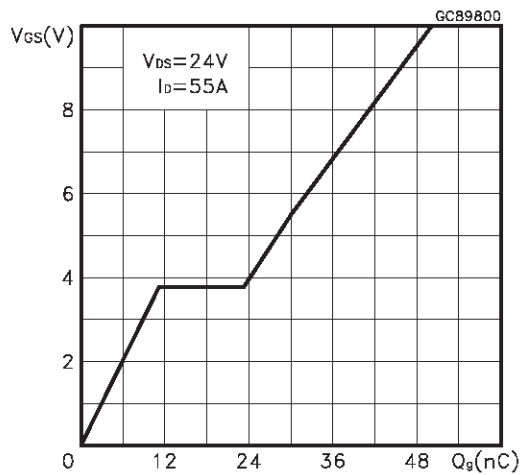
Transconductance



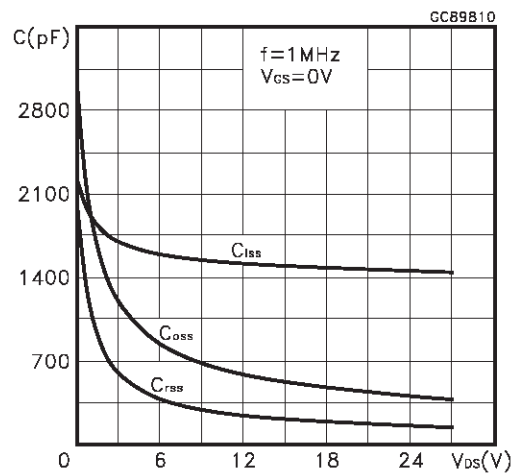
Static Drain-source On Resistance



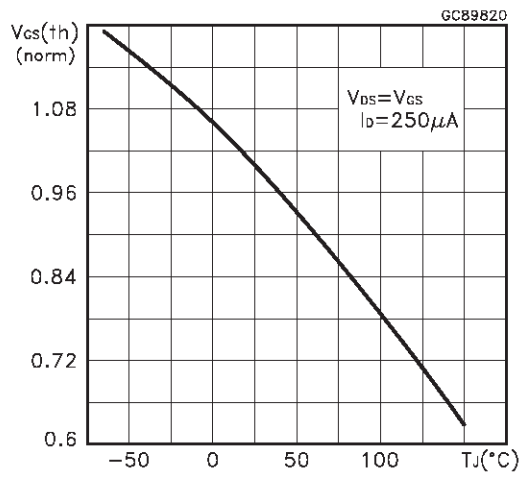
Gate Charge vs Gate-source Voltage



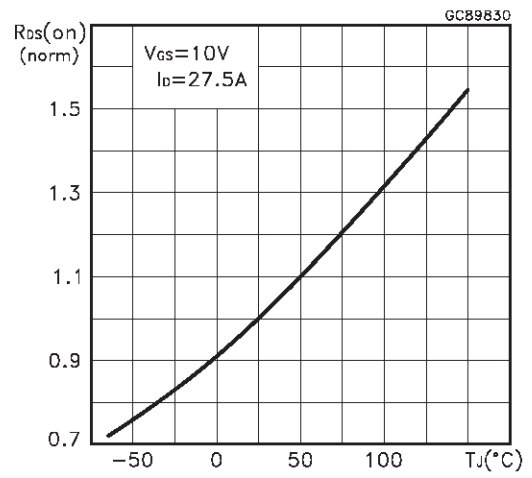
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

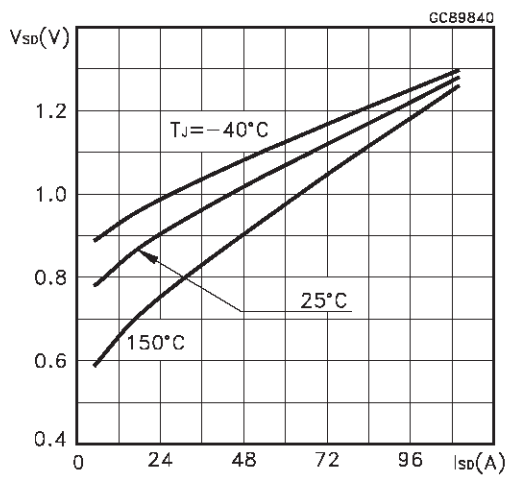


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Gate Charge test Circuit

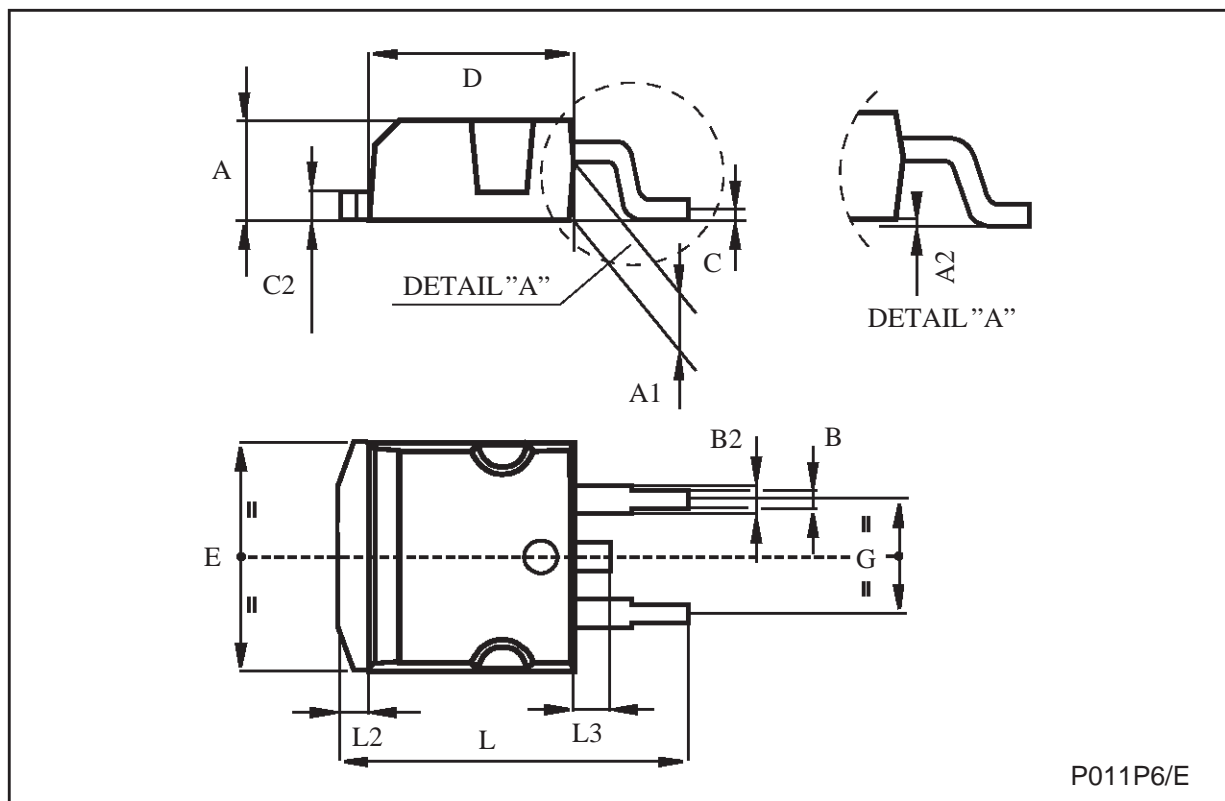


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-263 (D<sup>2</sup>PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.21		1.36	0.047		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



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