SONY

CXP881P60

CMOS 8-bit Single Chip Microcomputer

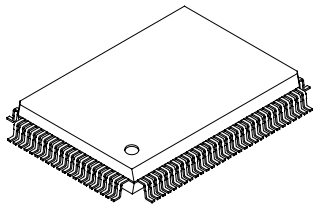
Description

The CXP881P60 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, high precision timing pattern generation circuits, PWM output, PWM for tuner, VISS/VASS circuit, 32kHz timer counter, remote control reception circuit, fluorescent display panel (FDP) controller/driver, VSYNC separator and the measurement circuit which measures signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, PROM, RAM and I/O port. They are integrated into a single chip.

Also, CXP881P60 provides sleep/stop function which enables to lower power consumption and ultra-low speed instruction mode in 32kHz operation.

The CXP881P60 is the PROM-incorporated version of the CXP88160 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

100 pin QFP (Plastic)



Structure

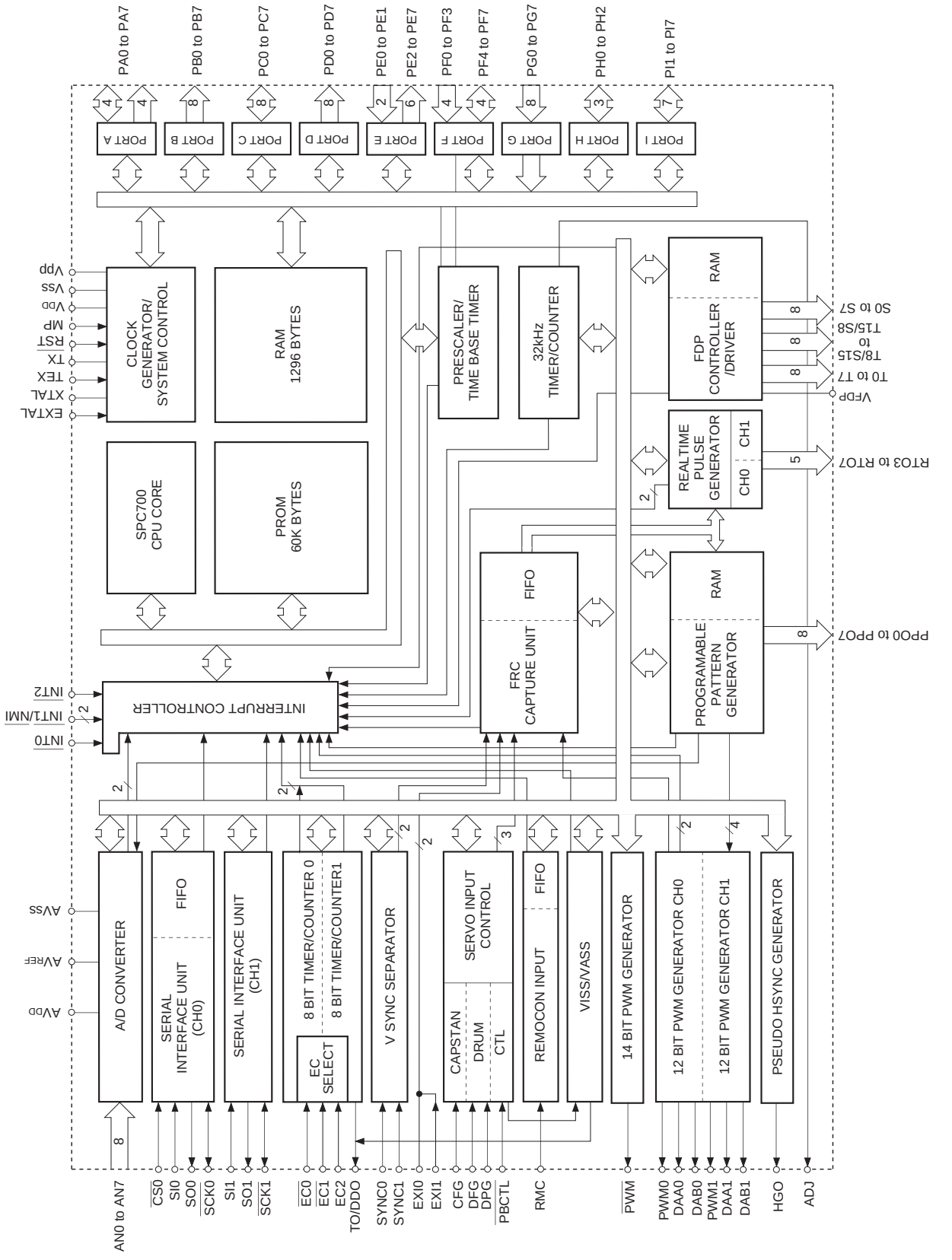
Silicon gate CMOS IC

Features

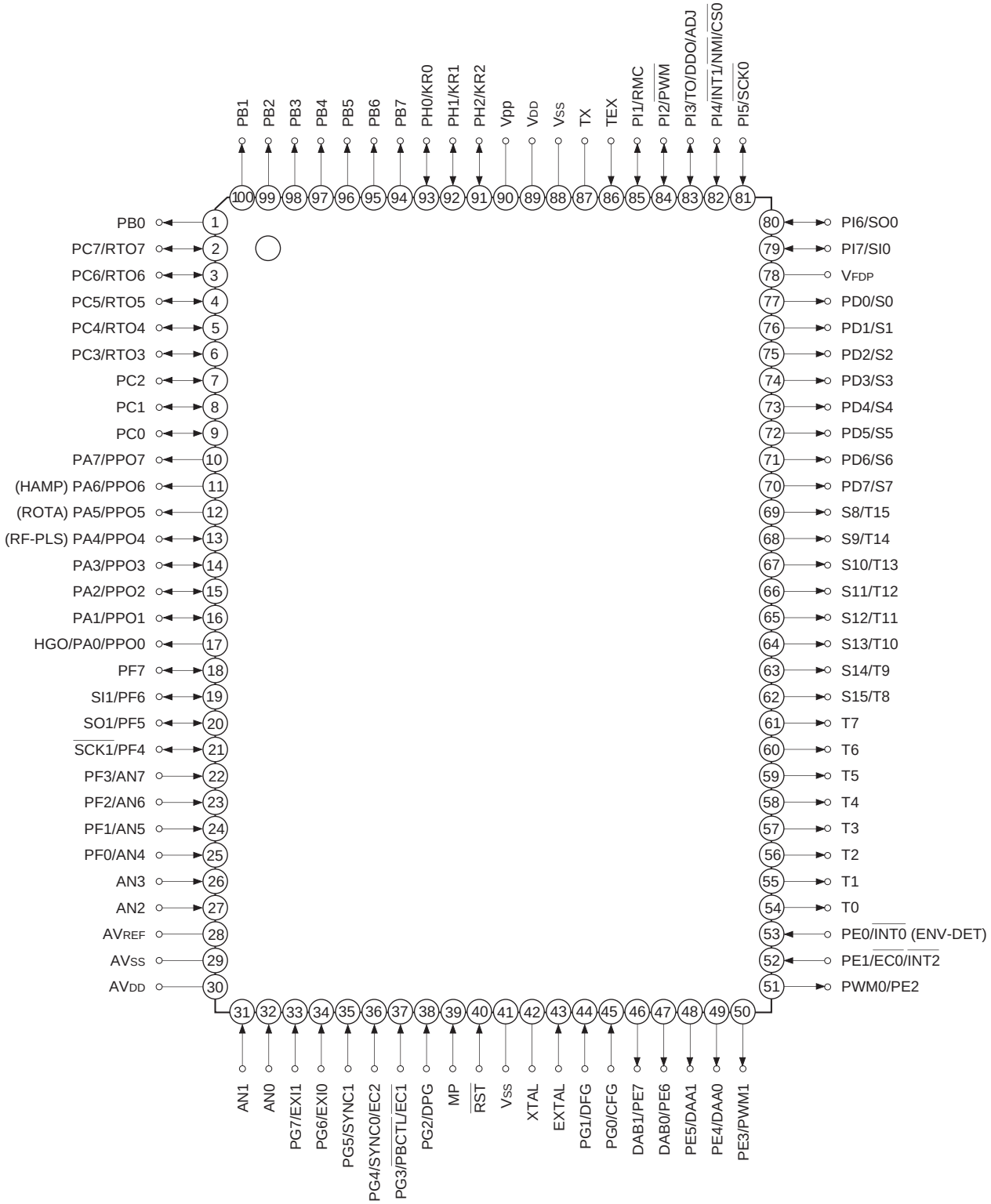
- A wide instruction set (213 instructions) which cover various types of data
  - — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle 250ns at 16MHz operation
  122µs at 32kHz operation
- Incorporated PROM capacity 60K bytes
- Incorporated RAM capacity 1296 bytes (including fluorescent display area)
- Peripheral function
  - — A/D converter: 8 bits, 8 channels, successive approximation system (Conversion time of 20µs/16MHz)
  - — Serial interface: Incorporated 8-bit 8-stage FIFO for data (Auto transfer for 1 to 8 bytes), 1 channel; 8-bit clock sync type, 1 channel
  - — Timer: 8-bit timer/counter, 2 channel; 19-bit time base timer; 32kHz timer/counter
  - — High precision timing pattern generator: PPG 8 pins, 21-stage programmable circuit; RTG 5 pins, 2 channels
  - — PWM/DA gate output: 12 bits, 2 channels (Repetitive frequency 62.5kHz/16MHz); DA gate pulse output, 13 bits, 4 channels
  - — Servo input control: Capstan FG, Drum FG/PG, CTL input
  - — VSYNC separator
  - — FRC capture unit: Incorporated 26-bit and 8-stage FIFO
  - — PWM output: 14 bits, 1 channel
  - — VISS/VASS circuit: Pulse duty auto detection circuit
  - — Remote control reception circuit: 8-bit pulse measurement counter, 6-stage FIFO
  - — Fluorescent display panel controller/driver: Maximum 144-segment display possible; Hardware key scan function (Maximum 16 x 3 key matrix available); Dimmer function; High voltage drive output (40V); Incorporated pull-down resistor (mask option)
  - — Tri-state output: PPG 1 pin, RTG 1 pin, output 8 pins
  - — Pseudo HSYNC output function
  - — High speed head switching circuit
- Interruption: 22 factors, 15 vectors, multi-interruption possible
- Standby mode: SLEEP/STOP
- Package: 100-pin plastic QFP

E95325-ST

Block Diagram



Pin Configuration (Top View)



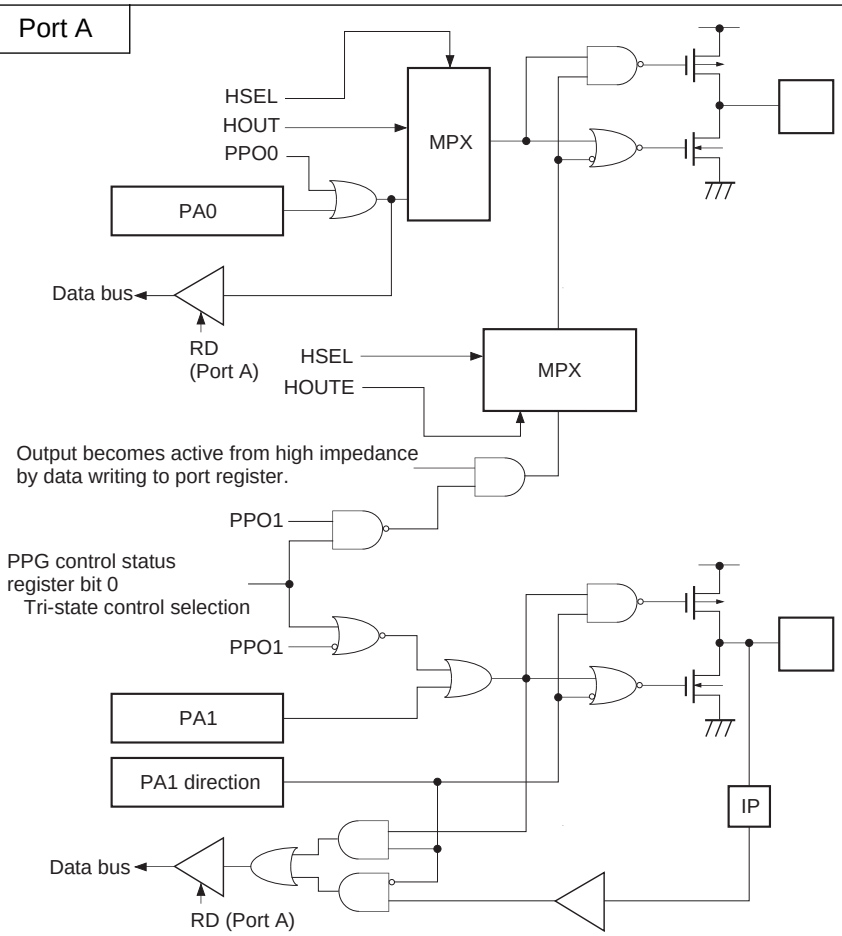
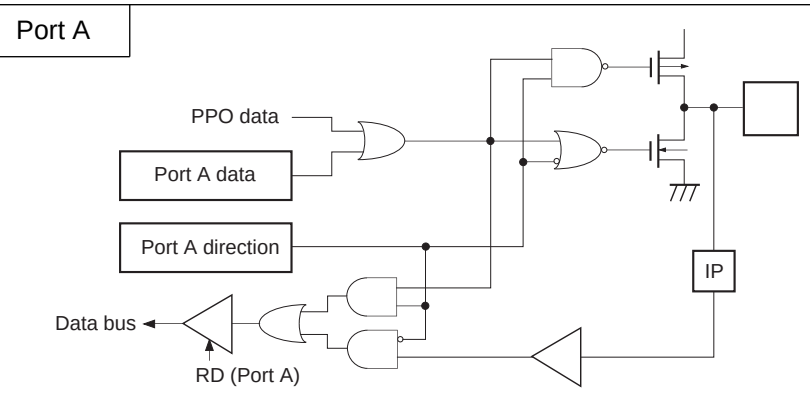
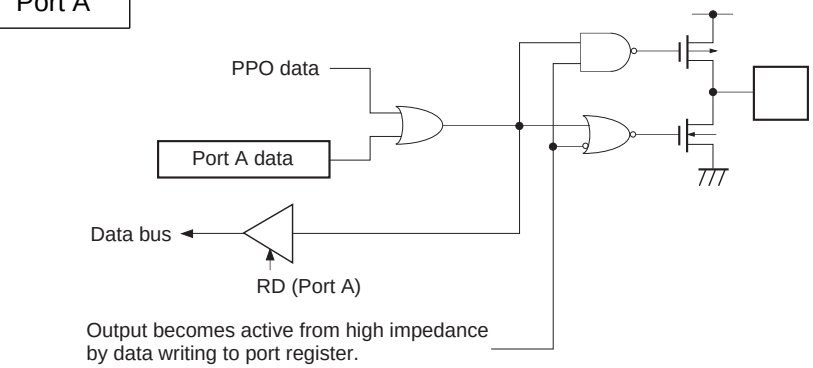
Note) 1. Vpp (Pin 90) is always connected to V_{DD}.
2. V_{SS} (Pins 41 and 88) are both connected to GND.
3. MP (Pin 39) must be connected to GND.

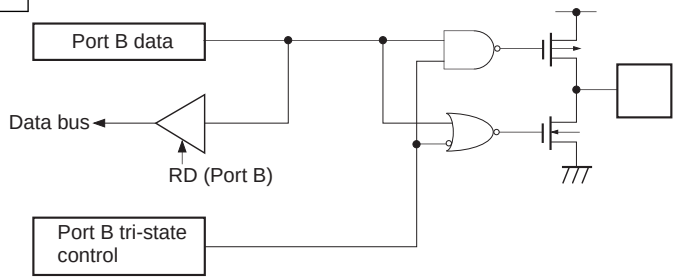
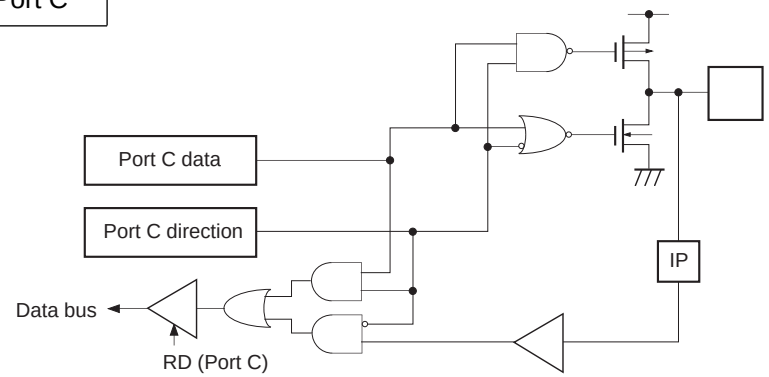
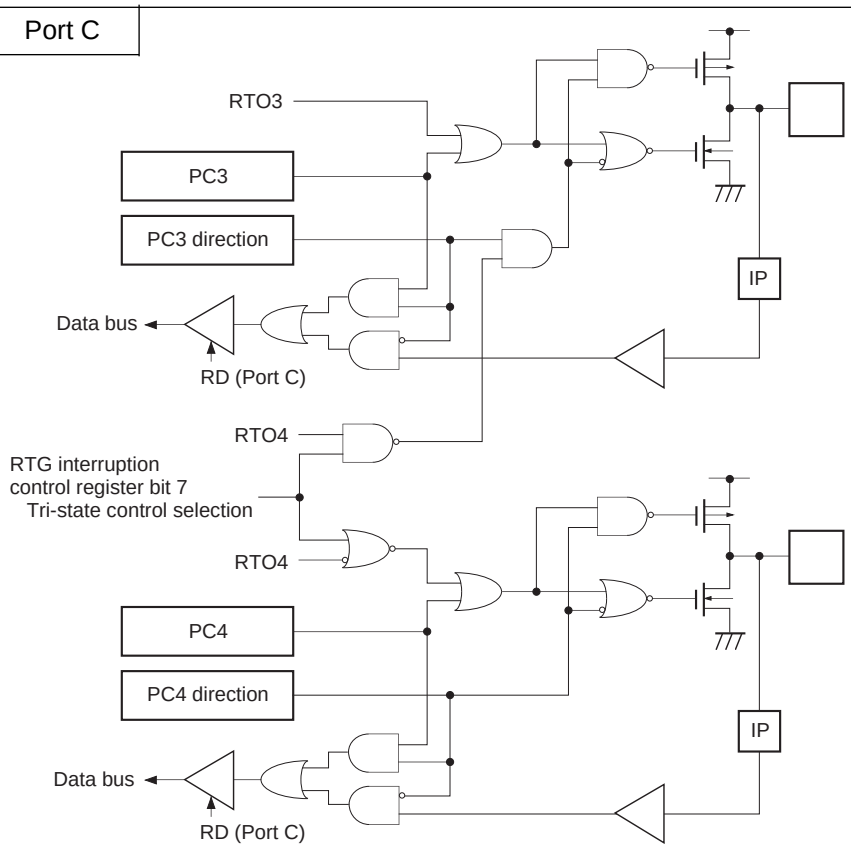
Pin Description

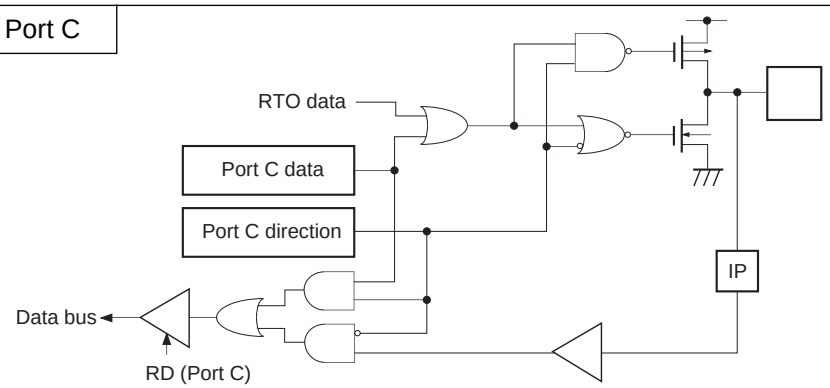
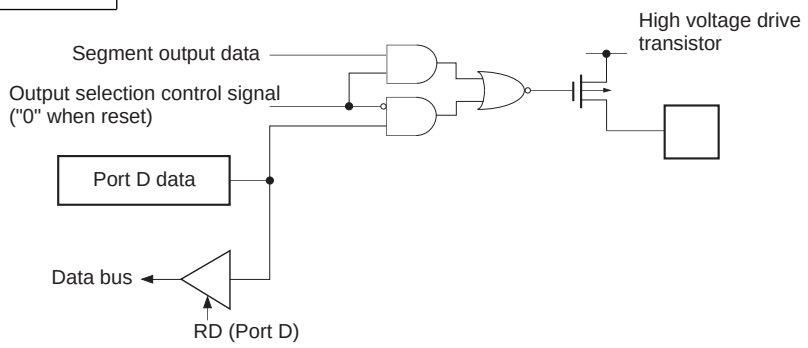
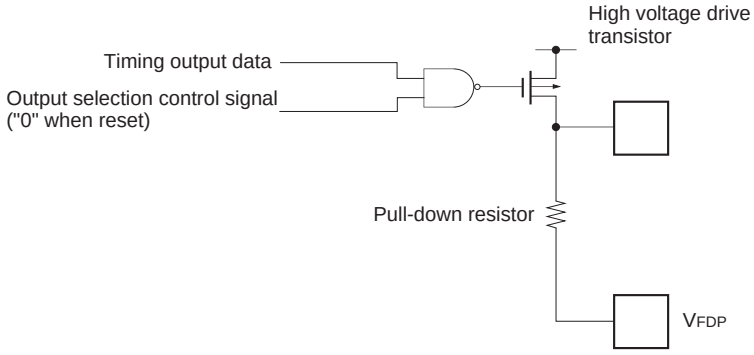
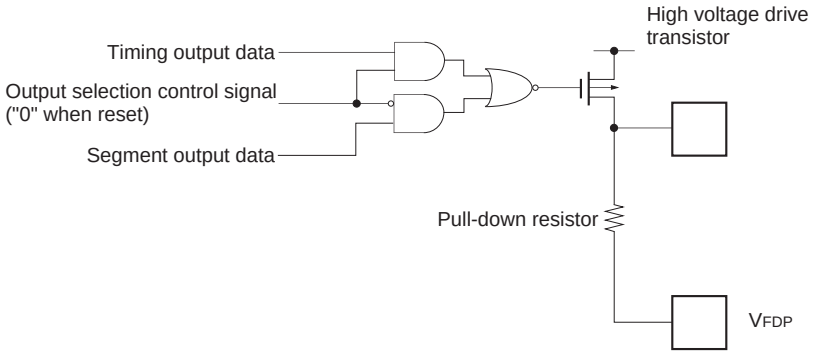
Symbol	I/O	Description		
PA0/PPO0/ HGO	Output/Real time output/Output	(Port A) PA0 and PA5 to PA7 are for outputs; PA1 to PA4 are for I/O. I/O can be set in a unit of single bits. Data is gated with PPO content by OR-gate and they are output. (8 pins)	Pseudo HSYNC output pin.	
PA1/PPO1	I/O/ Real time output		Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port. (8 pins)	
PA2/PPO2				
PA3/PPO3				
PA4/PPO4				
PA5/PPO5	Output/ Real time output		Head switching output pins. (2 pins)	
PA6/PPO6				
PA7/PPO7				
PB0 to PB7	Output	8-bit output port. Tri-state can be controlled. (8 pins)		
PC0 to PC2	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with RTO content by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real time output		Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins)	
T0 to T7	Output	FDP timing signal output pin. (8 pins)		
T8/S15 to T15/S8	Output/Output	Output pins for FDP timing signal and segment signal. (8 pins)		
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal output pin. (8 pins)	
PE0/$\overline{\text{INT0}}$	Input/Input	(Port E) 8-bit port. Lower 2 bits are for inputs; upper 6 bits are for outputs. (8 pins)	Trigger pulse input pin for head switching output.	Input pin to request external interruption. Active when falling edge.
PE1/$\overline{\text{EC0}}$/ $\overline{\text{INT2}}$	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/Output		PWM output pins. (2 pins)	
PE3/PWM1	Output/Output			
PE4/DAA0	Output/Output		DA gate pulse output pins. (4 pins)	
PE5/DAA1	Output/Output			
PE6/DAB0	Output/Output			
PE7/DAB1	Output/Output			
AN0 to AN3	Input	Analog input pins to A/D converter. (8 pins)		
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are for inputs; upper 4 bits are for I/O. I/O can be set in a unit of single bits. (8 pins)		
PF4/$\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.	
PF5/SO1	I/O/Output		Serial data (CH1) output pin.	
PF6/SI1	I/O/Input		Serial data (CH1) input pin.	
PF7	I/O			

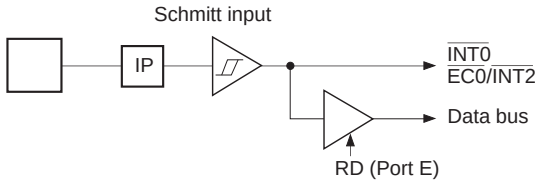
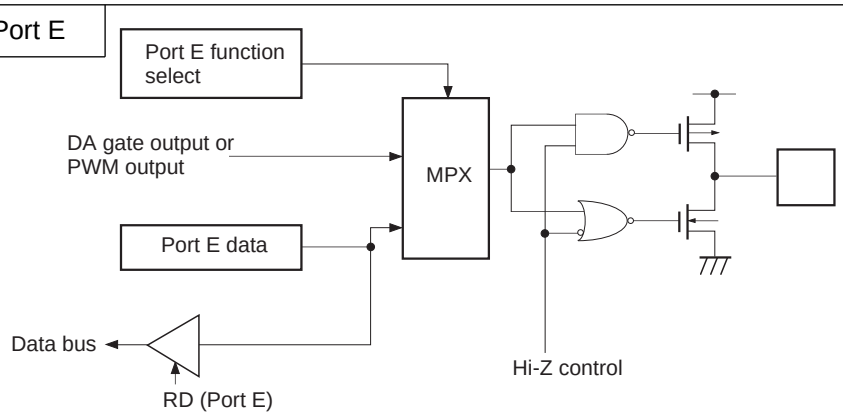
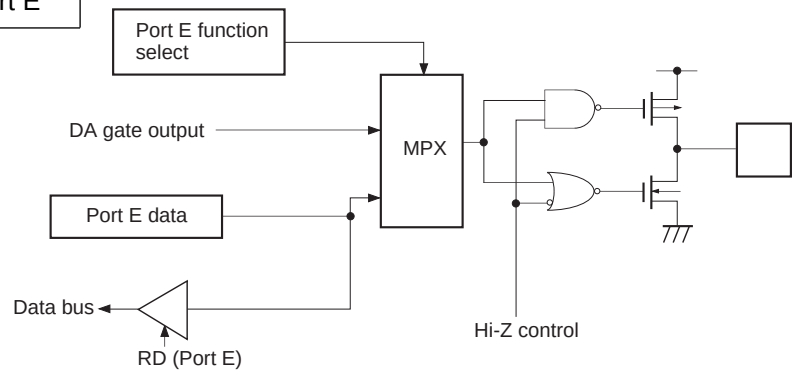
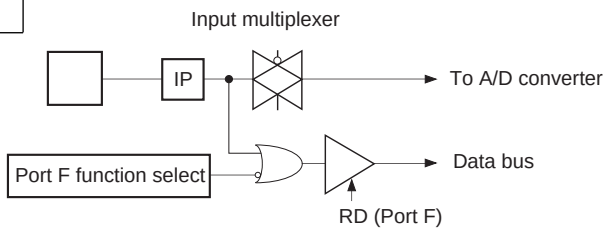
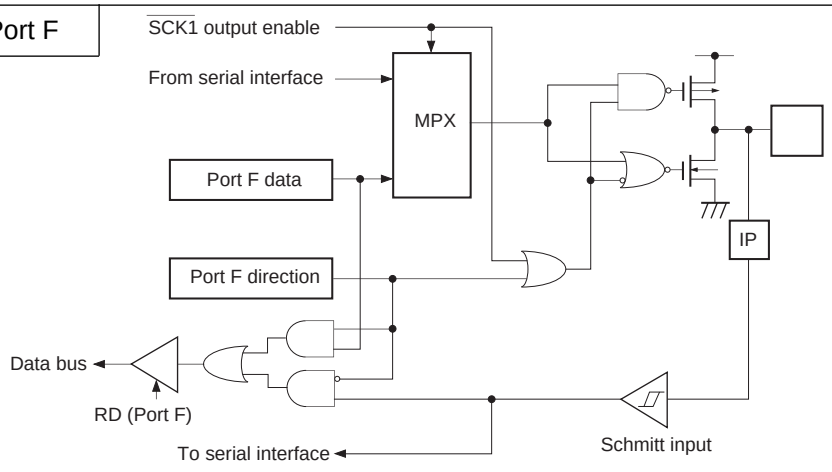
Symbol	I/O	Description		
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.	
PG1/DFG	Input/Input		Drum FG input pin.	
PG2/DPG	Input/Input		Drum PG input pin.	
PG3/ $\overline{\text{PBCTL}}$/$\overline{\text{EC1}}$	Input/Input/Input		Playback CTL input pin.	External event input pin for timer/counter.
PG4/ SYNC0/EC2	Input/Input/Input		Composite sync signal input pins.	External event input pin for timer/counter.
PG5/SYNC1	Input/Input			
PG6/EXI0	Input/Input		External input pins for FRC capture unit.	
PG7/EXI1	Input/Input			
PH0/KR0 to PH2/KR2	I/O/Input	(Port H) 3-bit I/O port. (3 pins)	Key return input signal for key scanning at FDP segment signal. (3 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O can be set in a unit of single bits. (7 pins)	Remote control reception circuit input pin.	
PI2/$\overline{\text{PWM}}$	I/O/Input		14-bit PWM output pin.	
PI3/TO/ DDO/ADJ	I/O/Output/ Output/Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.	
PI4/$\overline{\text{INT1}}$/ $\overline{\text{NMI}}$/CS0	I/O/Input/ Input/Input		Input pin to request external interruption, non-maskable interruption and for serial chip select (CH0). Active when falling edge.	
PI5/$\overline{\text{SCK0}}$	I/O/I/O		Serial clock (CH0) I/O pin.	
PI6/SO0	I/O/Output		Serial data (CH0) output pin.	
PI7/SI0	I/O/Input		Serial data (CH0) input pin.	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.		
XTAL	Output			
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (In this time, feedback resistor is not removed.)		
TX	Output			
$\overline{\text{RST}}$	Input	System reset pin of active "L" level.		
MP	Input	Test mode pin. Always connect to GND.		
V_{FDP}		FDP voltage supply pin when specifying internal resistor by mask option.		
AV_{DD}		Positive power supply pin of A/D converter.		
AV_{REF}	Input	Reference voltage input pin of A/D converter.		
AVss		GND pin of A/D converter.		
V_{DD}		Positive power supply pin.		
Vpp		Positive power supply pin for incorporated PROM writing connect to V_{DD} during normal operation.		
Vss		GND pin. Connect both Vss pins to GND.		

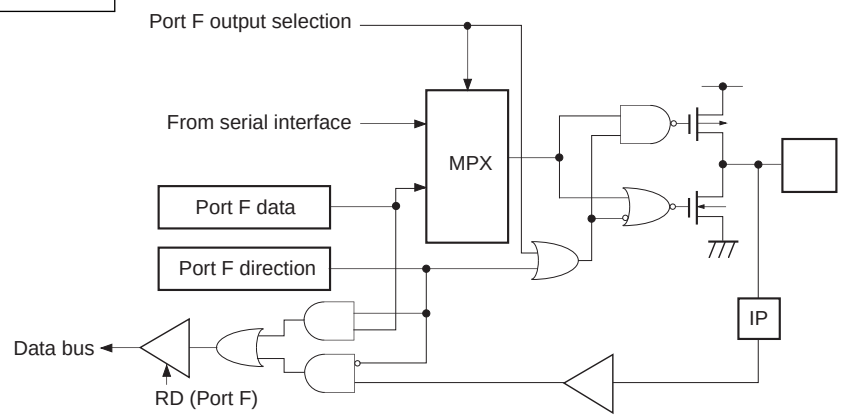
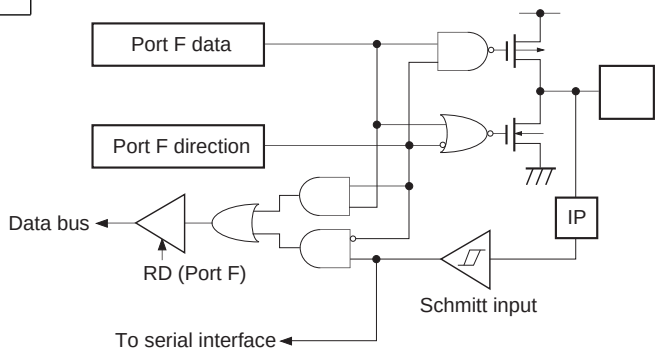
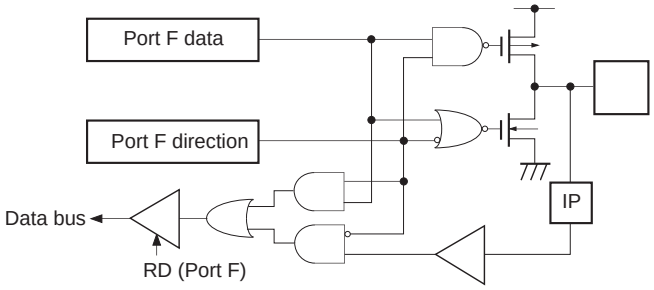
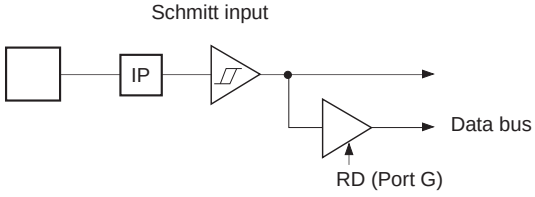
Input/Output Circuit Formats for Pins

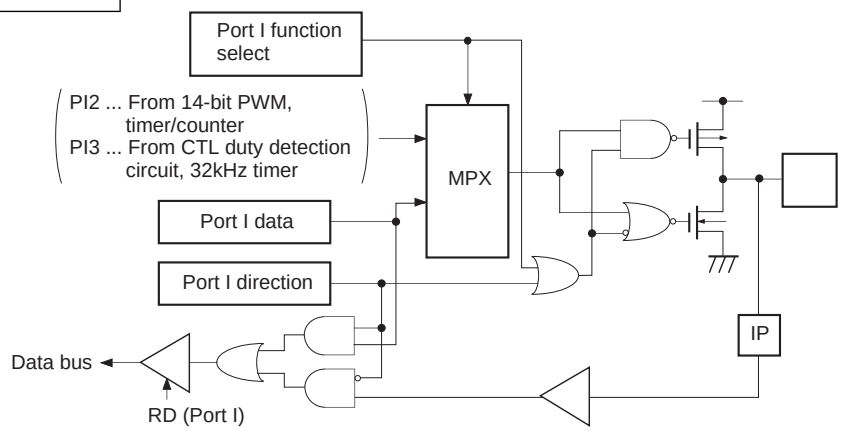
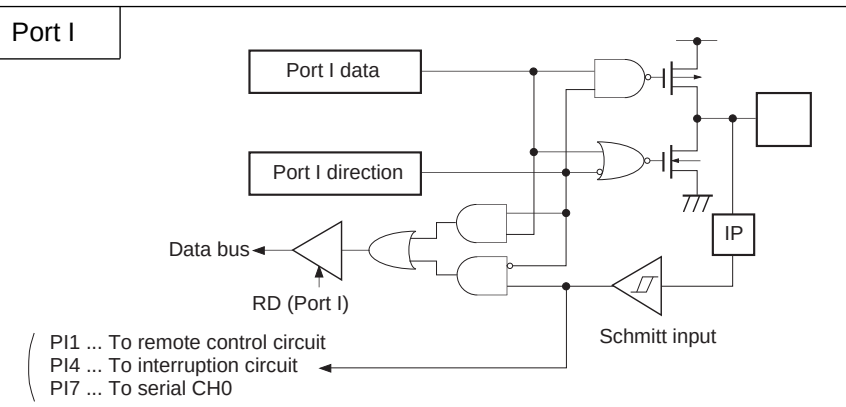
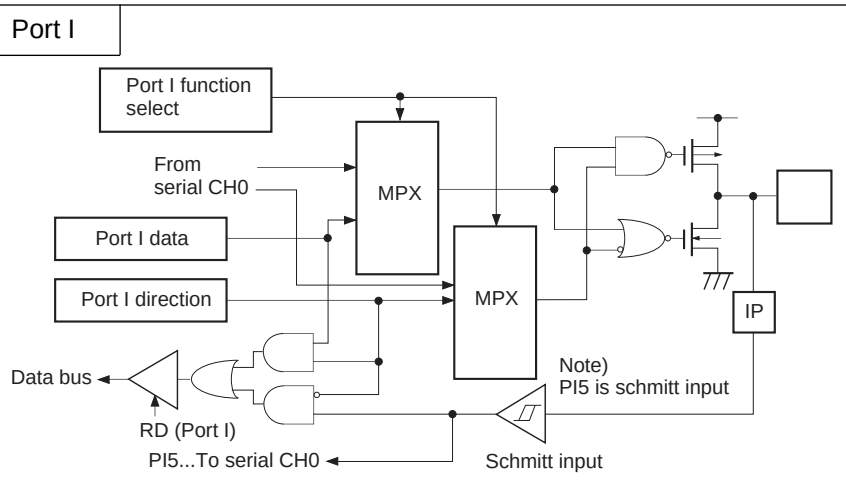
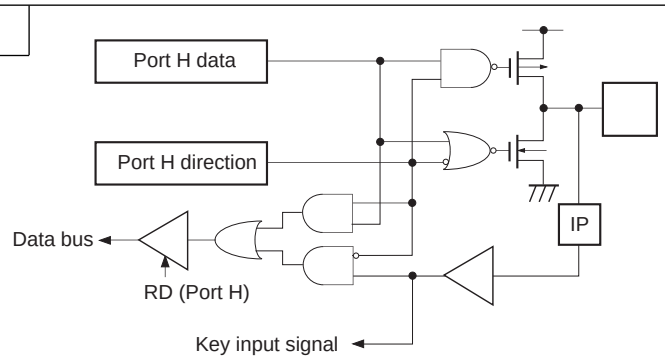
Pin	Circuit format	When reset
PA0/PPO0/ HGO 1 pin PA1/PPO1 1 pin	Port A 	Hi-Z Hi-Z
PA2/PPO2 to PA4/PPO4 3 pins	Port A 	Hi-Z
PA5/PPO5 to PA7/PPO7 3 pins	Port A 	Hi-Z

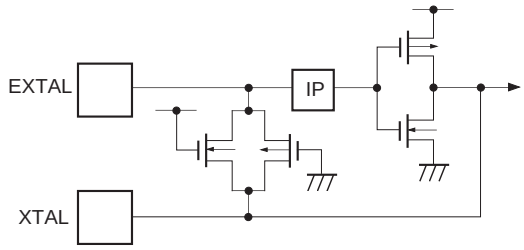
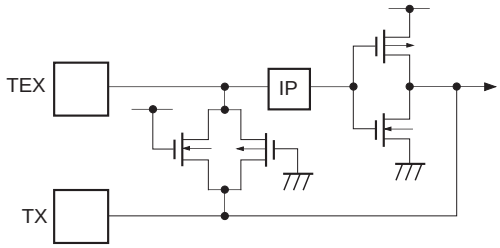
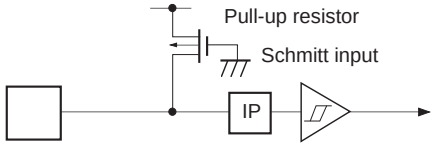
Pin	Circuit format	When reset
PB0 to PB7 8 pins	Port B 	Hi-Z
PC0 to PC2 3 pins	Port C 	Hi-Z
PC3/RTO3 1 pin PC4/RTO4 1 pin	Port C 	Hi-Z Hi-Z

Pin	Circuit format	When reset
PC5/RTO5 to PC7/RTO7 3 pins	Port C 	Hi-Z
PD0/S0 to PD7/S7 8 pins	Port D 	Hi-Z
T0 to T7 8 pins		Hi-Z
T8/S15 to T15/S8 8 pins		Hi-Z

Pin	Circuit format	When reset
PE0/$\overline{\text{INT0}}$ PE1/EC0/$\overline{\text{INT2}}$ 2 pins	Port E 	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E 	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E 	High level
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z
PF4/$\overline{\text{SCK1}}$ 1 pin	Port F 	Hi-Z

Pin	Circuit format	When reset
PF5/SO1 1 pin	Port F 	Hi-Z
PF6/SI1 1 pin	Port F 	Hi-Z
PF7 1 pin	Port F 	Hi-Z
PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL/ EC1 PG4/SYNC0/ EC2 PG5/SYNC1 PG6/EXI0 PG7/EXI1 8 pins	Port G 	Hi-Z

Pin	Circuit format	When reset
PI2/$\overline{\text{PWM}}$ PI3/TO/ DDO/ADJ 2 pins	Port I 	Hi-Z
PI1/RMC PI4/$\overline{\text{INT1}}$/ $\overline{\text{NMI}}$/$\overline{\text{CS0}}$ PI7/SI0 3 pins	Port I 	Hi-Z
PI5/$\overline{\text{SCK0}}$ PI6/SO0 2 pins	Port I 	Hi-Z
PH0/KR0 to PH2/KR2 3 pins	Port H 	Hi-Z

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop.	Hi-Z
TEX TX 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss=0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13	V	Incorporated PROM
	AV_{DD}	AVss to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
Display output voltage	V_{OD}	V_{DD}–40 to V_{DD}+0.3	V	As P-channel transistor is open drain, V_{DD} is reference.
High level output current	I_{OH}	–5	mA	All pins excluding display outputs (value per pin)*3
	I_{ODH1}	–15	mA	Display outputs S0 to S7 (value per pin)
	I_{ODH2}	–35	mA	Display outputs T0 to T7, and T8/S15 to T15/S8 (value per pin)
High level total output current	$\sum I_{OH}$	–50	mA	Total for all pins excluding display outputs
	$\sum I_{ODH}$	–100	mA	Total for all display outputs
Low level output current	I_{OL}	15	mA	
Low level total output current	$\sum I_{OL}$	130	mA	Total for all outputs
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

*1) AV_{DD} and V_{DD} should be set to the same voltage.

*2) V_{IN} and V_{OUT} should not exceed V_{DD}+0.3V.

*3) It specifies output current of general-purpose I/O port.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5		Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during STOP
	Vpp	Vpp = V_{DD}		V	*7
Analog power supply	AV_{DD}	4.5	5.5	V	*1
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS schmitt input*3
	V_{IHTS}	2.2	V_{DD}	V	TTL schmitt input*4
	V_{IHEX}	V_{DD}–0.4	V_{DD}+0.3	V	EXTAL pin*5 TEX pin*6
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2
	V_{ILS}	0	0.2V_{DD}	V	CMOS schmitt input*3
	V_{ILTS}	0	0.8	V	TTL schmitt input*4
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*5 TEX pin*6
Operating temperature	Topr	–10	+75	°C	

*1) AV_{DD} and V_{DD} should be set to the same voltage.

*2) Normal input port (each pin of PA1 to PA4, PC, PF0 to PF3, PF5, PF7, PH, PI2, PI3 and PI6), MP pin

*3) Each pin of $\overline{RST}$, PE0/$\overline{INT0}$, PE1/$\overline{EC0}$/$\overline{INT2}$, PF4/$\overline{SCK1}$, PF6/SI1, PI1/RMC, PI4/$\overline{CS0}$/$\overline{NMI}$/$\overline{INT1}$, PI5/$\overline{SCK0}$, PI7/SI1, PG0/CFG, PG1/DFG, PG2/DPG, PG3/$\overline{PBCTL}$/$\overline{EC}$, PG6/EXI0, PG7/EXI1.

*4) Each pin of PG4/SYNC0/EC2, PG5/SYNC1.

*5) It specifies only when the external clock is input.

*6) It specifies only when the external event is input.

*7) Vpp and V_{DD} should be set to the same voltage.

DC Characteristics (Ta=–10 to +75°C, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PC, PE PF4 to PF7, PH, PI1 to PI7	V_{DD}=4.5V, I_{OH}=–0.5mA	4.0			V
			V_{DD}=4.5V, I_{OH}=–1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD}=4.5V, I_{OL}=1.8mA			0.4	V
			V_{DD}=4.5V, I_{OL}=3.6mA			0.6	V
Display output current	I_{OH}	S0 to S7	V_{DD}=4.5V, V_{OH}=V_{DD}–2.5V	–8			mA
		S8/T15 to S15/T8, T0 to T7		–20			mA
Open drain output leakage current (P-CH Tr OFF in state)	I_{LOL}	S0 to S7, S8/T15 to S15/T8, T0 to T7	V_{DD}=5.5V, V_{OL}=V_{DD}–35V V_{FDP}=V_{DD}–35V			–20	µA
Pull-down resistor	R_L	S8/T15 to S15/T8, T0 to T7	V_{DD}=5V, V_{OD}–V_{FDP}=30V	60	100	270	kΩ
Input current	I_{IHE}	EXTAL	V_{DD}=5.5V, V_{IH}=5.5V	0.5		40	µA
			V_{DD}=5.5V, V_{IL}=0.4V	–0.5		–40	µA
	I_{ILE}	TEX	V_{DD}=5.5V, V_{IH}=5.5V	0.1		10	µA
			V_{DD}=5.5V, V_{IL}=0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$		–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PC, PE to PI, AN1 to AN3, MP	V_{DD}=5.5V, V_I=0, 5.5V			±10	µA
Supply current*1	I_{DD1}	V_{DD}, Vss	16MHz crystal oscillation (C_1=C_2=15pF), V_{DD}=5V±0.5V*2		28	50	mA
	I_{DDS1}		16MHz crystal oscillation (C_1=C_2=15pF), V_{DD}=5V±0.5V, SLEEP mode		1.7	8	mA
	I_{DD2}		32kHz crystal oscillation (C_1=C_2=47pF), V_{DD}=3V±0.3V		0.8	2	mA
	I_{DDS2}		32kHz crystal oscillation (C_1=C_2=47pF), V_{DD}=3V±0.3V, SLEEP mode		3	35	µA
	I_{DDS3}		V_{DD}=5.5V, STOP mode (32kHz, 16MHz oscillation stop)			30	µA
Input capacity	C_{IN}	PA1 to PA4 PC0 to PC7 PE0, PE1 AN0 to AN3 PF0 to PF7 PG0 to PG7 PH0 to PH2 PI1 to PI7	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) When entire output pins are open.
*2) When setting upper 2 bits (CPU clock selection) of clock control register (CLC: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing (Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC0}$, $\overline{EC1}$, EC2	Fig. 3	tsys+200*1			ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC0}$, $\overline{EC1}$, EC2	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD}=2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1) tsys indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).
tsys [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Fig. 1. Clock timing

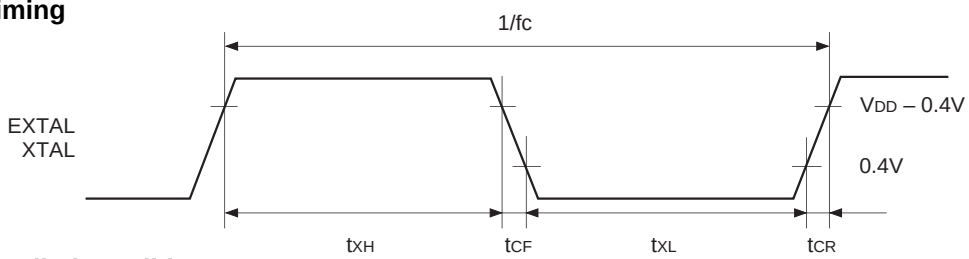


Fig. 2. Clock applied condition

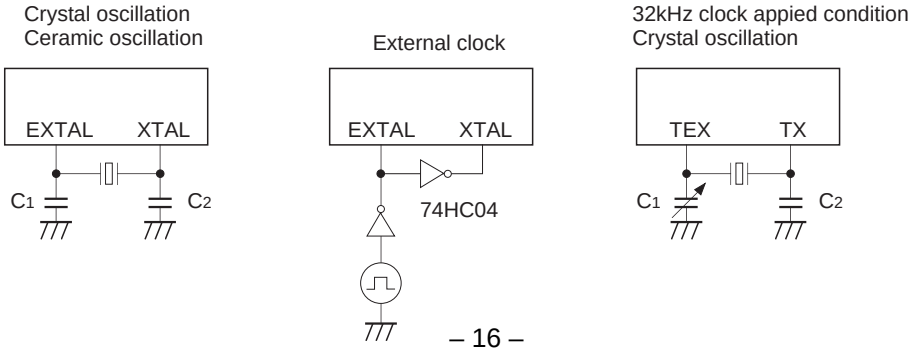
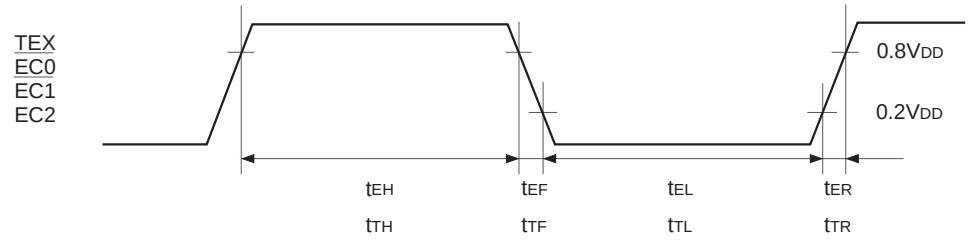


Fig. 3. Event count clock timing



(2) Serial transfer (CH0) (Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

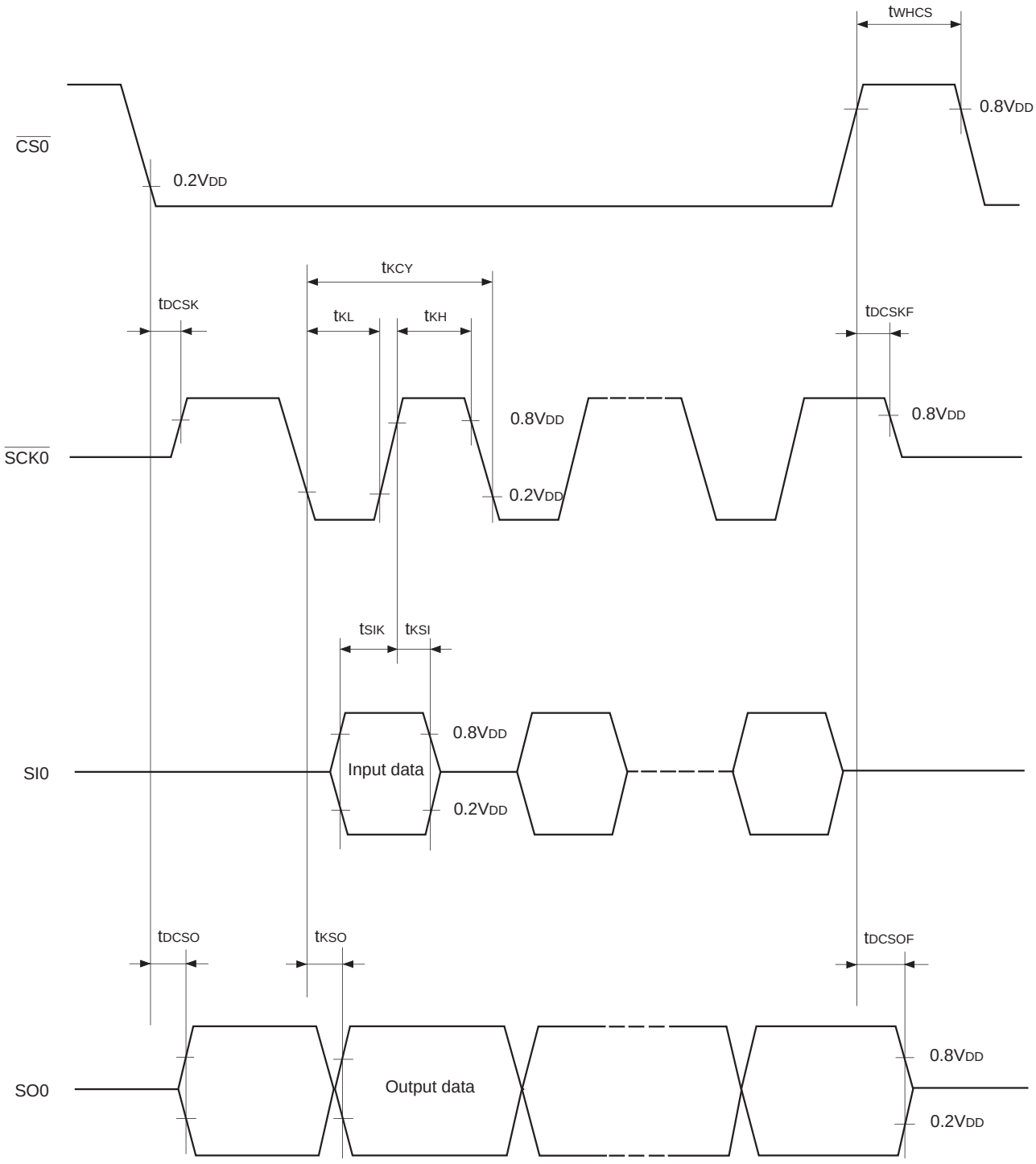
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0}\downarrow\rightarrow\overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$=output mode)		tsys+200	ns
$\overline{CS0}\uparrow\rightarrow\overline{SCK0}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$=output mode)		tsys+200	ns
$\overline{CS0}\downarrow\rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys+200	ns
$\overline{CS0}\uparrow\rightarrow$ SO0 floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys+200	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys+200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys+200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys+100		ns
			Output mode	8000/fc–50		ns
SI0 input set-up time (against $\overline{SCK0}\uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0}\uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys+200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0}\downarrow\rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys+200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC; 00FE$_H$) upper 2 bits (CPU clock selection).

tsys [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF +1TTL.

Fig. 4. Serial transfer timing (CH0)

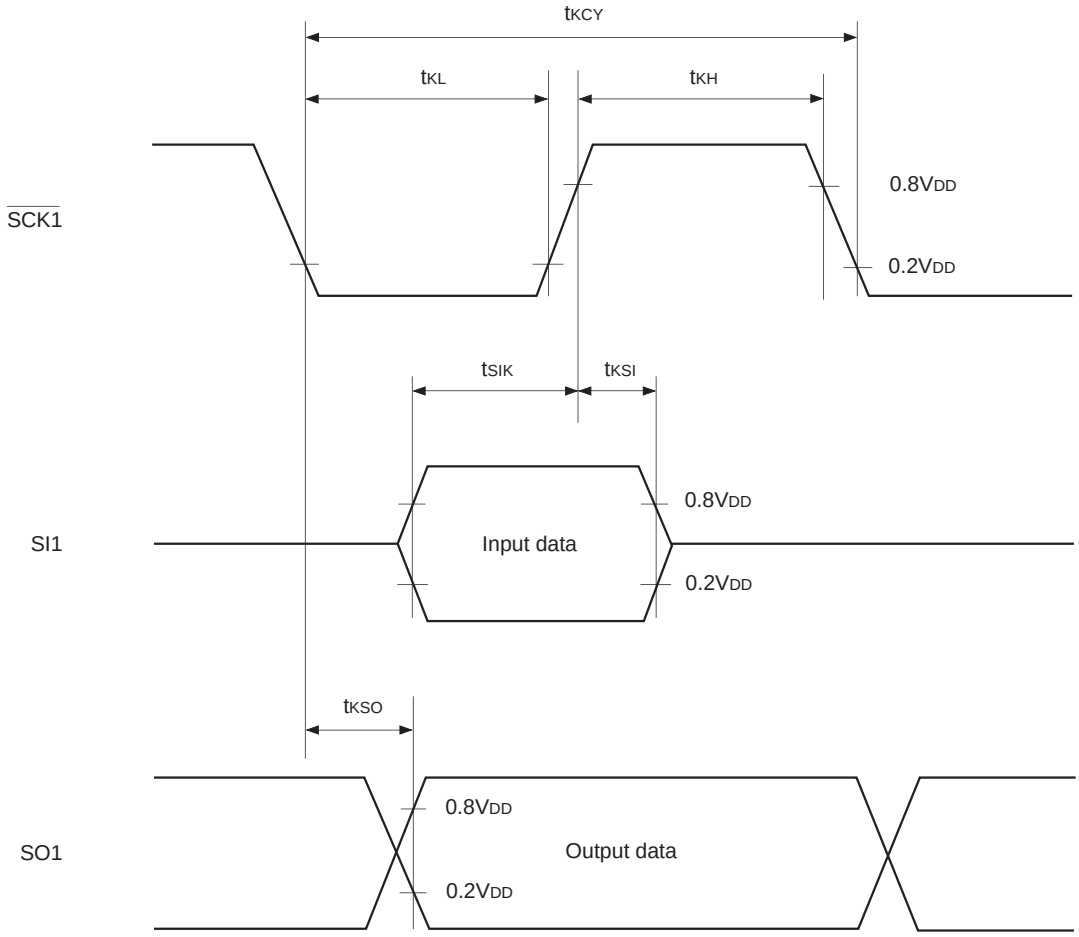


Serial transfer (CH1) (Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	8000/fc–50		ns
SI1 input set-up time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ output mode		100	ns

Note) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF +1TTL.

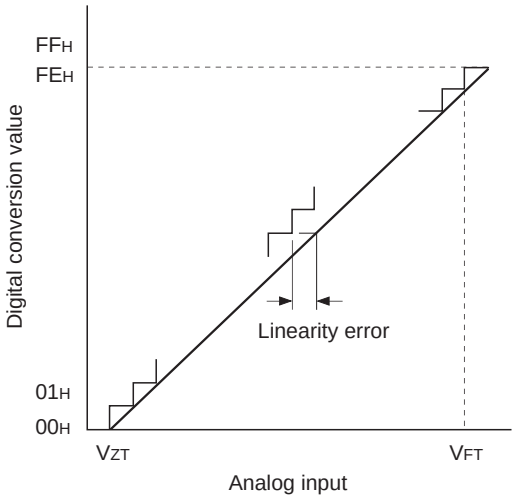
Fig. 5. Serial transfer timing (CH1)



(3) A/D converter characteristics (Ta=–10 to +75°C, V_{DD}=AV_{DD}=4.5 to 5.5V, AV_{REF}=4.0 to AV_{DD}, Vss=AVss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation Ta=25°C V_{DD}=AV_{DD}=AV_{REF}=5.0V V_{SS}=AVss=0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}			µs
Sampling time	t_{SAMP}			12/f_{ADC}			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD}–0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode AV_{REF}=4.0 to 5.5V		0.6	1.0	mA
			SLEEP mode STOP mode 32kHz operation mode			10	µA

Fig. 6. Definitions of A/D converter terms



* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: 01FFH bit 0).
When PS2 is selected, f_{ADC}=fc/2
When PS1 is selected, f_{ADC}=fc

(4) Interruption, reset input (Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 7. Interruption input timing

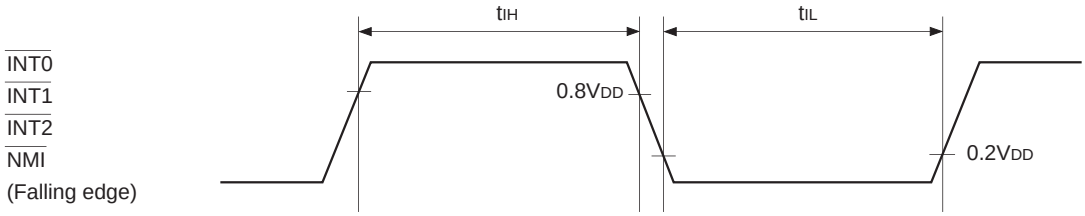
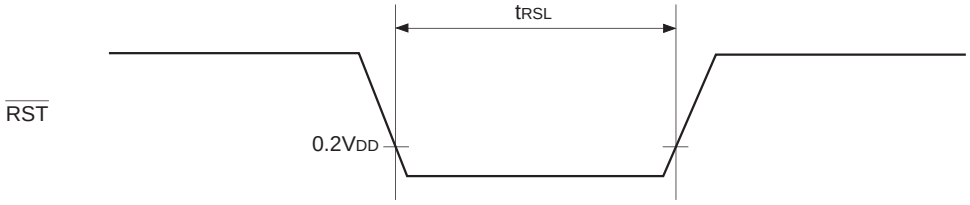


Fig. 8. Reset input timing



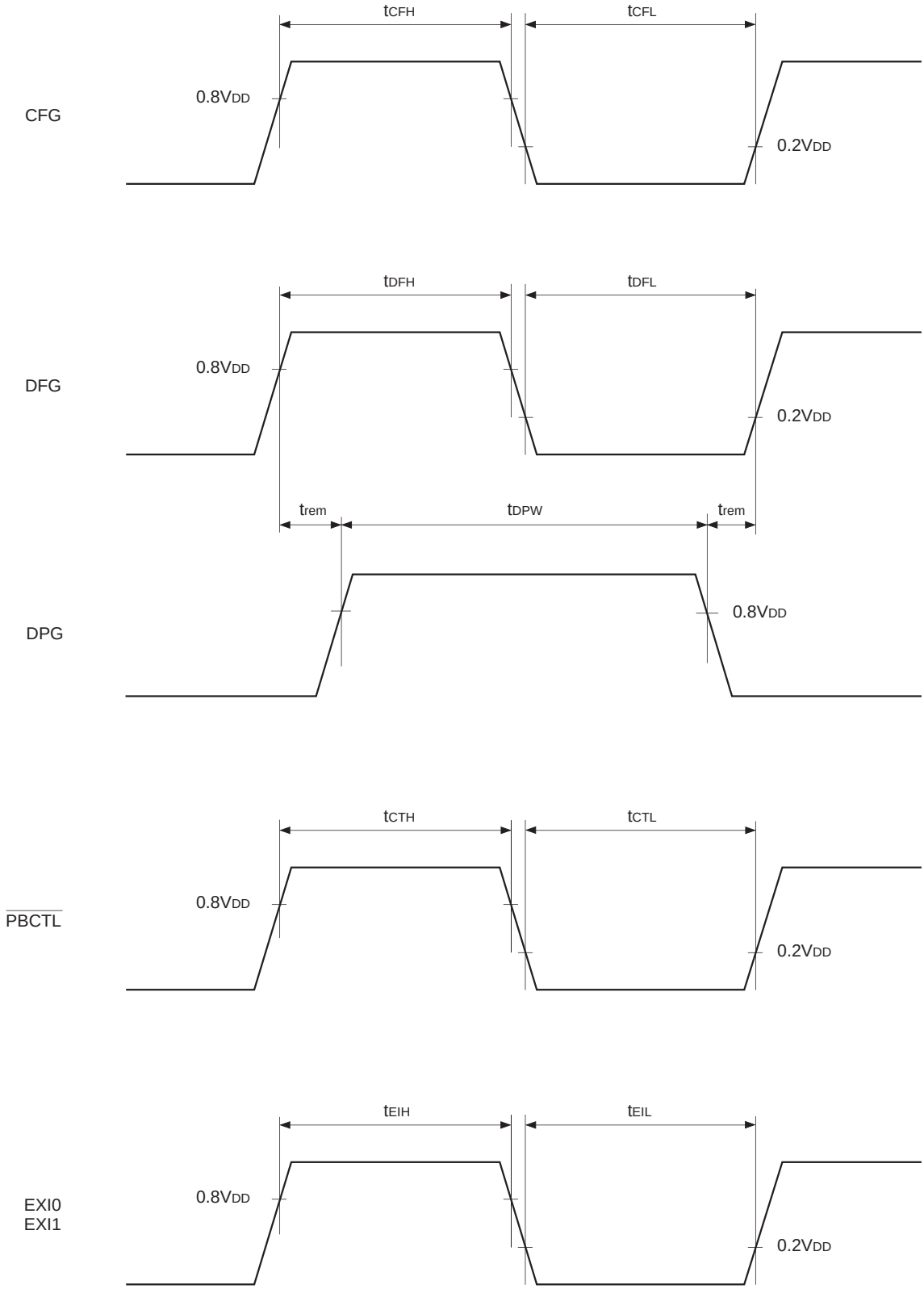
(5) Others (Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	t_{CFH} t_{CFL}	CFG		$t_{FRC} \times 24+200$		ns
DFG input high and low level widths	t_{DFH} t_{DFL}	DFG		$t_{FRC} \times 16+200$		ns
DPG minimum pulse width	t_{DPW}	DPG		$t_{FRC} \times 8+200$		ns
DPG minimum removal time	trem	DPG		$t_{FRC} \times 16+200$		ns
$\overline{PBCTL}$ input high and low level widths	t_{CTH} t_{CTL}	$\overline{PBCTL}$	tsys=2000/fc	$t_{FRC} \times 8+t_{sys}+200$		ns
EXI input high and low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	tsys=2000/fc	$t_{FRC} \times 8+t_{sys}+200$		ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Note 2) t_{FRC}=1000/fc (ns)

Fig. 9. Other timings



Supplement

Fig. 10. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12	0	
		16.00	12	12	0	
	P3	32.768kHz	30	18	470k	(ii)

Product list

Option item	Mask product	CXP881P60Q-1-□□□*2
Package	100-pin plastic QFP	100-pin plastic QFP
ROM capacitance	16K/20K/24K (CXP88216/88220/88224) 32K/40K (CXP88132/88140) 52K/60K (CXP88152/88160)	PROM 60K bytes
Reset pin pull-up resistor	Existent/non-existent	Existent
Input circuit format*1	CMOS schmitt /TTL schmitt	TTL schmitt
High voltage drive output port pull-down resistor	Existent/non-existent	Existent*3

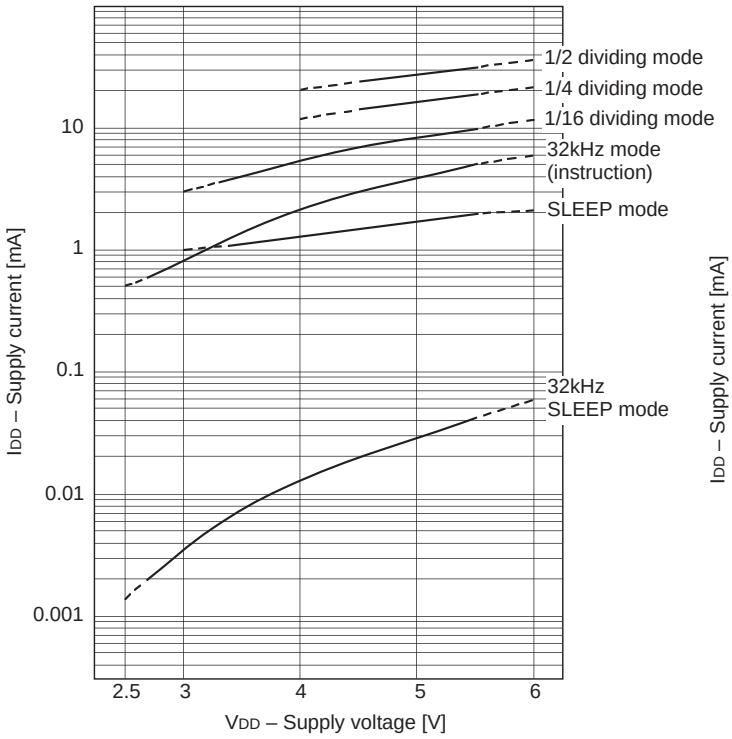
*1 In PG4/SYNC0/EC2 pin and PG5/SYNC1 pin only.

*2 OEM No.

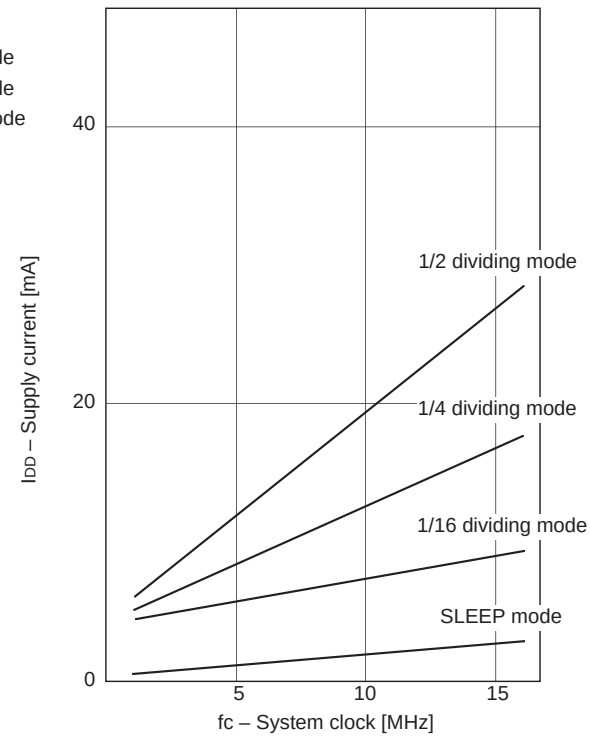
*3 No pull-down resistor for PD0/S0 to PD7/S7 pins.

Characteristics Curve

IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)

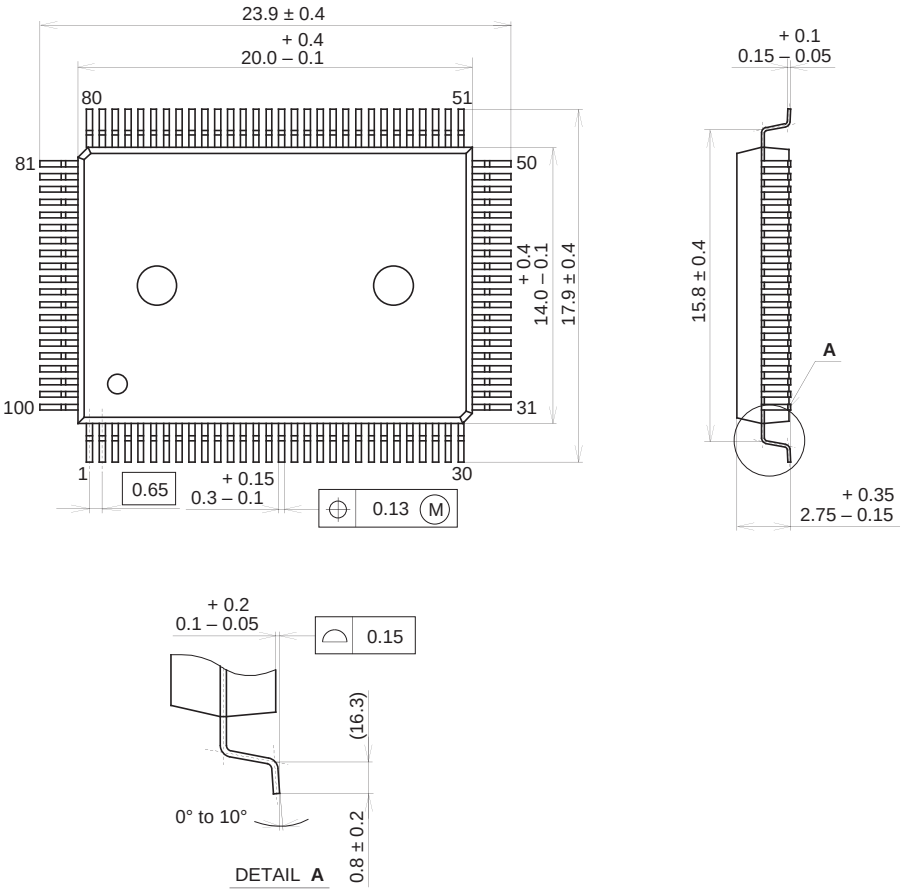


IDD vs. fc
(VDD = 5.0V, Ta = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g