LPC47N350

Legacy-Free Keyboard/Embedded Controller with SPI and LPC Docking Interface

Datasheet

Product Features

- 3.3V Operation with 5V Tolerant Buffers
- ACPI 2.0 PC2001 Compliant
- LPC Interface with Clock Run Support
  - Decode I/O, Memory, and FWH cycles
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - 15 Direct IRQs
  - ACPI SCI Interface
  - nSMI output and supporting PM registers
  - Shadowed write only registers
- LPC Switching
  - Hot Plug LPC Docking Interface
  - Secondary Switchable LPC interface (3.3V only)
- Internal 64K Flash ROM
  - Programmed From Direct Parallel Interface, 8051, or LPC Host
  - 2k-Byte Lockable Boot Block
  - Can be Programed Without 8051 Intervention
- Three Power Planes
  - Low Standby Current in Sleep Mode
- ACPI Embedded Controller Interface
- Configuration Register Set Compatible with ISA Plug-and-Play Standard (Version 1.0a)
- High-Performance Embedded 8051 Keyboard and System Controller
  - Provides System Power Management
  - System Watch Dog Timer (WDT)
  - 8042 Style Host Interface
  - Supports Interrupt and Polling Access
  - 512 Bytes Executable RAM
  - 512 Bytes Data RAM
  - On-Chip Memory-Mapped Control Registers
  - Access to RTC and CMOS Registers
  - Up to 16x8 Keyboard Scan Matrix
  - Two-16 Bit Timer/Counters
  - Integrated Full-Duplex Serial Port Interface
  - Eleven 8051 Interrupt Sources
  - Thirty-Two 8-Bit, Host/8051 Mailbox Registers
  - Thirty-Two Maskable Hardware Wake-Up Events
  - Fast GATEA20
  - Fast CPU_RESET
  - Multiple Clock Sources and Operating Frequencies
  - IDLE and SLEEP Modes
  - Fail-Safe Ring Oscillator
- Real-Time Clock
  - MC146818 and DS1287 Compatible
  - 256 Bytes of Battery Backed CMOS in Two 128-Byte Banks
  - 128 Bytes of CMOS RAM Lockable in 4x32-Byte Blocks
  - 12- and 24-Hour Time Format
  - Binary and BCD Format
  - <2μA Standby Current (typ)
- Two 8584-Style I^2C/SMBus Controllers
  - 8051 Controlled Logic Allows I^2C/SMBus Master or Slave Operation
  - I^2C/SMBus Controllers are Fully Operational on Standby Power
  - 2 Sets of Dedicated Pins per I^2C/SMBus Controller
- Serial Peripheral Interface (SPI)
- Four independent Hardware Driven PS/2 Ports
- 41 General Purpose I/O Pins
  - 25 Maskable Hardware Wake-Event Capable
  - 6 Programmable Open-Drain/Push-Pull Outputs
- Four Programmable Pulse-Width Modulator Outputs
  - Independent Clock Rates
  - 6-Bit Duty Cycle Granularity
  - Operational in both Full on and Standby modes
- Dual Fan Tachometer Inputs
- Debug Port (UART)
  - High-Speed 16550A-Compatible UART with 16-Byte Send/Receive FIFOs
  - Programmable Baud Rate Generator
  - Relocatable to 480 Different Base I/O Addresses
  - 15 IRQ Options
- XNOR-Chain Test Mode
- 128-Pin QFP and VTQFP Package

ORDERING INFORMATION

Order Number(s):

LPC47N350-NC for 128 pin QFP package

LPC47N350-NE for 128 pin VTQFP package

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Chapter 1 General Description

The LPC47N350 is a highly integrated LPC-based ACPI 2.0 and PC2001 compliant Keyboard, System, and Power Management Controller for Notebook PC Applications. See Figure 1.1.

The LPC47N350 incorporates a high-performance 8051-based keyboard and system controller with internal 64k byte Flash ROM; a hot-plug Docking LPC port; a Serial Peripheral Interface (SPI), four PS/2 ports; a real-time clock; a 16C550A-compatible 2 pin UART for Debug Port; two 8584-style I^2C/SMBus controllers with two selectable ports per controller; a Serial IRQ peripheral agent interface; an ACPI Embedded Controller Interface; forty-one General Purpose I/O pins; four independently programmable pulse width modulators; dual fan control through the implementation of two fan tachometer input pins; and maskable hardware wake-up events.

The LPC47N350 has three separate power planes to provide “instant on” and system power management functions. Additionally, the LPC47N350 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. Wake-up events and ACPI-related functions are supported through the SCI Interface.

The LPC47N350 supports the ISA Plug-and-Play Standard (Version 1.0a) and provides the recommended functionality to support Windows 2000 and Windows Me. The I/O Address and Hardware IRQ of each logical device in the LPC47N350 may be reprogrammed through the internal configuration registers. There are 480 I/O address location options and 15 IRQ’s for each logical device.

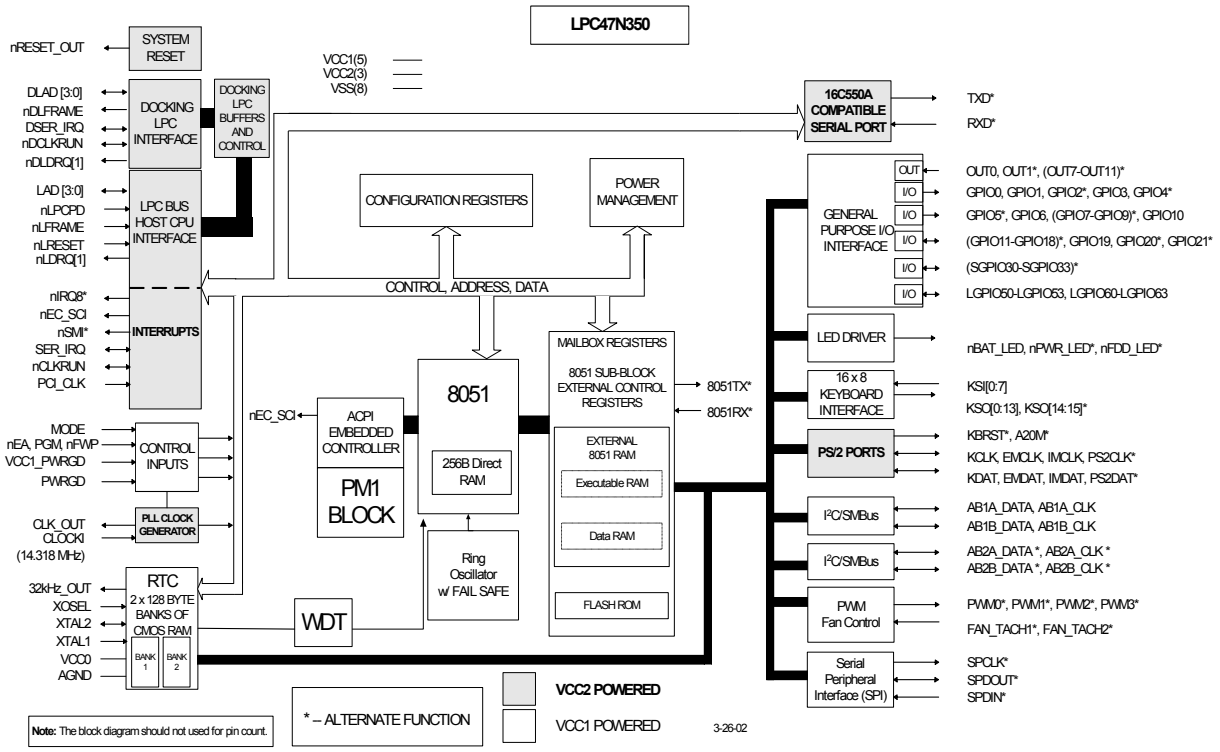


Figure 1.1 LPC47N350 Block Diagram

Chapter 2 Pin Functions

Table 2.1 LPC47N350 Pin Configuration

QFP PIN #	NAME	QFP PIN #	NAME	QFP PIN #	NAME	QFP PIN #	NAME
1	TEST_PIN	33	VSS	65	VCC0	97	GPIO20
2	KSO13	34	KCLK	66	XOSEL	98	VSS
3	KSO12	35	VCC2	67	XTAL1	99	GPIO21
4	KSO11	36	KDAT	68	XTAL2	100	VCC1
5	KSO10	37	EMCLK	69	AGND	101	nFWP
6	KSO9	38	EMDAT	70	PGM	102	nEA
7	KSO8	39	LRESET#	71	MODE	103	AB1B_DATA
8	VSS	40	PCI_CLK	72	32kHz_OUT	104	AB1B_CLK
9	KSO7	41	LPCPD#	73	nEC_SCI	105	AB1A_DATA
10	KSO6	42	LAD[0]	74	VCC1_PWRGD	106	AB1A_CLK
11	VCC1	43	DLAD[0]	75	PWRGD	107	nBAT_LED
12	KSO5	44	VSS	76	GPIO0	108	nFDD_LED
13	KSO4	45	LAD[1]	77	GPIO1	109	nPWR_LED
14	KSO3	46	DLAD[1]	78	GPIO2	110	nDMS_LED
15	KSO2	47	VCC2	79	GPIO3	111	VSS
16	KSO1	48	LAD[2]	80	GPIO4	112	OUT11
17	KSO0	49	DLAD[2]	81	VSS	113	VCC1
18	KSI7	50	LAD[3]	82	GPIO5	114	OUT10
19	KSI6	51	DLAD[3]	83	VCC1	115	OUT9
20	KSI5	52	LDRQ[1]#	84	GPIO6	116	OUT8
21	KSI4	53	DLDRQ[1]#	85	GPIO7	117	OUT7
22	KSI3	54	LFRAME#	86	GPIO8	118	VSS
23	KSI2	55	DLFRAME#	87	GPIO9	119	OUT0
24	KSI1	56	nCLKRUN	88	GPIO10	120	OUT1
25	KSI0	57	nDCLKRUN	89	GPIO11	121	LGPIO50
26	SGPIO30/ SPCLK	58	VSS	90	GPIO12	122	LGPIO60
27	SGPIO31/ SPDOUT	59	SER_IRQ	91	GPIO13	123	LGPIO51
28	VCC1	60	DSER_IRQ	92	GPIO14	124	LGPIO61
29	SGPIO32/SPDIN	61	CLOCKI	93	GPIO15	125	LGPIO52
30	SGPIO33	62	nRESET_OUT	94	GPIO16	126	LGPIO62
31	IMCLK	63	VCC2	95	GPIO17	127	LGPIO53
32	IMDAT	64	CLK_OUT	96	GPIO19	128	LGPIO63

VCC2 VCC1 VCC0

2.1 Description of Pin Functions

Device functions per pin are shown in Table 2.2. Buffer Modes symbols in Table 2.2 are described in Table 2.3. Multifunction pins are summarized in Table 2.4, including a multiplex controls reference.

The pins and descriptions in Table 2.2 are organized by primary pin function. For example, the PS2 Serial Clock and PS2 Serial Data pins are technically part of the KEYBOARD AND MOUSE INTERFACE but are listed in the GENERAL PURPOSE I/O INTERFACE because the GPIO function of these pins is the default.

Table 2.2 Pin Function Description

NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (SEE Note 2.1)
PCI POWER MANAGEMENT AND SIRQ INTERFACE (4)				
Note 2.5	nEC_SCI	Power Management Event	VCC1	PCI_OD
	PCI_CLK	PCI Clock	VCC2	PCI_ICLK
	SER_IRQ	Serial IRQ	VCC2	PCI_IO
	CLKRUN#	PCI Clock Control	VCC2	PCI_OD
LPC BUS (8)				
Note 2.14	LAD[3:0]	LPC address/data bus. Multiplexed command, address and data bus.	VCC2	PCI_IO
Note 2.12	LPCPD#	Powerdown Signal. Indicates that the LPC47N350 should prepare for power to be shut on the LPC interface. Used as LPC powergood	VCC1	PCI_I
	LFRAME#	Frame signal. Indicates start of new cycle and termination of broken cycle	VCC2	PCI_I
Note 2.13	LRESET#	LPC Reset. LRESET# is the same as the system PCI reset, PCIRST#	VCC2	PCI_I
Note 2.14	LDRQ[1]#	Encoded DMA request output for docking Super I/O	VCC2	-
DOCKING LPC INTERFACE (8)				
	DLAD[3:0]	LPC address/data bus for docking LPC Super I/O	VCC2	-
	DLFRAME#	Frame signal for docking LPC Super I/O	VCC2	-
	DSER_IRQ	Serial IRQ for docking LPC SUper I/O	VCC2	-
	DCLKRUN#	PCI Clock Control for docking LPC Super I/O	VCC2	-
	DLDRQ[1]#	Encoded DMA request output for docking Super I/O	VCC2	-
KEYBOARD AND MOUSE INTERFACE (28)				
Note 2.10	KSO[0:11]/ ATE Prog. Access/ Ext. Flash	Keyboard Scan Outputs (14 × 8). NOTE: GPIO4 and GPIO5 can be configured as KSO14 and KSO15 (16 × 8).	VCC1	OD4/IO4/IO4
Note 2.2	KSO12 OUT8/ KBRST	Keyboard Scan Output General Purpose Output CPU_RESET	VCC1	OD4/OD4/OD4
Note 2.3	KSO13/ GPIO18 (WK_SE27)	Keyboard Scan Output General Purpose I/O	VCC1	IOD4/IOD4

Table 2.2 Pin Function Description (continued)

NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (SEE Note 2.1)
Note 2.10	KSI[0:6]]/ ATE Prog. Access/ Ext. Flash	Keyboard Scan Inputs	VCC1	ISP/IO4/IO4
	KSI7	Keyboard Scan Inputs	VCC1	ISP
	EMCLK	EM Serial Clock	VCC2	IOD16
	EMDAT	EM Serial Data	VCC2	IOD16
	IMCLK	IM Serial Clock	VCC2	IOD16
	IMDAT	IM Serial Data	VCC2	IOD16
	KDAT	Keyboard Data	VCC2	IOD16
	KCLK	Keyboard Clock	VCC2	IOD16
GENERAL PURPOSE I/O INTERFACE (40)				
Note 2.5 Note 2.6	OUT0 (SCI)	General Purpose Output (SCI)	VCC1	(O12/OD12)
Note 2.2	OUT1/ nIRQ8	General Purpose Output/ Active Low RTC IRQ	VCC1	O12/O12
Note 2.2	OUT7/ nSMI	General Purpose Output SMI Output	VCC1	O12/OD12
Note 2.2	OUT8/ KBRST	General Purpose Output CPU_RESET	VCC1	O12/O12
Note 2.2	OUT9/ PWM2	General Purpose Output Pulse Width Modulator Output	VCC1	O12/O12
	OUT10/ PWM0	General Purpose Output Pulse Width Modulator Output	VCC1	O12/O12
	OUT11/ PWM1	General Purpose Output Pulse Width Modulator Output	VCC1	O12/O12
Note 2.3	GPIO0 (WK_SE02)	General Purpose I/O	VCC1	IO8
Note 2.3	GPIO1 (WK_SE03)	General Purpose I/O	VCC1	IO8
Note 2.3	GPIO2 (WK_SE04)	General Purpose I/O	VCC1	IO8
Note 2.4	GPIO3 (TRIGGER)	General Purpose I/O (Interrupt 1 Event)	VCC1	IO8
Note 2.3	GPIO4 (WK_SE07) KSO14	General Purpose I/O Keyboard Scan Output	VCC1	IO8/OD8
Note 2.3	GPIO5 (WK_SE10)/ KSO15	General Purpose I/O Keyboard Scan Output	VCC1	IO8/OD8

Table 2.2 Pin Function Description (continued)

NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (SEE Note 2.1)
Note 2.3	GPIO6 (WK_SE11)	General Purpose I/O	VCC1	IO8
Note 2.3 Note 2.6	GPIO7 (WK_SE06)/ PWM3	General Purpose I/O Pulse Width Modulator Output	VCC1	(IO12/IOD12)/O12)
Note 2.3	GPIO8 (WK_SE12)/ RXD	General Purpose I/O Receive Data	VCC1	IO8/I
Note 2.3	GPIO9 (WK_SE13)/ TXD	General Purpose I/O Transmit Data	VCC1	IO12/O12
Note 2.3	GPIO10 (WK_SE14)	General Purpose I/O	VCC1	IO8
Note 2.3	GPIO11 (WK_SE15)/ AB2A_DATA	General Purpose I/O I^2C/SMBus 2 Serial Data (switch position A)	VCC1	IO12/IOD12
Note 2.3	GPIO12 (WK_SE16) AB2A_CLK	General Purpose I/O I^2C/SMBus 2 Clock (switch position A)	VCC1	IO12/IOD12
Note 2.3	GPIO13 (WK_SE17) AB2B_DATA	General Purpose I/O I^2C/SMBus 2 Serial Data (switch position B)	VCC1	IO12 /IOD12
Note 2.3	GPIO14 (WK_SE20) AB2B_CLK	General Purpose I/O I^2C/SMBus 2 Clock (switch position B)	VCC1	IO12/IOD12
Note 2.3	GPIO15 (WK_SE21) FAN_TACH1	General Purpose I/O Fan Tachometer Input 1	VCC1	IO8/I
Note 2.3	GPIO16 (WK_SE22) FAN_TACH2	General Purpose I/O Fan Tachometer Input 2	VCC1	IO8/I
Note 2.2 Note 2.3	GPIO17 (WK_SE23)/ A20M	General Purpose I/O KBD GATEA20 Output	VCC1	IO8/O8
Note 2.3	GPIO19 (WK_SE24)	General Purpose I/O	VCC1	IO8
Note 2.2 Note 2.3	GPIO20 (WK_SE25)/ PS2CLK	General Purpose I/O PS2 Serial Clock	VCC1	IOD16/IOD16
Note 2.2 Note 2.3	GPIO21 (WK_SE26)/ PS2DAT	General Purpose I/O PS2 Serial Data	VCC1	IOD16/IOD16
Note 2.15	SGPIO30/ SPCLK	8051 SFT bit-wise addressable GPIO Serial Peripheral Clock Output	VCC1	IO8/IO8

Table 2.2 Pin Function Description (continued)

NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (SEE Note 2.1)
Note 2.15	SGPIO31/ SPDOUT	8051 SFR bit-wise addressable GPIO Serial Peripheral Data Output. SPDOUT can be configurated as bi-directional Data In/Data Out	VCC1	IO8/IO8
	SGPIO32/ SPDIN	8051 SFR bit-wise addressable GPIO Serial Peripheral Data Input	VCC1	IO8/I
	SGPIO33	8051 SFR bit-wise addressable GPIO	VCC1	IO8
	LGPIO50 - LGPIO53	LPC/8051 addressable GPIO	VCC1	IO8
Note 2.3	LGPIO60 - LGPIO63	LPC/8051 addressable GPIO	VCC1	(IO8/OD8)
MISCELLANEOUS (15)				
	32kHz_OUT	32.768kHz Output Clock	VCC1	O8
	CLK_OUT	Programmable clock output. Off (default) 1.8432 MHz 14.318 MHz 16 MHz 24 MHz 48 MHz	VCC2	O16
	CLOCKI	14.318MHz Clock Input	VCC2	ICLK
Note 2.11	MODE	Configuration Ports Base Address Select	VCC1	I
	TEST_PIN	No Connect. This pin provides acess to the SMSC board level XNOR-Chain test. See Chapter 26, "XNOR Chain Test Mode," on page 275.	VCC1	-
Note 2.7	VCC1_PWR GD	VCC1 Power Good Input	VCC1	I
	nRESET_O UT	System Reset	VCC2	O16
	nBAT_LED	Battery LED (0 = ON)	VCC1	OD12
	nPWR_LED/ 8051TX	Power LED (0 = ON) 8051 TX Input	VCC1	OD12/OD12
	nFDD_LED/ 8051RX	Floppy LED (0 = ON) 8051 RX Input	VCC1	OD12/I
	nDMS_LED	Dead Man Switch LED (0 = ON)	VCC1	OD12
Note 2.7	PWRGD	VCC2 Power Good Input	VCC1	I
Note 2.9	PGM	Flash Programming Enable (see Section 9.6, "ATE Flash Program Access")	VCC1	IPD
	nFWP	Flash Boot Block Write Protect (see Section 8.5, "8051 Flash Boot Block Protect Controls")	VCC1	I
	nEA	Internal/External Flash Select (see Section 9.7, "External Flash Interface")	VCC1	I

Table 2.2 Pin Function Description (continued)

NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (SEE Note 2.1)
		I²C/SMBUS INTERFACE (4)		
	AB1A_DATA	I²C/SMBus 1 Serial Data (switch position A)	VCC1	IOD12
	AB1A_CLK	I²C/SMBus 1 Clock (switch position A)	VCC1	IOD12
	AB1B_DATA	I²C/SMBus 1 Serial Data (switch position B)	VCC1	IOD12
	AB1B_CLK	I²C/SMBus 1 Clock (switch position B)	VCC1	IOD12
		REAL TIME CLOCK INTERFACE (3)		
	XTAL1	32.768kHz Crystal Input	VCC0	ICLK2
Note 2.8	XTAL2	32.768kHz Crystal Output	VCC0	(OCLK2/I)
Note 2.8 Note 2.9	XOSEL	External 32kHz Clock Enable Input	VCC0	IPD
		POWER PLANES (18)		
	VCC0	RTC (V_{BAT}) Supply Voltage (×1)		
	VCC1	+3.3V ± 10% Main Battery Supply (×5)		
	VCC2	+3.3V ± 10% Switched AC/Main Battery Supply (×3)		
	AGND	Analog Ground (×1)		
	VSS	Digital Ground (×8)		

Note 2.1 Buffer Modes per function on multiplexed pins are separated by a slash "/"; e.g., a pin with two multiplexed functions where the primary function is an input and the secondary function is an 8mA bi-directional driver is represented as "I/IO8". Buffer Modes in parenthesis represent multiple buffer modes for a single pin function.

Note 2.2 This pin is tristated when PWRGD is inactive and the pin is configured as a VCC2-powered alternate function.

Note 2.3 These devices can generate wake-up events on selectable edges of the signal that is applied when the pin is configured as an input. The interrupts are masked by the Wake-up Mask Registers and selected edges are programmed via the Edge Select registers (see Section 7.9.1, "8051 Internal Parallel Interrupts," on page 65)

Note 2.4 This interrupt is masked by INT1 Mask Register bit 3. GPIO3 is the only GPIO pin which does not generate a wakeup event.

Note 2.5 The nEC_SCI pin can be controlled by hardware and 8051 software. The nEC_SCI pin can drive either the ACPI Run-time GPE Chipset input or the Wake GPE Chipset input (Figure 22.1 on page 254). Depending how the nEC_SCI pin is used, other ACPI-related SCI functions may be best supplied by LPC47N350 general purpose output OUT0.

Note 2.6 OUT0 and GPIO7 are suitable as an SCI output pin because the buffer type can be configured as a push-pull or open-drain output (see Section 20.4.3.4)

Note 2.7 Input levels for the PWRGD and VCC1_PWRGD pins are as follows: $V_{IL} = V_{SS} \pm 400mV$ and $V_{IH} = V_{CC1} \pm 400mV$. VCC1_PWRGD must be driven high or low at all times. VCC1_PWRGD may be tied high but VCC0 must be connected to VCC1 and all RTC time-keeping and CMOS memory functions are invalidated.

Note 2.8 The function of these pins are described in Section 23.10, "32kHz Clock Input," on page 267.

Note 2.9 This pin has an internal pull-down resistor to guarantee that the input remains deasserted when unconnected.

Note 2.10 These pins are multiplexed according to the PGM and nEA pins to support an external Flash interface and to support internal Flash programming (see Section 9.6, "ATE Flash Program Access", Section 9.2, "Flash Program Interface Decoder", Section 9.7, "External Flash Interface" and Section 9.8, "Keyboard Controller Bus Monitor Interface").

Note 2.11 The input path for the MODE pin pad has a Vt drop when passing a logic high signal.

Note 2.12 LPCPD# is a VCC2-powered signal but is sensed by the 8051 on VCC1 (see Section 7.8.3.6, "8051 LPC Bus Monitor," on page 63).

Note 2.13 In the LPC47N350, Hard Reset is generated internally by the 8051 for all SIO blocks except for the LPC Host Interface where LRESET#, alone, provides this function.

Note 2.14 These pins require a weak pull-up resistors of 10k-100k ohms.

Table 2.3 Buffer Mode

BUFFER SYMBOL	DESCRIPTION
I	Input
IPD	Input with **30uA** pull**down**
ISP	Schmitt trigger input with **90uA** pull-up
ICLK	Clock input
ICLK2	Clock input 2
OCLK2	Clock output 2
OD4	Open drain – 4mA sink
O8	Output – 8mA, 4mA source
OD8	Open drain – 8mA sink
O12	Output – 12mA, 6mA source
OD12	Open drain – 12mA sink
O24	Output – 12mA, 6mA source
IO4	Bidirectional – 4mA, 2mA source
IO8	Bidirectional – 8mA, 4mA source
IOD8	Input, open drain output – 8mA sink
IO12	Bidirectional – 12mA sink, 6mA source
IOD12	Input, open drain output – 12mA sink
IOD16	Input, open drain output – 16mA sink
PCI_I	PCI input
PCI_ICLK	PCI clock input
PCI_IO	PCI bidirectional
PCI_IOD	PCI input, open drain output

Table 2.3 Buffer Mode (continued)

BUFFER SYMBOL	DESCRIPTION
PCI_O	PCI output
PCI_OD	PCI open drain

2.2 Alternate Function Pins

Many of the LPC47N350's signal pins provide alternate functions which may be enabled by the 8051 firmware based on the system design requirements. The pins are identified by primary pin function (Note that some functions are available on more than one pin; e.g., OUT8 and KBRST).

Table 2.4 Alternate Function Pins

DEFAULT FUNCTION	PIN BUFFER PWR	ALT FUNCT #1	ALT FUNCT PWR	ALT FUNCT #2	ALT FUNCT PWR	MULTIPLEX CONTROLS BIT	NOTES
OUT1	VCC1	nIRQ8	VCC2	-	-	MISC0	Note 2.15
OUT7		nSMI		-	-	MISC18	
OUT8		KBRST				MISC[17, 6]	
OUT9		PWM2	VCC1	-	-	MISC11	

Table 2.4 Alternate Function Pins (continued)

DEFAULT FUNCTION	PIN BUFFER PWR	ALT FUNCT #1	ALT FUNCT PWR	ALT FUNCT #2	ALT FUNCT PWR	MULTIPLEX CONTROLS BIT	NOTES
OUT10	VCC1	PWM0	VCC1	-	-	MISC4	
OUT11		PWM1		-	-	MISC12	
GPIO4		KSO14		-	-	MISC9	
GPIO5		KSO15		-	-		
GPIO7		PWM3		-	-	MISC22	
GPIO8		RXD	VCC2	-	-	MISC7	Note 2.15
GPIO9		TXD		-	-	MISC7	
GPIO11		AB2A_DATA	VCC1			MISC[20, 19]	
GPIO12		AB2A_CLK					
GPIO13		AB2B_DATA					
GPIO14		AB2B_CLK					
GPIO15		FAN_TACH1				MISC23	
GPIO16		FAN_TACH2				MISC21	
GPIO17		A20M	VCC2	-	-	MISC6	Note 2.15
GPIO20		PS2CLK		-	-	MISC1	
GPIO21		PS2DAT		-	-		
KSO12		OUT8	VCC1	KBRST	VCC2	MISC[17, 6]	
KSO13		GPIO18		-	-	MISC[17]	
SGPIO30		SPCLK				MISC[10]	
SGPIO31		SPDOUT					
SGPIO32		SPDIN				MISC[10], SPIMODE	
nFDD_LED		8051RX		-	-	MISC3	
nPWR_LED		8051TX		-	-	MISC2	

Note 2.15 When this pin is configured as a VCC2 powered alternate function output and PWRGD is inactive (i.e. VCC2 is 0v), the VCC1 powered pin buffer will tri-state to prevent back-biasing of external circuitry (see Chapter 20, GPIO Interface).

2.3 Power Configuration

There are three power planes in the LPC47N350 V_{CC0}, V_{CC1}, and V_{CC2} with the following power sequencing requirement:

V_{CC2} shall have power applied simultaneously with or after V_{CC1}.

V_{CC1} shall have power applied simultaneously with or after V_{CC0}.

$V_{CC2} - V_{CC}1 \leq 0.5V$

All internal components which utilize V_{CC0} power plane are switched internally between the VCC1 and VCC0 pins according to VCC1_PWRGD.

See Figure 2.2, "VCC2 Power-Up Timing" and Figure 2.3, "VCC1_PWRGD Timing".

See Table 28.3 for power consumption in various states.

Two LPC47N350 power supply configurations can be utilized. These power supply configuration types fundamentally differ upon the need for a backup battery (V_{BAT}) connection to V_{CC0}.

TYPE 1 devices do not require a V_{CC0} battery connection. Power supply requirements for TYPE 1 devices are as follows: V_{CC0} is tied to V_{SS}, V_{CC1} is connected to the main battery supply, and V_{CC2} is switched from either the main battery or AC power if available. In this configuration all internal components which utilize V_{CC0} power plane are switched internally to VCC1 upon POR according to VCC1_PWRGD.

TYPE 2 devices require a V_{CC0} battery connection. Power supply requirements for TYPE 2 devices are as follows: V_{CC0} is connected to a backup battery (V_{BAT}), V_{CC1} is connected to the main battery supply, and V_{CC2} is switched from either the main battery or AC power if available. In this configuration all internal components which utilize V_{CC0} power plane only when V_{CC1} is absent. Normally (when VCC1_PWRGD is asserted) they are switched internally to the VCC1 power plane.

The LPC47N350 provides unpredicted VCC2 power failures (See Section 7.6, "8051 Ring Oscillator Fail-Safe Controls," on page 46).

PWRGD and VCC1_PWRGD timing is illustrated in Figure 2.1 through Figure 2.3.

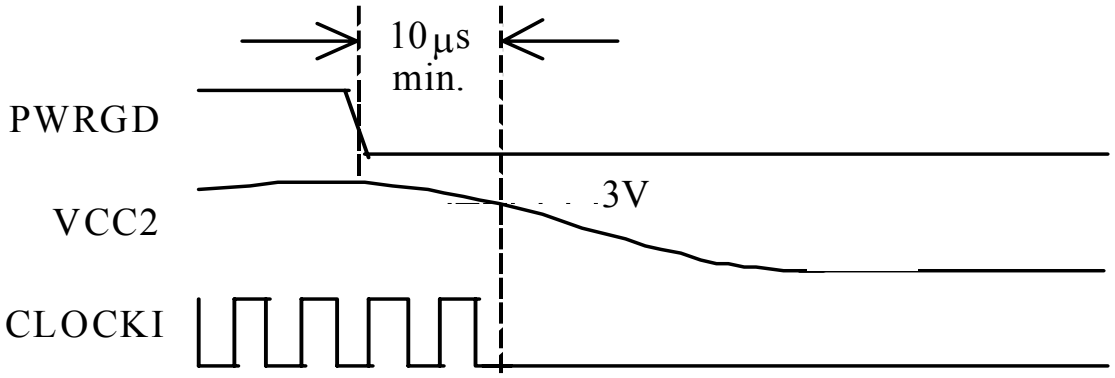


Figure 2.1 Power-Fail Event

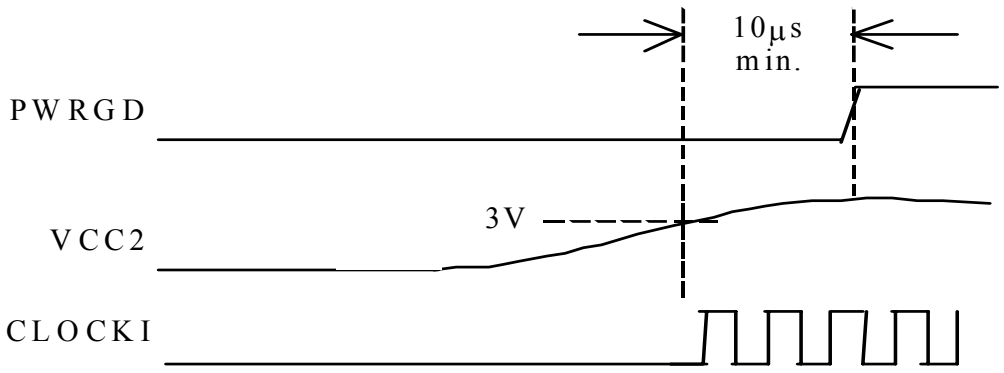


Figure 2.2 VCC2 Power-Up Timing

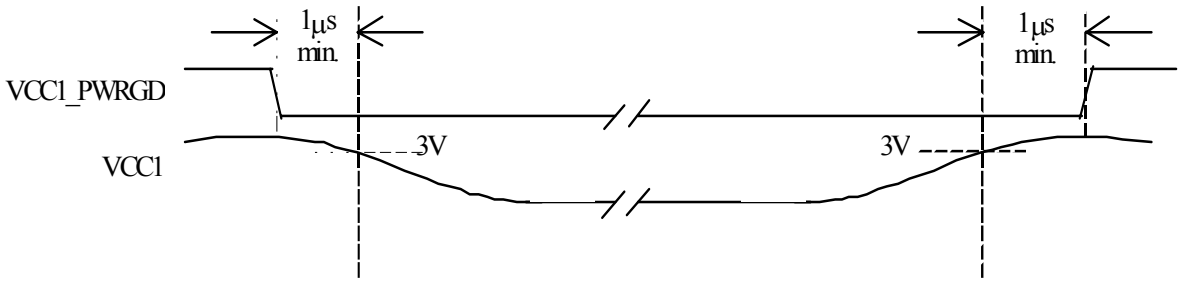


Figure 2.3 VCC1_PWRGD Timing

Chapter 3 Functional Description

The host processor communicates with the LPC47N350 through a series of read/write registers. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits. The address map, shown below in Table 3.1, shows the set of operating registers and addresses for each of the logical blocks of the LPC47N350 Notebook I/O controller. The base addresses of all the blocks, except the Keyboard Controller can be moved via the configuration registers.

Table 3.1 LPC47N350 Operating Register Addresses

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	FIXED / BASE OFFSETS	NOTES
0x04	Serial Port 1	+0: RB/TB | LSB div +1: IER | MSB div +2: IIR/FCR +3: LCR +4: MCR +5: LSR +6: MSR +7: SCR	
0x06	RTC 0x60, 0x61 0x62, 0x63	 Bank 0 Base address +0: Address Register +1: Data Register * Bank 1 Base address +0: Address Register +2: Data Register *	
0x07	KYBD	0x60: Data Register 0x64: Command/Status Reg.	
0x08	ACP1 EC	+0: Data Register +1: Command/Status Reg.	
0x09	Mailbox Reg. Interface	+0: Index Register +1: Data Register.	

Note: Refer to the configuration register descriptions for setting the base address

3.1 Host Processor Interface (LPC)

The LPC47N350 communicates with the host over a Low Pin Count (LPC) interface. The LPC interface uses 3.3V signaling. For electrical specifications see the *Intel Low Pin Count Specification* and the *PCI Local Bus Specification*. The following seven pins provide the LCP interface for the LPC47N350: LAD[3:0], LPCPD#, LFRAME#, LRESET#. (see Table 2.2 on page 4).

3.1.1 LPC Bus Cycles Description

For a complete description of the LPC Bus Cycles see the *Intel Low Pin Count Specification*. It provides the specific tailoring of the Intel Low Pin Count Specification implemented in the LPC47N350.

LPC data transfers are serialized over a 4-bit bus, LAD[3:0]. The LAD[3:0] pins communicate the type, cycle direction, chip selection, address, data, and wait states for each LPC Bus cycle. There is one control pin LFRAME# which is used exclusively by the host to start or stop transfers. The LPC47N350 does not drive this signal. Optionally implemented side-band signals convey interrupts and power management features using the same signals found on current motherboard implementations. The general flow of cycles is as follows (Table 3.2):

Table 3.2 Basic LPC Bus Cycle Description

1	A cycle is started by the host by driving LFRAME# active.
2	The host puts appropriate information related to the cycle on the LAD[3:0] signal lines such as address. For target cycles, the host also drives cycle type (memory or I/O), read/write direction, and size of the transfer.
3	The host optionally drives the data on the LAD[3:0] pins and turns the bus around to monitor the peripheral for completion of the cycle.
4	The peripheral indicates completion of the cycle by driving appropriate values on the LAD[3:0] signal lines, and potentially drives data.
5	The peripheral turns the bus around to the host, ending the cycle.

3.1.2 LPC Bus Cycles Summary

Table 3.3 illustrates cycle types are supported by the LPC Bus protocol.

Table 3.3 LPC Bus Cycles

CYCLE TYPE (See Note)	**TRANSFER SIZE**
I/O Write	1 Byte Transfer
I/O Read	
DMA Write	1, 2, or 4 bytes - Not supported in the LPC47N350
DMA Read	
Bus Master Write (I/O and Memory)	
Bus Master Read (I/O and Memory)	
Memory Read	
Memory Write	

Note: LPC47N350 ignores cycles that it does not support.

3.1.2.1 32-Bit Transfers

The LPC47N350 LPC Bus implementation does not support 32-bit transfers.

3.1.3 Standard LFRAME# Usage

See the *Intel Low Pin Count Specification* for general description of LFRAME#.

All LPC bus cycles start the same way: the chipset asserts LFRAME# for one or more clocks and drives a START value on the LAD[3:0] pins (see Section 3.1.7, "I/O Start Fields," on page 18). Upon observing LFRAME# active, the peripheral must stop driving the LAD[3:0] signals, even if in the middle of a transfer (see Section 3.1.4).

3.1.4 Abort Mechanism

The host can use LFRAME# to force the LPC47N350 off the LPC Bus. See the *Intel Low Pin Count Specification* for timing for the abort mechanism using LFRAME#.

Note: The LPC47N350 adheres to the following abort policy: on target I/O cycles, if the host signals an abort before the peripheral has asserted the ‘ready’ or ‘error’ SYNC, the cycle will be

terminated. No data is to be transferred to the host on I/O reads, and the data written to the LPC47N350 on I/O writes and DMA reads is to be ignored. Note that once the LPC47N350 asserts the ready SYNC, the host will not abort.

3.1.5 I/O Read and Write Cycles

I/O cycles are initiated by the host for register or FIFO accesses and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1. EPP cycles will depend on the speed of the external device, and may have much longer Sync times.

Data transfers are assumed to be exactly 1-byte. If the CPU requested a 16 or 32-bit transfer, the host will break it up into 8-bit transfers.

3.1.6 SYNC Protocol

See the *Intel Low Pin Count Specification* for a table of valid SYNC values.

3.1.6.1 Typical SYNC Usage

The SYNC pattern is used to add wait states. For read cycles, the LPC47N350 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the LPC47N350 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. On any particular access, the LPC47N350 chooses to assert 0101 or 0110, but not switch between the two patterns.

The data will immediately follow the 0000 or 1001 value. If no wait states are needed, the LPC47N350 just drives 0000 or 1001 followed by the data. Because the SYNC pattern of 0000 or 1001 is always required, there is effectively a minimum of 1 wait state for accesses.

The SYNC value of 0101 is used for normal wait states, wherein the cycle will complete within a few clocks.

The SYNC value of 0110 is used where the number of wait states is large.

The SYNC value must be driven within 3 clocks.

3.1.6.2 SYNC Timeout

The SYNC value is driven within 3 clocks. If the host observes 3 consecutive clocks without a valid SYNC pattern, it will abort the cycle. The LPC47N350 does not assume any particular timeout. When the host is driving SYNC, it may have to insert a very large number of wait states, depending on PCI latencies and retries.

3.1.6.3 Sync Patterns and Maximum Number of Syncs

If the SYNC pattern is 0101, then the host assumes that the maximum number of SYNCs is 8.

If the SYNC pattern is 0110, then no maximum number of SYNCs is assumed. The LPC47N350 must have protection mechanisms to complete the cycle.

3.1.6.4 Sync Error Indication

The peripheral reports errors via the LAD[3:0] = 1010 SYNC encoding.

If the host was reading data from the peripheral, data will still be transferred in the next two nibbles. This data may be invalid, but it is transferred by the LPC47N350. If the host was writing data to the LPC47N350, the data had already been transferred.

In the case of multiple byte cycles, such as memory cycles, an error SYNC terminates the cycle. Therefore, if the host is transferring 4 bytes from a device or if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

3.1.7 I/O Start Fields

I/O cycles use a START field of 0000.

3.1.8 Reset Policy

The following rules govern the reset policy:

1. When LRESET# goes inactive (high), the clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
2. When LRESET# goes active (low):

a. the host drives the LFRAME# signal high and tristates the LAD[3:0] signals.

b. LPC47N350 ignores LFRAME# and tristates the LAD[3:0] pins.

3.1.9 Electrical Specifications

The LPC interface uses 3.3V signaling. No output from the peripheral may drive higher than 3.3V nominal. See the *Intel Low Pin Count Specification*.

3.1.10 Wait State Requirements

3.1.10.1 I/O Transfers

Wait states are required for all I/O transfers. Three wait states are required for an I/O read and two wait states are required for an I/O write. A SYNC of 0110 is used for all I/O_transfers.

3.1.11 LPC Transfer I/O Sequence Examples

3.1.11.1 EXAMPLE 1: I/O Read, No Wait States

The I/O transfer is initiated when the host asserts LFRAME# for one or more clocks and drives a start value onto the LAD[3:0] signals. The following sequence of fields is encoded onto the LAD[3:0] signals as the transfer proceeds (Table 3.4):

Table 3.4 Example 1: I/O Read, No Wait States

FIELD	DRIVEN BY	CLOCKS	LAD[3:0]	COMMENT
START	Host	1	0000	LAD[3:0]=0000
CYCTYP+DIR			000x	LAD[3:2]=00 (I/O cycle), LAD[1]=0 (read)
ADDR			xxxx	Most significant nibble
			xxxx	
			xxxx	
			xxxx	Least significant nibble
TAR			1111	Host drives LAD[3:0] high in 1st half

Table 3.4 Example 1: I/O Read, No Wait States (continued)

FIELD	DRIVEN BY	CLOCKS	LAD[3:0]	COMMENT
TAR	Special	1	1111	Not driven
Sync	LPC47N350		0000	Sync=0000 (Sync achieved with no error) (See Note below))
Data			xxxx	First nibble of byte
			xxxx	Second nibble of byte
TAR			1111	LPC47N350 drives LAD[3:0] high in 1st half
	Special			Not driven

Note: The actual implementation requires that three wait states (SYNC=0110) precede the SYNC of 0000.

3.1.11.2 EXAMPLE 2: I/O Read, Many Wait States

The I/O transfer is initiated when the host asserts LFRAME# for one or more clocks and drives a start value onto the LAD[3:0] signals. The following sequence of fields is encoded onto the LAD[3:0] signals as the transfer proceeds (Table 3.5):

Table 3.5 Example 2: I/O Read, Many Wait States

FIELD	DRIVEN BY	CLOCKS	LAD[3:0]	COMMENT
START	Host	1	0000	LAD[3:0]=0000
CYCTYP+DIR			000x	LAD[3:2]=00 (I/O cycle), LAD[1]=0 (read)
ADDR			xxxx	Most significant nibble
			xxxx	
			xxxx	
			xxxx	Least significant nibble
TAR			1111	Host drives LAD[3:0] high in 1st half
	Special			Not driven
Sync	LPC47N350		0110	Sync=0110 (Sync not achieved yet)
.				
.				
.				
Sync	LPC47N350	1	0110	Sync=0110 (Sync not achieved yet)
			0000	Sync=0000 (Sync achieved with no error)
Data			xxxx	First nibble of byte
			xxxx	Second nibble of byte
TAR			1111	Peripheral drives LAD[3:0] high in 1st half
	Special			Not driven

EXAMPLE 3: I/O Write, No Wait States

The I/O transfer is initiated when the host asserts LFRAME# for one or more clocks and drives a start value onto the LAD[3:0] signals. The following sequence of fields is encoded onto the LAD[3:0] signals as the transfer proceeds (Table 3.6):

Table 3.6 Example 3: I/O Write, No Wait States

FIELD	DRIVEN BY	CLOCKS	LAD[3:0]	COMMENT
START	Host	1	0000	LAD[3:0]=0000
CYCTYP+DIR			001x	LAD[3:2]=00 (I/O cycle), LAD[1]=1 (write)
ADDR			xxxx	Most significant nibble
			xxxx	
			xxxx	
			xxxx	Least significant nibble
Data			xxxx	First nibble of byte
			xxxx	Second nibble of byte
TAR			1111	Host drives LAD[3:0] high in 1st half
	Special			Not driven
Sync	LPC47N350		0000	Sync=0000 (Sync achieved with no error) (See Note below)
TAR	LPC47N350		1111	LPC47N350 drives LAD[3:0] high in 1st half
	Special			Not driven

Note: The actual implementation requires that two wait states (SYNC=0110) precede the SYNC of 0000.

3.1.12 LPC Power Management

The LPCPD# signal and the CLKRUN# signal (see the the *Intel Low Pin Count Specification*) are implemented in the LPC47N350. The LPC47N350 tolerates the LPCPD# signal going active and then inactive again without LRESET# going active. This is a requirement for notebook power management functions.

The LPC Bus spec 1.0 section 8.2 states that "After LPCPD# goes back inactive, the LPC I/F will always be reset using LRST#". This text must be qualified for mobile systems where it is possible that when exiting a "light" sleep state (ACPI S1, APM POS), LPCPD# may be asserted but the LPC Bus power may not be removed, in which case LRESET# will not occur. When exiting a "deeper" sleep state (ACPI S3-S5, APM STR, STD, soft-off), LRESET# will occur.

The LPCPD# pin is implemented as a “local” powergood for the LPC bus in the LPC47N350. It is not to be used as a global powergood for the chip. It is used to minimize the LPC power dissipation. It should be used to reset the LPC block and hold it in reset.

Prior to going to a low-power state, the system asserts the LPCPD# signal. LPCPD# goes active at least 30 microseconds prior to the LCLK signal stopping low and power being shut to the other LPC interface signals. Upon recognizing LPCPD# active, there are no further transactions on the LPC interface.

Chapter 4 ACPI Embedded Controller

ACPI defines a standard hardware and software communications interface between the OS and an embedded controller. This interface allows the OS to support a standard driver that can directly communicate with the embedded controller, allowing other drivers within the system to communicate with and use the EC resources; for example, Smart Battery and AML code (Figure 4.1).

The LPC47N350 contains an Embedded Controller Interface (ECI) to handle SCI Wake and Run-time event processing (Figure 4.2). The ECI is configured in Logical Device Number 8 in the LPC47N350 configuration register map and presents an 8042-style interface to the ISA host.

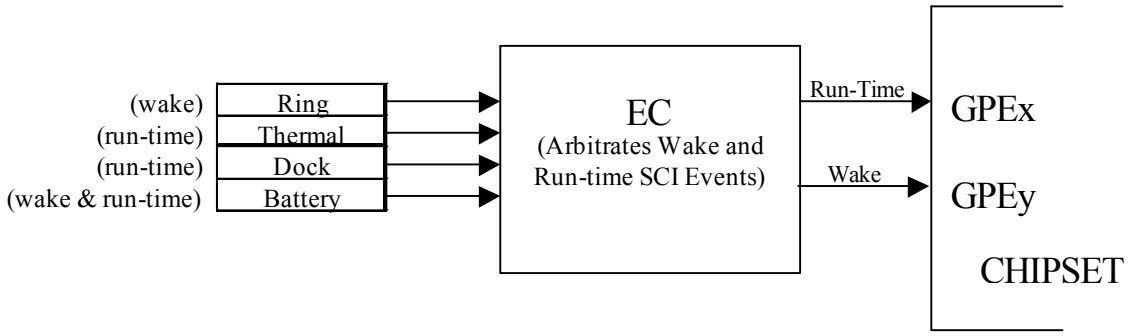


Figure 4.1 Embedded Control (EC) Illustration

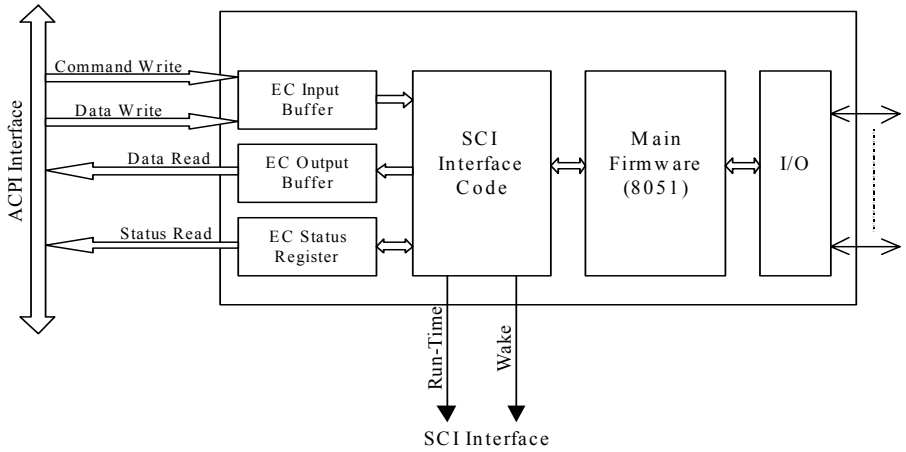


Figure 4.2 Generic ACPI EC Block Diagram

4.1 ECI Configuration Registers

The three device configuration registers in LDN8 provide ECI activation control and the base address for the ECI run-time registers (Table 4.1). Register 0x30 is the Activate register. The Activate register qualifies address decoding for the ECI; e.g., if the Activate bit D0 in the Activate register is “0”, ECI addresses will not be decoded; if the Activate bit is “1”, ECI addresses will be decoded depending on the values programmed in the ECI Primary Base Address registers. Registers 0x60 and 0x61 are the ECI Primary Base Address registers. Register 0x60 is the ECI Primary Base Address High Byte, register 0x61 is the ECI Primary Base Address Low Byte.

Note: Bits D0 and D2 in the ECI Primary Base Address Low Byte must be “0”. For example, 0x62 is a valid ECI Base Address, while 0x66 is not a valid ECI Base Address. The valid ECI Primary Base Address range is 0x0000 – 0x0FFA.

Table 4.1 ECI Configuration Registers (LDN8)

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1 & VCC0 POR	DESCRIPTION							
						D7	D6	D5	D4	D3	D2	D1	D0
0x30	R/W	0x00	0x00	0x00	-	ACTIVATE							
						Reserved							Activate
0x60	R/W	0x00	0x00	0x00	-	ECI PRIMARY BASE ADDRESS HIGH BYTE							
						“0”	“0”	“0”	“0”	A11	A10	A9	A8
0x61	R/W	0x62	0x62	0x62	-	ECI PRIMARY BASE ADDRESS LOW BYTE (See Note 4.1))							
						A7	A6	A5	A4	A3	“0”	A1	“0”

Note 4.1 Bits D0 and D2 of the ECI Base Address Low Byte must be “0”.

4.2 ECI Runtime Registers

An ACPI-compliant ECI contains three registers: EC_COMMAND, EC_STATUS, and EC_DATA. The ECI registers occupy two addresses in the Host I/O space (Table 4.2).

The EC_DATA and EC_COMMAND registers appear as a single 8-bit data register in the 8051. The CMD bit in the EC_STATUS register is used by the 8051 to discriminate commands from data written by the host to the ECI. CMD is controlled by hardware: host writes to the EC_DATA register set CMD = “0”; host writes to the EC_COMMAND register set CMD = “1”.

Descriptions of these registers follow in the sections below.

Table 4.2 ECI Run-Time Registers

	ISA HOST INTERFACE		8051 INTERFACE					
REGISTER NAME	HOST INDEX	HOST TYPE	CMD (Note 4.2)	8051 INDEX (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR
EC_DATA	ECI Base Address	R/W	0	0x53	R/W	VCC1	-	-
EC_COMMAND	ECI Base Address + 4	W	1	0x53	R		-	-
EC_STATUS		R	-	0x54	R/W		0x00	-

Note 4.2 CMD is bit D3 in the EC_STATUS register.

4.3 EC_STATUS Register

The EC_STATUS register indicates the state of the Embedded Controller Interface. To the host, the EC_STATUS register is read-only. To the 8051, some bits in the EC_STATUS register are read-only (Table 4.3). These bits are controlled by hardware. The 8051 software controlled bits in the EC_STATUS register are read/write.

Table 4.3 EC_Status Register

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R	R	R	R
8051 TYPE	R/W	R/W	R/W	R/W		R/W		
NAME	UD (Note 4.3)	SMI_EVT	SCI_EVT	BURST	CMD	UD (Note 4.3)	IBF	OBF

Note 4.3 The UD bits are User-Defined. UD bits are maintained by 8051 software, only.

OBF Bit – D0

The Output Buffer Full (OBF) flag is set when the 8051 writes a byte of data into the data port (EC_DATA), but the host has not yet read it.

Once the host reads the status byte and sees the OBF flag set, the host reads the data port to get the byte of data that the 8051 has written.

Once the host reads the data, the OBF flag is automatically cleared by hardware. An EC_OBF interrupt signals the 8051 that the data has been read by the host and the 8051 is free to write more data to the EC_DATA register.

The EC_OBF interrupt is generated whenever the OBF bit in the EC_STATUS register is reset. The EC_OBF interrupt is routed to bit 4 in the INT1 SRC register (see Section 7.9.4, "8051 INT1 Source Register," on page 68 and Figure 7.4 on page 65). The EC_OBF interrupt mask is bit 4 in the INT1 Mask register.

IBF Bit – D1

The Input Buffer Full (IBF) flag is set when the host has written a byte of data to the command or data port, but the 8051 has not yet read it.

An EC_IBF interrupt signals the 8051 that there is data available. Once the 8051 reads the status byte and sees the IBF flag set, the 8051 reads the data port to get the byte of data that the host has written.

Once the 8051 reads the data, the IBF flag is automatically cleared by hardware. The 8051 must then generate a software interrupt (SCI) to alert the host that the data has been read and that the host is free to write more data to the ECI as needed.

An EC_IBF interrupt is generated whenever the IBF bit in the EC_STATUS register is set. The EC_IBF interrupt is routed to bit 5 in the INT1 SRC register. The EC_IBF interrupt mask is bit 5 in the INT1 Mask register.

CMD Bit – D3

The CMD bit is “1” when the EC_DATA register contains a command byte; the CMD bit is “0” when the EC_DATA register contains a data byte.

The CMD bit is controlled by hardware: host writes to the EC_DATA register set CMD = “0”; host writes to the EC_COMMAND register set CMD = “1”.

The CMD bit allows the embedded controller to differentiate the start of a command sequence from a data byte write operation.

BURST Bit – D4

The BURST bit is “1” when the EC is in Burst Mode for polled command processing; the BURST bit is “0” when the EC is in Normal Mode for interrupt-driven command processing.

The BURST bit is an 8051-maintained software flag that indicates the embedded controller has received the Burst Enable command from the host, has halted normal processing, and is waiting for a series of

commands to be sent from the host. Burst Mode allows the OS or system management handler to quickly read and write several bytes of data at a time without the overhead of SCIs between commands.

Note: The BURST bit is maintained by 8051 software, only.

SCI_EVT Bit – D5

The SCI Event flag SCI_EVT is “1” when an SCI event is pending; i.e., the 8051 is requesting an SCI query; SCI_EVT is “0” when no SCI events are pending.

The SCI_EVT bit is an 8051-maintained software flag that is set when the embedded controller has detected an internal event that requires operating system attention. The EC sets SCI_EVT before generating an SCI to the OS.

Note: The SCI_EVT bit is maintained by 8051 software, only.

SMI_EVT Bit – D6

The SMI Event flag SMI_EVT is “1” when an SMI event is pending; i.e., the 8051 is requesting an SMI query; SMI_EVT is “0” when no SMI events are pending.

The SMI_EVT bit is an 8051-maintained software flag that is set when the embedded controller has detected an internal event that requires system management interrupt handler attention. The EC sets SMI_EVT before generating an SMI.

Note: The SMI_EVT bit is maintained by 8051 software, only.

4.4 EC_COMMAND Register

The EC_COMMAND register is a write-only register that allows the host to issue commands to the embedded controller.

Writes to the EC_COMMAND register are latched in the 8051 data register and the input buffer full flag is set in the EC_STATUS register. Writes to the EC_COMMAND register also cause the CMD bit to be set to “1” in the EC_STATUS register.

4.5 EC_DATA Register

The EC_DATA register is a read/write register that allows the host to issue command arguments to the embedded controller and allows the OS to read data returned by the embedded controller.

Host writes to the EC_DATA register are latched in the 8051 data register and the input buffer full flag is set in the EC_STATUS register. Host writes to the EC_DATA register also cause the CMD bit to be reset to “0” in the EC_STATUS register.

Host reads from the EC_DATA register return data from the 8051 data register and clear the output buffer full flag in the EC_STATUS register.

Chapter 5 Serial Port (UART)

The LPC47N350 incorporates one full function UART. The UART is compatible with the 16450, the 16450 ACE registers and the 16C550A. The UART performs serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UART contains a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UART is also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UART. The interrupt from a UART is enabled by programming OUT2 of the UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt.

5.1 Register Description

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Section 23.2, "Configuration Registers"). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The LPC47N350 contains a serial port, which contains a register set as described below.

Table 5.1 Addressing the Serial Port

DLAB (Note 5.1)	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0			Transmit Buffer (write)
0	0		1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0		0	FIFO Control (write)
X	0		1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1		1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1		1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0		1	Divisor MSB (read/write)

Note 5.1 DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

5.1.1 Receive Buffer Register (RB)

Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the

serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

5.1.2 Transmit Buffer Register (TB)

Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

5.1.3 Interrupt Enable Register (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower three bits of this register control the enables of the four interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the LPC47N350. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

BIT 0

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

BIT 1

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

BIT 2

This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

BIT 3

This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state. This bit is not supported.

BITS 4 – 7

These bits are always logic "0".

5.1.4 FIFO Control Register (FCR)

Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. This write only register has a shadow register at MBX9Bh (see Table 17.1, “Mailbox Registers Interface,” on page 191). **Note:** DMA is not supported.

BIT 0

Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

BIT 1

Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to “0”. The shift register is not cleared. This bit is self-clearing.

BIT 2

Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to “0”. The shift register is not cleared. This bit is self-clearing.

BIT 3

Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

BITS 4 and 5

Reserved.

BITS 6 and 7

These bits are used to set the trigger level for the RCVR FIFO interrupt.

Table 5.2 RCVR FIFO Trigger Level

BIT 7	BIT 6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

5.1.5 Interrupt Identification Register (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Three levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

BIT 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

BITS 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by Table 5.3, "Interrupt Control Table".

BIT 3

In non-FIFO mode, this bit is a logic "0". In FIFO mode, this bit is set along with bit 2 when a timeout interrupt is pending.

BITS 4 and 5

These bits of the IIR are always logic "0".

BITS 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

Table 5.3 Interrupt Control Table

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
		0		Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1					Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1		Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register

5.1.6 Line Control Register (LCR)

Address Offset = 3H, DLAB = 0, READ/WRITE

This register contains the format information of the serial line. The bit definitions are:

BITS 0 and 1

These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Table 5.4 Serial Character

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

The Start, Stop and Parity bits are not included in the word length.

BIT 2

This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

Table 5.5 Stop Bits

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
	6 bits	2
	7 bits	
	8 bits	

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

BIT 3

Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

BIT 4

Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1", an even number of bits is transmitted and checked.

BIT 5

Stick Parity bit. When parity is enabled, it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1, the Parity bit is transmitted and checked as a 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled. Bit 3 is a logic "1" and bit 5 is a logic "1", the parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

BIT 6

Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

BIT 7

Divisor Latch Access Bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

5.1.7 Modem Control Register (MCR)

Address Offset = 4H, DLAB = X, READ/WRITE

This register is used to enable the UART interrupt and enable the loopback feature. The contents of the MODEM control register are described below.

BIT 0

This bit controls the Data Terminal Ready (nDTR) output. This bit is not supported.

BIT 1

This bit controls the Request To Send (nRTS) output. This bit is not supported.

BIT 2

This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

BIT 3

Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

BIT 4

This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State (logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The interrupts are still controlled by the Interrupt Enable Register.

BITS 5 - 7

These bits are permanently set to logic zero.

5.1.8 Line Status Register (LSR)

Address Offset = 5H, DLAB = X, READ/WRITE

BIT 0

Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

BIT 1

Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely

received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

BIT 2

Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

BIT 3

Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

BIT 4

Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs, only one zero character is loaded into the FIFO. Restarting after a break is received requires the serial data (RXD) to be logic "1" for at least 1/2 bit time. **Note:** Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

BIT 5

Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode, this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

BIT 6

Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode, this bit is set whenever the THR and TSR are both empty,

BIT 7

This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

5.1.9 Modem Status Register (MSR)

Address Offset = 6H, DLAB = X, READ/WRITE

BIT 0

Delta Clear To Send (DCTS). This bit reads ‘0’.

BIT 1

Delta Data Set Ready (DDSR). This bit reads ‘0’.

BIT 2

Trailing Edge of Ring Indicator (TERI). This bit reads ‘0’.

BIT 3

Delta Data Carrier Detect (DDCD). This bit reads ‘0’

BIT 4

This bit is the complement of the Clear To Send (nCTS) input. This bit reads ‘0’.

BIT 5

This bit is the complement of the Data Set Ready (nDSR) input. This bit reads ‘0’.

BIT 6

This bit is the complement of the Ring Indicator (nRI) input. This bit reads ‘0’.

BIT 7

This bit is the complement of the Data Carrier Detect (nDCD) input. This bit reads ‘0’.

5.1.10 Scratchpad Register (SCR)

Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a Scratchpad register to be used by the programmer to hold data temporarily.

5.1.11 Programmable Baud Rate Generator (and Divisor Latches DLH, DLL)

The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal PLL clock by any divisor from 1 to 65535. The internal PLL clock is divided down to generate a 1.8462MHz frequency for Baud Rates less than 38.4k, a 1.8432MHz frequency for 115.2k, a 3.6864MHz frequency for 230.4k and a 7.3728MHz frequency for 460.8k. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers, the output divides the clock by the number 3. If a 1 is loaded, the output is the inverse of the input oscillator. If a two is loaded, the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded, the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

Table 5.6 shows the baud rates possible.

Table 5.6 UART Baud Rates

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL (SEE Note 5.2)	HIGH SPEED BIT (SEE Note 5.3)
50	2304	0.1	X
75	1536	-	
110	1047	-	
134.5	857	0.4	
150	768	-	
300	384	-	
600	192	-	
1200	96	-	
1800	64	-	
2000	58	0.5	
2400	48	-	
3600	32	-	
4800	24	-	
7200	16	-	
9600	12	-	
19200	6	-	
38400	3	-	
57600	2	0.16	
115200	1		
230400	32770		1
460800	32769		

Note 5.2 The percentage error for all baud rates, except where indicated otherwise, is 0.2%.

Note 5.3 The High Speed bit is located in the Device Configuration Space.

Baud Rates

Using 1.8462 MHz Clock for Baud Rate <= 57.6K;

Using 1.8432 MHz Clock for Baud Rate = 115.2k;

Using 3.6864 MHz Clock for Baud Rate = 230.4k;

Using 7.3728 MHz Clock for Baud Rate = 460.8k

5.2 FIFO Interrupt Mode Operation

5.2.1 RCVR Interrupts

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

1. The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR=06H) has higher priority than the received data available (IIR=04H) interrupt.
4. The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

5.2.2 RCVR FIFO Timeout Interrupts

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

1. A FIFO timeout interrupt occurs if all the following conditions exist:

- at least one character is in the FIFO
- The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay).
- The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum “character-received-to-interrupt-issued” delay of 160 msec at 300 BAUD with a 12 bit character.

2. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
3. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
4. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

5.2.3 XMIT Interrupts

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

1. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
2. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

5.3 FIFO Polled Mode Operation

With FCR bit 0 = "1", resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

Bit 0 = '1' as long as there is one byte in the RCVR FIFO.

Bits 1:4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.

Bit 5 indicates when the XMIT FIFO is empty.

Bit 6 indicates that both the XMIT FIFO and shift register are empty.

Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

5.3.1 Effect of the Reset on the Register File

The Reset Function Table (Table 5.7) details the effect of $V_{cc}2$ POR or nRESET_OUT on each of the registers of the Serial Port.

Table 5.7 Reset Function Table

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.		Bit 0 is high; Bits 1 - 7 low
FIFO Control		All bits low
Line Control Reg.		
MODEM Control Reg.		
Line Status Reg.		All bits low except 5, 6 high
MODEM Status Reg.		All bits low
TXD1, TXD2		High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	
INTRPT (THRE)	RESET/Read IIR/Write THR	
OUT2B	RESET	High
RTSB		
DTRB		
OUT1B	RESET	High
RCVR FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO		

Table 5.8 Register Summary for an Individual UART Channel

REG ADDR (Note 5.4)	REG NAME	REG SYMBOL	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 5.5	Data Bit 1	Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1	Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Enable Receiver Line Status Interrupt (ELSI)	Not Supported	0	0	0	0
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit	Interrupt ID Bit	Interrupt ID Bit (Note 5.9)			FIFOs Enabled (Note 5.9	FIFOs Enabled (Note 5.9)
ADDR = 2	FIFO Control Register (Write Only)	FCR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select (Note 5.10	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)	Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
ADDR = 4	MODEM Control Register	MCR	Not Supported	Not Supported	OUT1 (Note 5.7)	OUT2 (Note 5.7)	Loop	0	0	0
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)	Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 5.6)	Error in RCVR FIFO (Note 5.9)
ADDR = 6	MODEM Status Register	MSR	0	0	0	0	0	0	0	0
ADDR = 7	Scratch Register (Note 5.8)	SCR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7

Table 5.8 Register Summary for an Individual UART Channel (continued)

REG ADDR (Note 5.4)	REG NAME	REG SYMBOL	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 5.4 DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 5.5 Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 5.6 When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Note 5.7 This bit no longer has a pin associated with it.

Note 5.8 When operating in the XT mode, this register is not available.

Note 5.9 These bits are always zero in the non-FIFO mode.

Note 5.10 Writing a one to this bit has no effect. DMA modes are not supported in this chip.

5.3.2 Notes on Serial Port FIFO Mode Operation

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

5.3.3 TX and RX FIFO Operation

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. The UART will prevent loads to the Tx FIFO if it currently holds 16 characters. Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO, the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. Therefore, after the first byte has been loaded into the FIFO, the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. To prevent the software from having to check for this situation, the chip incorporates a timeout interrupt.

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

Chapter 6 Auto Power Management

Auto Power Management (APM) capabilities are provided for the UART logical device. For each logical device, two types of power management are provided; direct powerdown and auto powerdown.

6.1 System Power Management

See the Chapter 12, 8051 System Power Management for details.

6.2 UART Power Management

Direct power management is controlled by CR22. Refer to CR22 in the configuration section for more information.

Auto power management is enabled by CR23 bit 4 and bit 5. When set, these bits allow the following auto power management operations:

1. The transmitter enters auto powerdown when the transmit buffer and shift register are empty.
2. The receiver enters powerdown when the following conditions are all met:

a. Receive FIFO is empty

b. The receiver is waiting for a start bit

Note: While in powerdown the Ring Indicator interrupt is still valid.

6.3 Exit Auto Power-Down

The transmitter exits powerdown on a write to the transmit buffer. The receiver exits auto powerdown when RXD changes state.

Chapter 7 8051 Embedded Controller

7.1 8051 Functional Overview

The High-Performance 8051 embedded controller is a fully static CMOS core compatible with the industry-standard 80C51 microcontroller. The high-performance 8051 features include:

- 2.5X average instruction execution speed improvement over the entire instruction set; i.e., typical 4-clock instruction cycle in high-performance 8051 vs. 12-clock instruction cycle in standard 8051.
- Faster clock speed: 32MHz or higher vs. 16MHz in standard 8051.
- Dual Data Pointers
- More Interrupts: Power-Fail, External Interrupt 2, External Interrupt 3, etc.
- A set of External Memory/Mapped Control Registers provides the 80C51 core with the ability to directly control many functional blocks of the LPC47N350.

7.1.1 Features

- Internal 64K Flash ROM
- Programmed From Direct Parallel Interface, 8051, or LPC Host
- 2k-Byte Lockable Boot Block
- 512 Byte Scratch ROM
- 256 Bytes Internal Data RAM
- 512 Bytes of External Data RAM
- 256 Byte External Memory-Mapped Control Register Area
- 128 Byte Special Function Register Area
- Access to 256 Byte RTC CMOS RAM
- 8042 style Keyboard Controller Host Interface
- Eleven Interrupt Sources
- Watch Dog Timer (WDT)
- Ring Oscillator with Fail Safe Control

7.2 High-Performance 8051 Implemented Features

There are five significant features implemented in the high-performance 8051 core. These features, summarized in Table 7.1, are described more fully in the sub-sections that follow.

Table 7.1 High-Performance 8051 Implemented Features

FEATURE	VALUE	DESCRIPTION
Internal RAM Size	256 (bytes)	The internal RAM size is 256 bytes to maintain compatibility with existing implementations.
Internal Timers	3	There are three internal Timers (T0, T1 & T2). The external inputs for Timer/Counter T0, T1, and T2, as well as the Timer/Counter 2 capture/reload trigger T2EX are not supported in the LPC47N350.
Serial Ports	1	There is one Serial Port.

Table 7.1 High-Performance 8051 Implemented Features (continued)

FEATURE	VALUE	DESCRIPTION
Interrupts	11	The high-performance 8051 interrupt unit provides 11 interrupt sources (see Table 7.15 on page 66).

7.2.1 Functional Blocks

Below are the functional blocks that the 8051 core has control of through its on-chip memory/mapped external registers.

- 8042-Style Keyboard Controller Interface
- Extended Interrupts
- Power Management Functions
- Direct Keyboard Scan Matrix (up to 128 keys)
- Four channel PS/2 Interface
- Dual I^2C/SMBus Interface
- LED controls
- RTC CMOS RAM Access
- 24 General Purpose I/O (GPIO) pins
- ACPI Embedded Controller (see Chapter 4)
- PM1 Block
- Four Pulse Width Modulators
- Dual Fan Tachometer interface
- Mailbox Register Interface
- Serial Peripheral Interface (SPI)

7.2.2 High-Performance 8051 Cycle Timing and Instruction Set

The high-performance 8051 processor offers increased performance by executing instructions in a 4-clock cycle, as opposed to the standard 8051. The shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectures.

Some instructions require a different number of instruction cycles on the high-performance 8051than they do on the standard 8051. In the standard 8051, all instructions except for MUL and DIV take one or two instruction cycles to complete. In the high-performance 8051 architecture, instructions can take between one and five instructions to complete. The average speed improvement for the entire instruction set is approximately 2.5X. See Table A.1, “Legend for Instruction Set Table,” on page 309 for number of cycles on individual instruction requirements.

7.3 Powering Up or Resetting the 8051

7.3.1 Default Reset Conditions

The LPC47N350 has two sources of reset: a VCC1 Power On Reset (VCC1 POR) or a VCC2 POR. An LPC47N350 reset from any of these sources will cause the hardware response shown in Table 7.7, "8051 On-Chip External Memory Mapped Registers". Note that the values shown are those prior to any resident firmware control. Refer to Table 7.7 for the effect of each type of reset on each of the on-chip registers.

7.3.1.1 Power-Up Sequence

When the 8051 first powers up by VCC1, the ring oscillator is started. Once this has stabilized, the 8051 starts executing from program address 00. Once running, the 8051 can access all of the registers that are on VCC1 and if VCC2 is at 3.3V, it can access all of the registers on VCC2. For on-chip registers powered by VCC1 which are reset upon VCC2 Power On Reset (VCC2 POR), it is important that 8051 firmware not initialize or write to any of these registers until 1ms following VCC2 = 3.3V AND PWRGD = 1 (See Table 7.7).

Note: In order to guarantee that the external Flash device has powered up and is ready to operate before the 8051 attempts to access it, the internal VCC1 POR pulse has been extended to 20ms. The internal VCC1 POR signal is asserted upon VCC1 reaching a valid level and will remain asserted for a period of 20ms following the assertion of the VCC1_PWRGD pin.

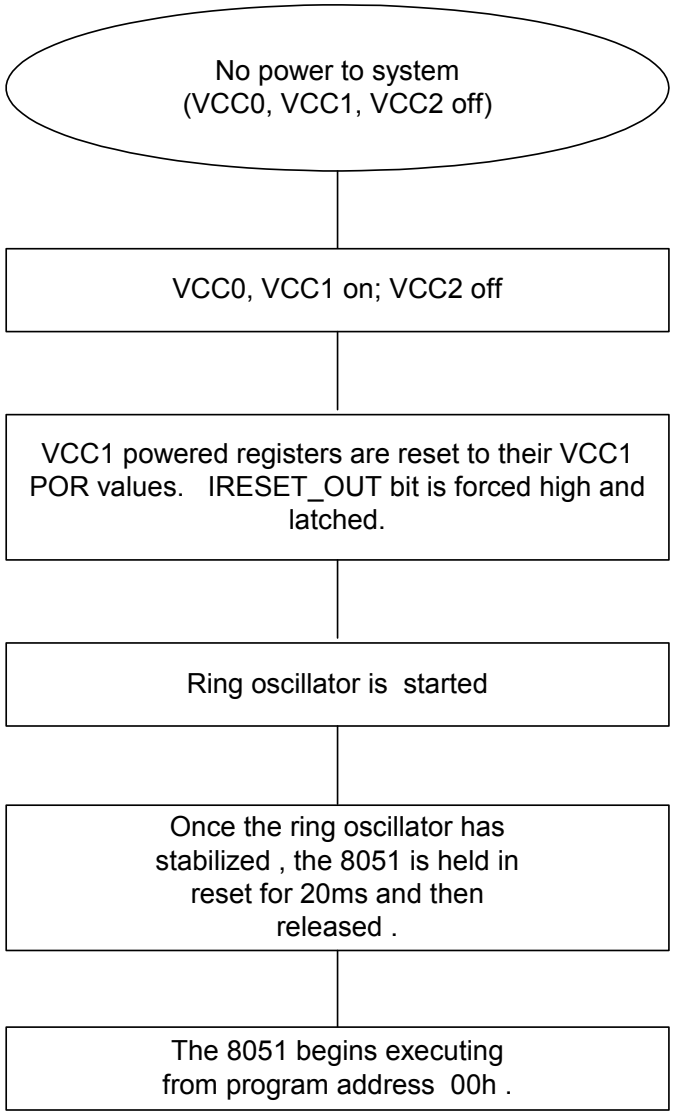
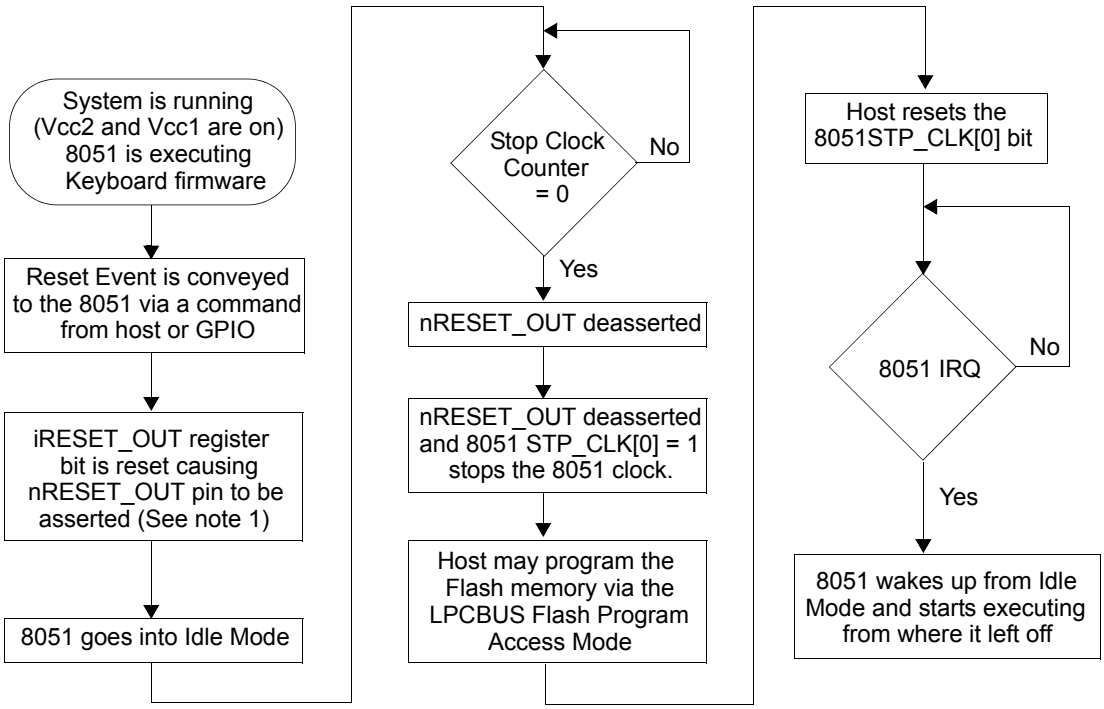


Figure 7.1 System Power-Up Sequence



Note 1:
Clearing the iRESET_OUT bit causes the following:

- 8051 STP_CLK[0] = 1
- Stop Clock Counter starts decrementing

Note 2: In order to leave Idle Mode, the 8051 must receive an interrupt; typically a software timer interrupt will be used.

Figure 7.2 Typical System Reset Sequence

7.4 CPU RESET Sequence

Often the Host CPU (Pentium) is reset by the hardware signal, CPU_RESET, which is issued by software to switch the Processor from Protected, or “Virtual 86”, mode back to Real mode. CPU_RESET can be generated from the LPC47N350 8051 core or it may be generated from other logic on the PC motherboard. CPU_RESET is meant only to reset the CPU; the rest of the system continues to run normally, including the keyboard BIOS in the 8051.

7.5 8051 Clock Controls

The LPC47N350 has two clock source:

The 8051 may program itself to run off of an internal ring oscillator having a frequency range between 4 and 12MHz. This is not a precise clock, but is meant to provide the 8051 with a clock source when VCC2 is shut down in the system.

When VCC2 is powered, the 8051 may be programmed to run off the PLL. The 14.318MHz external clock source. The 8051 PLL clock frequenies are programmable.

7.5.1 Frequency Controls

The KBDCLK ENABLE bit controls the running of the 8051 PLL clock and the KBDCLK[1:0] control bits in the KSTP_CLK register (MMCR 0x7F27) select the 8051 system clock frequencies. The LPC47N350 8051 can run up to 32MHz.

Table 7.2 STOP_COUNT Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F2F
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved				STP_CNT[3:0]			

STP_CNT[x]

This defines the number of machine cycles from when the internal IRESET_OUT bit is cleared until the external nRESET_OUT pin goes inactive high (deasserts). See Section 7.8.3.5, "Output Enable Register," on page 62

Table 7.3 KSTP_CLK Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F27
POWER	VCC1
DEFAULT	0x10

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
BIT NAME	KBDCLK[1:0] (See Table 7.4)		KBCLK/ ROSC	ROSCEN	Reserved		PLL_STOP	KBDCLK ENABLE

KBDCLK/ENABLE

When the KBDCLK ENABLE bit is “0”, the 8051 PLL clock is stopped. When KBDCLK ENABLE is “1”, the 8051 PLL clock is running (See Table 7.4, "KBDCLK Control Bit Encoding").

PLL_STOP

The PLL_STOP bit D1 is used to control the power state of the 14.318MHz PLL. When the PLL_STOP bit is “1,” the PLL and all of the internal clocks except for the RTC and Ring Oscillator are stopped. When the PLL_STOP bit is “0,” the PLL and all of the internal clocks are running. When VCC2 is active

and the PLL_STOP bit changes from “1” to “0”, there is a delay of 100µs max. before the PLL clocks are stable.

ROSCEN

This bit reflects the state of the ring oscillator clock at all times. The 8051 can write this bit to start or stop the ring oscillator. Other hardware events can also start or stop this clock.

= 1 turn on ring oscillator

= 0 turn off ring oscillator

This bit is reset when the 8051 goes into “SLEEP” mode and is set when the 8051 first wakes up from “SLEEP” mode.

Note 7.1 When VCC1 is active and the ROSCEN bit changes from “0” to “1”, there is a delay of 6 µs max. before the ring oscillator starts.

KBCLK/ROSC

This bit is used to control the clock source for the 8051.

1 = 8051 clock source is KBCLK

0 = 8051 clock source is ring oscillator.

This bit is reset when the 8051 just wakes up from the “SLEEP” mode

KBDCLK[1:0]

These 2 bits control the 8051 system clock frequencies (See Table 7.4, "KBDCLK Control Bit Encoding").

Table 7.4 KBDCLK Control Bit Encoding

KBDCLK[1:0] BITS (SEE Table 7.3) KSTP_CLK REGISTER		KBD CLOCK FREQUENCIES
D7 = KBDCLK[1]	D6 = KBDCLK[0]	LPC47N350
0	0	12MHz
	1	16MHz
1	0	24MHz
	1	32MHz

7.6 8051 Ring Oscillator Fail-Safe Controls

A fail-safe control for the 8051 ring oscillator protects against unpredicted VCC2 power failures. The fail-safe ring oscillator sequence occurs as follows:

1. A VCC2 power-fail event is detected when the PWRGD pin changes from “1” to “0” (see Figure 2.1 on page 12).
2. The power-fail event sequence starts the 8051 Ring Oscillator. The Ring Oscillator frequency range is 4MHz to 12MHz.
3. After a delay of 2.76µs max. the 8051 clock starts transitioning to the Ring Oscillator.
4. A smooth transition requires two ring clocks and two PPL clocks.
5. An additional 2 µs delay is incorporated to protect the rest of the chip.

6. After a maximum total elapsed time of less than 6 μs after PWRGD pin changes from “1” to “0”, the 8051 system clock is switched to the ring oscillator.

Note: Following a power fail event, VCC2 must be ≥ 3V and the 14.318MHz input clock CLOCKI must remain stable for 10μs min. (Figure 2.2).

An 8051power-fail interrupt (pfi) is generated to inform the 8051 of the power fail event.

There are four functional power-fail event scenarios. The actions taken for each are described in Table 7.5.

Table 7.5 Power-Fail Event Actions

	8051 STATE	ACTIONS			DESCRIPTION
		ASSERT PGI (SEE Note 7.2)	ASSERT RING OSC. (SEE Note 7.3)	ASSERT 8051 FLASH ACCESS	
1	Sleeping on Ring Osc.	yes	-	-	No fail-safe actions taken
2	Running on Ring Osc.		-	-	No fail-safe actions taken; 8051 can respond to PFI if needed.
3	Running on PLL		yes	-	Internal PWRGD is delayed until ring osc. is asserted.
4	Stopped on PLL			yes	Internal PWRGD is delayed until ring osc. is asserted and the 8051 controls the flash.

Note 7.2 PGI is the Powergood Interrupt bit D0 in the PWRGD_INT register (see Section 7.9.10, "Power Fail IRQ," on page 81).

Note 7.3 The 8051 is switched to the Ring Oscillator after a delay. (See PWRGD and VCC1_PWRGD timing is illustrated in Figure 2.1 through Figure 2.3).

7.7 8051 Memory Map

The LPC47N350 8051 has two types of Flash support:

64k embedded Flash ROM (see Chapter 8, 64K Embedded Flash ROM).

or

The External Flash Interface using the KBD Scan Interface that enables the 8051 program memory to reside in an external ROM device (see Section 9.10.10, "Flash Data Register," on page 125).

The 64k embedded Flash ROM flash support provides a 512-byte Scratch ROM from which the 8051 can execute program code when the 8051 Code Fetch Access interface or when the 8051 Program Access interface is selected by the Flash Program Interface Decoder (see Section 9.2, "Flash Program Interface Decoder"). The MMC bit in CONFIGURATION REGISTER 0 (MMCR 0x7FF4 see Section 7.8.3.4) controls the Scratch ROM.

7.8 8051 Control Registers

7.8.1 Special Function Registers (SFRs)

The high-performance 8051 includes SFRs to support the extended interrupt unit, timer 2, and Bit-wise Addressable 8051 SFR GPIOs. (See Appendix B "High-Performance 8051 Extended Interrupt Unit") The high-performance 8051 does not support the MISZ register.

Table 7.6 8051 Control Registers

SFR REGISTER NAME	ADDR	FIX BIT REGISTERS								VCC1 POR	NOTE
		D7	D6	D5	D4	D3	D2	D1	D0		
SGPIO	80H										Note 7.7 Note 7.8
SP	81h									7h	
DPLO	82h										
DPHO	83h										
DPL1	84h										Note 7.4
DPH1	85h										Note 7.4
DPS	86h	0	0	0	0	0	0	0	SEL		Note 7.4
PCON	87h	SMOD0	-	1	1	GF1	GF0	STOP	IDLE	30h	
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0		
TMOD	89h	GATE	C/T	M1	M0	GATE	C/T	M1	M0		
TL0	8Ah										
TL1	8Bh										
TH0	8Ch										
TH1	8Dh										
CKCON	8Eh	-	-	T2M	T1M	T0M	MD2	MD1	MD0	1h	Note 7.4 Note 7.6
SPC_FNC	8Fh								WRS	00h	Note 7.4
-	90h									00h	
EXIF	91h	IE5	IE4	IE3	IE2	1	0	0	0	8h	Note 7.4
MPAGE	92h									00h	Note 7.4 Note 7.5
SCON	98h	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0		Note 7.8
SBUF	99h										
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0		Note 7.8
IP	B8h	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0		Note 7.8

Table 7.6 8051 Control Registers (continued)

SFR REGISTER NAME	ADDR	FIX BIT REGISTERS								VCC1 POR	NOTE
		D7	D6	D5	D4	D3	D2	D1	D0		
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2		Note 7.8
RCAP2L	CAh										
RCAP2H	CBh										
TL2	CCh										
TH2	CDh										
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P		Note 7.8
EICON	D8h	SMOD1	1	EPFI	PFI	WDTI	0	0	0	40h	Note 7.4 Note 7.8
ACC	E0h										Note 7.8
EIE	E8h	1	1	1	EWDI	EX5	EX4	EX3	EX2	E0h	Note 7.4 Note 7.8
B	F0h										Note 7.8
EIP	F8h	1	1	1	PWDI	PX5	PX4	PX3	PX2	E0h	Note 7.4 Note 7.8

Note 7.4 Not part of standard 8051 architecture.

Note 7.5 The MPAGE special function register provides a means of 16-bit addressing without using the data pointer. During MOVX A, @Ri and MOVX @Ri, A instructions, the 8051 places the contents of the MPAGE register on the upper 8 address bits. The MPAGE register default is ‘00H’.

Note 7.6 The TM2 bit in the CKCON register is available, but not used, when Timer 2 is not implemented (timer =0).

Note 7.7 Not part of standard 8051 architecture. Supports SPGIO[30:33]. See Section 20.5, "Bit-Wise Addressable 8051 SFR GPIOs," on page 235.

Note 7.8 Bit-addressable register

7.8.2 Memory Mapped Control Register (MMCR)

The Memory Mapped Control Registers are on-chip memory-mapped registers that can be accessed by the 8051 but are external to the 8051 core (Table 7.7). The 8051 can access all of the Memory Mapped Control Registers. The 8051 MMCR addresses are described in Column #4 (8051 ADDR) in Table 7.7.

Some MMCRs can also be accessed through the LPC Host interface (LPCxxh), the Mailbox Registers interface (MBXxxh), the Embedded Controller Interface (ECI BASE), and the ACPI PM1 Block Interface (PM1). These addresses are described in Column #2 (SYSTEM ADDRESS) in Table 7.7.

These Memory Mapped Control Registers can be accessed by the following types of 8051 instructions:

1. movx A,@DPTR

2. movx @DPTR,A

3. mov MPAGE,#7FH
   movx A,@Rx (R0 or R1 only)

4. mov MPAGE,#7FH
   movx @Rx,A (R0 or R1 only)

Table 7.7 8051 On-Chip External Memory Mapped Registers

MMCR REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDRESS TYPE	8051 ADDRESS (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	NOTE
Reserved	-	-	F0h	-	-	-	-	
Host I/F Data Reg [KBD Data/Command Write Reg.]	LPC 60h LPC 64h	W	F1h	R	VCC1	-		Note 7.9
Host I/F Data Reg [KBD Data Read Reg.]	LPC 60h	R		W		-		
Host I/F Status Reg [KBD Status Reg.]	LPC 64h		F2h	R/W		00h		Note 7.10
RTC Address 1	LPC 70h	R/W	-	-				Note 7.16
RTC Data 1	LPC 71h		-	-		-		
RTC Address 2	LPC 74h		-	-		00h		
RTC Data 2	LPC 76h		-	-		-		
HTIMER	-	-	F3h	R/W		00h		
Config Reg 0	-	-	F4h					
RTCCNTRL	-	-	F5h			80h		
RTCADDRL	-	-	F6h			00h		
RTCDATAL	-	-	F7h			00		
RTCADDRH	-	-	F8h			00h		
RTCDATAH	-	-	F9h					
Aux Host Data Reg [KBD Data Read Reg.]	LPC 60h	R	FAh	W		-		Note 7.11
GATEA20	-	-	FBh	R/W		01h		
-	-	-	FCh	-	-	-	-	

Table 7.7 8051 On-Chip External Memory Mapped Registers (continued)

MMCR REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDRESS TYPE	8051 ADDRESS (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	NOTE
PCOBF	-	-	FDh	R/W	VCC1	00h		
SETGA20L	-	-	FEh	W		-		
RSTGA20L	-	-	FFh			-		
8051 Interrupt 0 Source Register	-	-	00h	R/WC		00h		
8051 Interrupt 0 Mask Register	-	-	01h	R/W				
8051 Interrupt 1 Source Register	-	-	02h	R/WC				
8051 Interrupt 1 Mask Register	-	-	03h	R/W				
Keyboard Scan out	-	-	04h	W		20h		
Keyboard Scan in	-	-	04h	R		-		
-	-	-	05h	-	-	-	-	
Device Rev register	-	-	06h	R	VCC1	XXh		
Device ID register	-	-	07h			15h		Note 7.19

Table 7.7 8051 On-Chip External Memory Mapped Registers (continued)

MMCR REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDRESS TYPE	8051 ADDRESS (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	NOTE
System-to-8051 Mailbox register 0	MBX 82h	R/W	08h	RC	VCC1	00		Note 7.12
8051-to-system Mailbox register 1	MBX 83h	RC	09h	R/W				Note 7.13
Mailbox register [2-F]	MBX 84h-91h	R/W	0A-17h			00h		
GPIO Direction register A	-	-	18h					
GPIO Output register A	-	-	19h					
GPIO Input register A	-	-	1Ah	R		-		
GPIO Direction register B	-	-	1Bh	R/W		00h		
GPIO Output register B	-	-	1Ch					
GPIO Input register B	-	-	1Dh	R		-		
GPIO Direction register C	-	-	1Eh	R/W		00h		
GPIO Output register C	-	-	1Fh					
GPIO Input register C	-	-	20h	R		-		
LED register	-	-	21h	R/W		00h		
OUT register D	-	-	22h					
OUT register E	-	-	23h					
-	-	-	24h	R	-	-		

Table 7.7 8051 On-Chip External Memory Mapped Registers (continued)

MMCR REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDRESS TYPE	8051 ADDRESS (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	NOTE
PWM0 register	MBX92h	R/W	25h	R/W	VCC1	00h		
PWM1 register	MBX93h		26h					
KSTP_CLK	-	-	27h			10h		
PWM Control Register	MBX9Dh	R/W	28h			30h		
PWM2 Speed Control Register	MBX95h		29h			00h		
WAKEUP Source 1	-	-	2Ah	R/WC				
WAKEUP Source 2	-	-	2Bh					
WAKEUP Mask 1	-	-	2Ch	R/W				
WAKEUP Mask 2	-	-	2Dh					
-	-	-	2Eh	R	-	-	-	
STOP COUNT	-	-	2Fh	R/W	VCC1	00h	-	
Multiplexing 3 register	-	-	30h					
I^2C/SMBus Control reg	-	-	31h	W				
I^2C/SMBus Status reg	-	-	31h	R		81h		
I^2C/SMBus Own Address reg	-	-	32h	R/W	VCC1	00h		
I^2C/SMBus Data reg	-	-	33h					
I^2C/SMBus Clock	-	-	34h					
Flash Program	MBX9Eh	R/W	35h			See Notes	-	
-	-	-	36h	-	-	-		
WDT Control/Status	-	-	37h	R/W	VCC1	00h		
WDT Timer	-	-	38h			FFh		
-	-	-	39h	-	-	-	-	
-		-	3Ah	-	-		-	-
-	-	-	3Bh	-	-		-	
--	-	-	3Ch	-	-		-	

Table 7.7 8051 On-Chip External Memory Mapped Registers (continued)

MMCR REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDRESS TYPE	8051 ADDRESS (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	NOTE
Multiplexing 1 register	-	-	3Dh	R/W	VCC1	00h		
Output Enable register			3Eh			see note	see note	Note 7.14
DISABLE register	-	-	3Fh			00h		
Multiplexing 2 register	-	-	40h					
PS/2 Chan A Tx/Rx	-	-	41h		VCC2	-	FFh	
PS/2 Chan A Control	-	-	42h	R/W		-	40h	
PS/2 Chan A Status	-	-	43h	R		-	00h	
Reserved	-	-	44h		-	-	-	
PS/2 Chan B Tx/Rx	-	-	45h	R/W	VCC2	-	FFh	
PS/2 Chan B Control	-	-	46h	R/W		-	40h	
PS/2 Chan B Status	-	-	47h	R		-	00h	
PS/2_STATUS_2	-	-	48h	R, R/WC		-		
PS/2 Chan C Tx/Rx	-	-	49h	R/W		-	FFh	
PS/2 Chan C Control	-	-	4Ah			-	40h	
PS/2 Chan C Status	-	-	4Bh	R		-	00h	
Reserved	-	-	4Ch		-	-	-	
PS/2 Chan D Tx/Rx	-	-	4Dh	R/W	VCC2	-	FFh	
PS/2 Chan D Control	-	-	4Eh			-	40h	
PS/2 Chan D Status			4Fh	R		-	00h	
-	-	-	50h-51h	-	-	-	-	

Table 7.7 8051 On-Chip External Memory Mapped Registers (continued)

MMCR REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDRESS TYPE	8051 ADDRESS (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	NOTE
8051_SIRQ	-	-	52h	R/W	VCC1	00h	-	
EC_DATA	ECI BASE	R/W	53h					Note 7.15
EC_COMMAND	ECI BASE+4	W	53h					Note 7.15
EC_STATUS	ECI BASE+4	R	54h					Note 7.15
Wake up SRC 8	-	-	55h	R/WC			-	
Wake up MSK 8	-	-	56h	R/W			-	
Edge Select 4A			57h				-	
Edge Select 4B			58h					
Wake up SRC 4			59h	R/WC				
Wake Up Mask 4			5Ah	R/W				
-	-	-	5Bh	-	-	-	-	
Edge Select 5A			5Ch	R/W	VCC1	00h		
Edge Select 5B			5Dh					
Wake up SRC 5			5Eh	R/WC				
Wake Up Mask 5			5Fh	R/W				
-	-	-	60h	-	-	-	-	
Edge Select 6A			61h	R/W	VCC1	00h		
Edge Select 6B			62h					
Wake up SRC 6			63h	R/WC				
Wake up SRC 7	-	-	64h					
Wake up MSK 7	-	-	65h	R/W				
Wake Up Mask 6			66h					
I^2C/SMBus 2 Control reg	-	-	67h	W				
I^2C/SMBus 2 Status reg	-	-	67h	R		81h		
I^2C/SMBus 2 Own Address reg	-	-	68h	R/W		00h		
I^2C/SMBus 2 Data reg	-	-	69h					
I^2C/SMBus 2 Clock	-	-	6Ah					
-	-	-	6Bh – 6Fh	-	-	-	-	

Table 7.7 8051 On-Chip External Memory Mapped Registers (continued)

MMCR REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDRESS TYPE	8051 ADDRESS (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	NOTE
Mailbox registers[10-1F]	MBX A0-AF	R/W	70h-7Fh	R/W	VCC1	00		
PM1_STS2	PM1+1	R/WC	80h					
PM1_EN2	PM1+3	R/W	81h	R				
PM1_CNTRL2	PM1+5		82h					
8051_PM_STS	-	-	83h	R/W	VCC1	00	-	
PWRGD_INT	-	-	84h	R/WC			-	
-	-	-	85h	R	-	-	-	
DMS Register	-	-	86h	R/W	VCC1	00	-	
-	-	-	87h	-	-	-	-	
Flash Boot Block Protect	-	-	88h	R/W	VCC1	00	-	
I^2C/SMBus Switch Register	-	-	89h			03	-	
LPC Bus Monitor	-	-	8Ah	R		00	-	
-	-	-	8Bh-8Dh	-	-	-	-	
Test Register	-	-	8Eh-8Fh	-	-	-	-	
-	-	-	90h-94h	-	-	-	-	

Table 7.7 8051 On-Chip External Memory Mapped Registers (continued)

MMCR REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDRESS TYPE	8051 ADDRESS (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	NOTE
PWM3 Speed Control Register	MBX98h		95h	R/W	VCC1	00h	-	
PWM3 Control Register	MBX99h		96h			04h	-	
PWM0 Frequency Multiply	MBXB0h		97h			00h	-	
PWM1 Frequency Multiply	MBXB1h		98h				-	
PWM2 Frequency Multiply	MBXB2h		99h		VCC2	-	00h	
PWM3 Frequency Multiply	MBXB3h		9Ah		VCC1	00h		
FAN1 Read Latch	-	-	9Bh	R			-	
FAN2 Read Latch	-	-	9Ch				-	
FAN1 Pulse Counter Preload	-	-	9Dh	R/W			-	
FAN2 Pulse Counter Preload	-	-	9Eh				-	
FAN TACH Timebase Prescaler			9Fh			05h	-	
LGPIO Dir. Reg. G	-	-	A0h			00h	-	
LGPIO In Reg. G	-	-	A1h	R			-	
LGPIO Out Reg. G	-	-	A2h	R/W			-	
LGPIO Dir. Reg. H	-	-	A3h				-	
LGPIO In Reg. H	-	-	A4h	R			-	
LGPIO Out Reg. H	-	-	A5h	R/W			-	
-			A6h-A8h	-			-	
LGPIO LPC Select			A9h	R/W	VCC1		-	
LGPIO Buffer Type H			AAh			00h	-	
-			ABh	R			-	
GPIO Buffer Type	-	-	ACh	R/W			--	
SPIO Dir. Reg J	-	-	ADh				-	
			AEh-AFh				-	
Flash High Address	MBX9Fh	R/W	B0h	R/W	VCC1	00h	-	
Flash Low Address	MBX80h	R/W	B1h				-	
Flash Data	MBX81h	R/W	B2h				-	

Table 7.7 8051 On-Chip External Memory Mapped Registers (continued)

MMCR REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDRESS TYPE	8051 ADDRESS (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	NOTE
-	-	-	B3h-BAh	-	-	-	-	-
SPICR	-	-	BBh	R/W	VCC1	00h	-	Note 7.17
SPISR	-	-	BCh	R		01h	-	
SPIDR	-	-	BDh	R/W		00h	-	Note 7.17 Note 7.18
SPICC	-	-	BEh				-	Note 7.17
SPIBR	-	-	BFh				-	
-	-	-	C0h-EFh	-	-	-	-	
512 bytes of RAM	-	-	7D00-7EFFh	R/W	VCC1			

Note 7.9 Although the Input and Output Data registers are physically separate, they share address 7FF1.

Note 7.10 The 8051 CPU cannot write to some bits of the Status register.

Note 7.11 Writing to the Auxiliary Output Data Register, loads the Output data register and can set the AUXOBF1 output if enabled. This does not set the PCOBF output.

Note 7.12 Interrupt is cleared when read by the 8051.

Note 7.13 Interrupt is cleared when read by the host.

Note 7.14 VCC1 POR = 00000X10b, VCC2 POR = 00000X1Xb where X is not affected by VCC2 POR, but is left at the current value.

Note 7.15 These registers have the same structure as the keyboard interface registers.

Note 7.16 The LPC RTC registers are relocatable and accessed by the 8051 through MMCRs 0x7FF5 – 0x7FF9.

Note 7.17 The SPICR, SPISR, SPIDR, SPICC, and SPIBR registers also reset when the MISC10 bit in the Multiplexing 2 register (40h) changes from 0 to 1 OR from 1 to 0.

Note 7.18 There are two SPI Data Registers that share the same address - one read only and one write only. However, reading the data register immediately after the data register is written may return invalid data. Reading the data register in the middle of a SPI transaction will return invalid data. Any writes to the data register in the middle of a SPI transaction is ignored.

Note 7.19 This register is read only and provides device revision information.

7.8.3 8051 Configuration/Control Memory Mapped Registers

7.8.3.1 Disable Register

Table 7.8 Disable Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F3F
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R/W	R	R	R/W	R/W	R	R
BIT NAME	Reserved	Serial Port	Reserved	Reserved	UD	System Flash	Reserved	Reserved

SERIAL PORT - When this bit is asserted ‘1’, the Serial port is enabled. When this bit is deasserted ‘0’, the Serial port is disabled.

UD - The UD bit is User-Defined. UD bits are maintained by 8051 software, only.

SYSTEM FLASH - When the SYSTEM FLASH bit is asserted ‘1’, the LPC Host Flash programming interface is disabled. When the SYSTEM FLASH bit is deasserted ‘0’, the LPC Host Flash programming interface is enabled (see Section 9.5, "LPC Bus Flash Program Access," on page 110).

RESERVED - Logic ‘0’ read only access.

7.8.3.2 Device Rev Register

By reading this register, 8051 firmware can confirm the device revision that it is running on.

Table 7.9 Device Rev Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F06
POWER	VCC1
DEFAULT	Current Revison

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R
BIT DESCRIPTION	CURRENT REVISION							

This register is read only and provides device revision information.

7.8.3.3 Device ID Register

By reading this register, 8051 firmware can determine which device it is running on.

Table 7.10 Device ID Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F07
POWER	VCC1
DEFAULT	0x15

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R
BIT DESCRIPTION	0	0	0	1	0	1	0	1

7.8.3.4 Configuration Register

Table 7.11 Configuration Register 0

HOST ADDRESS	N/A
8051 ADDRESS	0x7FF4
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R	R/W	R	R/W	R/W	R/W	R/W
BIT DESCRIPTION	AUXH	Reserved	OBFEN	Reserved	MMC	PCOBFEN	SAEN	SLEEP FLAG

AUXH

Aux in Hardware; when high, AUXOBF of the status register is set in hardware by a write to 7FFAh. When low, AUXOBF of the status register is a user defined bit (UD) and R/W.

OBFEN

When set, PCOBF is gated onto KIRQ and AUXOBF1 is gated onto MIRQ. When low, KIRQ and MIRQ are driven low. Software should not change this bit when OBF of the status register is equal to 1.

MMC

Memory Map Control Bit: When MMC=0, a 512 Byte Scratch RAM area at 7B00h is available to the 8051. When MMC=1, the Scratch RAM at 7B00h-7CFFh becomes Scratch ROM at FE00h-FFFFh. When the MMC bit is ‘1’, the Scratch RAM becomes Scratch ROM and occupies 512 bytes at the top of the 64k code space; i.e., FE00h – FFFFh (see Section 9.2, "Flash Program Interface Decoder," on page 107. When the MMC bit is deasserted ‘0’, there is 512 bytes of Scratch RAM located at address 0x7B00 in the 8051 Data Space. When the MMC bit is asserted ‘1’, the 8051 can execute out of the Scratch ROM either when the 8051 Code Fetch Access interface or when the 8051 Program Access interface is selected.

Note: When the 8051 is running from external flash, i.e. when the nEA pin = ‘0’, the MMC bit must be ‘0’.

PCOBFEN

When high, PCOBF reflects whatever value was written to the PCOBF firmware latch assigned to 7FFDH. When low, PCOBF reflects the status of writes to 7FF1H (the output data register).

SAEN

Software-assist enable. When set to “1,” SAEN allows control of the GATEA20 signal via firmware. If SAEN is reset to ‘0’, GATEA20 corresponds to either the last host-initiated control of GATEA20 or the firmware write to 7FFEh or 7FFFh.

SLEEPFLAG

If SLEEPFLAG="0", when PCON bit-0 is set, the 8051 enters "IDLE" mode, whereas if SLEEPFLAG="1", when PCON bit 0 is set the 8051enters "SLEEP" mode. This bit is cleared by the occurrence of any wake-up events and on VCC1 POR.

7.8.3.5 Output Enable Register

Table 7.12 Output Enable Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F3E
POWER	VCC1
DEFAULT	**00000X10b** on VCC1 POR **00000X1Xb** on VCC2 POR

BIT	D7 - D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-
8051 TYPE	R	R/W	R	R/W	R/W
BIT DESCRIPTION	Reserved	iRESET_ OVRD	POWER_ GOOD	iRESET_OUT	32kHz Output

Note 7.20 Output Enable Register VCC1 POR = 0x00000X10, VCC2 POR = 00000X1***X***b where ***X*** means the bit holds its setting preceding VCC2 POR.

iRESET_OUT

When POWER_GOOD = 1, iRESET_OUT is controlled by the 8051. When POWER_GOOD = 0, iRESET_OUT is forced high (within 100nsec) and latched. The nRESET_OUT pin is not driven until VCC2 is applied. iRESET_OUT cannot be cleared by the 8051 until POWER_GOOD =1.

See Note 7.21 below.

In the LPC47N350, nRESET_OUT is driven high by this sequence of events.

1. Sets STP_CNT to a non-zero value
2. Clears iRESET_OUT bit, causing 8051 STP_CLK bit 0 (see Table 17.6 on page 197) to get set and STOP Counter to start decrementing
3. When STP_CNT reaches 0, the nRESET_OUT pin deasserts (goes high) at which point the 8051's clock stops.

POWER_GOOD

The Power_Good bit D2 reflects the state of the LPC47N350 Vcc2 Power Good pin PWRGD. The Power_Good bit is read only.

iRESET_OVRD

iRESET Override. When cleared, the iRESET_OUT bit functions as described above. When set, iRESET_OUT is given direct control over the internal reset and nRESET_OUT pins without requiring the STOP_CLK counter or affecting the 8051 STP_CLK bit. In the override mode, setting iRESET_OUT drives nRESET_OUT low and clearing iRESET_OUT drives nRESET_OUT high.

The RESET_OUT Override function allows the 8051 to take the rest of the LPC47N350 chip (SIO) out of reset without giving up control (i.e., without stopping its clock).

Note 7.21 In the LPC47N350, iRESET Override mode is the typical mode of operation. When the iRESET_OVRD bit is asserted, the 8051 clock cannot be stopped. Providing the mode to stop the 8051 clock is a legacy mode. To stop the 8051 clock, the iRESET_OVRD bit must be deasserted.

32 KHZ OUTPUT

The 32 kHz Output bit controls the LPC47N350 32 kHz_OUT. When 32kHz Output is '0', the 32kHz Output Clock is disabled and the 32 kHz_OUT pin is driven low. When 32 kHz Output is '1', the 32 kHz Output Clock is enabled. The 32kHz Output bit is R/W and disabled by default following Vcc1 POR.

7.8.3.6 8051 LPC Bus Monitor

The 8051 can monitor the state of the LPCPD# input pin using the LPCPD STATUS bit D0 in the LPC Bus Monitor register (Table 7.3). The LPCPD STATUS bit is the inverse of the LPCPD# pin (see Section 3.1.12, "LPC Power Management" for a description of the LPCPD# pin function).

When the LPCPD STATUS bit is '0', the LPCPD# input pin is deasserted '1'. When the LPCPD STATUS bit is '1', the LPCPD# input pin is asserted '0'.

Table 7.13 LPC Bus Monitor Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F8A
POWER	VCC1
DEFAULT	'0000000X'b

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R
BIT NAME	RESERVED							LPCPD STATUS

Note 7.22 There is no LPCPD STATUS bit default.

7.8.4 LED Controls

The LPC47N350 has three independent LED outputs that are programmable under 8051 control.

Table 7.14 LED Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F21
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
DEFAULT	0	0	0	N/A	0	0	0	0
8051 ACCESS	R	R/W	R/W	R	R/W	R/W	R/W	R/W
BIT DEF	Reserved	FDD_ LED1	FDD_ LED0	status of MODE pin	PWR_ LED1	PWR_ LED0	BAT_ LED1	BAT_ LED0
		00 FDD LED is off 01 LED flash; P=1.0 sec 10 LED flash; P=0.5 sec 11 LED is fully on		See Note 7.23	00 PWR LED is off 01 LED flash; P=3.0 sec 10 LED flash; P=1.5 sec 11 LED is fully on		00 Battery LED is off 01 LED flash; P=1.0 sec 10 LED flash; P=0.5 sec 11 LED is fully on	

Note 7.23 See Section 27.2, "Configuration Register Access," on page 277.

LED on time is T=125msec; “0” is on, “1” is off. Period “P” is indicated above.

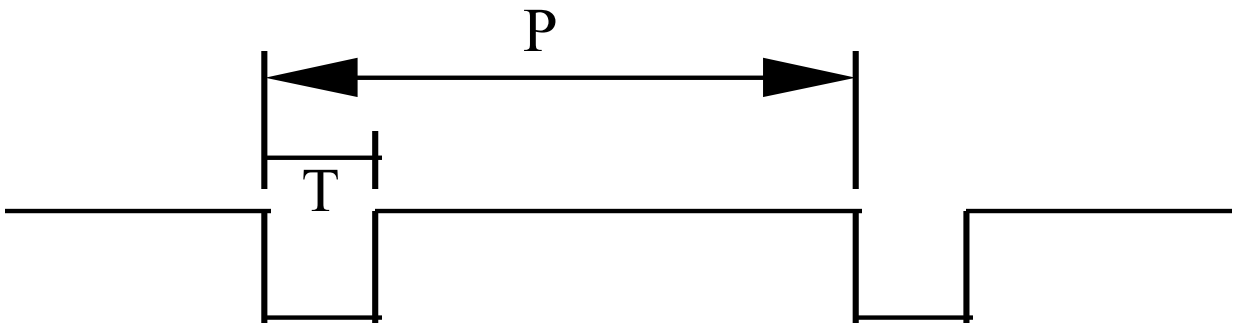


Figure 7.3 LED Output

7.9 8051 Interrupts

The eleven 8051 core interrupts are shown described in Table 7.15, "8051 Interrupts". See Appendix B, "High-Performance 8051 Extended Interrupt Unit," on page 315 for a desciption of the High Performance 8051 Extended Interrupt Unit.

The fanout of Interrupts and Wakeup Evnets are illustrated in Figure 7.4 and Figure 7.5. The active high Int3 and Int5 outputs from the Extended IRQs shown in Figure 8.4 are inverted into active low 8051 core

inputs Int3_n and Int5_n. The 8051 has the following run time sources: int0, int1, int2, int3 and int4. The Interrupt sources of Int5_n create 8051 Wakeup Events which are used to monitor and altar the power management state. The 8051 core has three interrupt priority levels: PFI, high and low. The PFI interrupt, if enabled, has priority over all other interrupts. See Section 12.3, "Wake-Up Events" for a description of Wake-up Events.

7.9.1 8051 Internal Parallel Interrupts

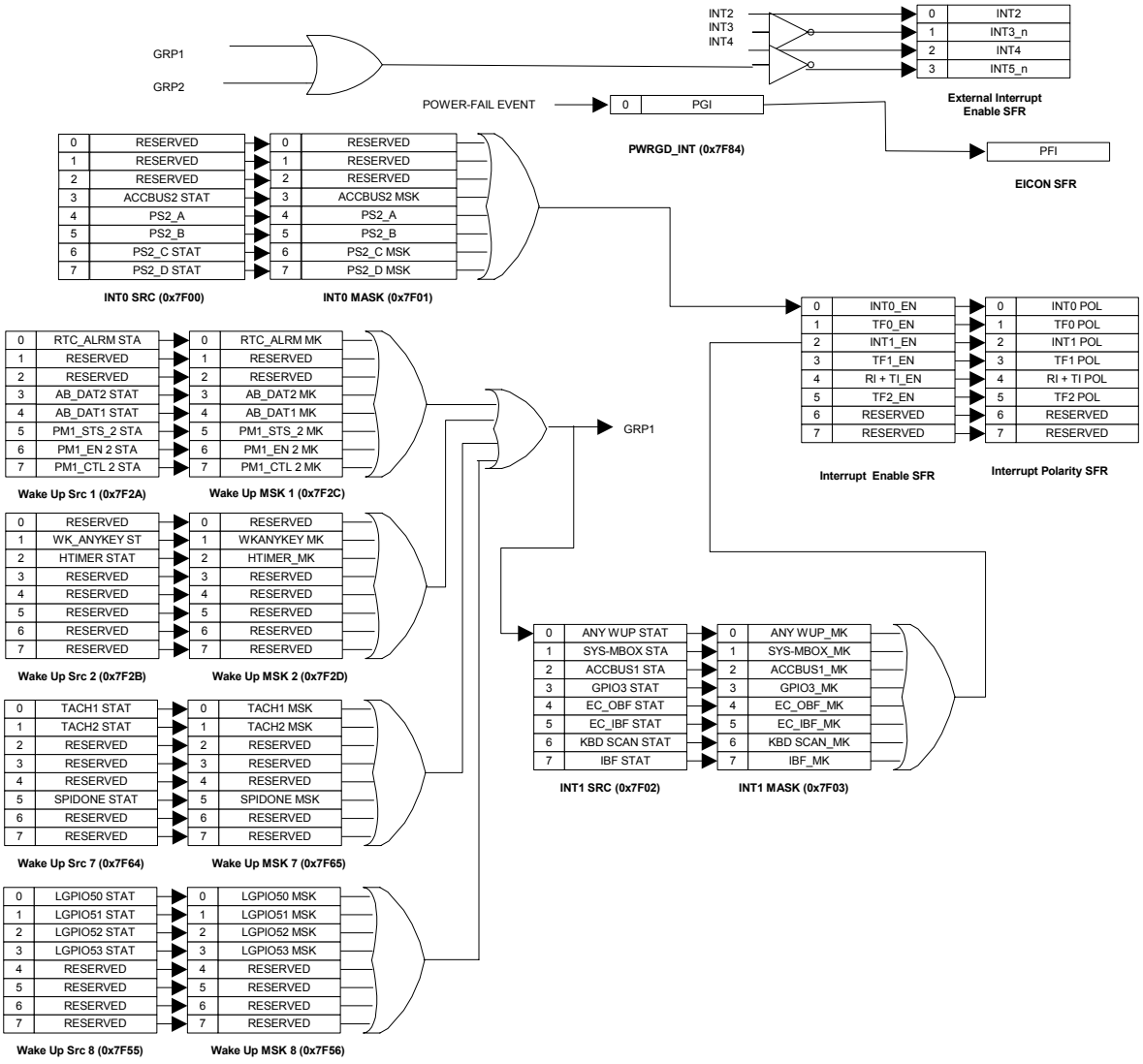


Figure 7.4 8051 Interrupts

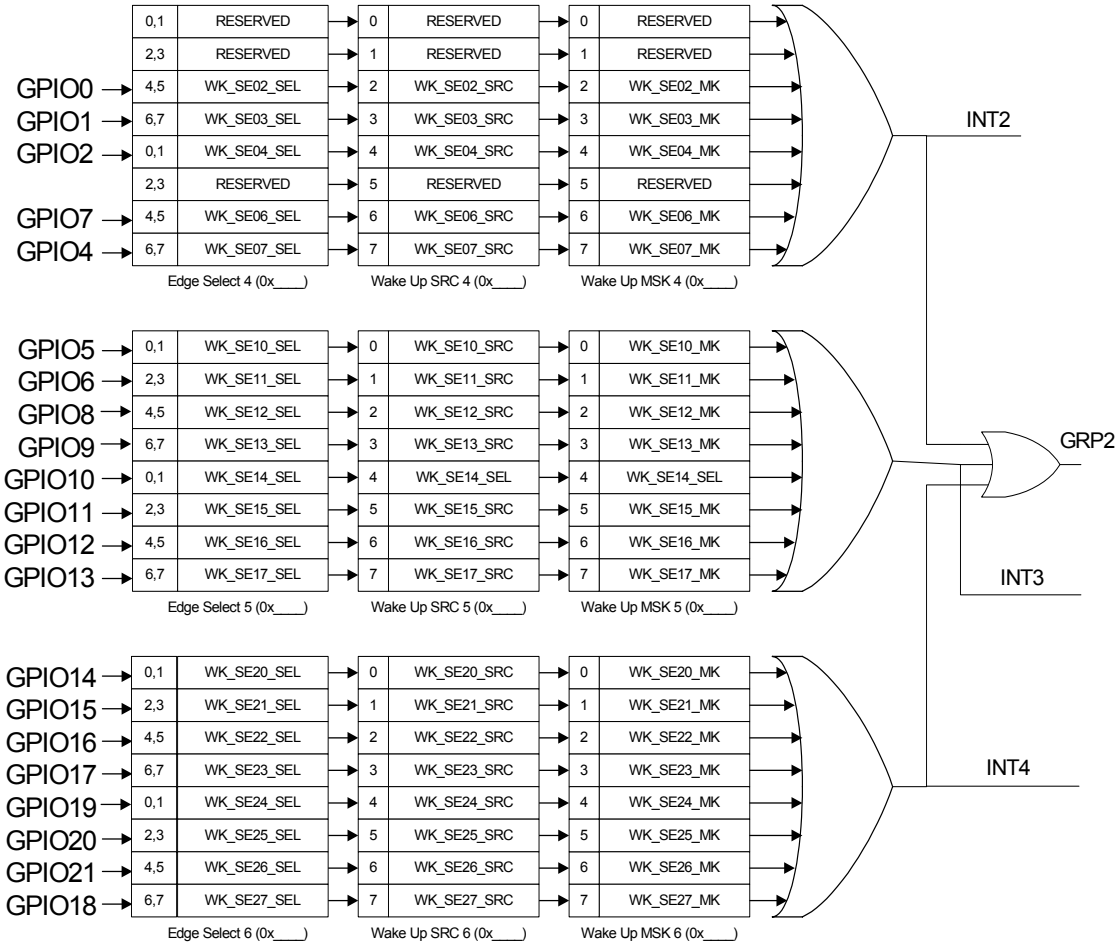


Figure 7.5 Extended Interrupts and Wake Events

Note: Wake events apply per pin and are available to all functions of that pin. For example, if the RXD function is selected as an alternate function of the GPIO8 pin (MISC7 = 1), the WK_SE12 event can be used for IR wake-up. See Section 12.3, "Wake-Up Events".

Table 7.15 8051 Interrupts

INTERRUPT	DESCRIPTION	NATURAL PRIORITY	FLAG	ENABLE	PRIORITY CONTROL	INTERRUPT VECTOR
pfi	Power Fail Interrupt	0	EICON.4	EICON.5	n/a	0x33
int0_n	External Interrupt 0	1	TCON.1	IE.0	IP.0	0x03
TF0	Timer 0 Interrupt	2	TCON.5	IE.1	IP.1	0x0B
int1_n	External Interrupt 1	3	TCON.3	IE.2	IP.2	0x13
TF1	Timer 1 Interrupt	4	TCON.7	IE.3	IP.3	0x1B
TI_0 or RI_0	Serial Port 0 Transmit or Receive	5	SCON0.0 (RI_0), SCON0.1 (RI_0)	IE.4	IP.4	0x23
TF2 or EXF2	Timer 2 Interrupt	6	T2CON.7 (TF2), T2CON.6 (EXF2)	IE.5	IP.5	0x2B
	RESERVED	7	RESERVED	IE.6	IP.6	0x3B

Table 7.15 8051 Interrupts (continued)

INTERRUPT	DESCRIPTION	NATURAL PRIORITY	FLAG	ENABLE	PRIORITY CONTROL	INTERRUPT VECTOR
int2	External Interrupt 2	8	EXIF.4	EIE.0	EIP.0	0x43
int3_n (1)	External Interrupt 3	9	EXIF.5	EIE.1	EIP.1	0x4B
int4	External Interrupt 4	10	EXIF.6	EIE.2	EIP.2	0x53
int5_n	External Interrupt 5	11	EXIF.7	EIE.3	EIP.3	0x5B
	RESERVED	12	EICON.3	EIE.4	EIP.4	0x63

Note 7.24 The int5_n interrupt is used to restart the 8051 from sleep mode. This interrupt includes the interrupt WAKE UP sources from GRP1 and Grp2 on Figure 7.4 and Figure 7.5.

7.9.2 8051 INT0 Source Register

The five interrupts in the INT0 Source register (Table 7.16) are logically OR'ed to drive the 8051 int0_n interrupt (Figure 7.4). When any bit in the INT0 Source register is '1', an interrupt has occurred and, assuming the interrupt is enabled, the 8051 int0_n input is asserted.

The bits in the INT0 Source register are cleared by a writing a "1" to the bit.

Table 7.16 8051 Int0 Source Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F00
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/WC	R/WC	R/WC	R/WC	R/WC	R	R	R
BIT DESCRIPTION	PS2_D	PS2_C	PS2_B	PS2_A	I2C_SM BUS 2	Reserved	Reserved	Reserved

SMSC PS/2 A:D Interrupts – D[7:4]

INT0 Source register bit D7 is the SMSC PS/2 Channel D interrupt, bit D6 is the SMSC PS/2 Channel C interrupt, bit D5 is the SMSC PS/2 Channel B interrupt, and bit D4 is the SMSC PS/2 Channel A interrupt.

The PS2_D interrupt is associated with the PS2CLK and PS2DAT alternate functions of the GPIO20 and GPIO21 pins. The PS2_C is associated with the IMCLK and IMDATA pins. The PS2_B interrupt is associated with the KCLK and KDAT pins. The PS2_A is associated with the EMCLK and EMDATA pins. Note that when a start bit is detected in receive mode for a channel, an interrupt is also generated for that channel.

I^2C/SMBus 2 Interrupt – D3

"1" Indicates an I^2C/SMBus 2 interrupt is active.

7.9.3 8051 INT0 Mask Register

Table 7.17 8051 INT0 Mask Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F01
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R	R	R
BIT DESCRIPTION	PS2_D	PS2_C	PS2_B/	PS2_A	ACCESS BUS 2	Reserved	Reserved	Reserved

7.9.4 8051 INT1 Source Register

The eight interrupts in the INT1 Source register (Table 7.18) are logically 'OR'ed to drive the 8051 external interrupt 1 input, int1_n (Figure 7.4). When any bit in the INT1 Source register is '1', an interrupt has occurred and, assuming the interrupt is enabled, the 8051 int1_n input is asserted.

Bits D0 and D2 – D6 in the INT1 Source register are cleared by a writing a "1" to the bit.

Table 7.18 8051 INT1 Source Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F02
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R/WC	R/WC	R/WC	R/WC	R/WC	R	R/WC
BIT DESCRIPTION	IBF	KBD SCAN	EC_IBF	EC_OBF	GPIO3	I2C_SM BUS 1	SYS-MBOX	ANY WUP

IBF [D7]

IBF interrupt bit D7 is set when the host writes to the KBD Data/Command Write register and is cleared when the 8051 reads from that register.

KBD SCAN [D6]

KBD SCAN interrupt bit D6 is set when any Keyboard Scan In (KSI) pins transition high to low.

EC_IBF [D5]

EC_IBF interrupt bit D5 is set when the host writes to the EC Command or Data port (see "IBF Bit – D1" in Chapter 4).

EC_OBF [D4]

EC_OBF interrupt bit D4 is asserted when the OBF bit in the EC Status register has been cleared (see "OBF Bit – D0" in Chapter 4).

GPIO3 [D3]

GPIO3 interrupt bit D3 is set on either positive or negative-going edge of transition of the GPIO3 pin

I^2C/SMBus 1 [D2]

When I^2C/SMBus 1 bit is equal to 1 an I^2C/SMBus IRQ is active.

SYS-MBOX [D1]

SYS-MBOX interrupt bit D1 is set when the host writes to mailbox register 0. The bit is cleared when mailbox register 0 is read (see Section 17.5, "The System/8051 Interface Registers").

ANY WUP [D0]

The ANYWUP interrupt bit D0 is set when any GRP1 on Figure 7.4 wakeup source is asserted. The bit is cleared bu writting a ‘1’ to this register.

7.9.5 8051 INT1 Mask Register

The eight interrupts in the INT1 Source register (Table 7.18) are enabled by bits of the same name in the INT1 Mask register (Table 7.19).

When any bit in the INT1 Mask register is ‘0’, the interrupt is enabled. When any bit in the INT1 Mask register is ‘1’, the interrupt is masked. When masked interrupts are asserted, the interrupt will be visible in the interrupt source register but will not assert an interrupt to the 8051.

The bits in the INT1 Mask register are read/write. The INT1 interrupts are enabled by default.

Table 7.19 8051 INT1 Mask Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F03
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT DESCRIPTION	IBF	KBD SCAN	EC_IBF	EC_OBF	GPIO3	I2C_SMBUS 1	SYS-MBOX	ANY WUP

7.9.6 8051 Wakeup Source Registers

There are six 8051 Wakeup Source Registers (see Figure 7.4 and Figure 7.5). Each Wakeup Source Register has eight Wakeup Source inputs which are logically 'OR'ed to drive the 8051 external interrupt 1 input (int1_n) and the WAKE interrupt (int5_n). When a Wakeup Source input is asserted '1' in a Wakeup Source Register, an interrupt has occurred and, assuming the interrupt is enabled, the 8051 int1_n and int5_n inputs are asserted. A read from a Wakeup Source Register indicates the status of the Wakeup Source inputs. Generally, the Wakeup Source bits in this register are cleared by a writing a "1" to the bit.

Table 7.20 Wakeup Source Register 1

HOST ADDRESS	N/A
8051 ADDRESS	0x7F2A
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/WC	R/WC	R/WC	R/WC	R/WC	R	R	R/WC
BIT DESCRIPTION	PM1 CTL 2	PM1 EN 2	PM1 STS 2	ACCESS.BUS 1	ACCESS.BUS 2	Reserved	Reserved	RTC_ALRM asserted

Note 7.25 The interrupt source bits in this register are cleared by a writing a "1" to the bit. When asserted, a read from a bit in this register is a logic '1'.

PM1 CTL 2, PM1 EN 2, PM1 STS 2 [D7:D5]

When asserted ‘1’, the corresponding PM1 register has been written (see Section 22.5, "Registers").

ACCESS. BUS 1 [D4]

When asserted ‘1’, a start condition or other event was detected on the I^2C/SMBus 1.

ACCESS. BUS 2 [D3]

When asserted ‘1’, a start condition or other event was detected on the I^2C/SMBus 2.

RTC_ALRM asserted [D0]

The RTC_ALRM Wake-up is an internally generated Low-to-High edge, produced when the RTC time updates to match the Time Of Day (TOD) alarm setting. This edge will set bit D0 of Wake-up Source 1 Register. Bit D0 will remain set and will only be reset on a read of Wake-up Source 1 Register. If the Wake-up source register is read before the clock has updated (i.e., RTC still equals the TOD alarm) bit D0 is reset and stays reset until the next occurrence of a RTC_ALRM Wake-up event.

Table 7.21 Wakeup Source Register 2

HOST ADDRESS	N/A
8051 ADDRESS	0x7F2B
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R/WC	R/WC	R
BIT DESCRIPTION	Reserved	Reserved	Reserved	Reserved	Reserved	HTIMER timeouts	WK_ANYKEY asserted	Reserved

Note 7.26 The interrupt source bits in this register are cleared by a writing a “1” to the bit. When an interrupt source is asserted, a read from the corresponding bit in this register is a logic ‘1’. Reserved bits are logic zero read only.

HTIMER timeouts [D2]

Asserted when HTIMER=1, the hibernation timer counted down to zero.

WK_ANYKEY asserted [D1]

When unmasked, the WK_ANYKEY will wake the 8051 from the “SLEEP” state when any of the Keyboard Scan In (KSI) pins goes low. The Boolean equation below defines the WK_ANYKEY function.

WK_ANYKEY = !(KSI0 & KSI1 & KSI2 & KSI3 & KSI4 & KSI5 & KSI6 & KSI7)

nGPWKUP asserted

Table 7.22 Wakeup Source Register 4

HOST ADDRESS	N/A
8051 ADDRESS	0x7F59
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/WC	R/WC	R	R/WC	R/WC	R/WC	R	R
BIT DESCRIPTION	WK_SE07 asserted	WK_SE06 asserted	Reserved	WK_SE04 asserted	WK_SE03 asserted	WK_SE02 asserted	Reserved	Reserved

Note 7.27 The interrupt source bits in this register are cleared by a writing a “1” to the bit. When an interrupt source is asserted, a read from the corresponding bit in this register is a logic ‘1’.

Table 7.23 Wakeup Source Register 5

HOST ADDRESS	N/A
8051 ADDRESS	0x7F5E
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC
BIT DESCRIPTION	WK_SE17 asserted	WK_SE16 asserted	WK_SE15 asserted	WK_SE14 asserted	WK_SE13 asserted	WK_SE12 asserted	WK_SE11 asserted	WK_SE10 asserted

Note 7.28 The interrupt source bits in this register are cleared by a writing a “1” to the bit. When an interrupt source is asserted, a read from the corresponding bit in this register is a logic ‘1’.

Table 7.24 Wakeup Source Register 6

HOST ADDRESS	N/A
8051 ADDRESS	0x7F63
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC
BIT NAME	WK_SE27 asserted	WK_SE26 asserted	WK_SE25 asserted	WK_SE24 asserted	WK_SE23 asserted	WK_SE22 asserted	WK_SE21 asserted	WK_SE20 asserted

Note 7.29 The interrupt source bits in this register are cleared by a writing a “1” to the bit. When an interrupt source is asserted, a read from the corresponding bit in this register is a logic ‘1’.

Table 7.25 Wakeup Source Register 7

HOST ADDRESS	N/A
8051 ADDRESS	0x7F64
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R/WC	R	R	R	R/WC	R/WC
BIT DESCRIPTION	Reserved		SPIDONE	Reserved			FAN TACH2	FAN TACH1

Note 7.30 The interrupt source bits in this register are cleared by a writing a “1” to the bit. When an interrupt source is asserted, a read from the corresponding bit in this register is a logic ‘1’. Reserved bits are logic zero read only.

Table 7.26 Wakeup Source Register 8

HOST ADDRESS	N/A
8051 ADDRESS	0x7F55
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R/WC	R/WC	R/WC	R/WC
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO53	LGPIO52	LGPIO51	LGPIO50

Note 7.31 The interrupt source bits in this register are cleared by a writing a “1” to the bit. When an interrupt source is asserted, a read from the corresponding bit in this register is a logic ‘1’.

7.9.7 8051 Wakeup Mask Registers

There are six 8051 Wakeup Mask Registers with Mask bits which correspond to the Wakeup Source Registers (see Figure 7.4 and Figure 7.5). When a bit in a Wakeup Mask Register is asserted ‘1’, the corresponding Wakeup Source interrupt is masked. When a bit in a Wakeup Mask Register is deasserted ‘0’, the corresponding Wakeup Source interrupt is enabled. When masked interrupts are asserted, the interrupt can be read in the Wakeup Source Register but will not assert an interrupt to the 8051. The Wakeup Mask Registers are read/write access. All Wakeup interrupts are enabled by default.

Table 7.27 Wakeup Mask Register 1

HOST ADDRESS	N/A
8051 ADDRESS	0x7F2C
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R	R	R/W
BIT DESCRIPTION	PM1 CTL 2	PM1 EN 2	PM1 STS 2	ACCESS. BUS 1	ACCESS. BUS 2	Reserved	Reserved	RTC_A LRM

Note 7.32 When set ‘1’, a bit in this register masks the corresponding bit in Table 7.20, "Wakeup Source Register 1".

Table 7.28 Wakeup Mask Register 2

HOST ADDRESS	N/A
8051 ADDRESS	0x7F2D
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R/W	R/W	R
BIT NAME	Reserved	Reserved	Reserved	Reserved	Reserved	HTIMER timeouts	WK_ANY KEY asserted	Reserved

Note 7.33 When set ‘1’, a bit in this register masks the corresponding bit in Table 7.21, "Wakeup Source Register 2". Reserved bits are logic zero read only.

Table 7.29 Wakeup Mask Register 4

HOST ADDRESS	N/A
8051 ADDRESS	0x7F5A
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R/W	R	R/W	R/W	R/W	R	R
BIT NAME	WK_SE07	WK_SE06	Reserved	WK_SE04	WK_SE03	WK_SE02	Reserved	Reserved

Note 7.34 When set ‘1’, a bit in this register masks the corresponding bit in Table 7.22, "Wakeup Source Register 4".

Table 7.30 Wakeup Mask Register 5

HOST ADDRESS	N/A
8051 ADDRESS	0x7F5F
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	WK_SE 17	WK_SE 16	WK_SE 15	WK_SE 14	WK_SE13	WK_SE 12	WK_SE11	WK_SE 10

Note 7.35 When set ‘1’, a bit in this register masks the corresponding bit Table 7.23, "Wakeup Source Register 5".

Table 7.31 Wakeup Mask Register 6

HOST ADDRESS	N/A
8051 ADDRESS	0x7F66
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC
BIT NAME	WK_SE27	WK_SE 26	WK_SE 25	WK_SE 24	WK_SE 23	WK_SE 22	WK_SE 21	WK_SE 20

When set ‘1’, a bit in this register masks the corresponding bit in Table 7.31, "Wakeup Mask Register 6".

Table 7.32 Wakeup Mask Register 7

HOST ADDRESS	N/A
8051 ADDRESS	0x7F65
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R/W	R	R	R	R/W	R/W
BIT NAME	Reserved		SPIDONE	Reserved			FAN TACH2	FAN TACH1

Note 7.36 When set ‘1’, a bit in this register masks the corresponding bit in Table 7.25, "Wakeup Source Register 7".

Table 7.33 Wakeup Mask Register 8

HOST ADDRESS	N/A
8051 ADDRESS	0x7F56
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO53	LGPIO52	LGPIO51	LGPIO50

Note 7.37 When set ‘1’, a bit in this register masks the corresponding bit in Table 7.26, "Wakeup Source Register 8".

7.9.8 8051 Hibernation Timer Register

Table 7.34 HTIMER Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7FF3
POWER	VCC1
DEFAULT	0x00

Hibernation Timer - This 8 bit binary count-down timer can be programmed from 30 seconds to 128 minutes in 30 second increments. When it expires (reaches “0”), it stops (remains at “0”) and causes a hardware event that will wake up the 8051. This timer is clocked by the 32 KHz clock and is powered by VCC1. Writing a non-zero value to this register starts the counter from that value.

7.9.9 8051 Edge Select Registers

There are six Edge Select Registers. The assertion of the corresponding interrupt is controlled by a two bit field as shown inTable 7.36.

Selectable Edge interrupts

Selectable interrupts SE04, SE06, and SE07 are on External INT2.

Selectable interrupts SE10, SE12, SE13, SE15-SE17 are on External INT3.

Selectable interrupts SE20-SE23, SE25-SE27 are on External INT4.

Table 7.35 Edge Select 4A

HOST ADDRESS	N/A
8051 ADDRESS	0x7F57
POWER	VCC1
DEFAULT	0x00

BIT	**D7:6**	**D5:4**	**D3:2**	**D1:0**
HOST TYPE	-	-	-	-
8051 R/W	R/W	R/W	R	R
BIT NAME	SE03 Select	SE02 Select	Reserved	Reserved

USER’S NOTE: Edge-generated interrupts may occur from a change in the edge select bits.

Table 7.36 Edge Selection

INTERRUPT ASSERTION	D7:6 D5:4 D3:2 D1:0
EDGE HIGH TO LOW	00
EDGE LOW TO HIGH	01
EITHER EDGE	10
RESERVED	11

Table 7.37 Edge Select 4B

HOST ADDRESS	N/A
8051 ADDRESS	0x7F58
POWER	VCC1
DEFAULT	0x00

BIT	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	R/W	R/W	R	R/W
BIT NAME	SE07 Select	SE06 Select	Reserved	SE04 Select

USER'S NOTE: Edge-generated interrupts may occur from a change in the edge select bits.

Refer to Table 7.36, "Edge Selection".

Table 7.38 Edge Select 5A

HOST ADDRESS	N/A
8051 ADDRESS	0x7F5C
POWER	VCC1
DEFAULT	0x00

BIT	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W
BIT NAME	SE13 Select	SE12 Select	SE11 Select	SE10 Select

USER'S NOTE: Edge-generated interrupts may occur from a change in the edge select bits.

Refer to Table 7.36, "Edge Selection".

Table 7.39 Edge Select 5B

HOST ADDRESS	N/A
8051 ADDRESS	0x7F5D
POWER	VCC1
DEFAULT	0x00

BIT	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W
BIT NAME	SE17 Select	SE16 Select	SE15 Select	SE14 Select

USER'S NOTE: Edge-generated interrupts may occur from a change in the edge select bits.

Refer to Table 7.36, "Edge Selection".

Table 7.40 Edge Select 6A

HOST ADDRESS	N/A
8051 ADDRESS	0x7F61
POWER	VCC1
DEFAULT	0x00

BIT	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W
BIT NAME	SE23 Select	SE22 Select	SE21 Select	SE20 Select

USER'S NOTE: Edge-generated interrupts may occur from a change in the edge select bits.

Refer to Table 7.36, "Edge Selection".

Table 7.41 Edge Select 6B

HOST ADDRESS	N/A
8051 ADDRESS	0x7F62
POWER	VCC1
DEFAULT	0x00

BIT	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W
BIT NAME	SE27 Select	SE26 Select	SE25 Select	SE24 Select

USER'S NOTE: Edge-generated interrupts may occur from a change in the edge select bits.

Refer to Table 7.36, "Edge Selection".

7.9.10 Power Fail IRQ

The PWRGD_INT register (Table 7.42) contains the Power Good Interrupt (PGI) bit, D0. When PGI = '1', the (VCC2) PWRGD input has been deasserted; otherwise, PGI = '0'.

Note: PGI is not asserted when PWRGD is asserted.

The PGI bit is the source for the high-performance 8051 Power Fail Interrupt (pfi) input (Figure 7.4). The VCC2 power fail detect function is implemented as described in Section 7.6, "8051 Ring Oscillator Fail-Safe Controls," on page 46.

The PGI bit is readable and is cleared by writing a '1' to D0 in the PWRGD_INT register.

Table 7.42 Power Good Interrupt Register (PWRGD_INT)

HOST ADDRESS	N/A
8051 ADDRESS	0x7F84
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R	R/WC
BIT NAME	Reserved							PGI

7.9.11 8051 External Serial IRQ Generation

The 8051 can assert an interrupt on the serial IRQ stream to support software-generated SCI, SMI, or PME events (Figure 7.6). The 8051 External Serial IRQ interface is controlled by the 8051_SIRQ register (Table 7.43).

Note: The 8051 External Serial IRQ is generated and cleared by software.

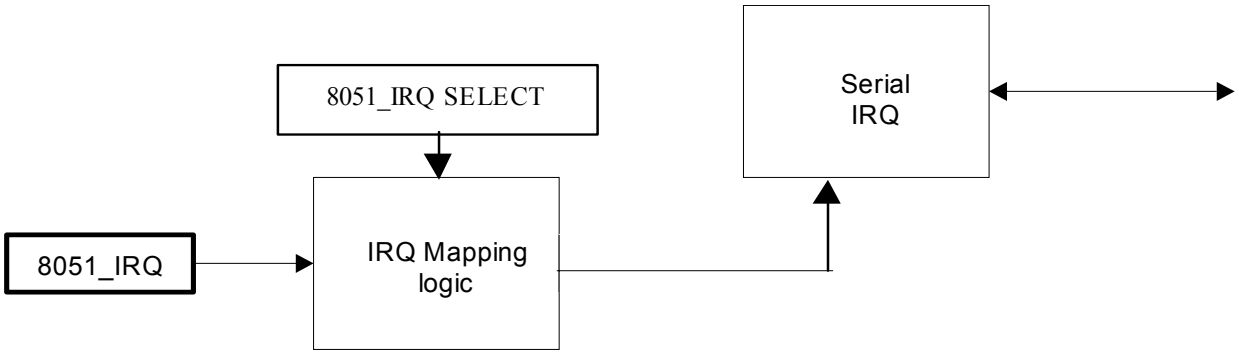


Figure 7.6 8051 External Serial IRQ Block Diagram

Table 7.43 8051_SIRQ Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F52
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
BIT NAME	8051_IRQ SELECT				8051_IRQ ENABLE	8051_IRQ	Reserved	

8051_IRQ SELECT

Four bits that selects which IRQ is utilized when an interrupt occurs. See Table 7.44.

8051_IRQ ENABLE

This bit must be set to one in order for an interrupt to occur.

8051 IRQ

This bit must set to one in order for the 8051 to assert the mapped interrupt request corresponding to the 8051_IRQ SELECT bits. The default state for a disabled IRQ is asserted.

Table 7.44 8051 IRQ Mapping Control Bits

8051_IRQ ENABLE	8051_IRQ SELECT	DESCRIPTION
0	XXXX	DISABLED
1	0000	NO INTERRUPT
	0001	MAP TO IRQ1
	0010	MAP TO IRQ2

Table 7.44 8051 IRQ Mapping Control Bits (continued)

8051_IRQ ENABLE	8051_IRQ SELECT	DESCRIPTION
1	0011	MAP TO IRQ3
	0100	MAP TO IRQ4
	0101	MAP TO IRQ5
	0110	MAP TO IRQ6
	0111	MAP TO IRQ7
	1000	MAP TO IRQ8
	1001	MAP TO IRQ9
	1010	MAP TO IRQ10
	1011	MAP TO IRQ11
	1100	MAP TO IRQ12
	1101	MAP TO IRQ13
	1110	MAP TO IRQ14
	1111	MAP TO IRQ15

7.10 8051 Code Debugging Features

The LPC47N350 8051 code debugging facilities include an external Flash interface, the 8051-controlled UART. Other capabilities include the 8051 single-step capabilities.

7.10.1 External Flash Interface

The LPC47N350 External Flash Interface enables the read-only portion of the internal 8051 program memory bus to access an external ROM device using the KBD Scan interface pins. For a detailed description of the External Flash Interface see Section 7.10.1, "External Flash Interface".

7.10.2 8051 Serial Port

The 8051 serial port can be used during program code development for diagnostic functions. The 8051 serial port pins 8051TX and 8051RX are available on VCC1.

7.10.3 8051 Single-Step Operation

The LPC47N350 8051 interrupt structure provides a method to perform single-step program execution.

When exiting an ISR with an **RETI** instruction, the 8051 will always execute at least one instruction of the task program. Therefore, once an ISR is entered, it cannot be re-entered until at least one program instruction is executed.

To perform a single-step operation, program one of the external interrupts (for example, int_0) to be level sensitive and write an ISR for that interrupt that terminates as shown in Figure 7.7. The CPU enters the ISR when int0_n goes low, then waits for a pulse on int0_n. Each time int0_n is pulsed, the CPU exits the ISR, executes one program instruction, then re-enters the ISR.

```
JNB    TCON.1, $          ; wait for high on int0_n
JB     TCON.1, $          ; wait for low on int0_n
RETI                      ; return for ISR
```

Figure 7.7 8051 Single-Step ISR

Chapter 8 64K Embedded Flash ROM

8.1 Overview

The LPC47N350 includes a 64k embedded Flash ROM (Figure 8.1). The embedded Flash ROM consists of two basic components: a Flash Memory Array and a Command Sequence Interface (CSI). The LPC47N350 Flash ROM stores the 8051-specific embedded keyboard/system controller runtime code.

The memory arrangement of the LPC47N350 64k embedded Flash ROM includes a Main memory block and an Information block. The bottom 2k of the Main Memory block (0x000 – 0x7FF), i.e. the boot block, can be locked by the write-protect pin nFWP.

All read, program and erase operations in the LPC47N350 embedded Flash ROM can be controlled by means of specific command sequences that can be written to the Flash ROM using standard microprocessor write timings.

The LPC47N350 embedded Flash ROM can be directly programmed by the 8051. The Flash ROM can also be programmed independently, i.e. without 8051 intervention, by both the LPC host through the LPC Bus interface and externally using the keyboard scan interface pins.

Note: The Following Specifications Are Preliminary And Subject To Change.

Characteristics of the 64k embedded Flash ROM are summarized in Table 8.1:

Table 8.1 LPC47N350 64K Embedded Flash ROM Feature Summary

FEATURE		DESCRIPTION
PROG/ERASE VOLTAGE		3.3V ± 10% (T_J = 0×C to 125×C)
READ VOLTAGE		
BUS WIDTH		8-bit
ACCESS TIME		45 ns
MEMORY ARRANGEMENT	**MAIN BLOCK**	64k x 8
	INFO. BLOCK	128k x 8
BOOT BLOCK	**SIZE**	2K-Byte, Lockable
	LOCATION	Bottom
ERASE	**TYPES**	Page/Mass (512 bytes/page)
	CYCLING	100,000 Cycles (Commercial Temp).
PROGRAMMING		Per Byte
INTERFACE		All Program and Erase Operations are Enabled via a Command Sequence Interface using Standard Microprocessor Write Timings.

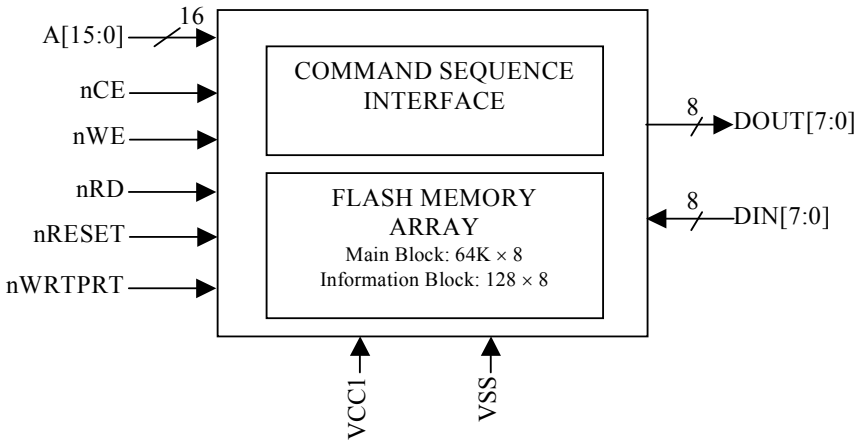


Figure 8.1 Embedded Flash ROM Block Diagram

8.2 Flash Memory Array

The Flash Memory Array (Figure 8.1) is a CMOS page-erasable, mass-erasable, byte-programmable embedded flash memory that is partitioned into two memory blocks. The main memory block is organized as 65,536 8-bit words. The information block is organized as 128 8-bit words.

An erase operation in the 64k Embedded Flash sets the affected memory array bits to one, while program operations write zeros. To reprogram any '0' bit in a page to '1', the page must be erased.

A page (512 bytes) is composed of eight adjacent rows for the main memory block and two adjacent rows for the information block. The page erase operation erases all bytes within a page.

To modify the contents of the 64k Embedded Flash, VCC2 must be > 3v for at least 250µs before program or erase operations may begin.

The Flash Memory Array erases and programs with a 3.3V-only power supply; i.e. LPC47N350 does not require an external VPP supply. A summary of the LPC47N350 Flash Memory Array features is shown below in Figure 8.2.

Table 8.2 Flash Memory Array Features

FEATURE		DESCRIPTION
PROG/ERASE VOLTAGE		3.3V ± 10% (T_J = 0C to 125C)
READ VOLTAGE		
MEMORY	**MAIN**	64k × 8
	INFO.	128 × 8
BUS-WIDTH		8-bit
ACCESS TIME		45ns (max)
ERASE	**TYPES**	Page, Mass
	CYCLING	100,000 Cycles (typ)

Table 8.2 Flash Memory Array Features (continued)

FEATURE	DESCRIPTION
DATA RETENTION	100 years
BYTE PROGRAM TIME	20μs (min)
PAGE ERASE TIME	10ms (min)
MASS ERASE TIME	10ms (min)

8.3 Command Sequence Interface (CSI)

8.3.1 Overview

The Command Sequence Interface handles all of the Flash-related operations; including, address mapping for the Flash Memory Array, command code decoding, power management, and programming.

The CSI includes host/flash interface logic, address and data latches for argument retention, a command register and a status register (Figure 8.2). These functions are described in the sub-sections that follow.

The CSI host interface logic is driven by the command register (see Section 8.3.4, "Command Register" below). The CSI host interface behavior is summarized in Figure 8.3.

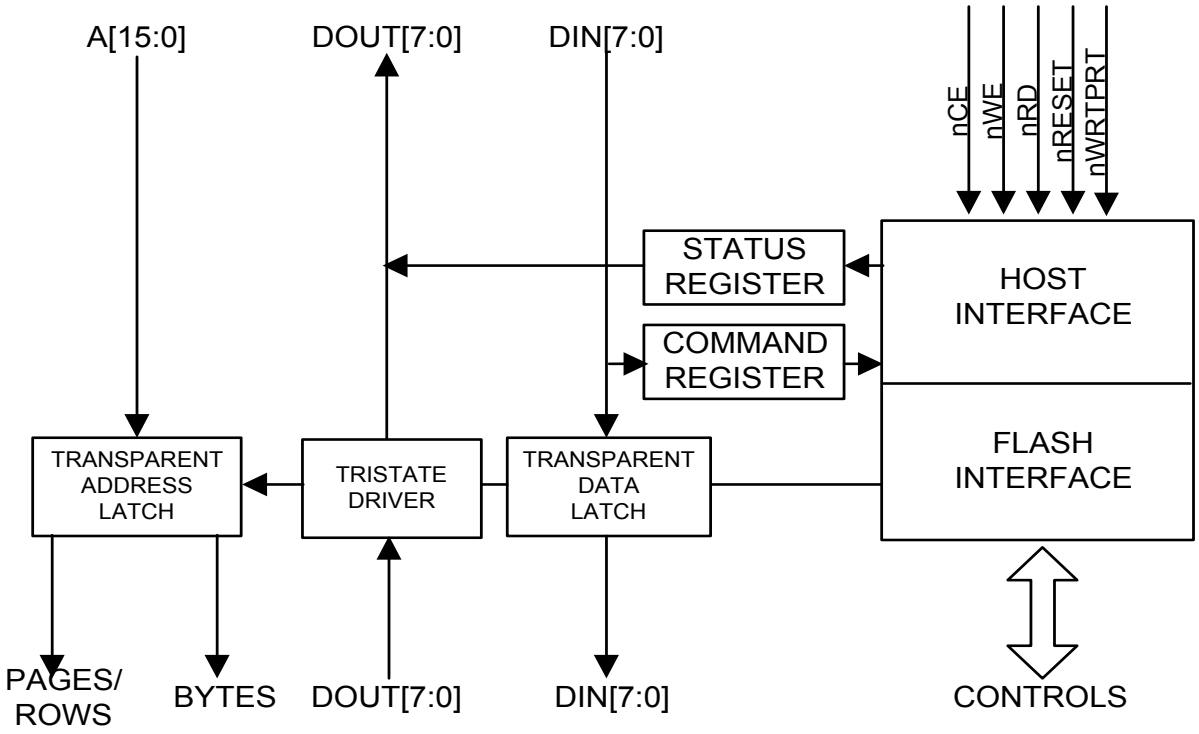


Figure 8.2 CSI Block Diagram

8.3.2 Address Mapping

The 64k Embedded Flash ROM address inputs A[15:0] access the pages, rows and bytes of the Flash Memory Array Main Memory and Information blocks. The relationship between the 64k Embedded Flash

ROM address bus and the Flash Memory Array Main Memory addressing is shown below in Table 8.3. The relationship between the 64k Embedded Flash ROM address bus and the Flash Memory Array Information block addressing is shown below in Table 8.4. The upper seven host address bits A15 – A9 determine the Flash page, the next three lower address bits A8 – A6 determine the row and the least significant six bits determine the byte.

Table 8.3 Main Memory- 64K Embedded Flash Address Mapping

FLASH ADDRESS															
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
PAGES							ROWS			BYTES					

Table 8.4 Information Block - 64K Embedded Flash Address Mapping

FLASH ADDRESS															
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	X	X	X	X	X	X	ROWS	BYTES					

8.3.3 Reset

The embedded flash block is reset when the CSI nRESET input is asserted (Figure 8.1). The CSI nRESET input is asserted during VCC1 POR, when the nEA pin is asserted '0', when the 8051 is idle or sleeping during 8051 code fetch access mode (Table 2.1), and when the RESET FLASH bit D7 in the Flash Program register is asserted '1' (see Section 9.10, "Flash Program Register," on page 122).

Reset forces the flash interface to the STANDBY state. STANDBY represents the lowest power consumption state for the Embedded Flash ROM. In the STANDBY state, the Flash Memory Array is disabled, the CSI state machine is stopped, and the microprocessor interface is disabled.

When the nRESET input is deasserted, the CSI switches the Flash ROM interface from STANDBY to READ ARRAY mode (see Section 8.3.7.2, "Read Array Mode").

The nRESET input is also asserted and deasserted when the PGM pin is deasserted to restore READ ARRAY mode following ATE Program Access cycles (see Section 9.6.3, "PGM Pin," on page 114).

APPLICATION NOTE: An effort should be made to prevent software from asserting the nRESET input while the BUSY bit is asserted to avoid programming errors or incomplete erase cycles (see Section 8.3.6, "Status Register," on page 93).

8.3.4 Command Register

The Embedded Flash Block command register is used to alter the state of the CSI Host Interface (Figure 8.2). The command register is write-only and set to FFh by default (Table 8.5).

The command register does not occupy an addressable memory location but is programmed using standard microprocessor write timings when the CSI nWE and nCE inputs are asserted.

Descriptions of the CSI command codes are shown below in Table 8.6. The command register is always write-accessible except when executing CSI argument bus cycles (see Section 8.3.5, "CSI Command Types", below) and when the BUSY bit is asserted.

Table 8.5 LPC47N350 Embedded Flash Command Register

ADDRESS	N/A
POWER	VCC1
DEFAULT	0xFF (VCC1 POR)

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	W	W	W	W	W	W	W	W
BIT NAME	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

Table 8.6 CSI Command Codes

CMD CODE (HEX)	CSI MODE	DESCRIPTION (Note 8.1)
FF	READ ARRAY	The READ ARRAY command places the CSI in READ ARRAY mode. In READ ARRAY mode, memory data is output on the DOUT data pins. READ ARRAY mode is the default following reset. NOTE: the READ ARRAY command does not return Flash data; to read from the Flash array following a READ ARRAY command, a read operation must be performed.
80	PROGRAM BYTE	The PROGRAM BYTE command prepares the CSI to accept the program address and program data in a second (argument) bus write cycle. Once the second bus cycle has completed, programming begins and the CSI host interface is placed into the READ STATUS mode. The boot block cannot be programmed using the PROGRAM BYTE command when the CSI nWRTPRT input is asserted (see Section 8.4, "Flash Write Protect").
40	ERASE PAGE	The ERASE PAGE command prepares the CSI to accept the page address in a second (argument) bus write cycle. Once the second bus cycle has completed, page erasing begins and the CSI host interface is placed into the READ STATUS mode. The boot block cannot be erased using the PAGE ERASE command when the CSI nWRTPRT input is asserted (see Section 8.4, "Flash Write Protect," on page 102).
20	MASS ERASE	The MASS ERASE command places the CSI in the MASS ERASE mode so that Flash Main Memory Block data and/or the Info Block data will be erased. If the Info block is selected (using the SET INFO BLOCK ACCESS command), both the Info Block and the Main Block will be erased by a MASS ERASE command. If the Main Block is selected (using the SET MAIN BLOCK ACCESS command), only the Main Block will be erased by a MASS ERASE command. Once the MASS ERASE command is given, erasing begins and the CSI host interface is placed into the READ STATUS mode. MASS ERASE is disabled if the Flash Boot Block is locked.
10	READ STATUS	The READ STATUS command prepares the CSI to output the status register in all subsequent read cycles, independent of the presented address. Once the READ STATUS command code has been written, the CSI is idle until the next valid command. The CSI automatically enters the READ STATUS mode following all valid and invalid commands except the READ ARRAY command. NOTE: the READ STATUS command does not return CSI data; to read the CSI Status register following a READ STATUS command, a read operation must be performed.

Table 8.6 CSI Command Codes (continued)

CMD CODE (HEX)	CSI MODE	DESCRIPTION (Note 8.1)
A0	CLEAR STATUS	The CLEAR STATUS command resets the error bits in the CSI Status register. Once the CLEAR STATUS command has completed, the CSI is idle and in the Read Status mode until the next valid command. NOTE: asserted CSI Status register error bits must be deasserted using the CLEAR STATUS command before executing subsequent CSI commands (see Section 8.3.6, "Status Register").
B0	SET MAIN BLOCK ACCESS	The SET MAIN BLOCK ACCESS command selects the 64k-byte Main Memory Block. Once the SET MAIN BLOCK ACCESS command has completed, the CSI is idle and in the Read Status mode until the next valid command. All subsequent commands apply to the Main Block until the SET INFO BLOCK ACCESS command is specified.
C0	SET INFO BLOCK ACCESS	The SET INFO BLOCK ACCESS command selects the 128-byte Information Memory Block. Once the SET INFO BLOCK ACCESS command has completed, the CSI is idle and in the Read Status mode until the next valid command. All subsequent commands apply to the Information Block until the SET MAIN BLOCK ACCESS command is specified.

Note 8.1 All command codes not shown in this table are RESERVED by SMSC and cannot be used. RESERVED command codes generate CSI command errors (see Section 8.3.6.2, "CMD Error Bit – D6").

8.3.5 CSI Command Types

There are two types of CSI commands: commands that require a single bus cycle (Type 1) and commands that require two bus cycles (Type 2).

Type 1 commands are executed as soon as the CSI command code is written to the command register. Type 1 commands include READ ARRAY, MASS ERASE, CLEAR STATUS, READ STATUS, SET MAIN BLOCK ACCESS and SET INFO BLOCK ACCESS.

Type 2 commands require an argument bus cycle following the command code bus cycle. Type 2 commands include PROGRAM BYTE, and ERASE PAGE. The required address and data arguments for Type 2 commands depends upon the command code.

Setup errors occur if PROGRAM BYTE and ERASE PAGE commands are not followed by a write cycle for address and/or data arguments.

The contents of the address bus are ignored during the command code bus cycle for both Type 1 and Type 2 commands.

A summary of the CSI command types and bus cycles is shown below in Table 8.7.

Table 8.7 CSI Command Types and Bus Cycles

COMMAND	TYPE	COMMAND CODE CYCLE			ARGUMENT CYCLE			NOTES
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA	
READ ARRAY	1	WRITE	X	FFH	-	-	-	Note 8.7
PROGRAM BYTE	2			80H	WRITE	PRA	PRD	Note 8.2, Note 8.3, Note 8.6, Note 8.7

Table 8.7 CSI Command Types and Bus Cycles (continued)

COMMAND	TYPE	COMMAND CODE CYCLE			ARGUMENT CYCLE			NOTES
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA	
ERASE PAGE	2	WRITE	X	40H	WRITE	PGA	X	Note 8.4, Note 8.6, Note 8.7
MASS ERASE	1			20H	-	-	-	Note 8.6, Note 8.7
READ STATUS	1			10H	-	-	-	Note 8.6, Note 8.7
CLEAR STATUS	1			A0H	-	-	-	Note 8.6, Note 8.7
SET MAIN BLOCK ACCESS	1			B0H	-	-	-	Note 8.6, Note 8.7
SET INFO BLOCK ACCESS	1			C0H	-	-	-	Note 8.6, Note 8.7

Note 8.2 PRA = Program Address

Note 8.3 PRD = Program Data

Note 8.4 PGA = Page Address

Note 8.5 SRD = Status Register Data

Note 8.6 The CSI is IDLE following this command

Note 8.7 X = Don't Care

8.3.6 Status Register

The CSI status register displays the working state of Command Sequence Interface hardware (Figure 8.2). The status register is read-only and is set to '00000X00'b by default (Table 8.8). Note that status register bit D2 always reflects the state of the CSI nWRTPRT input (see Section 8.3.6.6, "Lock Bit – D2" below).

The CSI Status register is cleared by the CLEAR STATUS command, VCC1 POR and nRESET.

APPLICATION NOTE: Asserted CSI status register error bits must be deasserted using the CLEAR STATUS command before executing subsequent CSI commands.

Table 8.8 CSI Status Register

ADDRESS	N/A
POWER	VCC1
DEFAULT	‘00000X00’b (VCC1 POR)

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R	R	R	R	R	R	R	R
BIT NAME	BUSY	CMD ERROR	PROTECT ERROR	SETUP ERROR	INFO	LOCK	Reserved	

8.3.6.1 Busy Bit – D7

The BUSY indicates the state of the PROGRAM BYTE, MASS ERASE, and PAGE ERASE operations. When the BUSY bit is ‘1’, either a PROGRAM BYTE, MASS ERASE or PAGE ERASE operation is in progress. When the BUSY bit is ‘1’, writes to the CSI will assert the status register CMD Error bit (see Section 8.3.6.2, "CMD Error Bit – D6" below). When the BUSY bit is ‘0’, program or erase operations have completed and the CSI is ready to accept a command. The BUSY bit is cleared by VCC1 POR.

During Byte Programming, Page Erase and Mass Erase cycles, the BUSY bit is asserted at the end of the argument bus cycle and deasserted at the falling edge of NVSTR plus Trcv (see Figure 8.5 and Table 8.10 in Section 8.3.7.3, "Program Byte Mode", Figure 8.6 and Table 8.11 in Section 8.3.7.4, "Page Erase Mode" and Figure 8.7 and Table 8.12 in Section 8.3.7.5, "Mass Erase Mode").

The BUSY bit is not asserted during READ ARRAY, READ STATUS, CLEAR STATUS, SET MAIN BLOCK ACCESS and SET INFO BLOCK ACCESS operations. The BUSY bit is not affected by the CLEAR STATUS command. The BUSY bit is cleared by VCC1 POR and nRESET.

8.3.6.2 CMD Error Bit – D6

The CMD ERROR identifies that either a valid command code or a RESERVED CSI command code has been received or a write to the CSI has been attempted while the BUSY bit is asserted. When the CMD ERROR bit is deasserted ‘0’, a valid command code has been written to the CSI command register. Valid CSI command codes are shown in Table 8.6. When the CMD ERROR bit is asserted ‘1’, a RESERVED command code has been written to the CSI command register or a write to the CSI has been attempted while the BUSY bit is asserted (see Section 8.3.7.10, "CSI Host Interface Error Handling").

The CMD ERROR bit is deasserted by the CLEAR STATUS command, VCC1 POR, and nRESET.

8.3.6.3 Protect Error Bit – D5

The PROTECT ERROR identifies byte programming and erase operations on write-protected memory (see Section 8.4, "Flash Write Protect"). When the PROTECT ERROR bit is deasserted ‘0’, assuming the bit was cleared initially, a byte programming or erase operation has been requested for non-write-protected memory. When the PROTECT ERROR bit is asserted ‘1’, a byte programming or erase operation has been requested for write-protected memory (see Section 8.3.7.10, "CSI Host Interface Error Handling").

The PROTECT ERROR bit is deasserted by the CLEAR STATUS command, VCC1 POR and nRESET.

8.3.6.4 Setup Error Bit – D4

The SETUP ERROR identifies byte programming and page erase setup errors. Setup errors specifically apply to Type 2 CSI commands (see Section 8.3.5, "CSI Command Types"). When the SETUP ERROR bit is deasserted '0', assuming the bit was cleared initially, the argument cycle for a Type 2 command has been completed successfully. When the SETUP ERROR bit is asserted '1', a Type 2 PROGRAM BYTE or ERASE PAGE command code cycle has been followed by a read bus cycle instead of a write (argument) cycle. (see Section 8.3.7.10, "CSI Host Interface Error Handling").

8.3.6.5 Info Bit – D3

The INFO identifies whether the Main Memory or Information Memory is selected in the Flash Memory Array (see the SET MAIN BLOCK ACCESS and SET INFO BLOCK ACCESS CSI command codes in Table 8.6 and Section 8.3.7, "CSI State Sequencing").

When Information Memory is selected, the CSI status register INFO bit is asserted '1'. When Main Memory is selected, the CSI status register INFO bit is deasserted '0'. The Main Memory is selected by default following VCC1 POR and nRESET.

The INFO bit is not affected by the CLEAR STATUS command.

8.3.6.6 Lock Bit – D2

The LOCK bit D2 in the CSI status register is the inverse of the nWRTPRT input (see Section 8.4, "Flash Write Protect"). When the nWRTPRT input is '1', i.e. the boot block is not write-protected (unlocked), the CSI status register LOCK bit is '0'. When the nWRTPRT input is '0', i.e. the boot block is write-protected (locked), the CSI status register LOCK bit is '1'. The LOCK bit is not affected by the CLEAR STATUS command and is not affected by VCC1 POR or nRESET; i.e., there is no LOCK bit default.

8.3.7 CSI State Sequencing

8.3.7.1 Overview

CSI state sequencing implies two independent and concurrent processes: the host interface function and the flash interface function (Figure 8.2). The CSI host interface function is illustrated in Figure 8.3. The host interface handles user commands for the flash interface so that, for example, a MASS ERASE operation can be executed by the flash interface while the host interface transitions to a state that allows to the initiator to measure the operation progress.

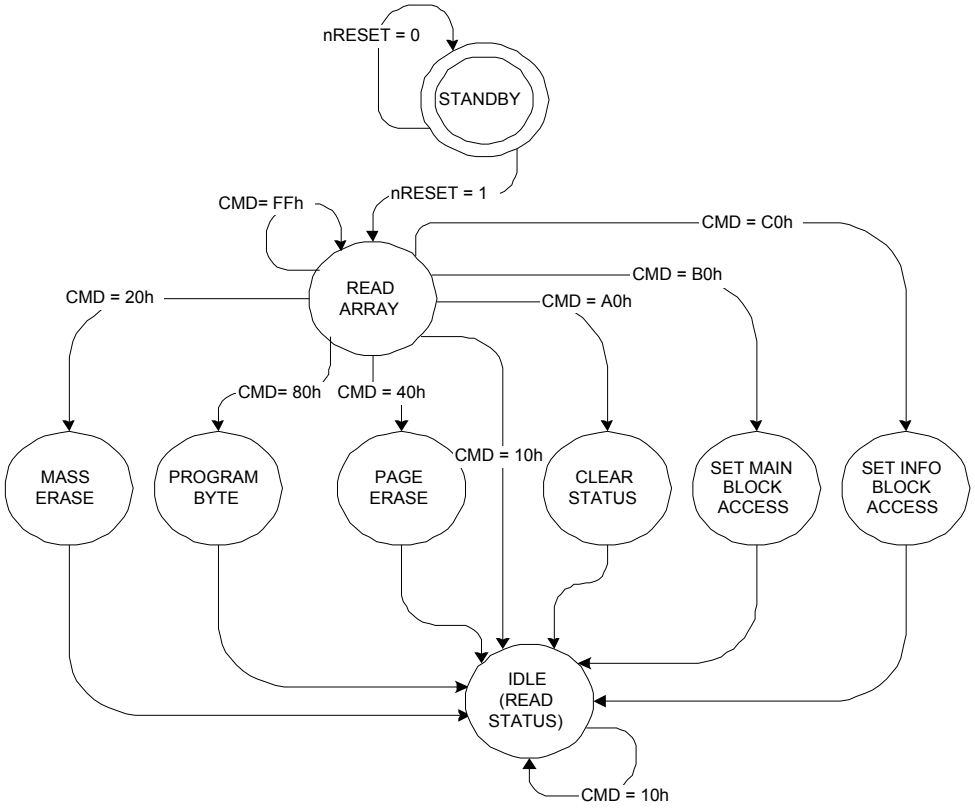


Figure 8.3 CSI Host Interface State Diagram

8.3.7.2 Read Array Mode

READ ARRAY mode is a pass-through mode for the CSI hardware: the address bus A[15:0] is directly connected to the memory array address inputs and the memory array data bus is directly connected to the DOUT[7:0] data bus (Figure 8.1). In READ ARRAY mode (Figure 8.4), the DOUT pins always contain the valid contents of the selected flash memory **45** ns max after the address bus has stabilized. READ ARRAY mode is the default for the LPC47N350 embedded flash following a CSI reset (Figure 8.3). READ ARRAY mode is used during 8051 execution.

The CSI remains in READ ARRAY mode indefinitely until nRESET is asserted or a command is given to explicitly change modes. The Flash Memory Array signals XE, YE, and SE behave as shown in Figure 8.4 for READ cycles. The Flash Memory Array signals PROG, ERASE, MAS1 and NVSTR are always ‘0’ for READ cycles. The Flash Memory Array signal OE may be driven by an inverted version of the host read signal.

In READ ARRAY mode, write cycles to the 64k Embedded Flash Host Interface program the CSI command register.

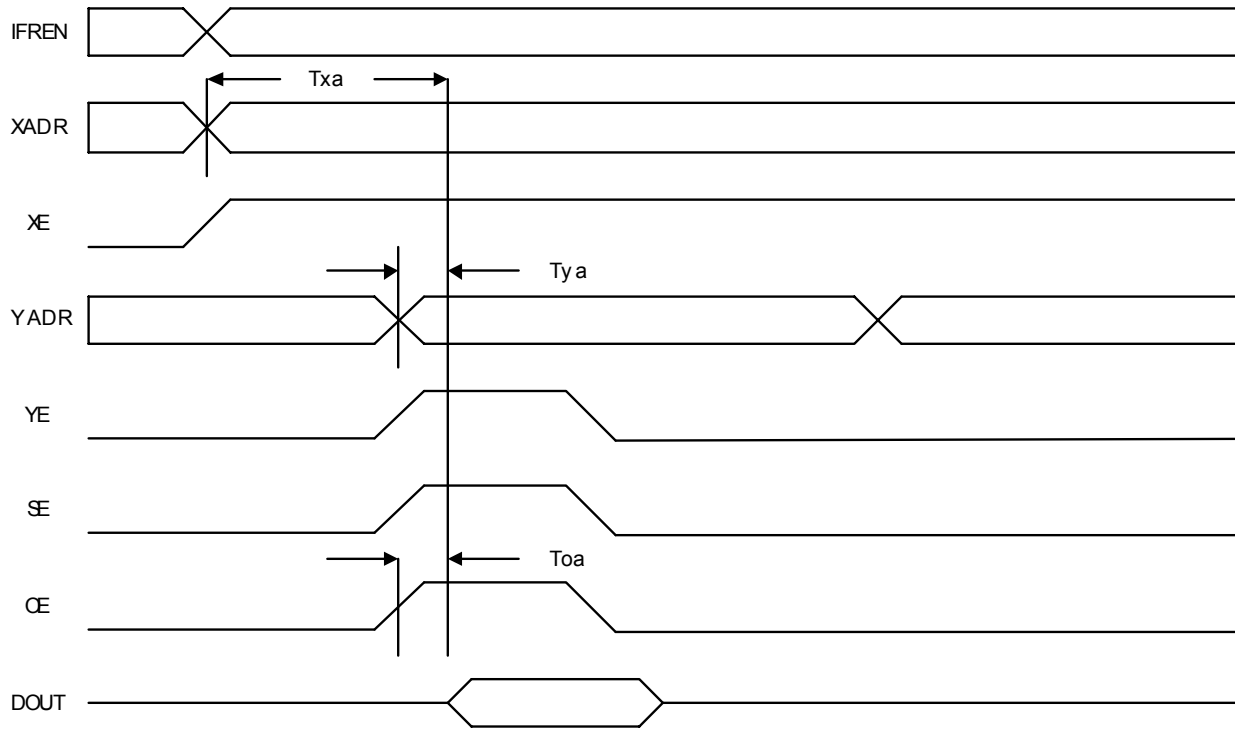


Figure 8.4 Flash Core Read Array Timing Diagram

Table 8.9 Flash Core Read Array Timing Values

	NAME	MAX (NS)	COMMENT
1	Txa	45	X address access time
2	Toa	4	OE access time
3	Tya	45	Y address access time

8.3.7.3 Program Byte Mode

In Program Byte mode, the CSI host interface uses the transparent address and data latches to maintain the byte programming arguments from the second host bus write cycle. The CSI flash interface then cycles the appropriate programming controls to write the flash with the new data (Figure 8.5).

The Flash Memory Array signals XE, and YE behave as shown in Figure 8.5 for Program Byte cycles; the SE signal is always “0”. The CSI status register BUSY bit is asserted as described in Section 8.3.6.1, "Busy Bit – D7," on page 94.

At the end of a Program Byte operation, the host interface and the flash interface idle until the next command is given.

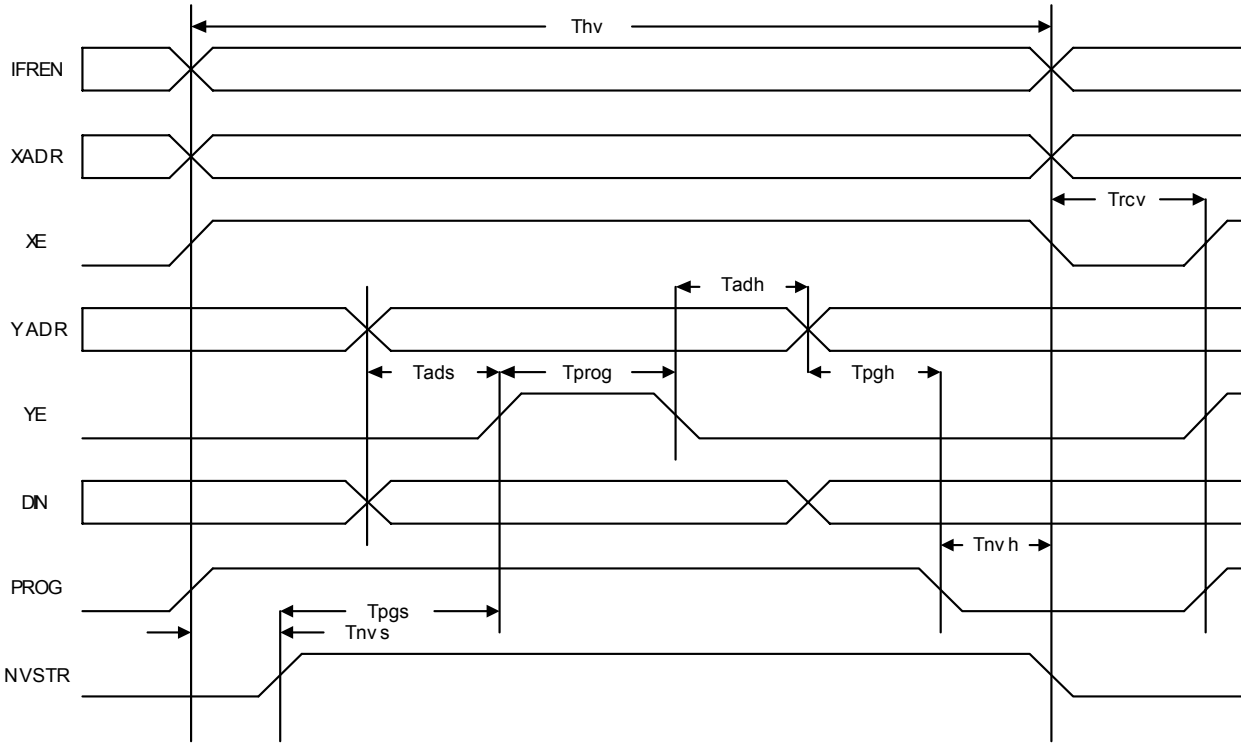


Figure 8.5 Flash Core Program Timing Diagram

Table 8.10 Flash Core Program Timing Values

NAME	MIN	MAX	UNITS	COMMENT
Tnvs	5		µs	PROG/ERASE to NVSTR set up time
Tnvh	5			NVSTR hold time
Tpgs	10			NVSTR to program set up time
Tpgh	20			program hold time
Tprog	20	40		program time
Tads			ns	address/data set up time
Tadh				address/data hold time
Trcv	1		µs	recovery time
Thv		25	ms	cumulative HV period

8.3.7.4 Page Erase Mode

In Page Erase mode, the CSI host interface uses the transparent address latch to maintain the page address argument from the second host bus write cycle. The CSI flash interface then cycles the appropriate controls to erase the page (Figure 8.6). The Flash Memory Array signals YE, SE, OE, MAS1 are always '0' for Page Erase cycles; the XE signal behaves as shown in Figure 8.6. The CSI status register BUSY bit is asserted as described in Section 8.3.6.1, "Busy Bit – D7," on page 94. At the end of a Page Erase operation, the host interface and the flash interface idle until the next command is given.

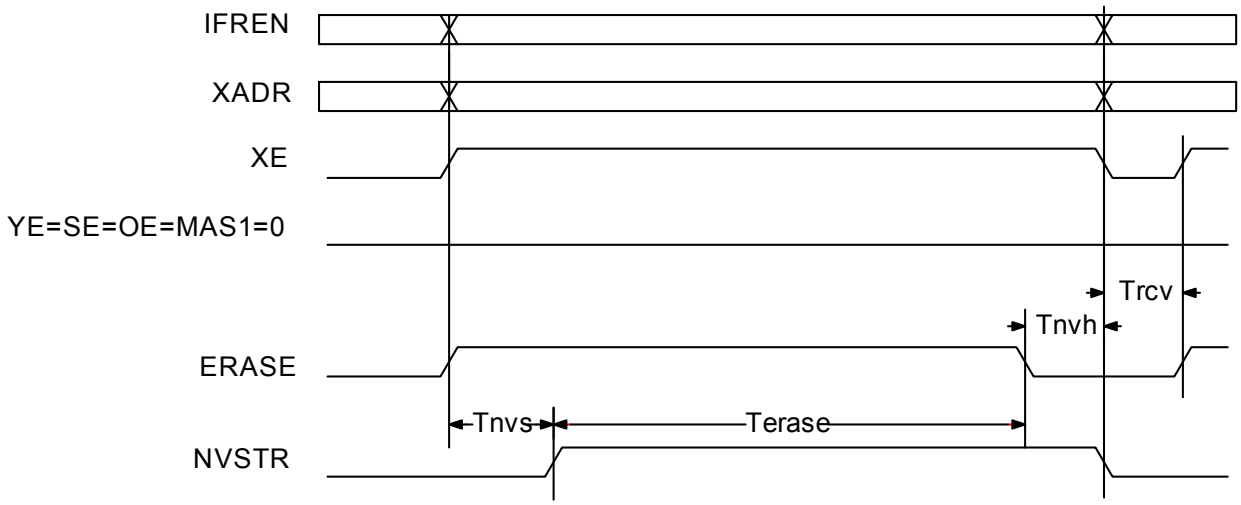


Figure 8.6 Flash Core Page Erase Timing Diagram

Table 8.11 Flash Core Page Erase Timing Values

NAME	MIN	MAX	UNITS	COMMENT
Tnvs	5		µs	PROG/ERASE to NVSTR set up time
Terase	2	4	ms	Erase time
Tnvh	5		µs	NVSTR hold time
Trcv	1			Recovery time

8.3.7.5 Mass Erase Mode

The Mass Erase mode uses the CSI flash interface to cycle the appropriate controls to mass erase the Flash Memory Array (Figure 8.7). The Flash Memory Array signals YE, SE, OE, are always '0' for Mass Erase cycles; the XE signal behaves as shown in Figure 8.7. The CSI status register BUSY bit is asserted as described in Section 8.3.6.1, "Busy Bit – D7," on page 94. At the end of a Mass Erase operation, the host interface and the flash interface idle until the next command is given.

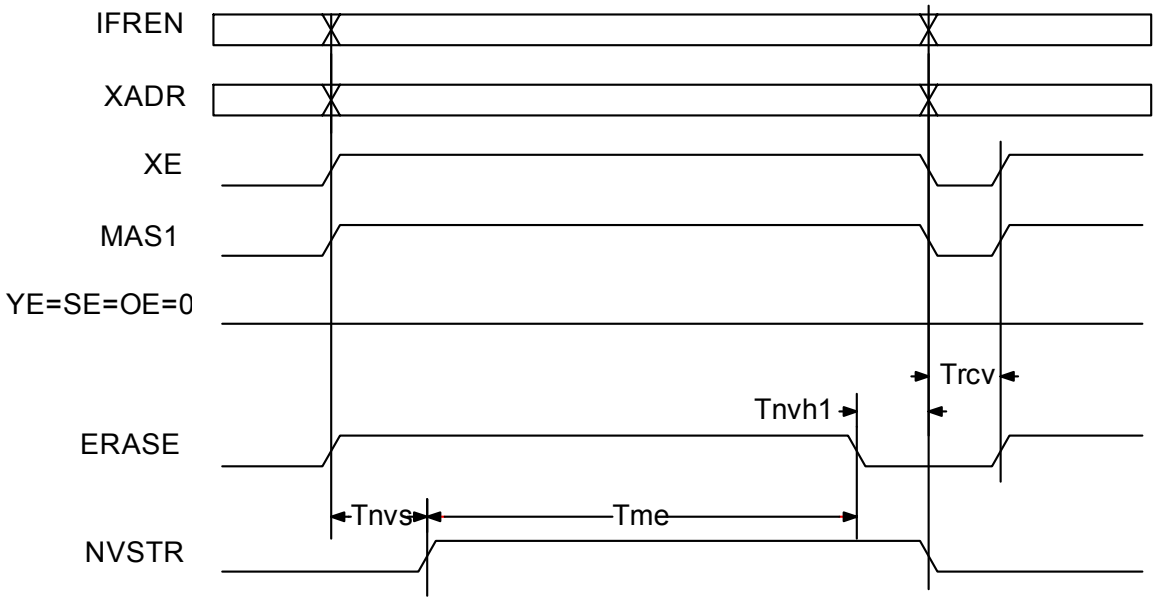


Figure 8.7 Flash Core Mass Erase Timing Diagram

Table 8.12 Flash Core Mass Erase Timing Values

NAME	MIN	MAX	UNITS	COMMENT
Tnvs	5		µs	PROG/ERASE to NVSTR set up time
Tnvh1	100			NVSTR hold time
Trcv	1			Recovery time
Tme	2	4	ms	Mass erase time

8.3.7.6 Read Status (Idle) Mode

The Read Status Mode uses the CSI host interface to disconnect the flash memory array from the DOUT bus and makes the CSI status register available for subsequent host read cycles (Figure 8.3). Assuming all program operations are complete, the CSI flash interface sets the Flash Memory Array interface signals to the standby mode for the duration of the Read Status mode. The CSI host interface and the Flash Memory Array remain in the Read Status (Idle) mode indefinitely until the next command is given. In Read Status mode, write cycles to the 64k Embedded Flash Host Interface program the CSI command register (not shown in Figure 8.3).

8.3.7.7 Clear Status Mode

The Clear Status Mode uses the CSI host interface to disconnect the flash memory array from the DOUT bus, deasserts the status register error bits (Table 8.8), and makes the CSI status register available for subsequent host read cycles (Figure 8.3). The CSI flash interface sets the Flash Memory Array signals to the standby mode for the duration of the Clear Status mode. The CSI host interface and the Flash Memory Array interface remain in the Read Status (Idle) mode until the next command is given.

8.3.7.8 Set Main Block Access Mode

The Set Main Block Access mode uses the CSI host interface to disconnect the flash memory array from the DOUT bus, selects the Main Memory block in the Flash Memory Array, resets the INFO bit in the CSI status register to '0' (see Section 8.3.6.5, "Info Bit – D3"), and makes the CSI status register available for subsequent host read cycles (Figure 8.3).

The CSI flash interface sets the Flash Memory Array interface signals to the standby mode for the duration of the Set Main Block Access mode.

The CSI host interface and the Flash Memory Array interface remain in the Read Status (Idle) mode until the next command is given.

8.3.7.9 Set Info Block Access Mode

The Set Info Block Access mode uses the CSI host interface to disconnect the flash memory array from the DOUT bus, selects the Information Memory block in the Flash Memory Array, sets the INFO bit in the CSI status register to '1' (see Section 8.3.6.5, "Info Bit – D3"), and makes the CSI status register available for subsequent host read cycles (Figure 8.3).

The CSI flash interface sets the Flash Memory Array interface signals to the standby mode for the duration of the Set Info Block Access mode.

The CSI host interface and the Flash Memory Array interface remain in the Read Status (Idle) mode until the next command is given.

8.3.7.10 CSI Host Interface Error Handling

Command Errors

When a write to the CSI command register has been attempted while the BUSY bit is asserted, the write data is rejected (i.e. the data in the command register is not overwritten), the state machine asserts the CMD ERROR bit in the CSI status register, and the command in progress continues to completion.

When a RESERVED command code is written to the CSI command register when the BUSY bit is deasserted, the data in the command register is ignored, the state machine asserts the CMD ERROR bit in the CSI status register, and the CSI host interface transitions to the IDLE state (not shown in Figure 8.3).

For information regarding RESERVED command codes see Note 8.1 in Table 8.6 and Section 8.3.6.2, "CMD Error Bit – D6". For information regarding the BUSY bit see Section 8.3.6.1, "Busy Bit – D7".

Write Protect Errors

When a byte programming or erase operation has been requested for write-protected memory, the command is rejected, the state machine asserts the PROTECT ERROR bit in the CSI status register and transitions to the IDLE state (not shown in Figure 8.3).

For information regarding write-protection errors see Section 8.4, "Flash Write Protect" and Section 8.3.6.3, "Protect Error Bit – D5".

Setup Errors

When a PROGRAM BYTE or ERASE PAGE command code cycle has been followed by a read bus cycle instead of a write cycle, the command is terminated, the state machine asserts the SETUP ERROR bit in the CSI status register and transitions to the IDLE state (not shown in Figure 8.3).

For information regarding setup errors see Section 8.3.5, "CSI Command Types" and Section 8.3.6.4, "Setup Error Bit – D4".

8.4 Flash Write Protect

When the CSI Flash Write Protect input nWRTPRT is asserted, the bottom 2k bytes (0x0000 – 0x07FF) of the Flash Main Memory Array (boot block) are write protected and cannot be changed by any programming method including byte programming, page erase or mass erase.

When nWRTPRT is asserted only the upper 62k of flash can be re-programmed or page erased; i.e., mass erase is disabled. When nWRTPRT is deasserted, all programming and erase functions, including mass erase, are enabled.

APPLICATION NOTE: To page erase or byte program the Information Block when the nWRTPRT input is asserted, set the page address to any non-boot block page. MASS ERASE for both the Information Block and Main Memory is always disabled when nWRTPRT is asserted.

The CSI nWRTPRT input is connected to the nFWP input pin and can also be controlled by the 8051 (see Section 8.5, "8051 Flash Boot Block Protect Controls").

8.5 8051 Flash Boot Block Protect Controls

8.5.1 Overview

The flash boot block can be hardware write-protected by the nFWP input pin. When the nFWP is asserted, the Flash boot block is locked and cannot be modified by any method until the nFWP pin is deasserted. There is also an 8051 runtime control FWRTPRT that can lock and unlock the flash boot block when the nFWP pin is deasserted. The LPC47N350 PGM pin can override both the nFWP pin and the FWRTPRT bit. The FWRTPRT bit is D0 in the 8051 Flash Boot Block Protect register (Table 8.14).

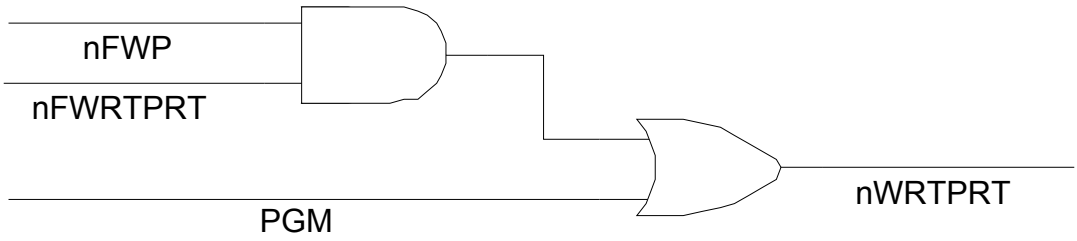


Figure 8.8 Flash Boot Block Write-Protect Controls

Note: Figure 8.8 is for illustration purposes only and is not intended to suggest specific implementation details.

Table 8.13 Flash Boot Block Controls Truth Table

NFWP (Note 8.8)	FWRTPRT (Note 8.9)	PGM (Note 8.10)	DESCRIPTION
1	1/0	0	When the nFWP input pin is deasserted, the 8051 can lock and unlock the Flash Boot Block using the FWRTPRT bit (see Section 8.5.2.2, "FWRTPRT – D0," on page 103).
0	X		When the nFWP input pin is asserted, the 8051 cannot unlock the Flash Boot Block.
X		1	The PGM input pin overrides the 8051 FWRTPRT bit and the nFWP input pin. When the PGM pin is asserted, the Flash Boot Block is not write protected.

Note 8.8 nFWP is the LPC47N350 Flash Write Protect input pin.

Note 8.9 FWRTPRT is the 8051 Flash Write Protect bit D0 in the Flash Boot Block Protect register (Table 8.14).

Note 8.10 PGM is the LPC47N350 External Program Enable input pin.

8.5.2 8051 Flash Boot Block Protect Register

The 8051 Flash Boot Block Protect register is shown below in Table 8.14.

Table 8.14 8051 Flash Boot Block Protect Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F88
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R	R/W
BIT NAME	Reserved							FWRTPRT

8.5.2.1 RESERVED – D[7:1]

Bits D7 – D1 are RESERVED. RESERVED bits cannot be written and return ‘0’ when read.

8.5.2.2 FWRTPRT – D0

The Flash Write Protect bit FWRTPRT permits the 8051 to lock the Flash boot block when the nFWP input pin is deasserted (see item # in Table 8.13). When FWRTPRT is ‘1’, the Flash Boot Block is locked, regardless of the state of the nFWP input pin. When FWRTPRT is ‘0’ (default), the Flash Boot Block is unlocked if the nFWP pin is deasserted.

8.6 Flash CSI Programming Examples

8.6.1 Overview

This section provides two C-like examples of LPC47N350 64k Embedded Flash programming using the CSI Program Byte and Mass Erase commands. As shown in the examples that follow, all transactions with the 64k Embedded Flash CSI Host Interface are simple read and write functions.

There is also another function NO_ERRORS_&_BUSY described here that is used in both the Program Byte and Mass Erase examples to check the CSI Status register during programming operations.

For the purposes of these examples all functions use the 8051 Flash Programming Interface (see Section 9.4, "8051 Flash Program Access"). It is also assumed that the 64k Embedded Flash ROM Main Memory Block is selected and that the Flash is in the Read Array mode before the examples begin.

8.6.1.1 CSIWRITE Function

The CSIWRITE function uses the 8051 Program Access registers to write to the CSI Host interface (Figure 8.9). For information regarding how to activate the 8051 Program Access Interface see Section 9.2, "Flash Program Interface Decoder".

The CSIWRITE function requires two parameters ‘address’ and ‘data’, although the address argument is not relevant during CSI Command Code cycles. Note that the address register arguments are initialized before the data register transaction occurs.

```
// Declarations
HIGH_ADDR_REG = 0x7FB0;                          // 16-bit High Addr. register MMCR Address.
LOW_ADDR_REG = 0x7FB1;                           // 16-bit Low Addr. register MMCR Address.
DATA_REG = 0x7FB2;                               // 16-bit Data register MMCR Address.

// Executable Code
void CSIWRITE(int address, int data)
  {                                              // Load Address Registers First.
    outportb(HIGH_ADDR_REG,                      // Load High Address Register.
                        ((address >> 8) & 0xFF));
    outportb(LOW_ADDR_REG, (address & 0xFF));           // Load Low Address Register.
    outportb(DATA_REG, (data & 0xff));                  // Write Data Register Last.
  };
```

Figure 8.9 CSIWRITE Command Function

8.6.1.2 CSIREAD Function

The CSIREAD function uses the 8051 Program Access registers to read to the CSI Host interface (Figure 8.10). For information regarding how to activate the 8051 Program Access Interface, see Section 9.2, "Flash Program Interface Decoder".

The CSIREAD function requires one parameter ‘address’ and returns the read data value. Note that the address parameter is not relevant during CSI Status Register read cycles.

```
// Declarations
HIGH_ADDR_REG = 0x7FB0;                          // 16-bit High Addr. register MMCR Address.
LOW_ADDR_REG = 0x7FB1;                           // 16-bit Low Addr. register MMCR Address.
DATA_REG = 0x7FB2;                               // 16-bit Data register MMCR Address.

// Executable Code
int CSIREAD(int address)
  {                                              // Load Address Registers First.
    outportb(HIGH_ADDR_REG,                      // Load High Address Register.
                        ((address >> 8) & 0xFF));
    outportb(LOW_ADDR_REG, (address & 0xFF));           // Load Low Address Register.
    return (inportb(DATA_REG));                         // Read and Return Data Register Value.
  };
```

Figure 8.10 CSIREAD Command Function

8.6.1.3 NO_ERRORS_&_BUSY Function

The NO_ERRORS_&_BUSY function (Figure 8.11) is used in a ‘while’ loop in Figure 8.12 and Figure 8.13 to check the CSI status register during byte program and page erase operations.

Note: The NO_ERRORS_&_BUSY function can only be used when the CSI Host interface is in the Read Status (Idle) state (see Section 8.3.7.6, "Read Status (Idle) Mode").

The NO_ERRORS_&_BUSY function requires one parameter ‘errors’ and returns TRUE when there are no errors and the BUSY bit is asserted or FALSE when errors have occurred or the BUSY bit is deasserted. The ‘errors’ parameter is an integer pointer for the CSI Status register error flags.

```
// Declarations
ERROR_MASK = 0x0070;                        // CSI Status Reg. Error Bits Mask.
BUSY_MASK = 0x0080;                         // CSI Status Reg. Busy Bit Mask.

// Executable Code
boolean NO_ERRORS_&_BUSY (int *errors)      // NOTE: Call only in CSI Idle (Read Status) State.
  {
   int etmp;                                // Temp Value for CSI Status Register.
   etmp = CSIREAD(0x0000);                  // Get CSI Status Register (Address = Don't Care).
   IF (*errors = (etmp & ERROR_MASK))       // First Check for Errors.
     return (FALSE);                        // Stop Loop Because of Error Flags.
   ELSE IF (etmp & BUSY_MASK)               // Look at Busy Bit.
     return (TRUE);                         // Continue Loop Because Busy Bit Asserted.
   ELSE return (FALSE);                     // Stop Loop Because Busy Bit Deasserted and No Errors.
  };
```

Figure 8.11 NO_ERRORS_and_BUSY Function

8.6.2 Byte Programming Example

Byte programming requires three basic steps: 1) activate the CSI Host Interface with the Program Byte command code, 2) send the program address and data arguments to the CSI address & data latches, and 3) monitor the completion status and check for errors.

The byte programming example pseudo-code is shown below in Figure 8.12. A return to the Read Array mode is also shown in Figure 8.12 to verify the Program Byte operation.

```
// Declarations                             // Programming Loop Control Variable
DONE = FALSE;                               // Program Byte Address Argument Value
WRITE_ADDRESS = 00F0;                       // Program Byte Data Argument Value
WRITE_DATA = 0xA0;                          // CSI Program Byte Command Code Value
PROGRAM_BYTE_CMD = 0x80;                    // CSI Read Array Command Code Value
READ_ARRAY_CMD = 0xFF;                      // CSI Clear Status Command Code Value
CLEAR_STATUS_CMD = 0xA0;                    // Variable for Status Register Errors
ERRORS = 0x00;
// Executable Code
WHILE (NOT DONE)
{                                           // Send Program Byte Command Code (Address = Don't
CSIWRITE(0x0000, PROGRAM_BYTE_CMD);         Care).
CSIWRITE(WRITE_ADDRESS, WRITE_DATA);        // Send Program Byte Argument.
WHILE (NO_ERRORS_&_BUSY(&ERRORS));          // Loop Until Errors Occur or BUSY Bit Deasserted.
IF (ERRORS)                                 // Take Remedial Steps.
{
FIX_ERRORS(ERRORS);                         // Correct Problems (e.g. Protect or Setup Errors).
CSIWRITE(0x0000, CLEAR_STATUS_CMD);         // Clear Status Register (Address = Don't Care).
}                                           // Try Again.
ELSE                                        // Restore Read Ar ray Mode To Verify Byte
{                                           Programming.
CSIWRITE(0x0000, READ_ARRAY_CMD);
IF (CSIREAD(WRITE_ADDRESS) = WRITE_DATA)
DONE = TRUE;                                // If Not Verified, Try Again.
}
}
```

Figure 8.12 Program Byte Example Pseudo-Code

8.6.3 Mass Erase Example

Mass Erase requires two basic steps: 1) activate the CSI Host Interface with the Mass Erase command code and 2) monitor the completion status and check for errors. The Mass Erase example pseudo-code is shown in Figure 8.13. A return to the Read Array mode is also shown in Figure 8.13.

```
// Declarations
DONE = FALSE;                              // Programming Loop Control Variable
MASS_ERASE_CMD = 0x20;                     // CSI Mass Erase Command Code Value
READ_ARRAY_CMD = 0xFF;                     // CSI Read Array Command Code Value
CLEAR_STATUS_CMD = 0xA0;                   // CSI Clear Status Command Code   Value
ERRORS = 0x00;                             // Variable for Status Register Errors

// Executable Code
WHILE (NOT DONE)
  {
   CSIWRITE(0x0000, MASS_ERASE_CMD);       // Send Mass Erase Command Code (Address = Don't Care).
                                           // No Argument Cycle Required.
   WHILE (NO_ERRORS_&_BUSY(&ERRORS));      // Loop Until Errors Occur or BUSY Bit Deasserted.
   IF (ERRORS)                             // Take Remedial Steps
     {
      FIX_ERRORS(ERRORS);                  // Correct Problems (e.g. Protect Error).
      CSIWRITE(0x0000, CLEAR_STATUS_CMD);  // Clear Status Registe r (Address = Don't Care).
     }                                     // Try Again.
   ELSE                                    // Restore Read Array Mode
     {
      CSIWRITE(0x0000, READ_ARRAY_CMD);    // Address = Don't Care.
      DONE = TRUE;
     }
  }
```

Figure 8.13 Mass Erase Example Pseudo-Code

Chapter 9 Flash Programming Interface

9.1 Overview

The LPC47N350 8051 has read and write access to the embedded Flash ROM in a single contiguous 64k-byte page (Figure 9.12). The LPC47N350 64k Embedded Flash can be programmed by the 8051, an external ATE Program interface, and by the LPC Host (Figure 9.12).

During normal operations, the Flash is dedicated as the 8051 Code space, the 8051 only has read access to the Flash, and the internal 8051 memory ROM bus is not accessible. The Keyboard Controller Bus Monitor (KCBM) function, which is controlled by the PGM and nEA pins, permits monitoring of the internal 8051 memory ROM bus using the KBD Scan interface pins. When the KCBM is enabled, reads from the 8051 code space and reads and writes from the 8051 data space are visible on the KCBM interface pins. (see Section 9.8, "Keyboard Controller Bus Monitor Interface").

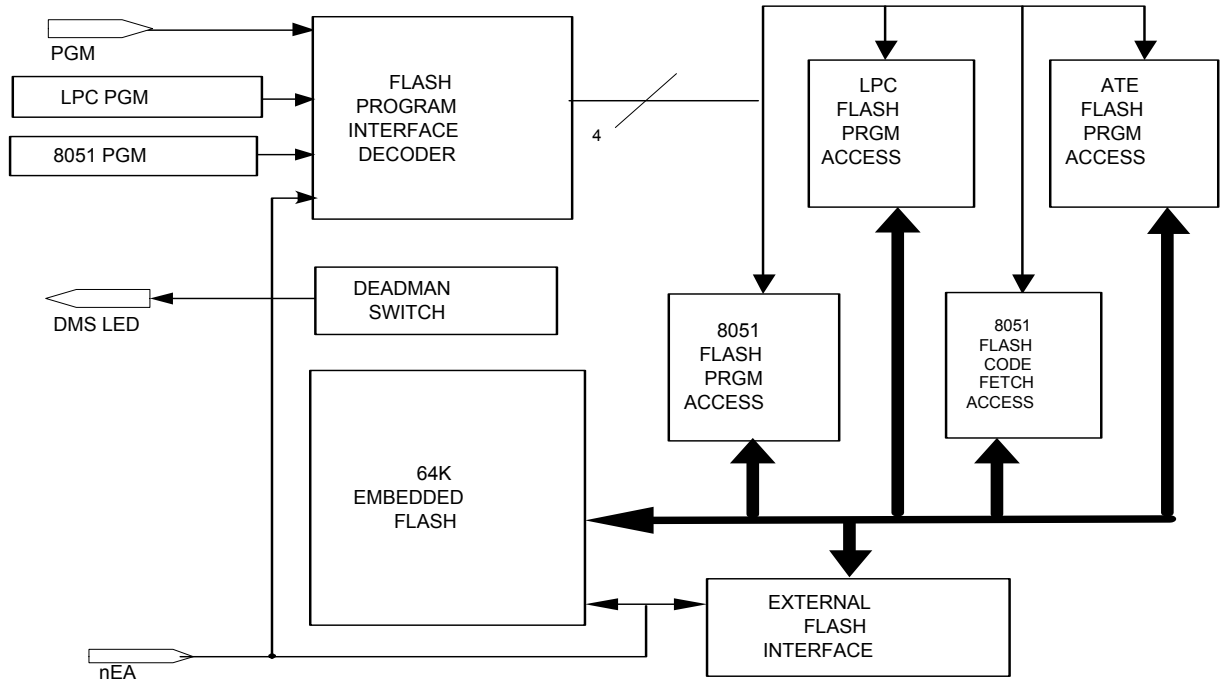


Figure 9.1 Flash System Interface

Note: This figure is for illustration purposes only and is not intended to suggest specific implementation details.

9.2 Flash Program Interface Decoder

The Flash Program Interface Decoder controls access to the 64k Embedded Flash (Figure 9.1).

The Flash configurations described below depend upon the state of the PGM and nEA pins and the LPC PGM and 8051 PGM bits in the Flash Program register. The ATE PGM and EXT FLASH bits in the Flash Program register reflect the state of the PGM and nEA pins. When the PGM and nEA pins are asserted, the Flash Program Interface Decoder enters the KCBM Interface state (see Table 9.1, "Flash Program Interface Decoder Truth Table", items# 6, 7 and 8). The PGM and nEA pins control both the function enable and the pin multiplexing for the KCBM Interface. Table 9.1, below provides the truth table for the Flash Program Interface Decoder. See Section 9.10, "Flash Program Register".

Table 9.1 Flash Program Interface Decoder Truth Table

ITEM #	FLASH PROGRAM REGISTER				MODE	DESCRIPTION
	EXT FLASH (D3) Note 9.1	ATE PGM (D2) Note 9.2	LPC PGM (D1)	8051 PGM (D0)		
1	0	0	0	0	8051 CODE FETCH ACCESS	The Flash is dedicated as the 8051 Code space. The 8051 only has read access to the Flash in this mode.
2	0	0	1	0	LPC PROGRAM ACCESS	The Flash is dedicated to the LPC Host programming interface.
3	0	0	X	1	8051 PROGRAM ACCESS	The Flash is dedicated to the 8051 programming interface. When this mode is selected, the LPC Host programming interface cannot be enabled; i.e., the LPC PGM bit is irrelevant. The 8051 must only execute program code from the 512-byte Scratch ROM.
4	0	1	0	0	ATE PROGRAM ACCESS	The Flash is dedicated to the ATE programming interface. When this mode is selected, both the LPC Host programming interface and the 8051 programming interface are disabled; i.e., the LPC PGM and the 8051 PGM bits are reset to '0'
5	1	0	X	X	EXTERNAL FLASH	The 8051 is running out of external Flash. When this mode is selected, the ATE, LPC Host and 8051 programming interfaces cannot be enabled
6	1	1	0	0	KCBM - 8051 CODE FETCH ACCESS	The KCBM function is enabled and the Flash is dedicated as the 8051 Code space. The 8051 only has read access to the Flash in this mode. The KCBM interface monitors activity on the internal 8051 ROM bus.
7	1	1	X	1	KCBM - 8051 PROGRAM ACCESS	The KCBM function is enabled and the Flash is dedicated to the 8051 programming interface. The 8051 executes program code from the 512-byte Scratch ROM. The KCBM interface monitors access to the Scratch ROM (8051 ROM bus).
8			1	0	KCBM - LPC PROGRAM ACCESS	The KCBM function is enabled and the the Flash is dedicated to the LPC programming interface. The 8051 is held in reset during all LPC Flash Program Access operations. The state of the KCBM interface is undefined in this mode.

Note 9.1 The EXT FLASH bit D3 in the Flash Program register is the inverse of the nEA pin.

Note 9.2 The ATE PGM bit D2 in the Flash Program register is the PGM pin.

9.3 8051 Code Fetch Access

The 8051 Code Fetch Access function uses the 64k Embedded Flash as the 8051 program memory space (). The 8051 Code Fetch Access function is enabled when bits D3 – D0 in the Flash Program register are '0' (see Table 9.1 and Section 9.10, "Flash Program Register").

Note: When the 8051 Code Fetch Access function is selected and the MMC bit is '1', the 8051 can execute from the 64k Embedded Flash and from the Scratch ROM (see Section 9.11, "Scratch ROM").

9.4 8051 Flash Program Access

The 8051 Flash Program Access function enables the 64k Embedded Flash to be programmed from an internal parallel hardware interface using 8051 memory-mapped control registers (see Section 9.10.7, "8051/LPC Flash Program Access Registers" and Figure 9.2). The 8051 PGM bit D0 in the Flash Program register is used to enable the 8051 Program Access function (see Section 9.10.6, "8051 PGM – D0").

APPLICATION NOTE: The 8051 must only execute program code from the 512-byte Scratch ROM to use the 8051 Flash Program Access function (see Section 9.11, "Scratch ROM"). When Flash programming operations are completed, the 8051 must return the Embedded Flash to the READ ARRAY state (Table 8.6) before returning to the 8051 Code Fetch Access mode (Table 9.1). The 8051 must return the Embedded Flash to Read-Array mode when programming has been completed before jumping out of the Scratch ROM code space.

To program the 64k Embedded Flash using the 8051 Flash Program Access function, first use the HIGH ADDRESS (0x7FB0) and LOW ADDRESS (0x7FB1) registers for program and page address arguments and then the DATA register (0x7FB2) for program data, read data, command codes and status data.

Note: Address arguments for Program Byte and Page Erase operations must be initialized in the 8051 Flash Program Access address registers before read and write commands to the CSI Host Interface are activated by reads and writes to the 8051 Flash Program Access DATA register (0x7FB2).

For information regarding the programming sequence for the LPC47N350 64k Embedded Flash, see Section 8.3, "Command Sequence Interface (CSI)".

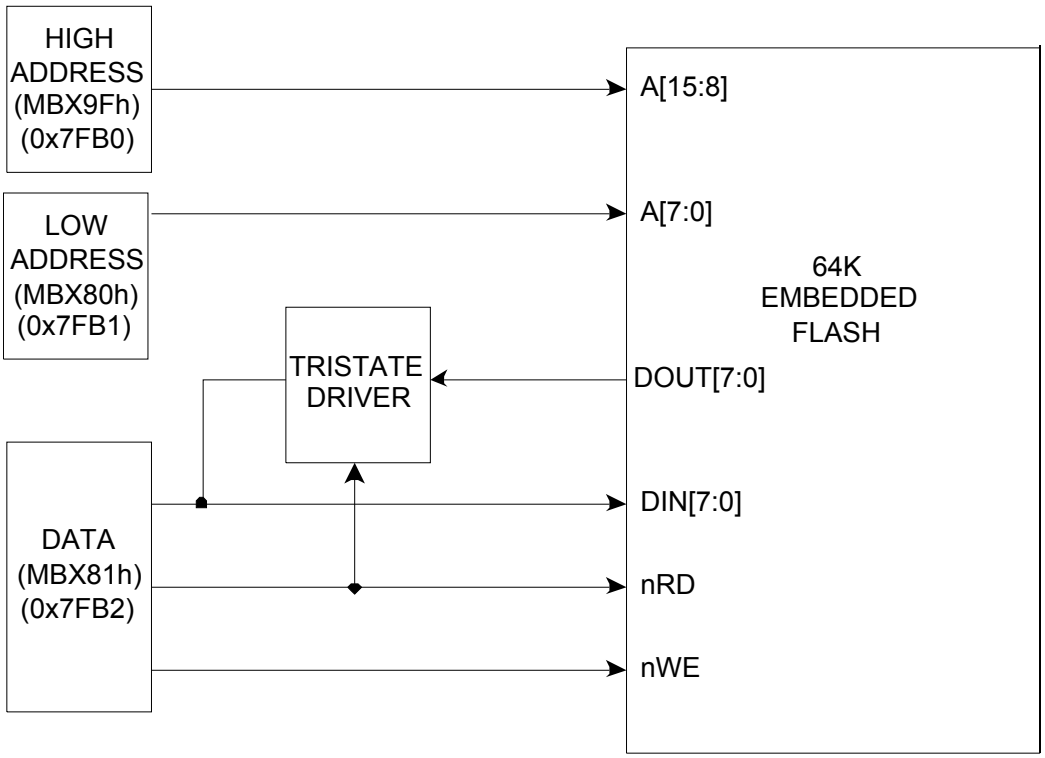


Figure 9.2 8051/LPC Flash Program Access

Note: This figure is for illustration purposes only and is not intended to suggest specific implementation details.

9.5 LPC Bus Flash Program Access

The LPC Flash Program Access function enables the 64k Embedded Flash to be programmed from an internal parallel hardware interface (see Figure 9.2 above). The LPC Flash Program Access function uses the registers in the Mailbox Registers Interface (see Section 9.10.7, "8051/LPC Flash Program Access Registers"). The LPC PGM bit D1 in the Flash Program register is used to enable the LPC Program Access function (see Section 9.10.5, "LPC PGM – D1" below). The LPC Flash Program Access function can only be enabled when the ATE PGM and the 8051 PGM bits are deasserted '0' (Table 9.1), and the SYSTEM FLASH bit in the Disable register is deasserted '0'(See Section 7.8.3.1, "Disable Register").

APPLICATION NOTE: The 8051 must be stopped to use the LPC Bus Flash Program Access function. When Flash programming operations are completed, the LPC Host must return the Embedded Flash to the READ ARRAY state (Table 8.6) before returning to the 8051 Code Fetch Access mode (Table 9.1) and restarting the 8051 clock.

To program the 64k Embedded Flash using the LPC Bus Flash Program Access function, first use the Flash High Address (MBX9Fh) and Flash Low Address (MBX80h) registers for program and page address arguments and then the Flash Data register (MBX81h) for program data, read data, command codes and status data.

Note: Address arguments for Program Byte and Page Erase operations must be initialized in the LPC Flash Program Access address registers before read and write commands to the CSI Host Interface are activated by reads and writes to the LPC Flash Program Access DATA register (MBX81h).

For information regarding the programming sequence for the 64k Embedded Flash see Section 8.3, "Command Sequence Interface (CSI)".

9.6 ATE Flash Program Access

9.6.1 Overview

The ATE Flash Program Access function enables the 64k Embedded Flash to be programmed from an external parallel hardware interface using the KBD Scan interface in the LPC47N350 pin configuration. The Flash Program Interface Decoder enables the ATE Flash Program Access function (Table 9.1, item #4) (see Section 9.6.3, "PGM Pin").

A block diagram of the ATE Flash Program Access Interface is shown below in Figure 9.3. The ATE Flash Program Access pin mapping to the KBD Scan interface pins is shown in Table 9.2. For information regarding the programming sequence for the LPC47N350 64k Embedded Flash see Section 8.3, "Command Sequence Interface (CSI)".

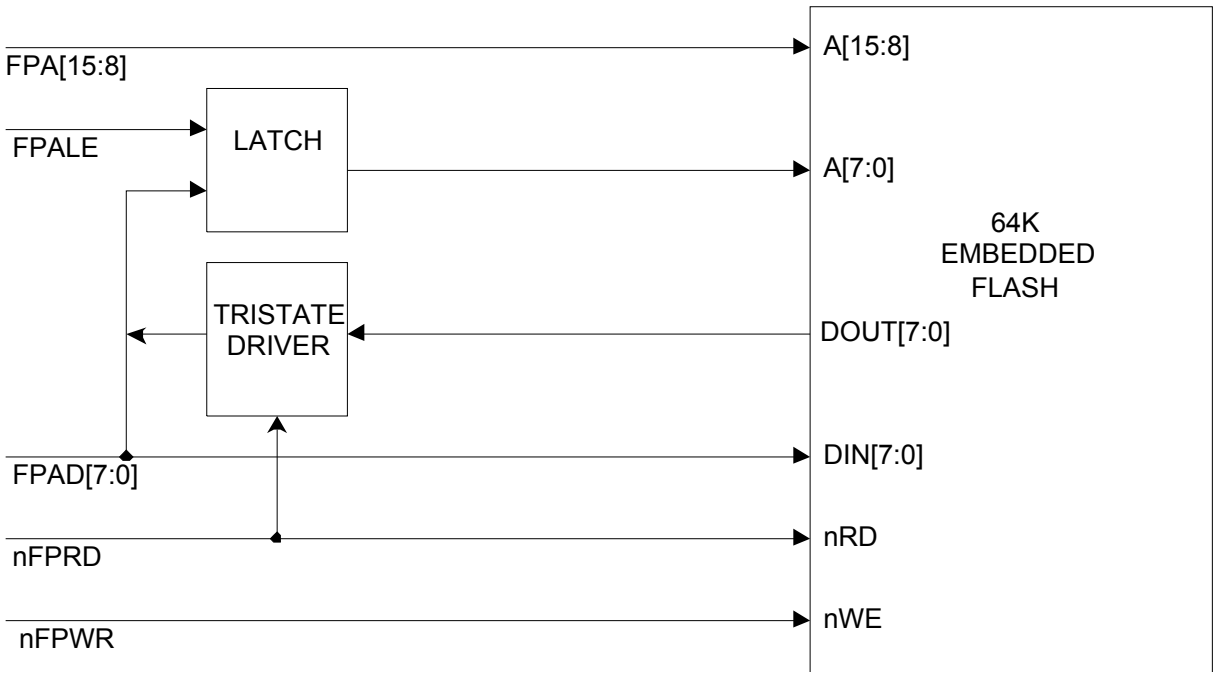


Figure 9.3 ATE Flash Program Access Interface

Note: This figure is for illustration purposes only and is not intended to suggest specific implementation details.

Table 9.2 ATE Flash Program Access Interface KBD Scan Pin Mapping

ITEM #	KBD SCAN INTERFACE PINS	ATE FLASH PROG ACCESS INTERFACE	DESCRIPTION
1	KSO0	FPA15	High-Order Address Bus A15 – A8
2	KSO1	FPA14	
3	KSO2	FPA13	
4	KSO3	FPA12	
5	KSO4	FPA11	
6	KSO5	FPA10	
7	KSO6	FPA9	High-Order Address Bus A15 – A8
8	KSO7	FPA8	
9	KSO8	FPAD7	Multiplexed Low-Order Address Bus A7 – A0 and Data Bus D0 – D7. The Low-Order Address Bus is Latched with FPALE.
10	KSO9	FPAD6	
11	KSO10	FPAD5	
12	KSO11	FPAD4	
13	KSI0	FPAD3	
14	KSI1	FPAD2	
15	KSI2	FPAD1	
16	KSI3	FPAD0	
17	KSI4	FPALE	Low-Order Address Bus Latch Control
18	KSI5	nFPRD	Active-Low ATE Flash Program Access Interface READ Signal.
19	KSI6	nFPWR	Active-Low ATE Flash Program Access Interface WRITE Signal.

Note: All ATE Flash Program Access Interface signals in Table 9.2 refer to Figure 9.3.

All KDB SCAN Interface pins refer to the pin configuration (See Table 2.1and Table 2.2 on page 4.)

9.6.2 ATE Flash Program Timing

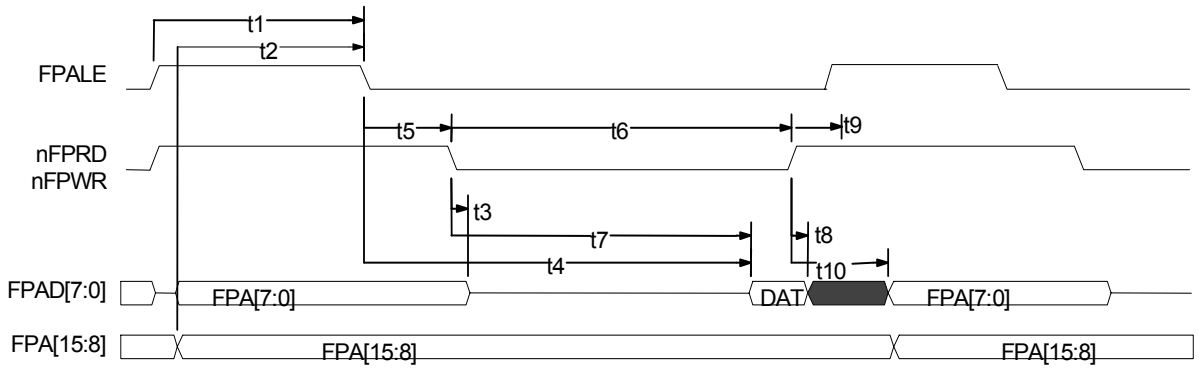


Figure 9.4 ATE Flash Program Access Interface Timing

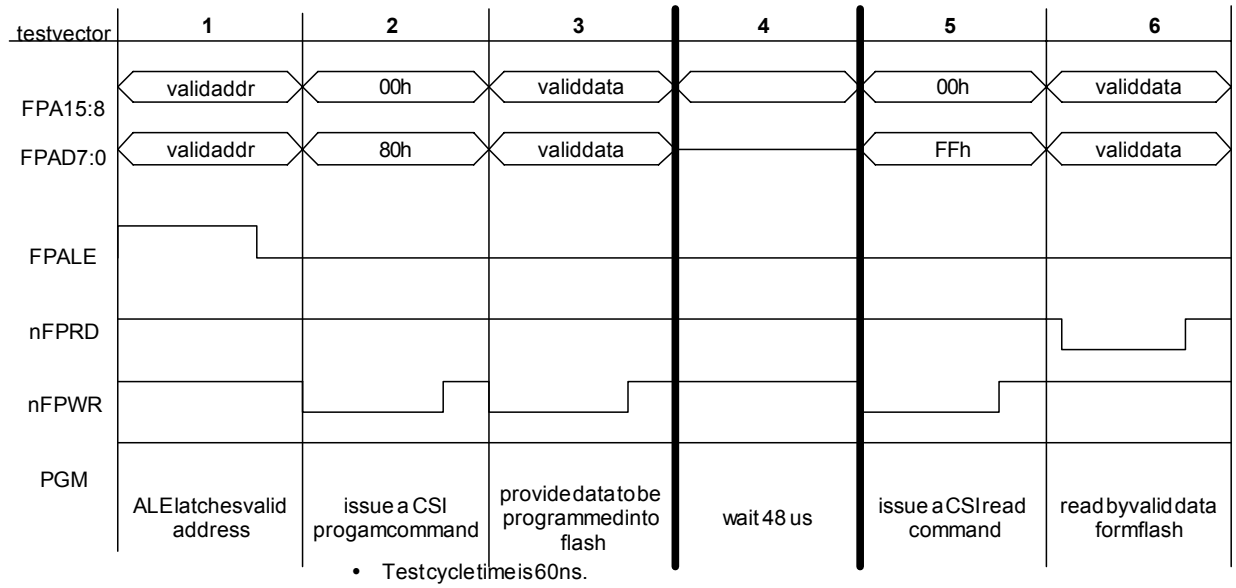
Table 9.3 ATE Flash Program Access Interface Write Timing Parameters

PARAMETER		MIN	TYP	MAX	UNITS
t1	FPALE Pulse Width	-	50	-	ns
t2	Address Valid to FPALE Low	-		-	ns
t4	FPALE Low to Valid data In	-	10	-	ns
t5	FPALE Low to nFPWR Low	-	5	-	ns
t6	nFPWR Pulse Width	-	50	-	ns
t7	nFPWR Low to Valid Data In	-	5	-	ns
t8	Valid data Hold Time Following nFPWR Low-To-High Transition	-	10	-	ns
t9	nFPWR High to FPALE High	-	0	-	ns

Table 9.4 ATE Flash Program Access Interface Read Timing Parameters

PARAMETER		MIN	TYP	MAX	UNITS
t1	FPALE Pulse Width	-	50	-	ns
t2	Address Valid to FPALE Low	-		-	
t3	nFPRD Low to Address Float	-		-	
t4	FPALE Low to Valid data Out	-	10	-	
t5	FPALE Low to nFPRD Low	-	5	-	
t6	nFPRD Pulse Width	-	50	-	
t7	nFPRD Low to Valid Data Out	-	5	-	
t8	Valid data Hold Time Following nFPRD Low-To-High Transition	-	10	-	
t9	nFPRD High to FPALE High	-	-	0	
t10	Data Float Following nFPRD Low-To-High Transition	-	-		ns

Note: The values in Table 9.3 and Table 9.4 come from SMSC ATE testing.



- Test cycle time is 60ns.
- Pulse width of FPALE, nFPRD, and nPFWR is 50ns.
- The wait in vector 4 is 1200x60ns=48us

Figure 9.5 ATE Flash Program Access Interface Write Timing Parameters

9.6.3 PGM Pin

The PGM pin enables the ATE Flash Program access function. When the PGM pin is the exclusively asserted input to the Flash Program Interface Decoder (Table 9.1, item #4), the 64k Embedded Flash interface is directly connected to the ATE Flash Program Access interface, the KBD Scan interface pin multiplexing is configured to support ATE Flash Program Access, the 8051 is stopped (reset), and all Flash write-protect functions are disabled (see Section 8.5, "8051 Flash Boot Block Protect Controls").

To stop the 8051, the PGM pin asserting (‘1’) causes the rst_in_n input to the 8051 is asserted (‘0’). When the PGM pin is deasserted, the 64k Embedded Flash interface is reconnected to the 8051, the Embedded Flash is reset to READ ARRAY mode, the rst_in_n input to the 8051 is deasserted and the Flash write-protect function is re-enabled.

9.7 External Flash Interface

The External Flash Interface function enables the 8051 program memory to reside in an external ROM device using the KBD Scan Interface in the LPC47N350 pin configuration.

A block diagram of the External Flash Interface is shown below in Figure 9.6. The External Flash Interface pin mapping to the KBD Scan interface pins is shown in Table 9.5. The Flash Program Interface Decoder enables the the External Flash Interface function (Table 9.1, item #5). When the nEA pin is asserted, the 8051 program memory is disconnected from 64k Embedded Flash interface and connected to the External Flash Interface, the KBD Scan interface pin multiplexing is configured to support the External Flash Interface, and the 64k Embedded Flash is placed in a Reset state (see Section 8.3.3, "Reset," on page 90).

Note: The LPC47N350 External Flash Interface only supports 8051 ROM read cycles (Figure 9.7 and Table 9.6). The External Flash Interface is compatible with flash devices like the Intel 28F004.

The 8051 normally uses the mem_wr_n signal as a write strobe for its data RAM. Optionally, it can perform writes to code ROM using the mem_pswr_n signal. When the WRS Control bit D0 is set to “1” in the SPC_FNC SFR (See Section 8.3.5, "CSI Command Types"), the DW8051 uses the mem_pswr_n signal instead of the mem_wr_n when MOVX instructions are executed. By attaching mem_pswr_n to its 64K code space, the 8051 can perform writes to its code space when the WRS bit is set to “1”.

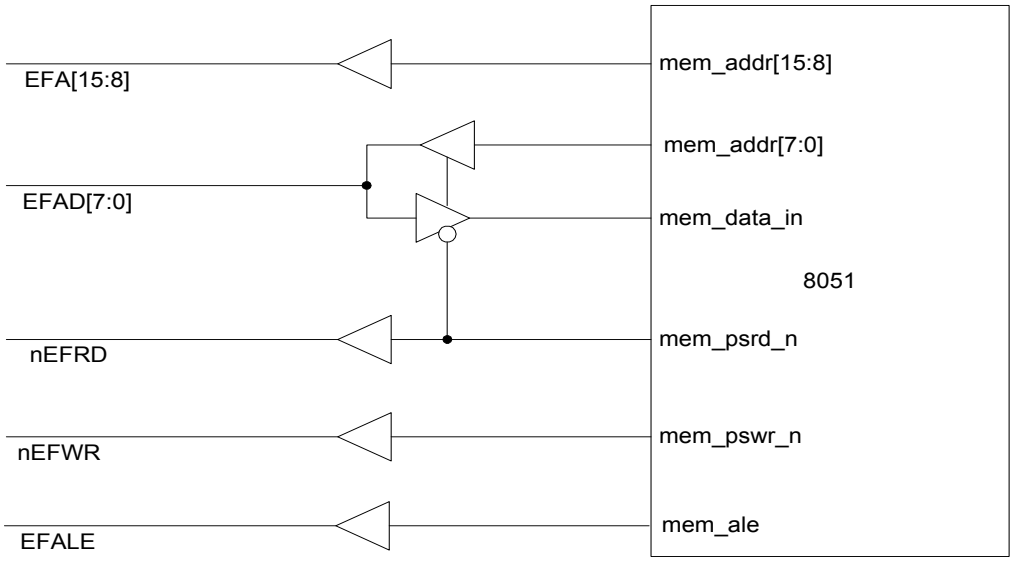


Figure 9.6 LPC47N350 External Flash Interface

Note: This figure is for illustration purposes only and is not intended to suggest specific implementation details.

Table 9.5 External Flash Interface KBD Scan Pin Mapping

KBD SCAN PINS	EXTERNAL FLASH INTERFACE	DESCRIPTION
KSO0	EFA15	High-Order Address Bus A15 – A8.
KSO1	EFA14	
KSO2	EFA13	
KSO3	EFA12	
KSO4	EFA11	
KSO5	EFA10	
KSO6	EFA9	
KSO7	EFA8	
KSO8	EFAD7	Multiplexed Low-Order Address Bus A7 - A0 and Data Bus D0 – D7. The Low-Order Address Bus is Latched Externally with EFALE.
KSO9	EFAD6	
KSO10	EFAD5	
KSO11	EFAD4	
KSI0	EFAD3	
KSI1	EFAD2	
KSI2	EFAD1	
KSI3	EFAD0	
KSI4	EFALE	Low-Order Address Bus Latch Control

Table 9.5 External Flash Interface KBD Scan Pin Mapping (continued)

KBD SCAN PINS	EXTERNAL FLASH INTERFACE	DESCRIPTION
KSI5	nEFRD	Active-Low External Flash Interface READ Signal.
KSI6	nEFWR	Active-Low External Flash Interface WRITE Signal.

Note: All External Flash Interface signals in Table 9.5 refer to Figure 9.6. All KDB SCAN Interface pins refer to the LPC47N350 pin configuration.

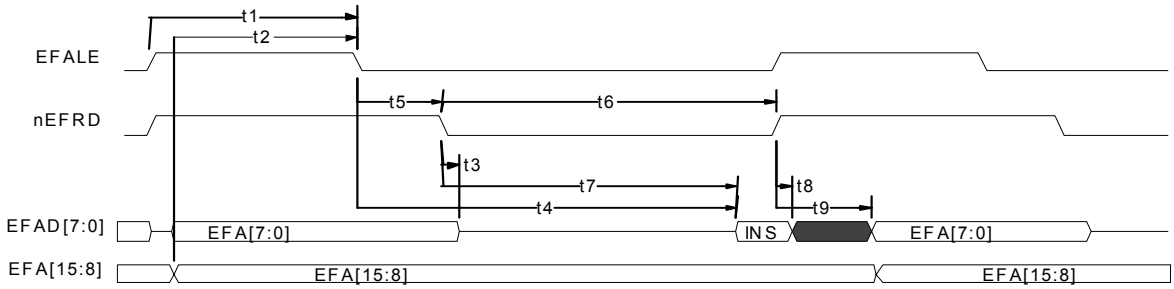


Figure 9.7 External Flash Interface Timing Diagram

Table 9.6 External Flash Interface Timing Values

PARAMETER		MIN	TYP	MAX	UNITS
t1	EFALE Pulse Width		125		ns
t2	Address Valid to EFALE Low		86		
t3	nEFRD Low to Address Float		5		
t4	EFALE Low to Valid Instruction In		83		
t5	EFALE Low to nEFRD Low		160		
t6	nEFRD Pulse Width		160		
t7	nEFRD Low to Valid Instruction In		145		
t8	Valid Instruction Hold Time Following nEFRD Low-To-High Transition	0			

Note: The values in Table 9.6 are for the 12MHz Clock. The SMSC evaluation board design utilizes an AM29F002NBT-120 (120 ns) flash and 8051 clock frequency of 12 MHz

9.8 Keyboard Controller Bus Monitor Interface

The Keyboard Controller Bus Monitor (KCBM) functions provide monitoring for the internal 8051 memory ROM bus using the KBD Scan interface pins. When the KCBM is enabled, reads from the 8051 code space are visible on the KCBM interface pins. The three KCBM functions provide external access modes corresponding to 8051 CODE FETCH ACCESS, LPC PROGRAM ACCESS, 8051 PROGRAM ACCESS (Table 9.1, items #6, 7 and 8)

When the PGM and nEA pins are asserted, the KCBM interface is enabled and all the pins shown in Table 9.2 are outputs.

Note: The 8051 will be reset when exiting KCBM mode if the PGM pin is asserted while the nEA pin is deasserted.

Table 9.7 KCBM Access Interfaces Mapped To KBD Scan Pin

KBD SCAN INTERFACE PINS	KCBM INTERFACE	KCBM INTERFACE DESCRIPTION
KSO0	KCA15	Keyboard Controller High-Order Address Bus A15 – A8.
KSO1	KCA14	
KSO2	KCA13	
KSO3	KCA12	
KSO4	KCA11	
KSO5	KCA10	
KSO6	KCA9	
KSO7	KCA8	
KSO8	KCAD7	Keyboard Controller Multiplexed Low-Order Address Bus A7 – A0 and Data Bus D0 – D7. The contents of this bus are indicated by the KCDSTB pin.
KSO9	KCAD6	
KSO10	KCAD5	
KSO11	KCAD4	
KSI0	KCAD3	
KSI1	KCAD2	
KSI2	KCAD1	
KSI3	KCAD0	
KSI4	KCCLK	Keyboard Controller (8051) Clock Output.
KSI5	KCDSTB	Keyboard Controller Data Strobe: asserted (‘1’) when the KCAD[7:0] pins contain program memory code data and deasserted (‘0’) when the KCAD[7:0] pins contain program memory address data.

Note: All KDB SCAN Interface pins refer to the LPC47N350 pin configuration.

When the KCBM mode is enabled, the KCA[15:8] pins contain the high-order Flash address bits and the KCAD[7:0] pins alternately contain the low-order Flash address bits and the Flash data bits. The Keyboard Controller Data Strobe (KCDSTB) determines the contents of the KCAD[7:0] pins. When the KCDSTB pin is deasserted (‘0’), the KCAD[7:0] pins contain the low-order Flash address, when KCDSTB is asserted (‘1’), the KCAD[7:0] pins contain the Flash data.

The Keyboard Controller Clock pin (KCCLK) contains the 8051 clock. Transitions on the KCA, KCAD, and KCDSTB pins occur following the rising edge of KCCLK. The Flash address and data values are stable before the subsequent rising edge of KCCLK.

Timing for the KCBM Interface is shown below in Figure 9.8 and Table 9.8.

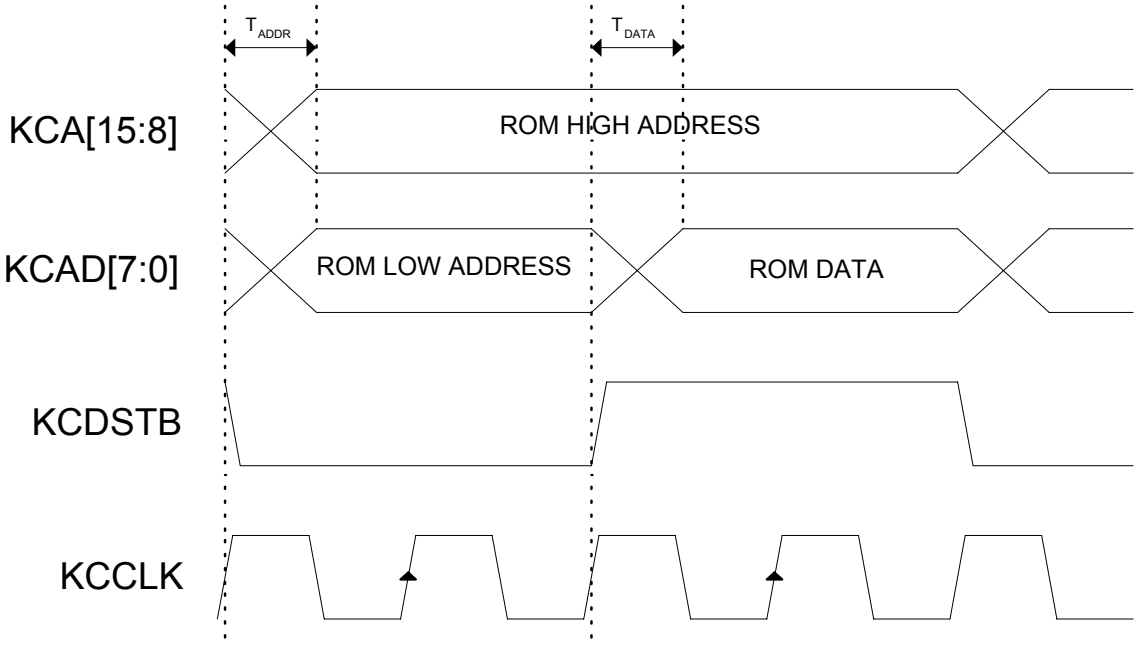


Figure 9.8 KCBM Interface Timing Diagram

Table 9.8 KCBM Interface Timing Values

	PARAMETER	MAX	UNITS
T_{ADDR}	KCCLK High to Address Valid (KCDSTB Low)	<30	ns
T_{DATA}	KCCLK High to Data Valid (KCDSTB High)		

9.9 Deadman Switch

9.9.1 Overview

The Deadman Switch (DMS) is used to identify 8051 boot sequences where the LPC47N350 2k boot block is unprogrammed or corrupted. The DMS is initialized when the 8051 is reset, for example following VCC1 POR or when the PGM pin is asserted, and begins counting as soon as the 8051 begins instruction execution. If the 8051 boot code does not disable the DMS counter using the DMS_DISABLE bit within 62.5ms, the DMS LED begins flashing.

For a description of the DMS_DISABLE bit see, Section 9.9.4, "DMS Register". For a description of the DMS Operation, see Section 9.9.2, "DMS Operation". For a description of the nDMS_LED output pin, see Section 9.9.3. Figure 9.9 which illustrates a boot sequence where the Flash is unprogrammed or corrupted.

1. Apply VCC1
2. Unprogrammed Flash Causes Deadman Switch Overflow
3. DMS LED Flashes
4. ATE Flash Program Access Interface Initializes 8051 Boot Block/Program Code (DMS LED Stops Flashing)
5. 8051 Boot Block Execution Begins

Figure 9.9 Example Boot Sequence for Unprogrammed or Corrupted Boot Block

9.9.2 DMS Operation

The DMS consists of a counter with a carry output, clock input, clear input and a count control input; a 32.768kHz RTC timebase input; an nDMS_LED output pin; and count/clear control logic (Figure 9.10). The DMS counter is an 11-bit binary counter. When the counter is cleared, using the 32.768kHz RTC timebase, the DMS counter carry output will be asserted 62.5ms after counting begins. When the carry output is asserted, the counter clock is stopped, the DMS_OVERFLOW bit is asserted and the DMS LED begins flashing. For a description of the nDMS_LED output pin (not shown in Figure 9.10) see Section 9.9.3, "nDMS_LED Pin".

There are four basic DMS operating states as shown in Table 9.9: Initialize, Counting, Overflow, Disabled. The DMS can also be enabled for test purposes (see Section 9.9.4.2, "DMS_TEST Bit – D1").

In normal operation, the DMS Initialize state occurs as a result of VCC1 POR. The Initialize state can also occur when the PGM pin is asserted (see Section 9.6, "ATE Flash Program Access") or when the DMS_TEST bit is asserted (see Section 9.9.4, "DMS Register"). In normal operation, the DMS Counting state begins when the 8051 begins executing program code. The DMS Counting state also occurs during DMS testing. The DMS Counting state can be terminated by the DMS_DISABLE bit, the DMS Counter carry output, 8051_RESET or the DMS_TEST bit.

The DMS Overflow state occurs when the DMS Counter carry output is asserted. The DMS Overflow state occurs when the 8051 boot block is unprogrammed or corrupted, or during DMS testing. In normal operation, the DMS Disable state occurs when the 8051 asserts the DMS_DISABLE bit. Typically, the DMS Disable state persists until the next VCC1 POR or until DMS testing begins.

Note: In normal operation, the 8051 boot code must assert the DMS_DISABLE bit before within 62.5ms to prevent the DMS Overflow state from asserting the DMS LED indicator.

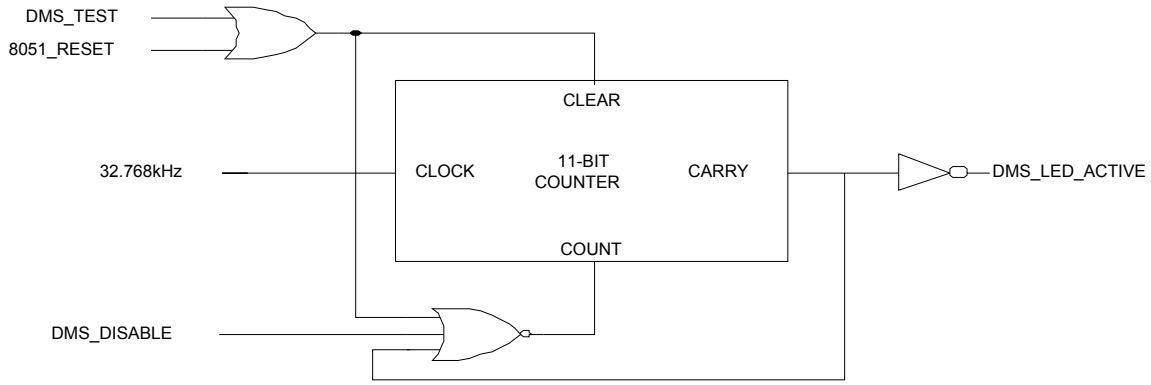


Figure 9.10 Deadman Switch Block Diagram

Note: This figure is for illustration purposes only and is not intended to suggest specific implementation details.

Table 9.9 DMS Truth Table

ITEM #	DMS CONTROLS			DMS STATE	DESCRIPTION
	8051_RESET OR DMS_TEST	DMS_DISABLE	CARRY		

Table 9.9 DMS Truth Table (continued)

1	1	0	0	INITIALIZE	The 8051_RESET is asserted because of VCC1 POR or the PGM pin, or the DMS is in test mode. The DMS counter is cleared, the DMS LED is not flashing, and the DMS counter is stopped.
2	0			COUNTING	DMS is counting. In normal operation, the 8051 must set the DMS_DISABLE bit before the DMS counter overflows and activates the DMS LED.
3			1	OVERFLOW	The 8051 has not disabled the DMS in time to prevent the DMS LED from flashing. The Flash is probably unprogrammed or corrupted, or the DMS LED is being tested. The DMS LED is activated and the DMS_OVERFLOW bit is asserted.
4	X	1	0	DISABLED	The 8051 has disabled the DMS in time to prevent the DMS LED from flashing. The Flash 2k boot block is intact. The DMS counter is permanently disabled (stopped) until the next VCC1 POR, or the DMS_DISABLE bit is deasserted for testing.

9.9.3 nDMS_LED PIN

In normal operation, the DMS Overflow state (Table 9.9) causes the DMS LED pin to blink (Figure 9.11). When the nDMS_LED pin is '0', the LED is 'on'; when the nDMS_LED pin is '1', the LED is 'off'. When the DMS LED is blinking, the LED on-time T is 125msec. The DMS LED blinking period P is 1 second. Once the DMS LED starts blinking, only an 8051 RESET or the DMS_TEST bit can turn the DMS LED off.

Note: The DMS LED can be forced to blink after 62.5ms using the DMS_TEST and DMS_DISABLE bits (see Section 9.9.4, "DMS Register").

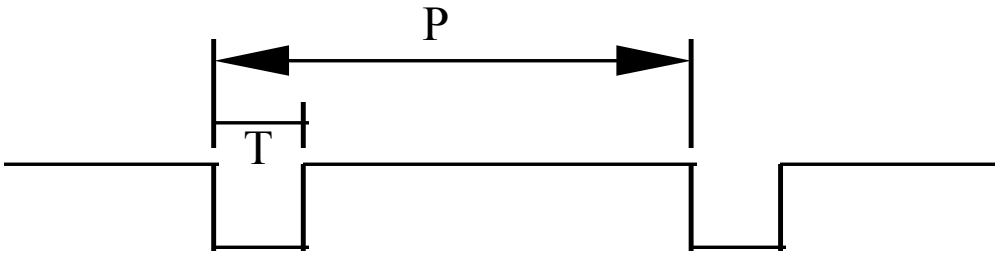


Figure 9.11 DMS_LED Output

9.9.4 DMS Register

The DMS register contains control and status bits for the Deadman Switch function (Table 9.10). The DMS register is available only to the 8051 at MMCR address 0x7F86 and is cleared by VCC1 POR.

Table 9.10 DMS Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F86
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R/WC	R/W	R/W
BIT NAME	Reserved					DMS_ OVER FLOW	DMS_TEST	DMS_DISABLE

9.9.4.1 DMS_OVERFLOW Bit – D2

The DMS_OVERFLOW bit indicates that the DMS overflow state has occurred (see Table 9.9, above). The DMS_OVERFLOW bit is the Carry output of the DMS counter (not shown in Figure 9.10).

When the DMS_OVERFLOW bit is deasserted ‘0’ (default), the DMS overflow state has not occurred or has been cleared. When the DMS_OVERFLOW bit is asserted ‘1’, the DMS overflow state has occurred. The DMS_OVERFLOW bit is R/WC. To deassert the DMS_OVERFLOW bit, write a ‘1’ to bit D2. The DMS_OVERFLOW bit is also deasserted by VCC1 POR. The DMS_OVERFLOW bit can inform the 8051 that an unprogrammed or corrupted Flash Boot Block has been restored without a VCC1 POR.

9.9.4.2 DMS_TEST Bit – D1

The DMS_TEST bit along with the DMS_DISABLE bit (D0) can be used to exercise the DMS counter and the nDMS_LED output pin for test purposes because in a properly functioning system the DMS_LED output will never be asserted.

When the DMS_TEST bit is deasserted ‘0’ (default), the DMS test function is disabled. When the DMS_TEST bit is asserted ‘1’, the DMS counter is cleared and disabled (Figure 9.10). The DMS_TEST bit is R/W and deasserted by VCC1 POR. To exercise the nDMS_LED output pin, follow the steps shown in Table 9.11.

Table 9.11 Exercising nDMS_LED Output Pin

ITEM #	PROCEDURE	DESCRIPTION
1	Deassert the DMS_DISABLE bit.	During normal boot procedure, the 8051 has asserted the DMS_DISABLE bit before the DMS overflow state has occurred. The DMS_TEST bit must remain deasserted.

Table 9.11 Exercising nDMS_LED Output Pin (continued)

ITEM #	PROCEDURE	DESCRIPTION
2	Wait for the DMS_OVERFLOW bit to be asserted.	When the DMS_DISABLE bit is deasserted, the DMS counter will resume until overflow. When the DMS_OVERFLOW bit is asserted, the nDMS_LED output pin should begin pulsing as shown in Figure 9.11.
3	Assert the DMS_DISABLE bit.	Permanently disable the DMS counter. Provide some means to signal the end of the nDMS_LED test.
4	Assert the DMS_TEST bit.	When the nDMS_LED test is complete, the nDMS_LED output pin is permanently deasserted when the DMS_TEST bit is asserted.
5	Deassert the DMS_OVERFLOW bit.	Remove indication that the DMS overflow state has been reached.

9.9.4.3 DMS_DISABLE Bit – D0

The DMS_DISABLE bit D0 is used to permanently stop the DMS counter (Figure 9.10). When the DMS_DISABLE bit is deasserted ‘0’ (default), the DMS counter is enabled and will begin counting until the DMS overflow state is reached, assuming the DMS_TEST bit and the 8051_RESET signal are deasserted. When the DMS_DISABLE bit is asserted ‘1’, the DMS counter is permanently disabled. The DMS_DISABLE bit can be used along with the DMS_TEST bit to exercise the nDMS_LED output pin (see Section 9.9.4.2, "DMS_TEST Bit – D1" above).

9.10 Flash Program Register

The Flash Program register contains the Flash Program Interface Decoder controls (see Section 9.2, "Flash Program Interface Decoder") and the RESET FLASH control.

The Flash Program register is shown in Table 9.12. The Flash Program register is always available to the LPC Host and to the 8051.

Table 9.12 Flash Program Register

HOST ADDRESS	MBX9Eh
8051 ADDRESS	0x7F35
POWER	VCC1
DEFAULT	‘000XXX00’b

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R/W	R	R	R	R	R	R/W	R/W
8051 R/W	R/W	R	R	R	R	R	R/W	R/W
BIT NAME	RESET FLASH	Reserved		FWP PIN	EXT FLASH	ATE PGM	LPC PGM	8051 PGM

9.10.1 RESET FLASH – D7

The RESET FLASH bit can reset the internal 64k Embedded Flash ROM (see Section 8.3.3, "Reset"). When the RESET FLASH bit is asserted ‘1’, the 64k Embedded Flash ROM is placed in a reset state. When the RESET FLASH bit is de-asserted ‘0’ (default), the 64k Embedded Flash ROM is placed in Read Array mode.

Note: The RESET FLASH bit is not self-clearing.

9.10.2 FWP – D4

The FWP Pin bit reflects the status of the nFWP input pin. When nFWP is asserted (‘0’), the boot block in the LPC47N350 Embedded 64K Flash ROM is write-protected and the FWP Pin bit is asserted ‘1’. When the nFWP pin is deasserted (‘1’), the boot block is writeable and the FWP Pin bit is deasserted ‘0’.

Note: The EXT FLASH bit is read-only and not affected by VCC1 POR.

9.10.3 EXT FLASH – D3

The EXT FLASH bit in the Flash Program register indicates the state of the LPC47N350 nEA pin. When the nEA pin is asserted ‘0’, the EXT FLASH bit is asserted ‘1’, when the nEA pin is deasserted ‘1’, the EXT FLASH bit is deasserted ‘0’. When the EXT FLASH bit is asserted (‘1’), the LPC47N350 Flash programming interface is disabled (see Table 9.1).

9.10.4 ATE PGM – D2

The ATE PGM bit in the Flash Program register directly reflects the state of the LPC47N350 PGM pin. When the PGM pin is asserted, the ATE PGM bit is asserted, when the PGM pin is deasserted, the ATE PGM bit is deasserted. When the ATE PGM bit is asserted (‘1’), the LPC47N350 Flash programming interface is dedicated to the ATE Flash Program Access function (see Table 9.1 and Section 9.6, "ATE Flash Program Access" above).

Note: The ATE PGM bit is read-only and not affected by VCC1 POR.

9.10.5 LPC PGM – D1

The LPC PGM bit in the Flash Program register is used to enable the LPC Flash Program Access function (see Table 9.1 and Section 9.5, "LPC Bus Flash Program Access", above). The LPC PGM bit can only be asserted when the ATE PGM and the 8051 PGM bits are deasserted ‘0’ (Table 9.1), and the SYSTEM FLASH bit in the Disable register is deasserted. When the LPC PGM bit is asserted ‘1’, the LPC47N350 64k Embedded Flash is dedicated to the LPC Host programming interface. The LPC PGM bit is read/write and deasserted by VCC1 POR.

9.10.6 8051 PGM – D0

The 8051 PGM bit in the Flash Program register is used to enable the 8051 Program Access function (see Table 9.1 and Section 9.3, "8051 Code Fetch Access" above). The 8051 PGM bit can only be asserted when the ATE PGM bit is deasserted ‘0’; the 8051 PGM bit overrides the LPC PGM bit (Table 9.1).

When the 8051 PGM bit is asserted ‘1’, the 64k Embedded Flash is dedicated to the 8051 programming interface. The 8051 PGM bit is read/write and deasserted by VCC1 POR.

9.10.7 8051/LPC Flash Program Access Registers

The 8051/LPC Flash Program Access registers are used by the 8051 and the LPC Host to program the LPC47N350 64k Embedded Flash (see Figure 9.2 on page 110). To the 8051, the 8051/LPC Flash Program Access registers are accessed using memory-mapped control registers; to the LPC host, the 8051/LPC Flash Program Access registers are accessed using the Mailbox Registers Interface. For

information regarding the 8051 and LPC Flash Program Access functions, see Section 9.4, "8051 Flash Program Access" and Section 9.5, "LPC Bus Flash Program Access". The 8051 and LPC Flash Program Access functions are enabled by the Flash Program Interface Decoder (see Section 9.2, "Flash Program Interface Decoder").

When the 8051 is using the 8051/LPC Flash Program Access interface, LPC Host access is disabled. The LPC Host will be able to read the contents of the 8051/LPC Flash Program Access registers, but it will not be able to write these registers and reads to the Flash Data register will return the contents of the Flash Data register but will not read-activate the Flash CSI interface.

When the LPC Host is using the 8051/LPC Flash Program Access interface, 8051 access is disabled. Typically, when LPC Host is using the 8051/LPC Flash Program Access interface the 8051 is stopped.

Note: The LPC Host must stop the 8051 to use the 8051/LPC Flash Program Access interface.

9.10.8 Flash High Address Register

The Flash High Address register contains Flash address bits A15 – A8 (Table 9.13). The LPC Host can access the Flash High Address register using the Mailbox Registers Interface address 0x9F. The 8051 can access the Flash High Address register using MMCR address 0x7FB0.

Note: To properly access the LPC47N350 64k Embedded Flash, the Flash High Address and the Flash Low Address registers must be initialized before reading or writing the Flash Data register.

Table 9.13 Flash High Address Register

HOST ADDRESS	MBX9Fh
8051 ADDRESS	0x7FB0
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	A15	A14	A13	A12	A11	A10	A9	A8

9.10.9 Flash Low Address Register

The Flash Low Address register contains Flash address bits A7 – A0 (Table 9.14). The LPC Host can access the Flash Low Address register using the Mailbox Registers Interface address 0x80. The 8051 can access the Flash Low Address register using MMCR address 0x7FB1.

Note: To properly access the LPC47N350 64k Embedded Flash, the Flash High Address and the Flash Low Address registers must be initialized before reading or writing the Flash Data register.

Table 9.14 Flash Low Address Register

HOST ADDRESS	MBX80h
8051 ADDRESS	0x7FB1
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	A7	A6	A5	A4	A3	A2	A1	A0

9.10.10 Flash Data Register

The Flash Data register contains either the LPC47N350 64k Embedded Flash data, CSI command-codes, or the contents of the CSI Status register (Table 9.15). The LPC Host can access the Flash Data register using the Mailbox Register Interface address 0x81. The 8051 can access the Flash Data register using MMCR address 0x7FB2.

Note: To properly access the LPC47N350 64k Embedded Flash, the Flash High Address and the Flash Low Address registers must be initialized before reading or writing the Flash Data register.

Table 9.15 Flash Data Register

HOST ADDRESS	MBX81h
8051 ADDRESS	0x7FB2
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0

9.11 Scratch ROM

The LPC47N350 8051 can execute program code from a 512-byte Scratch ROM when the MMC bit is '1'. The MMC bit is D3 in CONFIGURATION REGISTER 0 (MMCR 0x7FF4). The Configuration Register 0 register is described in Section 7.8.3.4, "Configuration Register").

When the MMC bit is '1', the 8051 can execute out of the Scratch ROM either when the 8051 Code Fetch Access interface or when the 8051 Program Access interface is selected. For example, the 8051 can execute code from the Scratch ROM even when the 8051 Code Fetch Interface is unselected by the Flash Program Interface Decoder (see Section 9.2, "Flash Program Interface Decoder" above). When the MMC bit = '0', there is 512 bytes of Scratch RAM located at address 0x7B00 in the 8051 Data Space (Figure 9.12). When the MMC bit is '1', the Scratch RAM becomes Scratch ROM and occupies 512 bytes at the top of the 64k code space; i.e., FE00h – FFFFh (Figure 9.13).

Note: When the 8051 is running from external flash, i.e. when the nEA pin = '0', the MMC bit must be '0'.

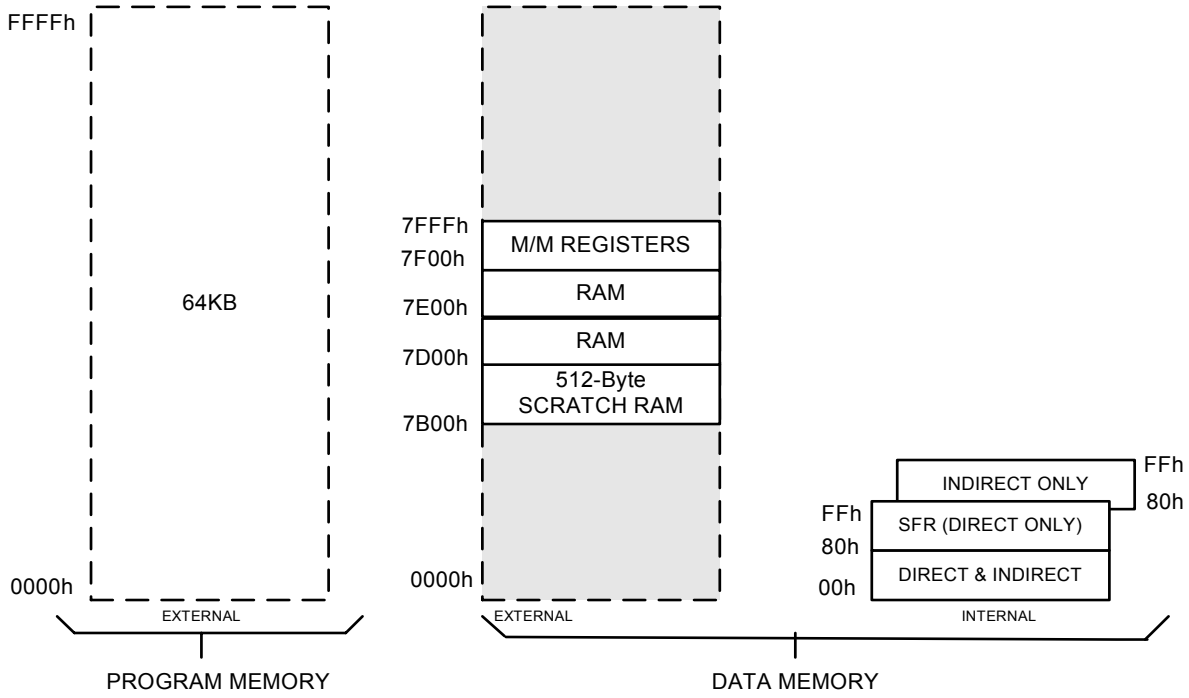


Figure 9.12 LPC47N350 Memory Map with Scratch RAM (MMC BIT = '0')

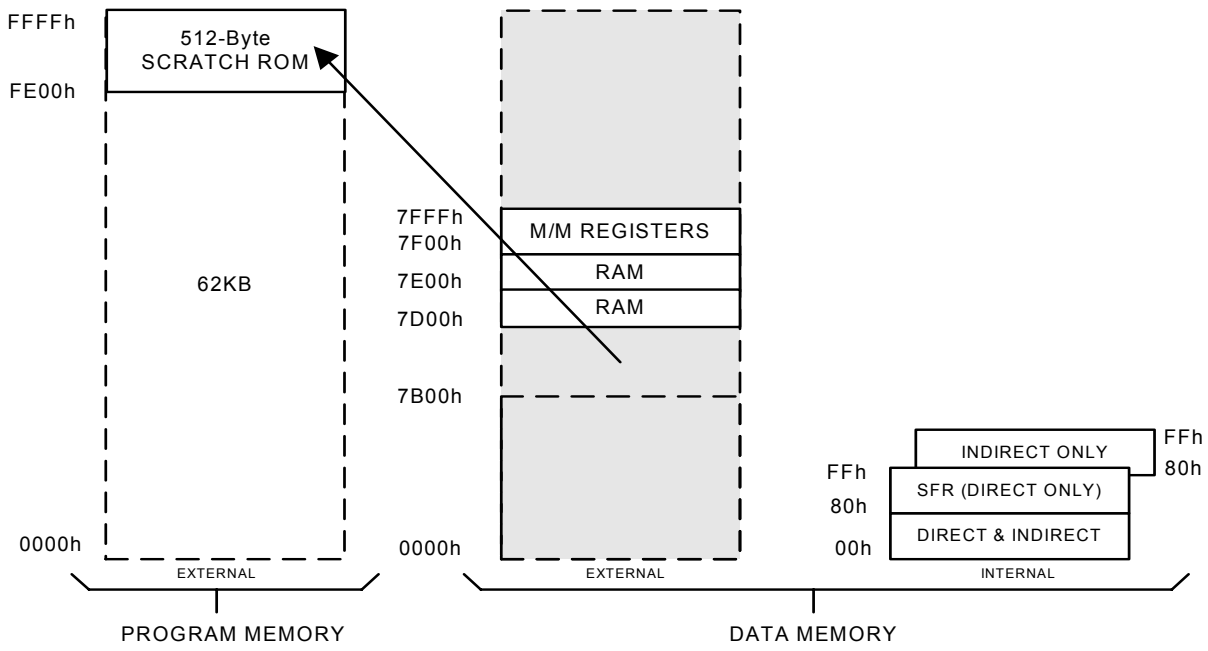


Figure 9.13 LPC47N350 Memory Map with Scratch ROM (MMC BIT = '1')

Chapter 10 Hot Plug LPC Docking Interface

10.1 Overview

A switchable LPC interface is available to be supplied to an external Super I/O device contained within a docking station. See Figure 10.1.

The Docking LPC bus signals, when enabled, will be routed through low impedance (10Ω), bi-directional switches contained in the LPC47N350.

The LPC47N350 controls the enabling of the LPC docking interface.

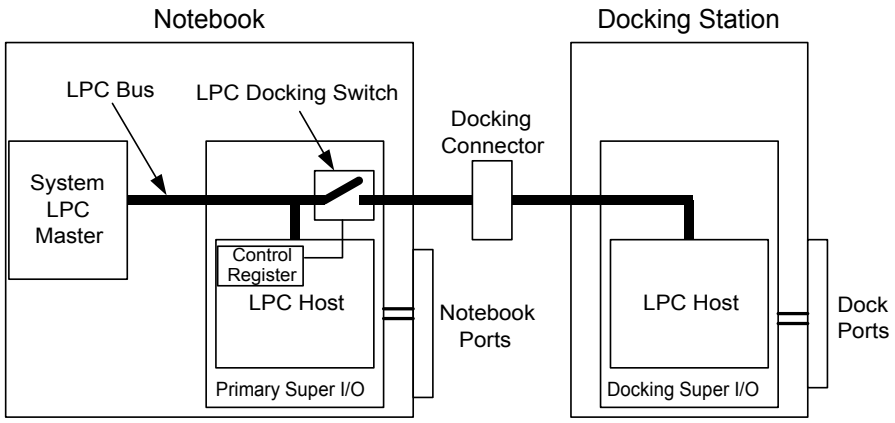


Figure 10.1 Switched LPC Architecture

10.2 Interface

The signals to be switched in the LPC Docking interface are shown in Table 10.1. All signals are 3.3V only. LPCPD#, LRESET#, and PCICLK signals will be routed externally.

Table 10.1 Switched LPC Bus Signals

1)	DLAD[0]
2)	DLAD[1]
3)	DLAD[2]
4)	DLAD[3]
5)	DLFRAME#
6)	DCLKRUN#
7)	DSER_IRQ
8)	DLDRQ#
9)	LDRQ# (See Note)

Note: LDRQ# is not part of the docking interface. DLDRQ# is an input from the docking interface and LDRQ# is an output from LPC47N350.

10.3 Docking Procedure

The switching for the Docking LPC interface Docking is controlled by the DLPC SWITCH bit in the Docking LPC Switch Register described in Section 10.4.2, "Docking LPC Switch Register" below.

When a docking event is detected, the system writes a value of 01h to the Docking LPC Switch Register connecting the LPC interface to the Docking LPC interface.

The Docking Super I/O will be accessible as any typical LPC device on the LPC bus.

10.4 Registers

10.4.1 Docking LPC Logical Device C Configuration Registers

Table 10.2 Logical Device C Configuration Registers

INDEX	TYPE	HARD RESET	VCC1 POR	SOFT RESET	CONFIGURATION REGISTER
0x30	R/W	0x00	-	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	-	0x00, 0x00	DLPC Runtime Registers Base I/O Address. Valid addresses are 0100h – 0FFFh

10.4.1.1 Docking LPC Interface Logical Device C Activate Bit

The DLPC Activate Bit (Logical Device C 0x30[0]) powers up in the deasserted (‘0’) state.

When the DLPC device is deactivated (Activate Bit = 0), the LPC47N350 LPC Host cannot decode the Docking LPC Switch register and therefore cannot activate the DLPC switches.

10.4.2 Docking LPC Switch Register

The Docking LPC Switch Register controls the connection and disconnection of the Docking LPC Interface.

Table 10.3 Docking LPC Switch Register

HOST ADDRESS	DLPC Runtime Registers Base Address + 0
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	00h

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R	R	R	R/W
8051 R/W	-	-	-	-	-	-	-	-
BIT NAME	Reserved							DLPC SWITCH

DLPC_SWITCH – D0

When DLPC SWITCH is asserted ‘1’, the bidirectional Docking LPC switches will be switched on and the DLPC pin connections will be connected to the LPC bus. When DLPC SWITCH is deasserted ‘0’, the DLPC pin connections will be disconnected from the LPC bus.

Chapter 11 Watch Dog Timer

11.1 WDT Operation

When enabled, the Watch Dog Timer (WDT) circuit will generate a system reset if the user program fails to reload the watchdog timer (WDT) within a specified length of time known as the 'watchdog interval'.

The WDT consists of an 8-bit timer (WDT) with a 9-bit prescaler. The prescaler is fed with 32 KHz which always runs, even if the 8051 is in SLEEP state. The 8 bit WDT timer is decremented every (1/32KHz) *512 seconds or 16.0 ms. Thus, the watchdog interval is programmable between 16ms and 4.08 seconds on 16ms intervals.

11.2 WDT Action

If the 8 bit timer (WDT) underflows, a VCC1 POR is generated.

8051 in Idle Mode - WDT will be active if enabled. When the WDT timer underflows in idle mode, the 8051 will be reset. It is up to the firmware engineer to design code that uses a timer to generate an interrupt that will exit idle mode and re-initialize the WDT timer and then put the 8051 back into idle mode.

8051 in Sleep Mode - If enabled, the WDT is active since it is running off of the 32 KHz clock. Therefore, if the WDT is enabled, the 8051 should never remain in the SLEEP state for more than 4 seconds.

11.3 WDT Activation

Upon VCC1 POR, the Watch Dog Timer powers up inactive. The Watch Dog Timer is activated when the WDT enable bit (WDT CONTROL bit D1) is set by 8051 firmware. The WDT may be disabled under software control through a specific sequence. Software can clear the SDT enable bit by:

- Setting the WLE (WDT Load enable) bit in the WDT Control/Status Register.
- Writing 00h to the WDT Timer Register (this causes the WDT Enable and the WLE bits to each reset to 0).

Once the WDT has been activated, this sequence must be executed in order to disable watchdog operation via software control.

Note: Since a VCC1 POR will reset the WDT enable bit, the WDT must be re-enabled after each occurrence.

11.4 WDT Reset Mechanism

The watchdog timer (WDT) must be reloaded within periods that are shorter than the programmed watchdog interval; otherwise the WDT will underflow and a VCC1 POR will be generated. It is the responsibility of the user program to continually execute sections of code which reload the 8 bit timer (WDT).

The WDT is reloaded in two stages in order to prevent erroneous software from reloading the watchdog. First, bit D0 (WLE) in the WDT CONTROL register must be set. Then, the WDT may be loaded. When the WDT is loaded, WLE is automatically reset. WDT can not be loaded when WLE is reset. Since the WDT timer is a down counter, a reload value of 01h results in the minimum WDT interval (16ms) and a reload value of 0FFh results in the maximum WDT interval (4.08 seconds). Loading 00h into the WDT disables the WDT and clears the WDT_EN bit.

Note: The 9 bit prescaler is initialized whenever the WDT timer is loaded.

11.5 WDT Memory Mapped Registers

Table 11.1 WDT

HOST ADDRESS	N/A
8051 ADDRESS	0x 7F38
POWER	VCC1
DEFAULT	0xFF

	D7	D6	D5	D4	D3	D2	D1	D0
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SYSTEM R/W	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
BIT DEF	WDT Timer							

Table 11.2 WDT Control/Status

HOST ADDRESS	N/A
8051 ADDRESS	0x 7F37
POWER	VCC1
DEFAULT	0x00

	D7-D2	D1	D0
8051 R/W	R	R/W	R/W
SYSTEM R/W	N/A	N/A	N/A
BIT DEF	Reserved	WDT Enable	WLE

WLE (WDT Load Enable)

Watchdog Load Enable bit must be set to enable writing to the WDT Timer register. This bit is automatically reset when the 8051 writes to the WDT register. If this bit is reset, writes to the WDT register are ignored.

WDT_EN

The WDT enable bit must be set by 8051 firmware to enable or start the Watch Dog Timer. A VCC1 POR or the above described software sequence will reset this bit.

See Section 11.3, "WDT Activation" AND Section 11.4, "WDT Reset Mechanism" for description of WDT_EN and WLE bits.

Chapter 12 8051 System Power Management

The High-Performance 8051 core provides support for two further power-saving modes, available when inactive: idle mode, typically entered between keystrokes; and sleep mode, entered upon command from the host. The High Performance 8051 is wakeable from sleep mode through a set of external and internal events called Wake-Up events. The events are listed in Table 12.1. When exiting the Sleep mode, the High Performance 8051 will continue executing code from where it left off when put into sleep with no changes to the SFR and pins.

The LPC47N350 is fully static and will pickup from where it left off in the event of a wake-up event.

12.1 Idle Mode

Entering IDLE mode: Idle mode is initiated by an instruction that sets the PCON.0 bit (SFR address 87H) in the keyboard. In idle mode, the internal clock signal to the keyboard CPU is gated off, but not to the Interrupt Timer and Serial Port functions. The CPU status is preserved in its entirety: The Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data. The port pins hold the logical levels they had when Idle mode was activated.

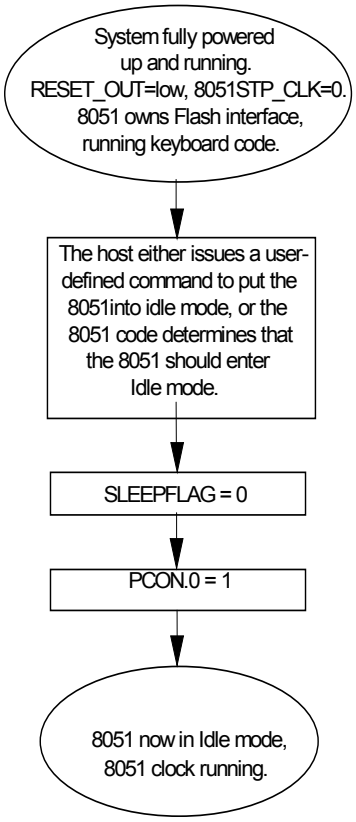


Figure 12.1 Entering Idle Mode

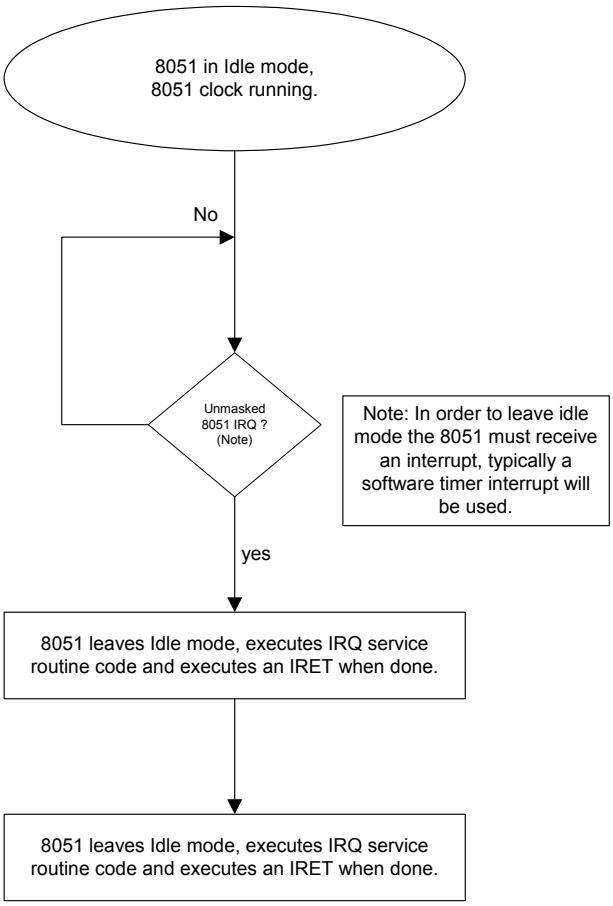


Figure 12.2 Exiting Idle Mode Due to IRQ

12.1.1 Exiting Idle Mode

There are two ways to terminate Idle mode. First, activation of any enabled interrupt will cause the PCON.0 bit to be cleared by hardware. The interrupt will be serviced and, following the RETI, the CPU will resume operation by executing the instruction following the one that put the CPU into Idle mode.

The second way to terminate the idle mode is with a VCC1 POR. Note that a VCC1 POR will clear the registers. The CPU will not resume program execution from where it left off.

12.2 Sleep Mode

When the CPU enters sleep mode, all internal clocks, including the core clocks, are turned off. If an external crystal is used, the internal oscillator is turned off. RAM contents are preserved. Sleep mode is initiated by a user defined 8051 command sequence.

Sleep Mode Sequence - To enter sleep mode, the 8051:

1. Turns on the ring oscillator (KSTP_CLK[4] = 1)
2. Switches the clock source (KSTP_CLK[5] = 0)
3. Turns off the clock chip (or the whole system power, VCC2)
4. Masks all interrupts except for INT5_h
5. Sets SLEEPFLAG = 1
6. Sets PCON.0 = 1

7. The ring oscillator will be automatically turned off
8. The 8051 goes into Sleep mode.

In sleep mode, the UART is powered off if VCC2 is removed, but the RTC and 8051 are in powerdown (sleep) mode. In Sleep mode, the LPC47N350 consumes less than 20μA, and all wake-up pins are still active.

When the 8051 is in sleep mode, all of the clocks are stopped and the 8051 is waiting for an unmasked wake-up event. When the wake-up event occurs, the ring oscillator is started and the 8051 starts executing from where it stopped in the sleep Mode Sequence. Once running, the 8051 can access all of the registers that are on VCC1 and if VCC2 is at 3.3V, it can access all of the registers on VCC2. The 8051 that was running off the ring oscillator (internal) clock source switches to an external clock source, and then turns off the ring oscillator (internal) clock source.

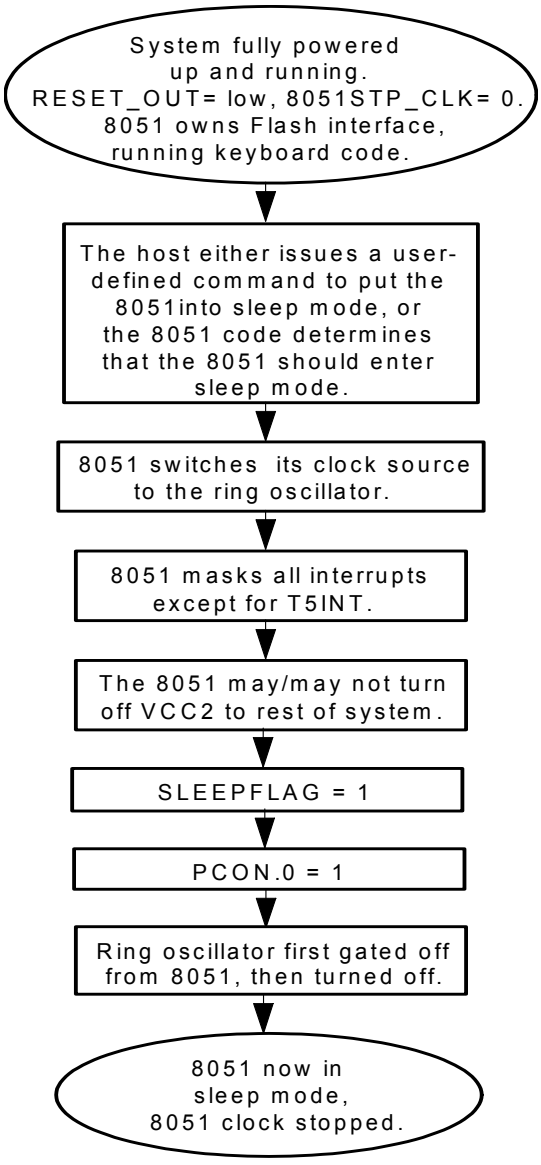


Figure 12.3 Entering Sleep Mode

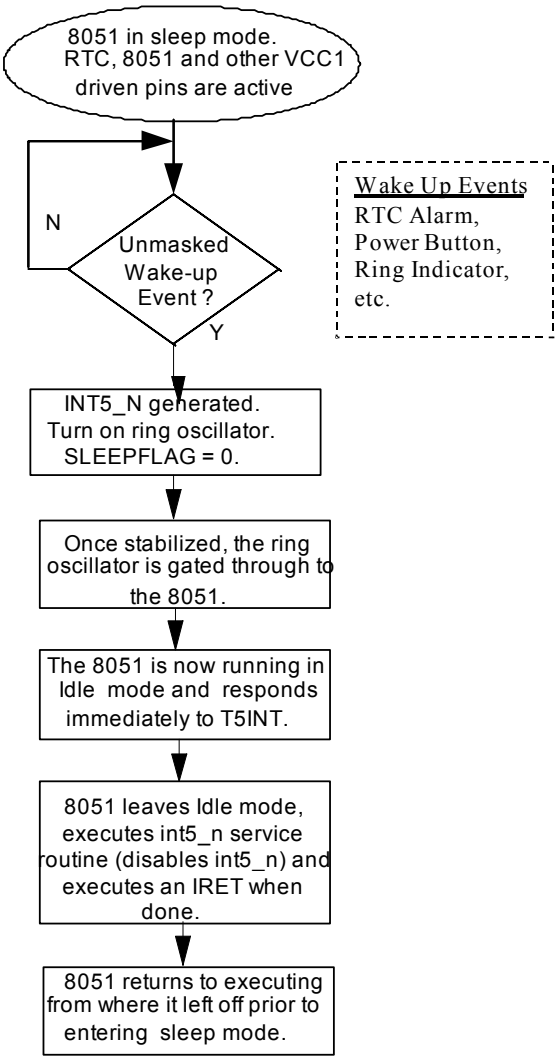


Figure 12.4 Exiting Sleep Mode

12.3 Wake-Up Events

There are two types of wake-up events that can occur, internal (Table 12.1, "Internal System Wake-Up Events") and external (Table 12.2, "External System Wake-Up Events"). Wake-up events on General Purpose Pins can be either edge or selectable edges. Refer to Table 12.1 for further description. Wake-up events can occur when VCC2 is off. VCC1 must be on for a wake-up event to occur, but the high-performance 8051 can be in sleep mode.

Table 12.1 Internal System Wake-Up Events

WAKE-UP EVENTS	REGISTER	DESCRIPTION
RTC_ALRM	Wake Up Src 1 (0x7F2B) [D0]	RTC alarm
HTIMER	Wake Up Src 2 (0x7F2B) [D2]	Hibernation timer
PM1_STS2	Wake Up Src 1 (0x7F2A) [D5]	PM1 Status

Table 12.1 Internal System Wake-Up Events (continued)

WAKE-UP EVENTS	REGISTER	DESCRIPTION
PM1_EN2	Wake Up Src 1 (0x7F2A) [D6]	PM1 Enable
PM1_CTL2	Wake Up Src 1 (0x7F2A) [D7]	PM1 Control

Table 12.2 External System Wake-Up Events

PIN	WAKE-UP EVENTS	ACTIVE EDGE	REGISTER	DESCRIPTION
AB1_DATA	ACCBUS1	Leading edge, high-to-low	Wake Up Src1 (0x7F2A) [D4]	AB_DAT I^2C/SMBus 1
AB2_DATA	ACCBUS2		Wake Up Src1 (0x7F2A) [D3]	AB_DAT I^2C/SMBus 2
KSI[7:0]	WK_ANYKEY	Edge, high-to-low	Wake Up Src 2 (0x7F2B) [D1]	Any Keyboard Key pressed
GPIO0	WK_SE02	Programmable	Wake Up Src 4 (0x7F59) [D2]	General Purpose Pin
GPIO1	WK_SE03		Wake Up Src 4 (0x7F59) [D3]	
GPIO2	WK_SE04		Wake Up Src 4 (0x7F59) [D4]	
GPIO3	TRIGGER		INT SRC 1 (0x7F02) [D3]	
GPIO4	WK_SE07		Wake Up Src 4 (0x7F59) [D7]	
GPIO5	WK_SE10		Wake Up Src 5 (0x7F5E) [D0]	
GPIO6	WK_SE11		Wake Up Src 5 (0x7F5E) [D1]	
GPIO7	WK_SE06		Wake Up Src 4 (0x7F59) [D6]	
GPIO8	WK_SE12		Wake Up Src 5 (0x7F5E) [D2]	GPIO8 or RXD Receive pin.
GPIO9	WK_SE13		Wake Up Src 5 (0x7F5E) [D3]	General Purpose Pin
GPIO10	WK_SE14		Wake Up Src 5 (0x7F5E) [D4]	
GPIO11	WK_SE15		Wake Up Src5 (0x7F5E) [D5]	GPIO11 or I^2C/SMBus 2 Serial Data
GPIO12	WK_SE16		Wake Up Src5 (0x7F5E) [D6]	GPIO12 or I^2C/SMBus 2 Clock

Table 12.2 External System Wake-Up Events (continued)

PIN	WAKE-UP EVENTS	ACTIVE EDGE	REGISTER	DESCRIPTION
GPIO13	WK_SE17	Programmable	Wake Up Src5 (0x7F5E) [D7]	General Purpose Pin
GPIO14	WK_SE20		Wake Up Src6 (0x7F63) [D0]	
GPIO15	WK_SE21		Wake Up Src6 (0x7F63) [D1]	
GPIO16	WK_SE22		Wake Up Src6 (0x7F63) [D2]	
GPIO17	WK_SE23		Wake Up Src6 (0x7F63) [D3]	
KSO13/GPIO18	WK_SE27		Wake Up Src6 (0x7F63) [D7]	Keyboard Scan Output/General Purpose Pin
GPIO19	WK_SE24		Wake Up Src6 (0x7F63) [D4]	General Purpose Pin
GPIO20/ PS2CLK	WK_SE25		Wake Up Src6 (0x7F63) [D5]	General Purpose Pin/ PS2 Serial Clock
GPIO21/ PS2DAT	WK_SE26		Wake Up Src6 (0x7F63) [D6]	General Purpose Pin/ PS2 Serial Data
FAN_TACH1	TACH1	When the output of the fan pulse counter threshold detector is asserted.	Wake Up Src 7 (0x7F64) [D0]	When the fan speed drops below a predetermined value.
FAN_TACH2	TACH2	When the output of the fan pulse counter threshold detector is asserted.	Wake Up Src 7 (0x7F64) [D1]	When the fan speed drops below a predetermined value.
LGPIO50	LGPIO50	Either Edge	Wake Up Src 8 (0x7F55) [D0]	LPC/8051 addressable GPIOs
LGPIO51	LGPIO51	Either Edge	Wake Up Src 8 (0x7F55) [D1]	
LGPIO52	LGPIO52	Either Edge	Wake Up Src 8 (0x7F55) [D2]	
LGPIO53	LGPIO53	Either Edge	Wake Up Src 8 (0x7F55) [D3]	

Note: All alternate functions of wake-capable GPIO primary function pins can generate wake events. Not all GPIO pins can generate wake events (See Table 20.1, “LPC47N350 GPIO Types,” on page 217).

Chapter 13 Keyboard Controller

13.1 8042 Style Host Interface

The LPC47N350 keyboard controller uses a High-Performance 8051 microcontroller CPU core to produce a superset of the features provided by the industry-standard 8042 keyboard controller. Added features include two high-drive serial interfaces, and additional interrupt sources. The LPC47N350 provides an industry standard 8042-style LPC host interface to the High-Performance 8051 to emulate standard 8042 keyboard controller and preserve software backward compatibility with the system BIOS.

The LPC47N350's LPC keyboard interface is functionally compatible with the 8042-style host interface. The keyboard controller has the KBD (Keyboard) Status register, KBD Data/Command Write register, and KBD Data Read register.

Table 13.1 shows how the has the LPC interface accesses the keyboard controller. In addition to the above signals, the host interface includes keyboard and mouse interrupts.

13.2 Keyboard Controller Register Description

Table 13.1 Keyboard Controller LPC I/O Address Map

HOST ADDRESS	COMMAND	FUNCTION
0x60	Write	Keyboard Data Write (C/D=0)
	Read	Keyboard Data Read
0x64	Write	Keyboard Command Write (C/D=1)
	Read	Keyboard Status Read

Note: These registers consist of three separate 8 bit registers: KBD Status, KBD Data/Command Write and KBD Data Read.

13.2.1 Keyboard Data Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is cleared to zero and the IBF bit is set.

13.2.2 Keyboard Data Read

This is an 8 bit read only register. When read, the PBOBF and/or AUXOBF interrupts are cleared and the OBF flag in the status register is cleared.

13.2.3 Keyboard Command Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is set to one and the IBF bit is set.

13.2.4 Keyboard Status Read

This is an 8 bit read only register. Refer to the description of the Status Register (7FF2H) for more information.

13.2.5 8051-to-Host Keyboard Communication

The 8051 can write to the KBD Data Read register via address 7FF1H and 7FFAH (Aux Host Data Register), respectively. A write to either of these addresses automatically sets bit 0 (OBF) in the Status register. A write to 7FF1H also sets PCOBF. A write to 7FFAH also sets AUXOBF1. See Table 13.2.

Table 13.2 Host-Interface Flags

8051 ADDRESS	FLAG
7FF1H (R/W)	PCOBF (KIRQ) output signal goes high
7FFAH (W)	AUXOBF1 (MIRQ) output signal goes high

Table 13.3 Host I/F Data Register

HOST	0x60
8051	0x7FF1
POWER	VCC1
DEFAULT	N/A

The Input Data register and Output Data register are each 8 bits wide. A write to this 8 bit register by the 8051 will load the Keyboard Data Read Buffer, set the OBF flag, and set the PCOBF output if enabled. A read of this register by the 8051 will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag. Refer to the PCOBF and Status register descriptions for more information.

Table 13.4 Host I/F Command Register

HOST	0x64 (W)
8051	0x7FF1
POWER	VCC1
DEFAULT	N/A

The host CPU sends commands to the keyboard controller by writing command bytes to this register.

Table 13.5 Host I/F Status Register

HOST	0x64 (R)
8051	0x7FF2
POWER	VCC1
DEFAULT	N/A

The Status register is 8 bits wide. Shows the contents of the KBD Status register.

Table 13.6 KBD Status Register

D7	D6	D5	D4	D3	D2	D1	D0
UD	UD	AUXOBF/UD	UD	C/D	UD	IBF	OBF

This register is read-only for the Host and read/write by the 8051. The 8051 cannot write to bits 0, 1, or 3 of the Status register.

UD

Read/Writeable by 8051. These bits are user-definable.

C/D

Command Data - This bit specifies whether the input data register contains data or a command (“0” = data, “1” = command). During a host data/command write operation, this bit is set to "1" if SA2 = “1” or reset to "0" if SA2 = 0.

IBF

Input Buffer Full - This flag is set to “1” whenever the host system writes data into the input data register. Setting this flag activates the 8051's nIBF interrupt if enabled. When the 8051 reads the input data register, this bit is automatically reset and the interrupt is cleared. There is no output pin associated with this internal signal.

OBF

Output Buffer Full - This flag is set to “1” whenever the 8051 writes into the data registers at 7FF1H or 7FFAH. When the host system reads the output data register, this bit is automatically reset.

AUXOBF

Auxiliary Output Buffer Full - This flag is set to “1” whenever the 8051 writes into the data registers at 7FFAH. This flag is reset to “0” whenever the 8051 writes into the data registers at 7FF1H.

Table 13.7 PCOBF

HOST	N/A
8051	0x7FFD
POWER	VCC1
DEFAULT	0x00

Refer to the PCOBF description for information on this register. This is a “1” bit register (bits 1-7=0 on read)

13.3 Host-to 8051 Keyboard Communication

The host system can send both commands and data to the KBD Data/Command Write register. The CPU differentiates between commands and data by reading the value of bit 3 of the Status register. When bit 3 is "1", the CPU interprets the register contents as a command. When Bit 3 is "0", the CPU interprets the register contents as data. During a host write operation, bit 3 is set to "1" if SA2 = 1 or reset to "0" if SA2 = 0.

13.3.1 PCOBF Description

(The following description assumes that OBFEN = 1 in Configuration Register 0); PCOBF is gated onto KIRQ. The KIRQ signal is a system interrupt which signifies that the 8051 has written to the KBD Data Read register via address 7FF1H. On power-up, PCOBF is reset to 0. PCOBF will normally reflect the status of writes to 7FF1H, if PCOBFEN (bit 2 of Configuration register “0”) = “0”. (KIRQ is normally selected as IRQ1 for keyboard support). PCOBF is cleared by hardware on a read of the Host Data Register.

Additional flexibility has been added which allows firmware to directly control the PCOBF output signal, independent of data transfers to the host-interface data output register. This feature allows the LPC47N350 to be operated via the host "polled" mode. This firmware control is active when PCOBFEN = 1 and firmware can then bring PCOBF high by writing a "1" to the LSB of the 1 bit data register, PCOBF, allocated at 7FFDH. The firmware must also clear this bit by writing a "0" to the LSB of the 1 bit data register at 7FFDH.

The PCOBF register is also readable; bits 1-7 will return a "0" on the read back. The value read back on bit 0 of the register always reflects the present value of the PCOBF output. If PCOBFEN = 1, then this value reflects the output of the firmware latch at 7FFDH. If PCOBFEN = 0, then the value read back reflects the in-process status of write cycles to 7FF1H (i.e., if the value read back is high, the host interface output data register has just been written to). If OBFEN=0, then KIRQ is driven inactive (low).

13.3.2 AUXOBF1 Description

(The following description assumes that OBFEN = 1 in Configuration Register 0); This bit is multiplexed onto MIRQ. The AUXOBF1/MIRQ signal is a system interrupt which signifies that the 8051 has written to the output data register via address 7FFAH.

On power-up, after VCC1 POR, AUXOBF1 is reset to 0. AUXOBF1 will normally reflects the status of writes to 7FFAH. (MIRQ is normally selected as IRQ12 for mouse support). AUXOBF1 is cleared by hardware on a read of the Host Data Register. If OBFEN=0, then KIRQ is driven inactive (low).

Table 13.8 Status and Interrupt Behavior of Writing to Output Data Register

	HOST I/F STATUS REGISTER BITS			
Write to Register	AUXOBF (D5)	OBF (D0)	OBFEN=0	OBFEN=1
7FF1	0	1	KIRQ=0	KIRQ=1
7FFA	1	1	MIRQ=0	MIRQ=1

Table 13.9 OBFEN and PCOBFEN Effects on KIRQ

OBFEN	PCOBFEN	
0	X	KIRQ is inactive and driven low
1	0	KIRQ = PCOBF@7FF1
	1	KIRQ = PCOBF@7FFD

Table 13.10 OBFEN and AUX Effects on MIRQ

OBFEN	AUXH	
0	X	MIRQ is inactive and driven low
1	0	MIRQ = PCOBF@7FFA; Status Register D5 = User Defined
	1	MIRQ = PCOBF@7FFA; Status Register D5 = Hardware Controlled

13.3.2.1 8051 AUXOBF1 Control Register

Table 13.11 AUX Host Data Register

HOST	0x60
8051	0x7FFA
POWER	VCC1
DEFAULT	N/A

Refer to the AUXOBF1 description for information on this register.

13.4 GATEA20 Hardware Speed-Up

GATEA20 is multiplexed onto GPIO17 using MISC6. The LPC47N350 contains on-chip logic support for the GATEA20 hardware speed-up feature. GATEA20 is part of the control required to mask address line A20 to emulate 8086 addressing.

In addition to the ability for the host to control the GATEA20 output signal directly, a configuration bit called "SAEN" (Software Assist Enable, bit 1 of Configuration register 0) is provided; when set, SAEN allows firmware to control the GATEA20 output.

When SAEN is set, a 1-bit register assigned to address 7FFBH controls the GATEA20 output. The register bit allocation is shown in Table 13.12.

Table 13.12 Register Bit Allocation

D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	x	x	x	GATEA20

Writing a "0" into location D0 causes the GATEA20 output to go low, and vice versa. When the register at location 7FFBH is read, all unused bits (D7-D1) are read back as "0".

Host control and firmware control of GATEA20 affect two separate register elements. Read back of GATEA20 through the use of 7FFBH reflects the present state of the GATEA20 output signal: if SAEN is set, the value read back corresponds to the last firmware-initiated control of GATEA20; if SAEN is reset, the value read back corresponds to the last host-initiated control of GATEA20.

Host control of the GATEA20 output is provided by the hardware interpretation of the "GATEA20 sequence" (see Table 13.13). The foregoing description assumes that the SAEN configuration bit is reset.

When the LPC47N350 receives a "D1" command followed by data (via the host interface), the on-chip hardware copies the value of data bit 1 in the received data field to the GATEA20 host latch. At no time during this host-interface transaction will PCOBF or the IBF flag (bit 1) in the Status register be activated; i.e., this host control of GATEA20 is transparent to firmware, with no consequent degradation of overall system performance. Table 13.13 details the possible GATEA20 sequences and the LPC47N350 responses.

On VCC1 POR, GATEA20 will be set.

An additional level of control flexibility is offered via a memory-mapped synchronous set and reset capability. Any data written to 7FFEH causes the GATEA20 host latch to be set; any data written to 7FFFH causes it to be reset. This control mechanism should be used with caution. It was added to augment the "normal" control flow as described above, not to replace it. Since the host and the firmware have asynchronous control capability of the host latch via this mechanism, a potential conflict could arise. Therefore, after using the 7FFEH and 7FFFH addresses, firmware should read back the GATEA20 status via 7FFBH (with SAEN = 0) to confirm the actual GATEA20 response.

Table 13.13 GATEA20 Command/Data Sequence Examples

SA2	R/W	D[0:7]	IBF FLAG	GATEA20	COMMENTS
1 0 1	W W W	D1 DF FF	0 0 0	Q 1 1	GATEA20 Turn-on Sequence
1 0 1	W W W	D1 DD FF	0 0 0	Q 0 0	GATEA20 Turn-off Sequence

Table 13.13 GATEA20 Command/Data Sequence Examples (continued)

SA2	R/W	D[0:7]	IBF FLAG	GATEA20	COMMENTS
1 1 0 1	W W W W	D1 D1 DF FF	0 0 0 0	Q Q 1 1	GATEA20 Turn-on Sequence(*)
1 1 0 1	W W W W	D1 D1 DD FF	0 0 0 0	Q Q 0 0	GATEA20 Turn-off Sequence(*)
1 1 1	W W W	D1 XX** FF	0 1 1	Q Q Q	Invalid Sequence

Notes:

- All examples assume that the SAEN configuration bit is 0.
- "Q" indicates the bit remains set at the previous state.
- *Not a standard sequence.
- **XX = Anything except D1.

If multiple data bytes, set IBF and wait at state 0. Let the software know something unusual happened.

For data bytes SA2=0, only D[1] is used; all other bits are don't care.

13.4.1 8051 GATEA20 Control Registers

Table 13.14 GATEA20

HOST	N/A
8051	0x7FFB
POWER	VCC1
DEFAULT	0x01

Refer to the GATEA20 Hardware Speed-up description for information on this register. This is a one bit register (Bits 1-7=0 on read)

Table 13.15 SETGA20L

HOST	N/A
8051	0x7FFE (W)
POWER	VCC1
DEFAULT	N/A

Refer to the GATEA20 Hardware Speed-up description for information on this register. A write to this register sets GateA20.

Table 13.16 RSTGA20L

HOST	N/A
8051	0x7FFF (W)
POWER	VCC1
DEFAULT	N/A

Refer to the GATEA20 Hardware Speed-up description for information on this register. A write to this register resets GateA20.

GateA20 Logic

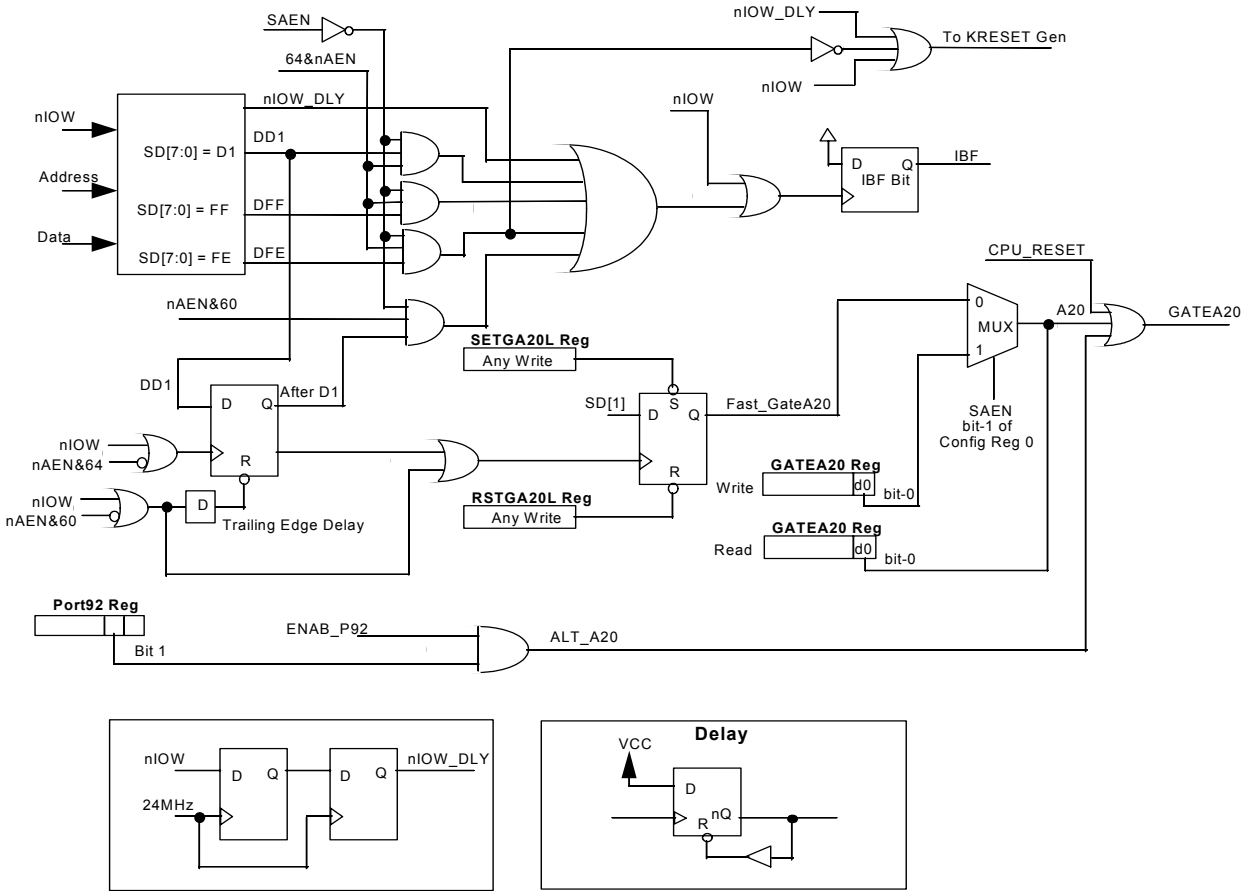


Figure 13.1 GATEA20 Implementation Diagram

13.4.2 CPU_RESET Hardware Speed-Up

The ALT_CPU_RESET bit generates, under program control, the nALT_RST signal, which provides an alternate, means to drive the LPC47N350 CPU_RESET pin which in turn is used to reset the Host CPU. The nALT_RST signal is internally NANDed together with the nKBDRESET pulse from the KRESET Speed up logic to provide an alternate software means of resetting the host CPU. Note: before another nALT_RST pulse can be generated, ALT_CPU_RESET must be cleared to “0” either by a system reset (nRESET_OUT asserted) or by a write to the Port92 register with bit 0 = “0”. A nALT_RST pulse is not generated in the event that the ALT_CPU_RESET bit is cleared and set before the prior nALT_RESET pulse has completed.

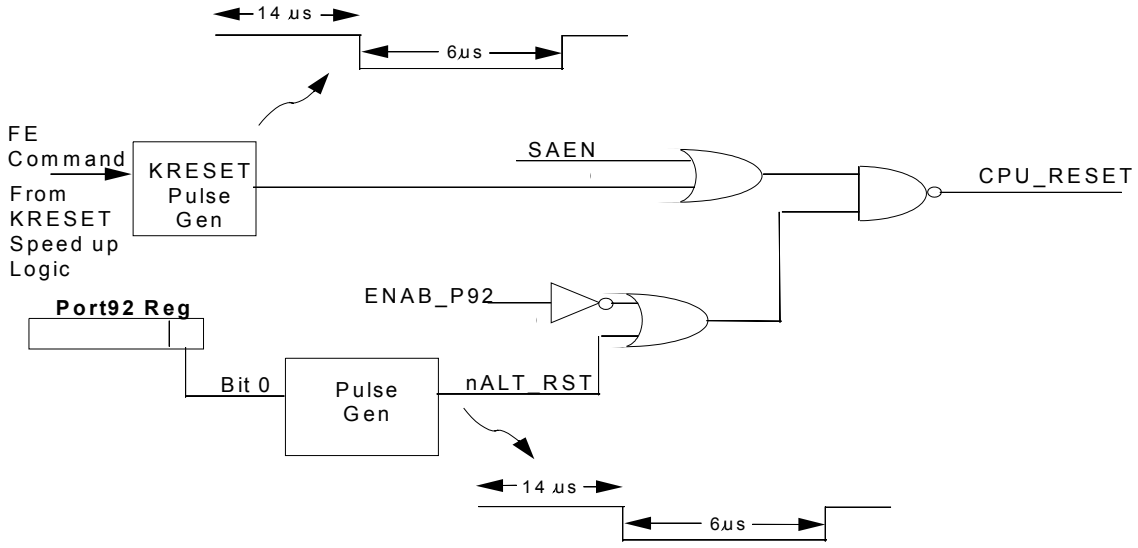


Figure 13.2 CPU_Reset Implementation Diagram

13.4.3 Port 92

The LPC47N350 supports LPC I/O writes to port 92h as a quick alternate mechanism for generating a CPU_RESET pulse or controlling the state of GATEA20.

Port 92 Register Description

	D7-D2	D1	D0
HOST R/W	R/W	R/W	R/W
BIT DEF	0 Reserved	ALT_GATEA20	ALT_CPU_RESET

The Port92h register resides at host address 0x92 and is used to support the alternate reset (nALT_RST) and alternate GATEA20 (ALT_A20) functions. This register defaults to 0x00 on assertion of nRESET_OUT or on VCC2 Power On Reset.

Setting the Port 92 Enable bit (bit 0 of Logical Device 7 Configuration Register 0xF0) enables the Port92h Register. When Port92 is disabled, by clearing the Port 92 Enable bit, then access to this register is completely disabled (I/O writes to host 92h are ignored and I/O reads float the system data bus SD[7:0]).

When Port92h is enabled the bits have the following meaning:

D7-D2 Reserved

A write are ignored and a read return 0.

ALT_GATEA20

This bit provides an alternate means for system control of the LPC47N350 GATEA20 pin.

= 0: ALT_A20 is driven low

= 1: ALT_A20 is driven high

When Port 92 is enabled, writing a 0 to bit 1 of the Port92 Register forces ALT_GATEA20 low. ALT_GATEA20 low drives GATEA20 low, if A20 from the keyboard controller is also low. When Port 92

is enabled, writing a 1 to bit 1 of the Port92 register forces ALT_GATEA20 high. ALT_GATEA20 high drives GATEA20 high regardless of the state of A20 from the keyboard controller.

ALT_CPU_RESET

This bit provides an alternate means to generate a CPU_RESET pulse. The CPU_RESET output provides a means to reset the system CPU to effect a mode switch from Protected Virtual Address Mode to the Real Address Mode. This provides a faster means of reset than is provided through the 8051 keyboard controller. Writing a "1" to this bit will cause the nALT_RST internal signal to pulse (active low) for a minimum of 6μs after a delay of 14μs. Before another nALT_RST pulse can be generated, this bit must be written back to "0".

13.4.4 GATEA20

The hardware GATEA20 state machine returns to state S1 from state S2 when CMD = D1 (Figure 13.3).

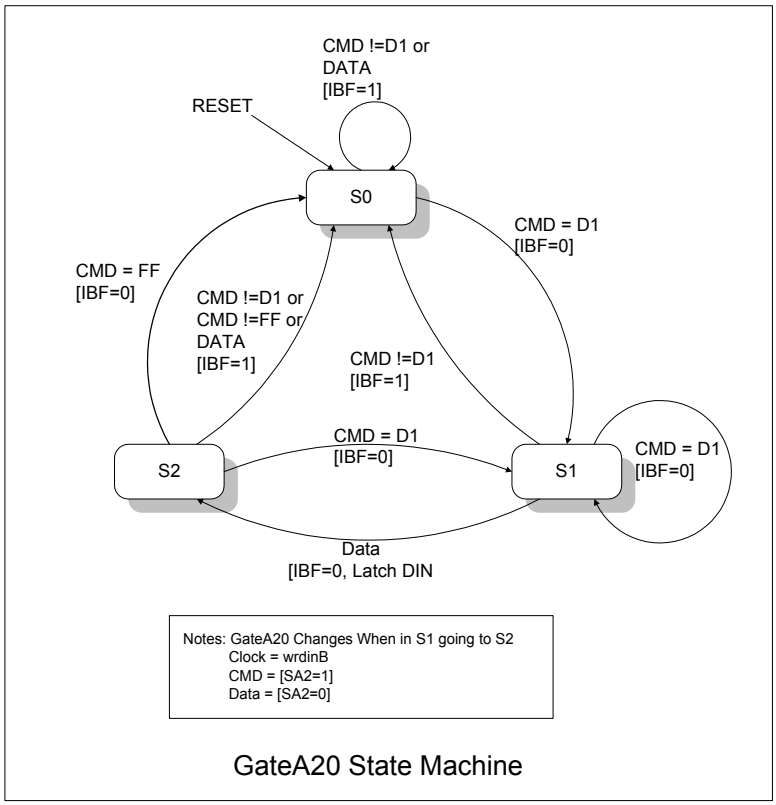


Figure 13.3 GATEA20 State Machine

13.5 Direct Keyboard Scan

The LPC47N350 scanning keyboard controller is designed for intelligent keyboard management in computer applications. By properly configuring GPIO4 and GPIO5, the LPC47N350 may be programmed to directly control keyboard interface matrixes of up to 16x8.

Table 13.17 Keyboard Scan-Out Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F04 (W)
POWER	VCC1
DEFAULT	0x20

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	W	W	W	W	W	W	W	W
BIT NAME	N/A		KSEN	1 = forces all KSO lines to go low	D5 and D4 must be '0' D[3:0] = 0000 KSO[0] is asserted low D[3:0] = 0001 KSO[1] is asserted low D[3:0] = 0010 KSO[2] is asserted low D[3:0] = 0011 KSO[3] is asserted low . . . D[3:0] = 1101 KSO[13] is asserted low D[3:0] = 1110 KSO[14] is asserted low D[3:0] = 1111 KSO[15] is asserted low			

KSEN

1 = disable scanning of internal keyboard (all the KSOUT lines going high) (D4-D0 are don't cares)

0 = enable scanning of internal keyboard

Note: Setting D[3:0] to 111x puts KSO0 - KSO13 outputs as Hi-Z.

Table 13.18 Keyboard Scan-In Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F04 (R)
POWER	VCC1
DEFAULT	N/A

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R	R
BIT NAME	Reflects the state of KSI [7:0]							

The value of the KSI[x] pins can be read through this register.

The pin values are latched during the read.

13.6 External Keyboard and Mouse Interface

Industry-standard PC/AT-compatible keyboards employ a two-wire, bidirectional TTL interface for data transmission. Several sources also supply PS/2 mouse products that employ the same type of interface. To facilitate system expansion, the LPC47N350 provides four pairs of signal pins that may be used to implement this interface directly for an external keyboard and mouse.

The LPC47N350 has four high-drive, open-drain output (external pull-ups are required), bidirectional port pins that can be used for external serial interfaces, such as ISA external keyboard and PS/2-type mouse interfaces. They are KBCLK, KBDAT, EMCLK, EMDAT, IMCLK, IMDAT, PS2CLK and PS2DAT.

The following function is assumed to be in the PS/2 PORT logic: The serial clock lines, KBCLK, EMCLK, IMCLK and PS2CLK, are cleared to a low by VCC2 POR. This is so that any power-on self-test completion code transmitted from the serial keyboard will not be missed by the LPC47N350 due to power-up timing mismatches.

Chapter 14 PS/2 Device Interface

The LPC47N350 has four independent PS/2 serial ports implemented in hardware which are directly controlled by the on chip 8051 The hardware implementation eliminates the need to bit bang I/O ports to generate PS/2 traffic, however bit banging is still available if required.

Each of the four PS/2 serial channels use a synchronous serial protocol to communicate with the auxiliary device. Each PS/2 channel has two signal lines: Clock and Data. Both signal lines are bi-directional and employ open drain outputs capable of sinking 16mA. A pull-up resistor (typically 10K) is connected to the clock and data lines. This allows either the LPC47N350 SMSC PS/2 logic or the auxiliary device to control both lines. Regardless, the auxiliary device provides the clock for transmit and receive operations. The serial packet is made up of eleven bits, listed in order as they will appear on the data line: start bit, eight data bits (least significant bit first), odd parity, and stop bit. Each bit cell is from 60µS to 100µS long.

The SMSC PS/2 interface is available in the LPC47N350. The SMSC PS/2 registers are shown in Table 7.7, "8051 On-Chip External Memory Mapped Registers" between addresses 0x7F41 and 0x7F4F.

Table 14.1 Pin Definitions

PIN NAME	SMSC PS/2 FUNCTION	SMSC PS/2 DESCRIPTION
GPIO20	PS2CLK	Channel D Serial Clock
GPIO21	PS2DAT	Channel D Serial Data
IMCLK	IMCLK	Channel C Serial Clock
IMDAT	IMDAT	Channel C Serial Data
KCLK	KCLK	Channel B Serial Clock
KDAT	KDAT	Channel B Serial Data
EMCLK	EMCLK	Channel A Serial Clock
EMDAT	EMDAT	Channel A Serial Data

All PS/2 Serial Channel signals (CLK and DAT) are driven by open collector (TYPE I/OD16) drivers pulled to VCC2 (+3.3V nominal) through 10K-ohm resistors.

14.1 SMSC PS/2 Logic Overview

The SMSC PS/2 logic allows the host to communicate to any serial auxiliary devices compatible with the PS/2 interface through any one of four channels. The PS/2 Logic consists of four identical SMSC PS/2 channels, each containing a set of four operating registers. The four Channels are PS/2 Chan A, PS/2 Chan B, PS/2 Chan C, and PS/2 Chan D. During a reception, the LPC47N350 latches the data on the high to low transition of the clock. During a transmission, the LPC47N350 transitions the data line on the high to low transition of the clock. See Figure 14.1, "SMSC PS/2 Logic Block Diagram".

Note 14.1 Each PS/2 channel has the ability to “busy” the communication link by pulling the clock line low. This is accomplished by simultaneously clearing the PS2_EN and WR_CLK bits in the Control Register.

Note 14.2 Each PS/2 channel has the ability to abort, prior to the parity bit (10th bit), the transfer in progress.

Note 14.3 Clock bit time (cycle time) typically varies between 60 and 100 us. The LPC47N350 PS/2 Logic is designed such that it is immune to variations in the clock cycle times within the limit of the transfer timeout.

Note 14.4 Once a transmission has begun, the PS/2 `peripheral is allowed up to 300us per bit transfer. If the time between falling clock edges exceeds 300us a transfer timeout occurs resulting in either XMIT_TIMEOUT or REC_TIMEOUT being set along with the generation of an interrupt.

Note 14.5 Once a transmission has started, the PS/2 peripheral has approximately 2ms to complete the transfer. This transfer timeout applies to transmissions as well as receptions. In the case of a transmission (reception), if a 2ms timeout occurs the XMIT_TIMEOUT(REC_TIMEOUT) bit in the status register is set and an interrupt is generated.

Note 14.6 When the controller is ready to transmit data, it floats the data line and drives the clock line low. Once data is written to the Transmit Register, the data line is driven low and after a delay the clock line is released (floated) so that the PS/2 peripheral knows data is ready. Releasing the clock signals the start of a transmission. The PS/2 peripheral has 25ms to acknowledge the transmit start condition above by driving the clock line low. If the PS/2 peripheral does not acknowledge in the allotted time, then a Transmit timeout occurs: setting the XMIT_TIMEOUT error bit in the Status register and generating an interrupt.

Note 14.7 By clearing the PS/2 channels PS2_EN bit in its Control Register, the PS/2 Channel can be operated in a fully software controlled “Bit-bang” mode. This allows operation of auxiliary devices that do not meet standard PS/2 protocol timing handled by the LPC47N350’s PS/2 Logic block.

Note 14.8 See Section 29.7, "PS/2 Timing" for timing information.

PROGRAMMER’S NOTE:

1. The PS2_T/R bit should never be used to abort an active transmission by setting it to 0 in the middle of a transmission. To properly abort, refer to Programmer’s Note
2. To abort a transfer from the peripheral, the WR_CLK and PS2_EN bits can be set low simultaneously and held for at least 300us.
3. A transmission may be started immediately if PS2_T/R is set to “1” within 30us of a XMIT finished Interrupt or within 30us of reading the Receive Register, otherwise the channel may be in the middle of receiving data from the peripheral. If PS2_T/R is not set to one under the above conditions, software should wait 300us before transmitting to insure that the peripheral has aborted it’s transmission.

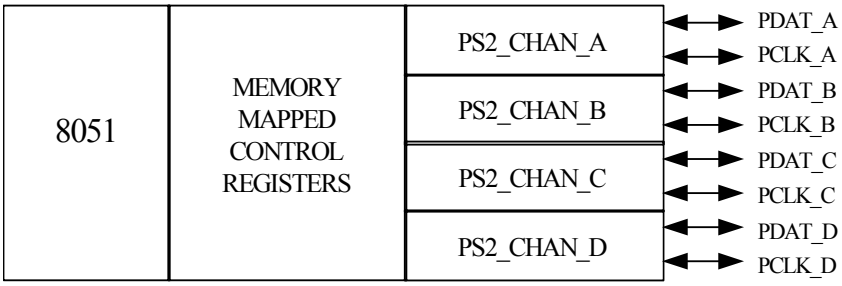


Figure 14.1 SMSC PS/2 Logic Block Diagram

14.2 PS/2 Data Frame

Data transmissions to and from the auxiliary device connector on each PS/2 channel consist of an 11-bit data stream sent serially over the data line. Table 14.2 shows the function of each bit.

Table 14.2 PS/2 Device Data Stream Bit Definitions

Start Bit Always 0	8 data bits, least sig bit first	Parity Bit Odd on xmit Prog. on rec.	Stop Bit High on xmit Prog. on rec.

14.3 SMSC PS/2 Memory Mapped Control Registers

Each SMSC PS/2 channel has a separate set of identical control registers: Transmit, Receive, Control, and Status. These are shown in Table 7.6 between addresses 0x7F41 and 0x7F4F. The transmit and receive register share the same address (for example, PS/2 Chan A Tx/Rx) In addition, one register is shared by all four channels to provide RX_Busy indicators.

14.3.1 SMSC PS/2 Transmit Registers

The byte written to this register, when PS2_T/R, PS2_EN, and XMIT_IDLE are set, is transmitted automatically by the PS/2 channel control logic. If any of these three bits (PS2_T/R, PS2_EN, and XMIT_IDLE) are not set, then writes to this register are ignored. On successful completion of this transmission or upon a Transmit Time-out condition, the PS2_T/R bit is automatically cleared and the XMIT_IDLE bit is automatically set. The PS2_T/R bit must be written to a '1' before initiating another transmission to the remote device.

Table 14.3 SMSC Transmit Registers (A–D)

HOST ADDRESS	n/a
8051 ADDRESS	0x7F41 (CHAN A) 0x7F45 (CHAN B) 0x7F49 (CHAN C) 0x7F4D (CHAN D)
POWER	VCC2
DEFAULT	0x00

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	W	W	W	W	W	W	W	W
BIT NAME	Transmit Data							

Note 14.9 Even if PS2_T/R, PS2_EN, and XMIT_IDLE are all set, writing the Transmit Register will not kick off a transmission if RDATA_RDY is set. The automatic PS2 logic forces data to be read from the Receive Register before allowing a transmission.

Note 14.10 An interrupt is generated on the low to high transition of XMIT_IDLE.

Note 14.11 All bits of this register are write only.

14.3.2 SMSC PS/2 Receive Registers

When PS2_EN=1 and PS2_T/R=0, the PS2 Channel is set to automatically receive data on that channel (both the CLK and DATA lines will float waiting for the peripheral to initiate a reception by sending a start bit followed by the data bits). After a successful reception, data is placed in this register and the RDATA_RDY bit is set and the CLK line is forced low by the PS2 channel logic. RDATA_RDY is cleared

and the CLK line is released to hi-z following a read of this register. This automatically holds off further receive transfers until the 8051 has had a chance to get the data.

Table 14.4 SMSC Receive Registers (A–D)

HOST ADDRESS	n/a
8051 ADDRESS	0x7F41 (CHAN A) 0x7F45 (CHAN B) 0x7F49 (CHAN C) 0x7F4D (CHAN D)
POWER	VCC2
DEFAULT	0xFF

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R	R
BIT NAME	Receive Data							

Note 14.12 The Receive Register is initialized to 0xFF after a read or after a Timeout has occurred.

Note 14.13 The channel can be enabled to automatically transmit data (PS2_EN=1) by setting PS2_T/R while RDATA_RDY is set, however a transmission can not be kicked off until the data has been read from the Receive Register.

Note 14.14 An interrupt is generated on the low to high transition of RDATA_RDY.

Note 14.15 If a receive timeout (REC_TIMEOUT=1) or a transmit timeout (XMIT_TIMEOUT=1) occurs, the channel is busied (CLK held low) for 300us (Hold Time) to guarantee that the peripheral aborts. Writing to the Transmit Register will be allowed, however the data written will not be transmitted until the Hold Time expires and until the PS/2 status register is read.

Note 14.16 All bits in this register are read only.

Table 14.5 SMSC PS/2 Transmit Registers (A - D)

HOST ADDRESS	N/A
8051 ADDRESS	0x7F41 (CHAN A), 0x7F45 (CHAN B), 0x7F49 (CHAN C), 0X7F4D (CHAN D)
POWER	VCC2
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	W	W	W	W	W	W	W	W
BIT NAME	Transmit Data							

14.3.3 SMSC PS/2 Control Registers

Table 14.6 SMSC PS/2 Control Registers (A - D)

HOST ADDRESS	N/A
8051 ADDRESS	0x7F42 (CHAN A), 0x7F46 (CHAN B), 0x7F4A (CHAN C), 0x7F4E (CHAN D)
POWER	VCC2
DEFAULT	0x40

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	WR_CLK	WR_DATA	STOP		PARITY		PS2_EN	PS2_T/R

Default = 0x40 on VCC2 POR only.

Note: There are four PS/2 Control Registers, one for each channel.

PS2_T/R

PS/2 Channel Transmit/Receive (default = 0). This bit is only valid when PS2_EN=1 and sets the PS2 logic for automatic transmission or reception when PS2_T/R equals '1' or '0' respectively.

When set, the PS/2 channel is enabled to transmit data. To properly initiate a transmit operation, this bit must be set prior to writing to the Transmit Register; writes are blocked to the Transmit Register when this bit is not set. Upon setting the PS2_T/R bit, the channel will drive its CLK line low and then float the DATA line and hold this state until a write occurs to the Transmit Register or until the PS2_T/R bit is cleared. Writing to the Transmit Register initiates the transmit operation. LPC47N350 drives the data line low and, within 80ns, floats the clock line (externally pulled high by the pull-up resistor) to signal to the external PS/2 device that data is now available. The PS2_T/R bit is cleared on the 11th clock edge of the transmission or if a Transmit Timeout error condition occurs.

Note: If the PS2_T/R bit is set while the channel is actively receiving data prior to the leading edge of the 10th (parity bit) clock edge, the receive data is discarded. If this bit is not set prior to the 10th clock signal, then the receive data is saved in the Receive Register.

When the PS2_T/R bit is cleared, the PS/2 channel is enabled to receive data. Upon clearing this bit, if RDATA_RDY=0, the channel's CLK and DATA will float waiting for the external PS/2 device to signal the start of a transmission. If the PS2_T/R bit is set while RDATA_RDY=1, then the channel's DATA line will float but its CLK line will be held low, holding off the peripheral, until the Receive Register is read.

PS2_EN

PS2 Channel ENable (default = 0). When PS2_EN=1, the PS/2 State machine is enabled allowing the channel to perform automatic reception or transmission depending on the bit value of PS2_T/R. When PS2_EN = 0, the channel's automatic PS/2 state machine is disabled and the channel can be bit-banged through the WR_DATA and WR_CLK bits in the Control Register and the RD_DATA and RD_CLK bits in the Status Register. Thus, when PS2_En=0, the channel's CLK and DATA lines are forced to the level specified in the Control Register WR_CLK and WR_DATA bits.

Note: If the PS2_EN bit is cleared prior to the leading edge (falling edge) of the 10th (parity bit) clock edge the receive data is discarded (RDATA_RDY remains low). If the PS2_EN bit is cleared following the leading edge of the 10th clock signal, then the receive data is saved in the Receive Register (RDATA_RDY goes high) assuming no parity error.

PROGRAMMER'S NOTE: To abort a transfer from the peripheral the WR_CLK and PS2_EN bits can be set low simultaneously and held for at least 300us.

PARITY

Bits [3:2] of the Control Register are used to set the parity expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits[3:2] = 00: Receiver expects Odd Parity (default).

= 01: Receiver expects Even Parity.

= 10: Receiver ignores level of the parity bit (10th bit is not interpreted as a parity bit).

= 11: Reserved.

STOP

Bits [5:4] of the Control Register are used to set the level of the stop bit expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits[5:4] = 00: Receiver expects an active high stop bit.

= 01: Receiver expects an active low stop bit.

= 10: Receiver ignores the level of the Stop bit (11th bit is not interpreted as a stop bit).

= 11: Reserved.

WR_DATA

Write DATA bit: When PS2_EN=1, writes to the WR_DATA bit are accepted but result in no action other than setting or clearing this bit. When PS2_EN=0, setting this bit to a 1 or 0 either floats or drives low the PS/2 channel's Serial DATA pin. This bit is used for transmitting bit-banged data over the PS2 channel. Bit-banging of the PS/2 channel is enabled when PS2_EN= 0.

Note: While the Hold timeout is in effect (300us following a Receive or Transmit Timeout) writes to this bit are blocked.

WR_CLK

Write CLK bit: When PS2_EN=1, writes to the WR_CLK bit are accepted but result in no action other than setting or clearing this bit. When PS2_EN=0, setting this bit to a 1 or 0 either floats or drives low the PS/2 channel's Serial CLK pin. Bit-banging of the PS/2 channel is enabled when the PS2_EN bit is set to 0.

Note 14.17 While the Hold timeout is in effect (300us following a Receive or Transmit Timeout) writes to this bit are blocked.

Note 14.18 When PS2_EN = 0, high to low transitions on the CLK pin caused by the peripheral will generate a PS2 Chan interrupt. A timeout event or writing this bit low will not cause an interrupt.

The default for the WR_DATA bit D6 in the four SMSC PS/2 Control Registers is "1". The default in earlier devices is "0" (Table 14.6). The VCC2 Power-on Default for each Control Register is 40h.

14.3.4 SMSC PS/2 Status Registers

Table 14.7 SMSC PS/2 Status Registers (A - D)

HOST ADDRESS	N/A
8051 ADDRESS	0x7F43 (CHAN A), 0x7F47 (CHAN B), 0x7F4B (CHAN C), 0x7F4F (CHAN D)
POWER	VCC2
DEFAULT	0x00

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R	R
BIT NAME	RD_CLK	RD_DATA	XMIT_ TIMEOUT	XMIT_IDLE	FE	PE	REC_ TIMEOUT	RDAT _RDY

Default = 0x40 on VCC2 POR only.

Note 14.19 There are four PS/2 Status Registers, one for each channel.

Note 14.20 XMIT_TIMEOUT, FE, PE, REC_TIMEOUT are cleared to zero upon a read of this register.

RDATA_RDY

Receive Data Ready: Under normal operating conditions, this bit is set following the falling edge of the 11th clock given successful reception of a data byte from the PS/2 peripheral (i.e., no parity, framing, or receive timeout errors) and indicates that the received data byte is available to be read from the Receive Register. This bit may also be set in the event that the PS2_EN bit is cleared following the 10th CLK edge (see the PS2_EN bit description for further details). Reading the Receive Register clears this bit.

Note 14.21 An Interrupt is generated on the low to high transition of the RDATA_RDY bit.

REC_TIMEOUT

Under PS2 automatic operation, PS2_EN=1, this bit is set on one of 4 receive error conditions, and in addition, the channel's CLK line is automatically pulled low and held for a period of 300us (and until the PS/2 Status register is read) following assertion of the REC_TIMEOUT bit:

1. When the receiver bit time (time between falling edges) exceeds 300us.
2. If the time from the 1st (start) bit to the 10th (parity) bit exceeds 2ms.
3. On a receive parity error along with the parity error (PE) bit.
4. On a receive framing error due to an incorrect STOP bit along with the framing error (FE) bit.

The REC_TIMEOUT bit is cleared when the Status Register is read.

Note 14.22 An Interrupt is generated on the low to high transition of the REC_TIMEOUT bit.

PE

Parity Error: When receiving data, the parity bit is clocked in on the falling edge of the 10th CLK edge. If the channel has been set to expect either even or odd parity and the 10th bit is contrary to the expected parity, then the PE and REC_TIMEOUT bits are set following the falling edge of the 10th CLK edge and an Interrupt is generated.

FE

Framing Error: When receiving data, the stop bit is clocked in on the falling edge of the 11th CLK edge. If the channel has been set to expect either a high or low stop bit and the 11th bit is contrary to the expected stop polarity, then the FE and REC_TIMEOUT bits are set following the falling edge of the 11th CLK edge and an Interrupt is generated.

XMIT_IDLE

Transmitter Idle: When low, the XMIT_IDLE bit is a status bit indicating that the PS2 channel is actively transmitting data to the PS2 peripheral device. Writing to the Transmit Register when the channel is ready to transmit will cause the XMIT_IDLE bit to deassert and remain deasserted until one of the following conditions occur:

1. The falling edge of the 11th CLK; upon a Transmit Timeout condition (XMIT_TIMEOUT goes high);
2. Upon the PS2_T/R bit being written to 0;
3. Upon the PS2_EN bit being written to 0.

Note 14.23 An interrupt is generated on the low to high transition of XMIT_IDLE.

XMIT_TIMEOUT

This bit is set on one of 3 transmit conditions, and in addition the channel's CLK line is automatically pulled low and held for a period of 300us (and until the PS/2 Status register is read) following assertion of the XMIT_TIMEOUT bit during which time the PS2_T/R is also held low:

1. When the transmitter bit time (time between falling edges) exceeds 300us.
2. When the transmitter start bit is not received within 25ms from signaling a transmit start event.
3. If the time from the 1st (start) bit to the 10th (parity) bit exceeds 2ms.

RD_DATA

Read DATA bit: Reading this bit returns the current level of the PS2 channel's Serial DATA pin. This bit is used for receiving bit-banged data over the PS2 channel. Bit-banging of the PS2 channel is enabled when the PS2_EN bit is set to 0. To receive data properly using this bit, PS2_EN must be set to 0 and the WR_DATA bit in the PS2 Channel's Control Register must be set to 1.

RD_CLK

Read CLK bit: Reading this bit returns the current level of the PS2 channel's Serial CLK pin. This bit is used when receiving bit-banged data over the PS2 channel. Bit-banging of the PS2 channel is enabled when the PS2_EN bit is set to 0. To receive bit banged data properly, the PS2_EN must be set to 0 and the WR_CLK bit in the PS2 Channel's Control Register must be set to 1.

Note 14.24 When PS2_EN = 0, high to low transitions on the CLK pin will generate a PS2 Chan interrupt. A timeout event or writing this bit low will not cause an interrupt.

Note 14.25 When PS2_EN=1, bit-banging is disabled for any of the following 3 conditions:

Time-out is active.

300us following a time-out (Hold Time).

RDATA_RDY = 1.

14.3.5 SMSC PS/2 Status_2 Registers

Table 14.8 SMSC PS/2_Status_2 Register

HOST ADDRESS	-
8051 ADDRESS	0x7F48
POWER	VCC2
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/WC	R	R/WC	R	R/WC	R	R/WC	R
BIT NAME	XMIT_START_TIMEOUT_D	RX_BUSYD	XMIT_START_TIMEOUT_C	RX_BUSYC	XMIT_START_TIMEOUT_B	RX_BUSYB	XMIT_START_TIMEOUT_A	RX_BUSYA

PROGRAMMER'S NOTE: Always check that an SMSC PS/2 channel is idle, i.e. the RX_BUSY bit is "0", before attempting to transmit on that channel. Receive data may or may not be lost by setting an SMSC PS/2 channel to transmit while the RX_BUSY bit is asserted depending where in the message frame the transmit mode change occurs.

RX_BUSY

When a RX_BUSY bit is set, the associated channel is actively receiving PS/2 data; when a RX_BUSY bit is clear, the channel is idle.

XMIT_START_TIMEOUT

The XMIT_START_TIMEOUT bit is set when the transmitter start bit was not received within 25 ms from signaling a transmit start event.

Chapter 15 I²C/SMBus

15.1 Overview

The LPC47N350 supports I²C/SMBus. I²C/SMBus is a serial communication protocol between a computer host and its peripheral devices. It provides a simple, uniform and inexpensive way to connect peripheral devices to a single computer port. A single I²C/SMBus controller on a host can accommodate up to 125 peripheral devices.

The I²C/SMBus protocol includes a physical layer and several software layers. The software layers include the base protocol, the device driver interface, and several specific device protocols.

The LPC47N350 implements two I²C/SMBus controllers (I²C/SMBus 1 Controller and I²C/SMBus 2 Controller). Each controller, through a multiplexer, can drive two independent sets of Clock and Data pins, as shown in Figure 15.1, "I2C/SMBus Controllers".

Four I²C/SMBus 2 controller pins, AB2A_DATA, AB2A_CLK, AB2B_DATA and AB2B_CLK are multiplexed on GPIO11 through GPIO14. For information regarding multiplexed I²C/SMBus pins see Table 2.4 on page 10 and Section 21.5, "Multiplexing_3 Register - MISC[23:17]".

APPLICATION NOTE: When VCC1=0, the I2C bus pins present a high impedance and draw only leakage current. Therefore no additional external circuity is required to isolate the LPC47N350 Vcc1 powered the I2C bus pins from an I2C bus with VCC0 powered devices and/or resistor pull-ups to VCC0.

The I²C/SMBus interface is fully and directly controlled by the on-chip 8051 through its set of on-chip memory mapped control registers. Addresses for the registers are shown in Table 15.1, "I2C/SMBus Register Address Summary".

The I²C/SMBus logic is powered on the VCC1 power plane and clocked by the 8051 clock to provide the ability to wake-up the 8051 on an I²C/SMBus event. When a wakeup event occurs, there is a 6 µs max. delay before the ring oscillator starts and an I²C/SMBus event can be detected. This limits the I²C/SMBus Bus Master Operating Frequency for wakeup events to 60 KHz. Once the ring oscillator is running, the I²C/SMBus Operating Frequency is a full 100 KHz.

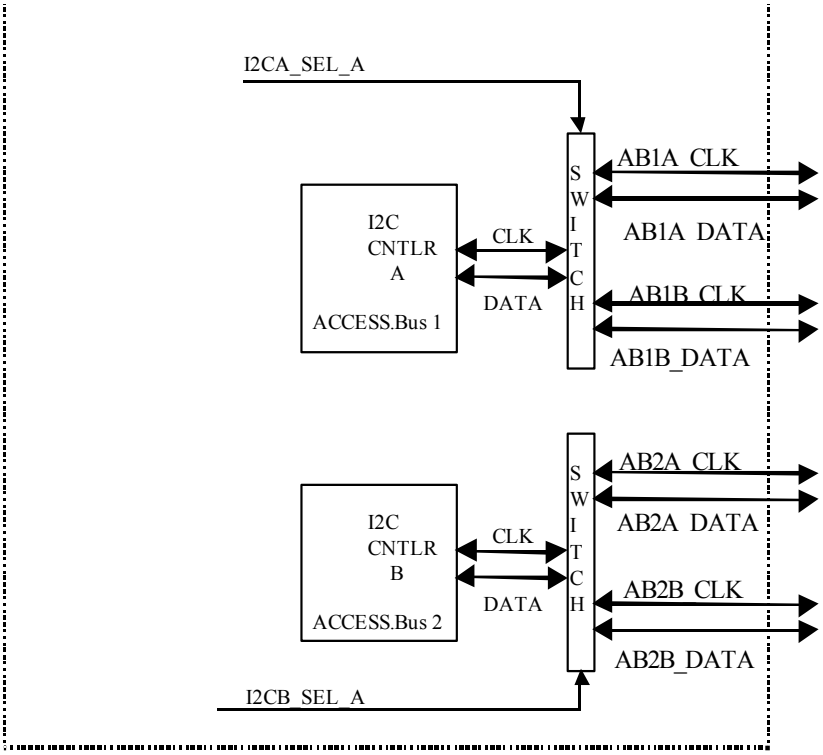


Figure 15.1 I²C/SMBus Controllers

Table 15.1 I²C/SMBus Register Address Summary

ADDRESS (Note 15.1)	REGISTER ACCESS	REGISTER NAME
7F31h	W	I²C/SMBus 1 Control
7F31h	R	I²C/SMBus 1 Status
7F32h	R/W	I²C/SMBus 1 Own Address
7F33h		I²C/SMBus 1 Data
7F34h	R/W (Note 15.2)	I²C/SMBus 1 Clock
7F67h	W	I²C/SMBus 2 Control
7F67h	R	I²C/SMBus 2 Status
7F68h	R/W	I²C/SMBus 2 Own Address
7F69h		I²C/SMBus 2 Data
7F6Ah	R/W (Note 15.2)	I²C/SMBus 2 Clock
7F89h	R/W (Note 15.3)	I²C/SMBus Switch

Note 15.1 These Registers are only directly accessible by the 8051 and reside within the 8051's external Memory Mapped Data address space.

Note 15.2 Bits 2 through 6 are read only reserved.

Note 15.3 Bits 2 through 7 are read only reserved.

15.2 I²C/SMBus Register Descriptions

Each I²C/SMBus controller has five internal registers. Two of these, Own Address Register and Clock Register, are used for initialization of the controller. Normally they are only written once directly after resetting of the chip. The other registers, Data Register, Control Register and Status Register are used during actual data transmission/reception. The Control Register and Status Register are accessed at the same location. The Data Register performs all serial-to-parallel interfacing with the I²C/SMBus interface. The Status Register contains I²C/SMBus status information required for bus access and/or monitoring.

The I²C/SMBus Switch Register is used to select one of two sets of Clock and Data pins for each controller.

15.2.1 I²C/SMBus Control Register

Table 15.2 I²C/SMBus Control Register

HOST ADDRESS	N/A
8051 ADDRESS	I²C/SMBus 1 = 0x7F31 I²C/SMBus 2 = 0x7F67
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	W	W	W	W	W	W	W	W
BIT NAME	PIN	ESO	Reserved		ENI	STA	STO	ACK

BIT 7 - PIN

Pending Interrupt Not. Writing the PIN bit to a logic “1” deasserts all status bits except for the nBB (Bus Busy); nBB is not affected. The PIN bit is a self-clearing bit. Writing this bit to a logic “0” has no effect. This may serve as a software reset function.

BIT 6 - ESO

Enable Serial Output. ESO enables or disables the serial I²C/SMBus I/O. When ESO is high, I²C/SMBus communication is enabled; communication with the Data Register is enabled and the Status Register bits are made available for reading. With ESO = 0, bits ENI, STA, STO and ACK of the Control Register can be read for test purposes.

BIT 5 and 4 - Reserved

BIT 3 - ENI

This bit enables the internal interrupt, nINT, which is generated when the PIN bit is active (logic 0).

BIT 2 and 1 - STA and STO

These bits control the generation of the I2C/SMBus Start condition and transmission of slave address and R/nW bit, generation of repeated Start condition, and generation of the STOP condition (see Table 15.3).

Table 15.3 Instruction Table for Serial Bus Control

STA	STO	PRESENT MODE	FUNCTION	OPERATION
1	0	SLV/REC	START	Transmit START+address, remain MST/TRM if R/nW=0; go to MST/REC if R/nW=1.
1	0	MST/TRM	REPEAT START	Same as for SLV/REC
0	1	MST/REC; MST/TRM	STOP READ; STOP WRITE	Transmit STOP go to SLV/REC mode; Note 15.4
1	1	MST	DATA CHAINING	Send STOP, START and address after last master frame without STOP sent; Note 15.5
0	0	ANY	NOP	No operation; Note 15.6

Note 15.4 In master receiver mode, the last byte must be terminated with ACK bit high (‘negative acknowledge’).

Note 15.5 If both STA and STO are set high simultaneously in master mode, a STOP condition followed by a START condition + address will be generated. This allows ‘chaining’ of transmissions without relinquishing bus control.

Note 15.6 All other STA and STO mode combinations not mentioned in Table 15.1 are NOPs.

BIT 0 - ACK

This bit must be set normally to logic “1”. This causes the I2C/SMBus to send an acknowledge automatically after each byte (this occurs during the 9th clock pulse). The bit must be reset (to logic “0”) when the I2C/SMBus controller is operating in master/receiver mode and requires no further data to be sent from the slave transmitter. This causes a negative acknowledge on the I2C/SMBus, which halts further transmission from the slave device.

15.2.2 I²C/SMBus Status Register

Table 15.4 I²C/SMBus Status Register

HOST ADDRESS	N/A
8051 ADDRESS	I²C/SMBus 1 = 0x7F31 I²C/SMBus 2 = 0x7F67
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R	R
BIT NAME	PIN	Reserved	STS	BER	LRB/AD0	AAS	LAB	nBB

BIT 7 - PIN

Pending Interrupt Not. This bit is a status flag which is used to synchronize serial communication and is set to logic "0" whenever the chip requires servicing. The PIN bit is normally read in polled applications to determine when an I²C/SMBus byte transmission/reception is completed.

When acting as transmitter, PIN is set to logic "1" (inactive) each time the Data Register is written. In receiver mode, the PIN bit is automatically set to logic "1" each time the Data Register is read.

After transmission or reception of one byte on the I²C/SMBus (nine clock pulses, including acknowledge), the PIN bit will be automatically reset to logic "0" (active) indicating a complete byte transmission/reception. When the PIN bit is subsequently set to logic "1" (inactive), all status bits will be reset to "0" on a BER (bus error) condition.

In polled applications, the PIN bit is tested to determine when a serial transmission/reception has been completed. When the ENI bit (bit 3 of the Control Register) is also set to logic "1," the hardware interrupt is enabled. In this case, the PI flag also triggers and internal interrupt (active low) via the nINT output each time PIN is reset to logic "0".

When acting as a slave transmitter or slave receiver, while PIN = "0", the chip will suspend I²C/SMBus transmission by holding the SCL line low until the PIN bit is set to logic "1" (inactive). This prevents further data from being transmitted or received until the current data byte in the Data Register has been read (when acting as slave receiver) or the next data byte is written to the Data Register (when acting as slave transmitter).

PIN Bit Summary:

- The PIN bit can be used in polled applications to test when a serial transmission has been completed. When the ENI bit is also set, the PIN flag sets the internal interrupt via the nINT output.
- In transmitter mode, after successful transmission of one byte on the I²C/SMBus, the PIN bit will be automatically reset to logic "0" (active) indicating a complete byte transmission.
- In transmitter mode, PIN is set to logic "1" (inactive) each time the Data Register is written.
- In receiver mode, PIN is set to logic "0" (inactive) on completion of each received byte. Subsequently, the SCL line will be held low until PIN is set to logic "1".

- In receiver mode, when the Data Register is read, PIN is set to logic “1” (inactive).
- In slave receiver mode, an I2C/SMBus STOP condition will set PIN=0 (active).
- PIN=0 if a bus error (BER) occurs.

BIT 6 - Reserved (Read returns 0)

BIT 5 - STS

When in slave receiver mode, this flag is asserted when an externally generated STOP condition is detected (used only in slave receiver mode).

BIT 4 - BER

Bus error; a misplaced START or STOP condition has been detected. Resets nBB (to logic “1”; inactive), sets PIN = “0” (active).

BIT 3 - LRB/AD0

Last Received Bit or Address 0 (general call) bit. This status bit serves a dual function, and is valid only while PIN=0.

LRB holds the value of the last received bit over the I2C/SMBus while AAS=0 (not addressed as slave). Normally, this will be the value of the slave acknowledgment; thus checking for slave acknowledgment is done via testing of the LRB.

When AAS = 1 (Addressed as slave condition), the I2C/SMBus controller has been addressed as a slave. Under this condition, this bit becomes the AD0 bit and will be set to logic “1” if the slave address received was the ‘general call’ (00h) address, or logic “0” if it was the I2C/SMBus controller’s own slave address.

BIT 2 - AAS

Addressed As Slave bit. Valid only when PIN=0. When acting as slave receiver, this flag is set when an incoming address over the I2C/SMBus matches the value in own address register S0’ (shifted by one bit) or if the I2C/SMBus ‘general call’ address (00h) has been received (‘general call’ is indicated when AD0 status bit is also set to logic “1”).

BIT 1 - LAB

Lost Arbitration Bit. This bit is set when, in multi-master operation, arbitration is lost to another master on the I2C/SMBus.

BIT 0 - nBB

Bus Busy bit. This is a read-only flag indicating when the I2C/SMBus is in use. A zero indicates that the bus is busy, and access is not possible. This bit is set/reset (logic “1”/logic “0”) by Stop/Start conditions.

15.2.3 Own Address Register

When the chip is addressed as slave, this register must be loaded with the 7-bit I2C/SMBus address to which the chip is to respond. During initialization, the Own Address Register must be written to, regardless whether it is later used. The Addressed As Slave (AAS) bit in the Status Register is set when this address is received (the value in the Data Register is compared with the value in the Own Address Register). Note that the Data Register and Own Address Register are offset by one bit; hence, programming the Own Address Register with a value of 55h will result in the value AAh being recognized as the chip’s I2C/SMBus slave address.

After reset, the Own Address Register has default address 00h.

Table 15.5 Own Address Register

HOST ADDRESS	N/A
8051 ADDRESS	I^2C/SMBus 1 = 0x7F32 I^2C/SMBus 2 = 0x7F68
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Slave Address 6	Slave Address 5	Slave Address 4	Slave Address 3	Slave Address 2	Slave Address 1	Slave Address 0

15.2.4 Data Register

The Data Register acts as serial shift register and read buffer interfacing to the I^2C/SMBus. All read and write operations to/from the I^2C/SMBus are done via this register. I^2C/SMBus data is always shifted in or out of the Data Register.

In receiver mode, the I^2C/SMBus data is shifted into the shift register until the acknowledge phase. Further reception of data is inhibited (SCL held low) until the Data Register is read.

In the transmitter mode, data is transmitted to the I^2C/SMBus as soon as it is written to the Data Register if the serial I/O is enabled (ESO=1).

Table 15.6 Data Register

HOST ADDRESS	N/A
8051 ADDRESS	I^2C/SMBus 1 = 0x7F33 I^2C/SMBus 2 = 0x7F69
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0

15.2.5 Clock Register

The Clock Register controls selection of the internal chip clock frequency used for the I^2C/SMBus block. This determines the SCL clock frequency generated by the chip. The selection is made via Bits[2:0].

Table 15.7 Clock Register

HOST ADDRESS	N/A
8051 ADDRESS	I^2C/SMBus 1 = 0x7F34 I^2C/SMBus 2 = 0x7F6A
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R	R	R	R	R/W	R/W	R/W
BIT NAME	AB_RST	Reserved				CLK_DIV	CLOCK SELECT 00 = Clock Off 01 = Reserved 10 = 8051 Clock 11 = 24 MHz. Clock	

BIT 7 – AB_RST

I²C/SMBus Reset. Setting this bit re-initializes all logic and registers in the I²C/SMBus block. AB_RST is not self-clearing. It must be written high and then written low.

BITS 6 through 3 – Reserved (Reads return 0)

BIT 2 - CLK_DIV

Clock Divider Bit. The clock divider bit CLK_DIV affects all I²C/SMBus clock inputs. When CLK_DIV is "1", the I²C/SMBus input clock is divided by 2. When CLK_DIV is "0", the I²C/SMBus input clock is not divided.

BITS 1 and 0 – CLOCK SELECT

Clock Selection Bits. These bits determine the source of the clock used by the I²C/SMBus Controller. Encoding of these bits are as shown in Table 15.7, "Clock Register", above. Data rates produced by the selected clock are shown in Table 15.8.

Table 15.8 Internal Clock Rates and I²C/SMBus Data Rates

CLOCK SELECT	CLOCK RATE	DATA RATE (F/240)	NOMINAL HIGH (96/F)	NOMINAL LOW (144/F)	MINIMUM HIGH (18/F) Note 15.7
00	Off	-	-	-	-
01	n/a	-	-	-	-
10 (8051 Clock Selection)	Ring Osc=4 MHz	16.7 KHz	24 µs	36 µs	4.5 µs
	Ring Osc=6 MHz	25 KHz	16 µs	24 µs	3 µs
	Ring Osc=8 MHz	33.3 KHz	12 µs	18 µs	2.25 µs
	12 MHz	50 KHz	8 µs	12 µs	4 µs
	16 MHz	67 KHz	6 µs	9 µs	4 µs
	24 MHz	100 KHz	4 µs	6 µs	4 µs
	32 MHz	133 KHz	3 µs	4.5 µs	4 µs
11	24 MHz	100 KHz	4 µs	6 µs	4 µs

f = frequency of the ring oscillator.

Note 15.7 18/f pertains to Ring Osc rates only.

15.2.6 I²C/SMBus Switch Register

The I²C/SMBus Switch register is used to control the I²C/SMBus Multiplexer. Each of the two I²C/SMBus controllers in the LPC47N350 can drive two independent sets of Clock and Data pins (Figure 15.1). The selected Clock and Data pins for each I²C/SMBus controller are determined by the I²C_SMBusA_SEL_A and I2C_SMBusB_SEL_A bits, D1 and D0 respectively, in the I²C/SMBus Switch register.

Table 15.9 I²C/SMBus Switch Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F89
POWER	VCC1
DEFAULT	0x03

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R/W	R/W
BIT NAME	Reserved						I2C_SMBusB_SEL_A	I2C_SMBusA_SEL_A

Note: BITS 7 through 2 – Reserved (Reads return 0)

BIT 1 - I2C_SMBusB_SEL_A

The I2C_SMBusB_SEL_A bit determines the selected Clock and Data pins for the I²C/SMBus 2 controller (Figure 15.1). When the I2C_SMBusB_SEL_A bit is '1' (default), the AB2A_CLOCK and AB2A_DATA pins are driven by the I²C/SMBus B controller. The AB2B_CLOCK and AB2B_DATA pins are tristated. When the I2C/SMBusB_SEL_A bit is '0', the AB2B_CLOCK and AB2B_DATA pins are driven by the I²C/SMBus 2 controller. The AB2A_CLOCK and AB2A_DATA pins are tristated.

BIT 0 - I2C_SMBusA_SEL_A

The I2C_SMBusA_SEL_A bit determines the selected Clock and Data pins for the I²C/SMBus 1 controller (Figure 15.1). When the I2C_SMBusA_SEL_A bit is '1' (default), the AB1A_CLOCK and AB1A_DATA pins are driven by the I²C/SMBus 1 controller. The AB1B_CLOCK and AB1B_DATA pins are tristated. When the I2C_SMBusA_SEL_A bit is '0', the AB1B_CLOCK and AB1B_DATA pins are driven by the I²C/SMBus 1 controller. The AB1A_CLOCK and AB1A_DATA pins are tristated.

Chapter 16 Serial Peripheral Interface (SPI)

16.1 Overview

- The LPC47N350 SPI port is a configurable 3-wire serial interface for communicating with various peripheral devices (EEPROMS, DACs, ADCs).
- 8-bit serial data is transmitted and received simultaneously over two data pins in Full Duplex mode with options to transmit and receive on one data pin in Bidirectional mode.
- An internal programmable Baud Rate Generator and clock polarity and phase controls allow communication with various SPI peripherals with specific clocking requirements.
- SPI cycle completion can be determined by status polling or interrupts.
- The SPI port pins can be configured as GPIOs when SPI functionality is not needed.
- The LPC47N350 SPI is a master only device and does not support multiple-master SPI configurations.
- The SPI is powered by VCC1 and can run on suspend power only.

16.2 SPI Block Diagram

Figure 16.1 shows the SPI block diagram. See Section 16.3, "Interface Description," on page 176, Section 16.4, "SGPIO vs. SPI Function Control," on page 177, Section 16.7, "SPI Registers," on page 179, and Section 16.8, "SPIDONE - 8051 Interrupt," on page 185 for description on SPI block signals, SPI pins and registers.

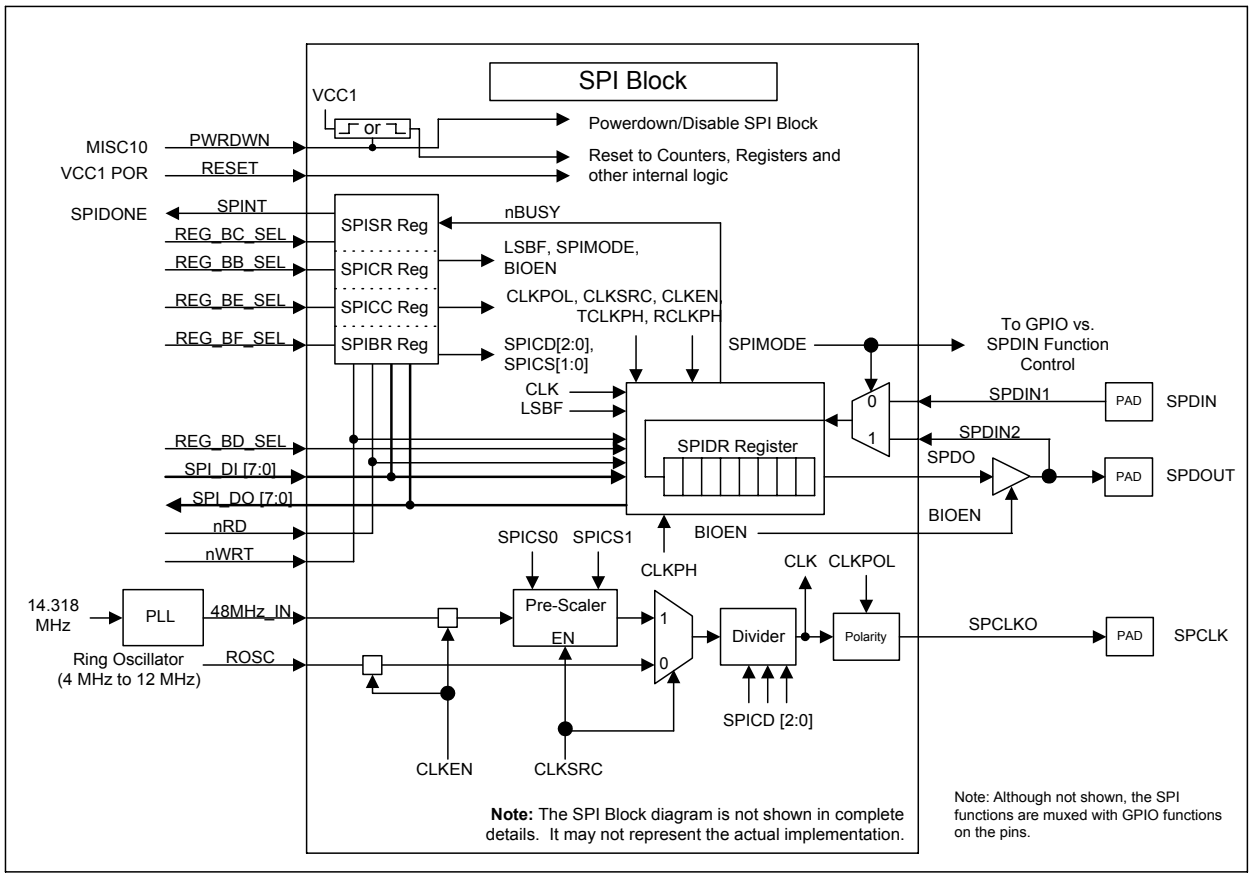


Figure 16.1 SPI Block Diagram

16.3 Interface Description

16.3.1 SPI Block Signals

Table 16.1 shows the SPI Block signals. Note that these signals are internal to LPC47N350.

Table 16.1 SPI Block Signals

	SIGNAL	DIRECTION	DESCRIPTION
1.	SPDO	O	Serial Data Out.
2.	SPDIN1	I	Serial Data In 1. Input in full-duplex mode.
3.	SPDIN2		Serial Data In 2. Input in bi-direction mode.
4.	SPCLKO	O	Serial Clock
5.	BIOEN		SPDOUT Output enable in bi-directional mode
6.	SPIMODE		Output to GPIO vs. SPDIN Function Control
7.	ROSC	I	Clock Input from Ring Oscillator
8.	48MHz_IN		48MHz Clock Input from PLL
9.	REG_BB_SEL		SPICR register select input
10.	REG_BC_SEL		SPISR register select input
11.	REG_BD_SEL		SPIDR register select input
12.	REG_BE_SEL		SPICC register select input
13.	REG_BF_SEL		SPIBR register select input
14.	SPI_DO [7:0]	O	SPI Data Out
15.	SPI_DI [7:0]	I	SPI Data Input
16.	nRD		Read Strobe
17.	nWRT		Write Strobe
18.	SPINT	O	Interrupt output to 8051
19.	PWRDWN	I	MISC10 Bit from Multiplexing_2 Register
20.	RESET		VCC1 POR signal

16.3.2 SPI Pins

The following subsections describe the SPI Pins.

16.3.2.1 SPDOUT - Serial Peripheral Data Out

This is the serial data output from the LPC47N350 SPI interface. When the interface is configured for Bi-directional mode, SPDOUT is used for SPI serial I/O. This pin can be configured as SGPIO31 (See Section 16.4, "SGPIO vs. SPI Function Control," on page 177). The data OUT is shifted out on the edge as selected using the TCLKPH bit in the SPI Clock Control Register (SPICC).

USER'S NOTE: In the Bi-directional mode, some slave devices may tristate the last few bits to signal a turn-around; therefore, an external weak pull-up may be required on the pin.

16.3.2.2 SPDIN - Serial Peripheral Data In

This is the serial data input to the LPC47N350 SPI. When the interface is configured for Bidirectional mode, SPDIN is unused. This pin can be configured as SGPIO32 (Section 16.4, "SGPIO vs. SPI Function Control," on page 177). The data IN is sampled on the edge as selected using the RCLKPH bit in the SPI Clock Control Register (SPICC).

USER'S NOTE: Some slave device may tristate the SPDIN pin during command phase; therefore, an external weak pull-up or pull-down may be required on the pin.

16.3.2.3 SPCLK - Serial Peripheral Clock

This is the serial clock driven by the LPC47N350 SPI (master) and connected to all SPI slaves. All data (input and output) is sampled/shifted on SPCLK according to the clock controls CLKPH and CLKPOL (See Section 16.7.4.1, "D0 - TCLKPH - Transmit Clock Phase," on page 183 and Section 16.7.4.2, "D1 - CLKPOL - SPI Clock Polarity," on page 183). This pin can be configured as LGPIO60 (See Section 16.4, "SGPIO vs. SPI Function Control," on page 177).

16.4 SGPIO vs. SPI Function Control

Bit[1] (MISC10) in register Multiplexing_2 Register (8051 Address 0x7F40) can be used to control SGPIO vs. SPI function selection. This bit applies to all SPI functions. The SPDIN on SGPIO32 PIN also requires SPIMODE bit (see Section 16.7.1.2, "D1 - SPIMODE - SPI Mode," on page 180) for its function selection. The BIOEN bit (see Section 16.7.1.3, "D2 - BIOEN - Bidirectional Mode Output Enable," on page 180) is also needed to select between the SPDOUT and SPDIN functions on the SGPIO31 PIN in the bi-directional mode. The default of MISC10 bit is '0' - GPIO function. See Table 16.2 for MISC10 Bit functionality. See Table 21.10 on page 244 for the Multiplexing_2 Register.

Table 16.2 MISC10 BIT

MISC10	SPIMODE	BIOEN	SGPIO60 PIN	SGPIO61 PIN	SGPIO62 PIN
0 (DEFAULT)	X	X	SGPIO30	SGPIO31	SGPIO32
1	0 (DEFAULT)		SPCLK	SPDOUT	SPDIN
	1	1			LGPIO62
		0 (DEFAULT)		SPDIN	

The 8051 SGPIO registers control the direction and state of the LGPIO30-32 functions. The registers related to SGPIO (input/output and direction) do not apply when the SPI functions are selected. If MISC10 bit '0', writes to SPIDR are ignored and therefore transactions cannot be initiated. The internal clocks and all Baud Rate Generator circuitry is stopped to conserve power. Changing MISC10 bit causes all SPI register to reset to their default values. The MISC10 should not be switched to temporary powerdown the SPI Block, the CLKEN bit in SPICC register should be used instead.

Figure 16.2 shows the SPI vs. GPIO function control logic LGPIO60-LGPIO62 in the LPC47N350.

16.5 Functional Description

During a typical SPI transfer, data is shifted out of the SPI master and received by an SPI slave. Data is also shifted out of the slave and received by the master. The duration of the data transfer cycle depends on the mode chosen - Bidirectional or Full Duplex. Data is shifted and latched by both the master and slave using an I/O shift register in each device. These registers are clocked by a serial clock which is generated by the master only during a transfer. Figure 16.2 illustrates SPI transfer logic.

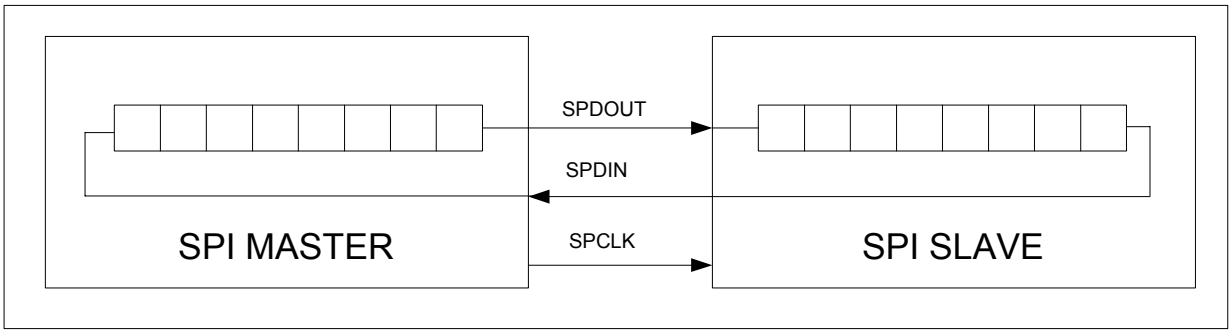


Figure 16.2 SPI Logic (Full Duplex)

- The LPC47N350 SPI Interface contains an 8-bit shift register and therefore must transmit and receive data in 8-bit cycles. Communication with SPI peripherals that have input registers of varying lengths can be achieved with multiple 8-bit cycles and/or leading zeros in the command stream.
- The LPC47N350 SPI can be configured to operate in two modes: Full Duplex and Bidirectional (see Figure 16.1 on page 175). See Section 16.5.1, "Full Duplex Mode" and Section 16.5.2, "Bidirectional Mode" for detailed descriptions of each operating mode.
- All SPI transactions (send or receive) are initiated by writing a value to the SPI Data register (Section 16.7.3, "SPIDR - SPI Data Register") with the nBUSY bit deasserted '1' (Section 16.7.2.1, "D0 - nBUSY (Status)"). If only receive data is desired, a dummy data value must be written to SPIDR to start the packet transfer. If only transmit data is to be sent, invalid data will also be sampled from SPDIN and will be loaded into SPIDR at the end of the transaction.
- All received data can be sampled on a rising or falling SPCLK edge using RCLKPH (See Section 16.7.4.5, "D4 - RCLKPH - Receive Clock Phase" for clock controls). This clock setting must be identical to the clocking requirements of the current SPI slave.
- The transmit data is shifted out on the edge as selected by TCLKPH bit in the SPICC register (see Section 16.7.4.1, "D0 - TCLKPH - Transmit Clock Phase").
- The nBUSY bit (SPISR - Section 16.7.2.1, "D0 - nBUSY (Status)") is asserted '0' when a transfer is in progress and is deasserted '1' when a transfer is complete. A completed transfer also asserts the SPIDONE interrupt (See Section 16.8, "SPIDONE - 8051 Interrupt").
- When a transaction is completed in the full-duplex mode, the SPIDR always contains received data (valid or not) from the last transaction. When transmission is completed in the bi-directional mode, the SPIDR contains the transmitted data. When receive transaction is completed in the bi-directional mode, the SPIDR contains the received data. The length and order of data sent to and received from a SPI peripheral varies between peripheral devices. The SPI must be properly configured and software-controlled to communicate with each device and determine whether SPIDR data is valid slave data.
- Common peripheral devices require a chip select signal to be asserted during a transaction. Chip selects for SPI devices may be controlled by LPC47N350 GPIO pins.

16.5.1 Full Duplex Mode

- In Full Duplex Mode, serial data is transmitted and received simultaneously by the SPI master over two separate data transmission lines as shown in Figure 16.1 on page 175. See Section 16.7.1.2, "D1 - SPIMODE - SPI Mode," on page 180 for SPI mode configuration.

- Every data exchange is a simultaneous transmit and receive operation. Data shifted out of the master is shifted into the slave and data shifted out of the slave is shifted into the master synchronized by the master-driven SPCLK.

16.5.2 Bidirectional Mode

- SPI data can be transmitted and received over a single data line using Bidirectional mode. See Section 16.7.1.2, "D1 - SPIMODE - SPI Mode," on page 180 for SPI mode configuration.
- Input and output serial data share the SDOUT pin, as shown in Figure 16.1 on page 175 using the BIOEN bit (See Section 16.7.1.3, "D2 - BIOEN - Bidirectional Mode Output Enable," on page 180).
- The Software driver must properly drive the BIOEN bit and store received data depending on the transaction format of the specific slave device.

16.5.3 Baud Rate Generator

- The SPI Baud Rate Generator divides the SPI input clock to provide a SPCLK for SPI peripheral of various frequencies.
- The LPC47N350 SPI can be configured to run from the Ring Oscillator or a PLL source (See Section 16.7.4.3, "D2 - CLKSRC - SPI Clock Source," on page 183 and Section 16.7.4.4, "D3 - CLKEN - Clock Enable," on page 183). The PLL uses the 14.318 MHz input clock and is active under VCC2 power only. The Ring Oscillator frequency range is from 4MHz to 12 MHz. See Figure 16.1.

USER'S NOTE: The CLKSRC bit shouldn't be changed during SPI transaction.

- If the PLL output is selected, the SPICS0 and SPICS1 bits (See Section 16.7.5.2, "D7:D6 - PLL Clock Scale Bits," on page 185) in the SPI Baud Rate register can be used to scale the input clock (4 MHz, 8 MHz or 12 MHz) to the SPI Baud Rate Generator. If the ring oscillator is selected the SPICS0 and SPICS1 bits are ignored and the ring oscillator clock output is directly connected to the SPI Baud Rate Generator (see Section 16.7.5.1, "D2:D0 - SPI Clock Divider Bits," on page 184).
- The divisor bits (SPICD0, SPICD1 and SPICD2 - (see Section 16.7.5.1, "D2:D0 - SPI Clock Divider Bits," on page 184) in the SPI Baud Rate register can be programmed to divide down the clock from 1 to 128. Note that ring oscillator output varies from 4 MHz to 12 MHz. The actual SPCLK frequency will vary. The actual frequency of the ring oscillator can be determined by a proper algorithm. Describing such algorithm is beyond the scope of this document.
- The PLL will be stopped when VCC2 is removed. The input clock to the SPI block can be switched to ring oscillator, using the CLKSRC bit to operate the SPI Block, when VCC2 is removed.
- The 8051 should not be put into sleep mode in the middle of a transaction. If the 8051 goes in the sleep mode in the middle of a SPI transaction, the SPI transaction will be suspended. All the clocks to 8051, including PLL and ring oscillator, are stopped when 8051 is in the sleep mode.

16.6 External Interrupt from SPI Slave Device to Wake Up 8051

USER'S NOTE: External SPI slave devices that need to wakeup 8051 (when 8051 is in the sleep mode) can do so using a GPIO that is part of 8051 wakeup sources. An example is a Temperature Sensor slave device that compares the temperature reading with a set limit. If the temperature reading goes beyond the set limit, the slave device generates an interrupt to wakeup 8051 which processes the interrupt accordingly.

16.7 SPI Registers

There are 5 registers with which to control and monitor the status of the LPC47N350 SPI. These registers are 8051 MMCRs (See Table 7.7 on page 50). These registers return to their default values when the SPI is switched (using the MISC10 bit) from GPIO to SPI mode and from SPI to GPIO mode (See Section 16.4, "SGPIO vs. SPI Function Control") AND on VCC1 POR.

Table 16.3 LPC47N350 - SPI Registers

REGISTER	DESCRIPTION
SPICR	SPI Control Register
SPISR	SPI Status Register
SPIDR	SPI Data Register
SPICC	SPI Clock Control Register
SPIBR	SPI Baud Rate Register

16.7.1 SPICR - SPI Control Register

Table 16.4 SPI Control Register (SPICR)

HOST ADDRESS	N/A
8051 ADDRESS	BBh
POWER	VCC1
DEFAULT	00h on VCC1 POR and when MISC10 bit changes

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R/W	R/W	R/W
BIT NAME	Reserved					BIOEN	SPIMODE	LSBF

16.7.1.1 D0 - LSBF - Least Significant Bit First

When LSBF is deasserted '0', the 8-bit value from the SPI data register is transferred across the SPI interface in MSB-first order. When LSBF is asserted '1', the data is transferred in LSB-first order.

16.7.1.2 D1 - SPIMODE - SPI Mode

This bit configures the interface for Bidirectional or Full Duplex mode. When SPIMODE is deasserted '0', the interface will operate in Full Duplex mode (See Section 16.5.1, "Full Duplex Mode"). When SPIMODE is asserted '1', the interface will operate in Bidirectional mode (See Section 16.5.2, "Bidirectional Mode").

16.7.1.3 D2 - BIOEN - Bidirectional Mode Output Enable

When the SPI is configured for Bidirectional Mode (see Section 16.7.1.2, "D1 - SPIMODE - SPI Mode"), the BIOEN bit controls access to SDOUT. When BIOEN is deasserted '0', the SDOUT signal is configured as the serial data input. When BIOEN is asserted '1', the SDOUT signal is configured as the serial data output. See Figure 16.1 for details.

16.7.2 SPISR - SPI Status Register

Table 16.5 SPI Status Register (SPISR)

HOST ADDRESS	N/A
8051 ADDRESS	BCh
POWER	VCC1
DEFAULT	01h on VCC1 POR and when MISC10 bit changes

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R	R
BIT NAME	Reserved							nBUSY

16.7.2.1 D0 - nBUSY (Status)

The nBUSY bit reflects the state of the internal nBUSY signal. When nBUSY signal is asserted '0', a SPI transfer is in progress and data should not be written to the SPI Data register (SPIDR). Any writes to SPIDR while nBUSY signal is asserted will be ignored. When nBUSY signal is deasserted '1', a transaction has completed and the 8-bit value contained in the SPIDR is data acquired during the last transaction. Software must determine if the data contained in SPIDR is valid. New data may be written to SPIDR to begin a new transaction. When the nBUSY signal goes from '0' to '1' at the end of an SPI cycle, the 8051 SPIDONE interrupt is set (See Section 16.8, "SPIDONE - 8051 Interrupt"). See Figure 16.3 for nBUSY signal and SPIDONE functionality.

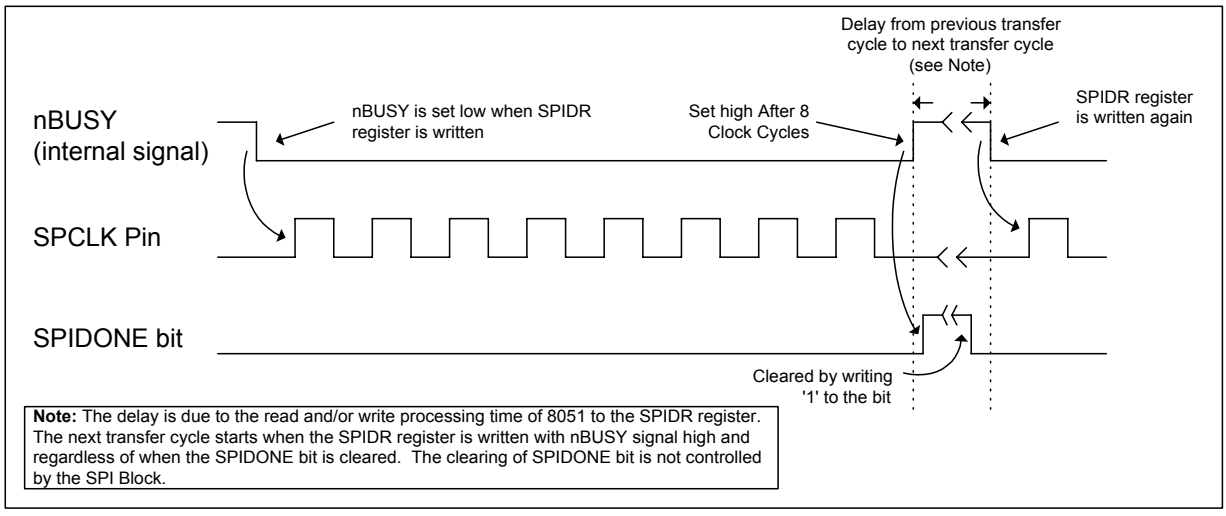


Figure 16.3 nBUSY and SPIDONE Functionality

16.7.3 SPIDR - SPI Data Register

Table 16.6 SPI Data Register (SPIDR)

HOST ADDRESS	N/A
8051 ADDRESS	BDh
POWER	VCC1
DEFAULT	00h on VCC1 POR and when MISC10 bit changes

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W See Note 16.1	R/W See Note 16.1	R/W See Note 16.1	R/W See Note 16.1	R/W See Note 16.1	R/W See Note 16.1	R/W See Note 16.1	R/W See Note 16.1
BIT NAME	SPIDR7	SPIDR6	SPIDR5	SPIDR4	SPIDR3	SPIDR2	SPIDR1	SPIDR0

A write to this register with the nBUSY bit deasserted '1' initiates an SPI transaction. At the end of an SPI transaction, SPIDR contains serial input data (valid or not) from the last transaction. Writes to SPIDR with the nBUSY bit asserted '0' are ignored.

Note 16.1 There are two SPI Data Registers that share the same address - one read only and one write only. However, reading the data register immediately after the data register is written may return invalid data. Reading the data register in the middle of SPI transaction will return invalid data. Any writes to the data register in the middle of SPI transaction is ignored.

16.7.4 SPICC - SPI Clock Control Register

Table 16.7 SPI Clock Control Register (SPICC)

HOST ADDRESS	N/A
8051 ADDRESS	BEh
POWER	VCC1
DEFAULT	00h on VCC1 POR and when MISC10 bit changes

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved			RCLKPH	CLKEN	CLKSRC	CLKPOL	TCLKPH

16.7.4.1 D0 - TCLKPH - Transmit Clock Phase

The TCLKPH bit determines the SPCLK edge on which the master will clock data out. When TCLKPH is deasserted '0', valid data is clocked out on the SPDOUT signal prior to the first SPCLK edge. The slave device should sample this data on the first and following odd SPCLK edges. When TCLKPH is asserted '1', data on SPDOUT signal is clocked out on the first SPCLK edge. The slave device should sample this data on the second and following even SPCLK edges. Note that this functionality is independent of the polarity of SPCLK. See Section 16.9, "SPI Timings" for timing diagrams.

16.7.4.2 D1 - CLKPOL - SPI Clock Polarity

This bit controls the polarity of the SPI clock. When CLKPOL is deasserted '0', the SPCLK is low when the interface is idle and the first clock edge is a rising edge. When CLKPOL is asserted '1', the first clock edge is a falling edge and the SPCLK signal is high when the interface is idle. See Section 16.9, "SPI Timings" for timing diagrams.

16.7.4.3 D2 - CLKSRC - SPI Clock Source

When CLKSRC is deasserted '0', the SPI is running from the Ring Oscillator. When CLKSRC is asserted '1', the SPI is running from the PLL.

USER'S NOTE: The CLKSRC bit shouldn't be changed during SPI transaction.

16.7.4.4 D3 - CLKEN - Clock Enable

This bit enables the clock into the SPI logic. When CLKEN is deasserted '0', the clock source into the SPI logic is disabled. When CLKEN is asserted '1', the clock source into the SPI logic is enabled.

16.7.4.5 D4 - RCLKPH - Receive Clock Phase

The RCLKPH bit determines the SPCLK edge on which the master will sample data. When RCLKPH is deasserted '0', valid data is expected on the SPDIN signal on the first SPCLK edge. This data is sampled on the first and following odd SPCLK edges. When RCLKPH is asserted '1', data on SPDIN signal is expected after the first SPCLK edge. This data is sampled on the second and following even

SPCLK edges. Note that this functionality is independent of the polarity of SPCLK. See Section 16.9, "SPI Timings" for timing diagrams.

16.7.5 SPIBR - SPI Baud Rate Register

Table 16.8 SPI Baud Rate Register (SPIBR)

HOST ADDRESS	N/A
8051 ADDRESS	BFh
POWER	VCC1
DEFAULT	00h on VCC1 POR and when MISC10 bit changes

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R/W	R	R	R	R/W	R/W	R/W
BIT NAME	SPICS1	SPICS0	Reserved			SPICD2	SPICD1	SPICD0

16.7.5.1 D2:D0 - SPI Clock Divider Bits

The clock divider bits (SPICD2:SPICD0) configure the rate of the SPI Baud Rate Generator after clock source is selected and pre-scaled. Table 16.9 shows various SPCLK frequencies. The columns for PLL Source show the frequencies when the PLL source is pre-scaled and divided down. The ROSC column shows the relationship between the ring oscillator frequency and the divider bits. Note when the ring oscillator is selected, the SPCLK frequency will vary since the ring oscillator (ROSC) frequency varies from 4MHz to 12MHz

.

Table 16.9 SPCLK Frequencies

SPICD2 BIT	**SPICD1 BIT**	**SPICD0 BIT**	**DIVIDE RATIO**	**PLL SOURCE**			**ROSC**
				4 MHZ	**8 MHZ**	**12 MHZ**	
0	0	0	1	4 MHz	8 MHz	12 MHz	ROSC / 1
		1	2	2 MHz	4 MHz	6 MHz	ROSC / 2
	1	0	4	1 MHz	2 MHz	3 MHz	ROSC / 4
		1	8	500 kHz	1 MHz	1.5 MHz	ROSC / 8
1	0	0	16	250 kHz	500 kHz	750 kHz	ROSC / 16
		1	32	125 kHz	250 kHz	375 kHz	ROSC / 32
	1	0	64	62.5 kHz	125 kHz	187.5 kHz	ROSC / 64
		1	128	31.3 kHz	62.5 kHz	93.75 kHz	ROSC / 128

16.7.5.2 D7:D6 - PLL Clock Scale Bits

These bits scale the clock source to the SPI Baud Rate Generator when the BRG clock source is the PLL. These bits only apply when CLKSRC bit in the SPI Clock Control Register is set to '1' for the PLL. The D7 and D6 are ignored when CLKSRC is deasserted '0'. See Section 16.5.1, "Full Duplex Mode" for information and supported frequencies.

Table 16.10 SPI Baud Rate Generator Clock Sources

D7 (SPICS1)	D6 (SPICS0)	CLOCK
0	0	4 MHz
0	1	8 MHz
1	0	12 MHz
1	1	Reserved

16.8 SPIDONE - 8051 Interrupt

- SPIDONE interrupt is in Wakeup Source Register 7 and Wakeup Mask Register 7. See Table 7.25 on page 73, Table 7.32 on page 77, and Figure 7.4 on page 65.
- The SPIDONE interrupt notifies the 8051 MCU that the SPI interrupt has completed an 8-bit serial transaction. The SPIDONE interrupt is asserted whenever the SPINT (internal signal) goes from '0' to '1' at the end of SPI cycle. The SPINT is a pulse that is generated at the end of every SPI cycle (when the internal nBUSY signal goes from '0' to '1' - see Section 16.7.2.1, "D0 - nBUSY (Status)"). Writing a '1' to the SPIDONE clears it. The SPIDONE interrupt also generates 8051 INT5. The SPIDONE interrupt can be masked from generating 8051 INT5 (see Figure 7.4 on page 65) by using the mask bit in Wakeup Mask Register 7.

16.9 SPI Timings

Refer to Section 29.8, "Serial Peripheral Interface (SPI) Timings," on page 301.

16.10 SPI Examples

16.10.1 Full Duplex Mode Transfer Examples

16.10.1.1 Read Only

The slave device used in this example is a MAXIM MAX1080 10 bit, 8 channel ADC:

- The MISC10 bit is '1' and SPIMODE bit is deasserted '0' to enable the SPI interface in Full Duplex mode.
- The CLKPOL and TCLKPH bits are deasserted '0', and RCLKPH is asserted '1' to match the clocking requirements of the slave device.
- The LSBF bit is deasserted '0' to indicate that the slave expects data in MSB-first order.
- Assert #CS using a GPIO pin.
- Write a valid command word (as specified by the slave device) to the SPI Data register (SPIDR) with nBUSY deasserted '1'. The SPI master automatically clears the nBUSY bit, begins shifting the data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.

- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted (See Section 16.8, "SPIDONE - 8051 Interrupt"). The data now contained in SPIDR is invalid since the last cycle was initiated solely to transmit command data to the slave. This particular slave device drives '0' on the SPDIN pin to the master while it is accepting command data. This SPIDR data is ignored.
- Next, a dummy 8 bit data value (any value) as written to the SPIDR. The SPI master automatically clears the nBUSY bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted. The data now contained in SPIDR is the first half of a valid 16 bit ADC value. SPIDR is read and stored.
- The final SPI cycle is initiated when another 8 bit data value is written to the SPIDR. Note that this value may be another dummy value or it can be a new 8 bit command to be sent to the ADC. The new command will be transmitted while the final data from the last command is received simultaneously. This overlap allows ADC data to be read every 16 SPCLK cycles after the initial 24 clock cycle. The SPI master automatically clears the nBUSY bit, begins shifting the data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the final SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted. The data now contained in SPIDR is the second half of a valid 16 bit ADC value. SPIDR is read and stored.
- If a command was overlapped with the received data in the final cycle, #CS should remain asserted and the SPI master will initiate another SPI cycle. If no new command was sent, #CS is released and the SPI is idle.

16.10.1.2 Read/Write

The slave device used in this example is a Fairchild NS25C640 FM25C640 64K Bit Serial EEPROM. The following sub-sections describe the read and write sequences.

Read

- The MISC10 bit is '1' and SPIMODE bit is deasserted '0' to enable the SPI interface in Full Duplex mode.
- The CLKPOL, TCLKPH and RCLKPH bits are deasserted '0' to match the clocking requirements of the slave device.
- The LSBF bit is deasserted '0' to indicate that the slave expects data in MSB-first order.
- Assert CS# low using a GPIO pin.
- Write a valid command word (as specified by the slave device) to the SPI Data register (SPIDR) with nBUSY deasserted '1'. The SPI master automatically clears the nBUSY bit, begins shifting the data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted (See Section 16.8, "SPIDONE - 8051 Interrupt"). The data now contained in SPIDR is invalid since the last cycle was initiated solely to transmit command data to the slave. This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIDR data is ignored.

USER'S NOTE: External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

- Next, EEPROM address A15-A8 is written to the SPIDR. The SPI master automatically clears the nBUSY bit, begins shifting the address value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock. Note: The particular slave device ignores address A15-A13.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted (See Section 16.8, "SPIDONE - 8051 Interrupt"). The data now contained in SPIDR is invalid since the last cycle was initiated solely to transmit address to the slave. This particular slave

device tri-states the SPDIN pin to the master while it is accepting command data. This SPIDR data is ignored.

USER'S NOTE: External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

- Next, EEPROM address A17-A0 is written to the SPIDR. The SPI master automatically clears the nBUSY bit, begins shifting the address value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted (See Section 16.8, "SPIDONE - 8051 Interrupt"). The data now contained in SPIDR is invalid since the last cycle was initiated solely to transmit address to the slave. This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIDR data is ignored.

USER'S NOTE: External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

- Next, a dummy 8 bit data value (any value) as written to the SPIDR. The SPI master automatically clears the nBUSY bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted. The data now contained in SPIDR is the 8-bit EEPROM data. SPIDR is read and stored.
- If more than 8-bit data needs to be read, another dummy 8 bit value is written to the SPIDR. The SPI master automatically clears the nBUSY bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted. The data now contained in SPIDR is the second 8-bit EEPROM data. SPIDR is read and stored.
- If no more data needs to be received by the master, CS# is released and the SPI is idle. Otherwise, master continues reading the data by writing a dummy value to the SPIDR after every 8 clock cycles.

Write

- The MISC10 bit is '1' and SPIMODE bit is deasserted '0' to enable the SPI interface in Full Duplex mode.
- The CLKPOL, TCLKPH and RCLKPH bits are deasserted '0' to match the clocking requirements of the slave device.
- The LSBF bit is deasserted '0' to indicate that the slave expects data in MSB-first order.
- Assert WR# high using a GPIO pin.
- Assert CS# low using a GPIO pin.
- Write a valid write enable command word (as specified by the slave device) to the SPI Data register (SPIDR) with nBUSY deasserted '1'. The SPI master automatically clears the nBUSY bit, begins shifting the data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted (See Section 16.8, "SPIDONE - 8051 Interrupt"). The data now contained in SPIDR is invalid since the last cycle was initiated solely to transmit write enable command to the slave. This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIDR data is ignored.

USER'S NOTE: External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

- Write a valid write command word (as specified by the slave device) to the SPI Data register (SPIDR) with nBUSY deasserted '1'. The SPI master automatically clears the nBUSY bit, begins shifting the data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted (See Section 16.8, "SPIDONE - 8051 Interrupt"). The data now contained in SPIDR is

invalid since the last cycle was initiated solely to transmit command data to the slave. This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIDR data is ignored.

USER'S NOTE: External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

- Next, EEPROM address A15-A8 is written to the SPIDR. The SPI master automatically clears the nBUSY bit, begins shifting the address value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock. Note: The particular slave device ignores address A15-A13.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted (See Section 16.8, "SPIDONE - 8051 Interrupt"). The data now contained in SPIDR is invalid since the last cycle was initiated solely to transmit address to the slave. This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIDR data is ignored.

USER'S NOTE: External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

- Next, EEPROM address A17-A0 is written to the SPIDR. The SPI master automatically clears the nBUSY bit, begins shifting the address value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted (See Section 16.8, "SPIDONE - 8051 Interrupt"). The data now contained in SPIDR is invalid since the last cycle was initiated solely to transmit address to the slave. This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIDR data is ignored.

USER'S NOTE: External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

- Next, data bits D7-D0 is written to the SPIDR. The SPI master automatically clears the nBUSY bit, begins shifting the address value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted (See Section 16.8, "SPIDONE - 8051 Interrupt"). The data now contained in SPIDR is invalid since the last cycle was initiated solely to transmit data to the slave. This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIDR data is ignored.

USER'S NOTE: External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

- If no more data needs to be received by the master, CS# is released and the SPI is idle. Otherwise, master continues writing data (up to max byte page allowed by the device) to the SPIDR after every 8 clock cycles.

16.10.2 Bidirectional Mode Transfer Example

The slave device used in this example is a National LM74 12 bit (plus sign) temperature sensor.

- The MISC10 bit is asserted '1' and the SPI interface is enabled.
- The interface is configured for Bidirectional mode by asserting ('1') the SPIMODE bit.
- The CLKPOL, TCLKPH and RCLKPH bits are deasserted '0' to match the clocking requirements of the slave device.
- The LSBF bit is deasserted '0' to indicate that the slave expects data in MSB-first order.
- BIOEN is asserted '0' to indicate that the first data in the transaction is to be received from the slave.
- Assert #CS using a GPIO pin.
- Write a dummy command byte to the SPI Data register (SPIDR) with nBUSY deasserted '1'. The SPI master automatically clears the nBUSY bit, begins shifting the data value and driving the SPCLK. This data is lost because the output buffer is disabled. Data on the SPDIN pin is sampled on each clock.

- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted (See Section 16.8, "SPIDONE - 8051 Interrupt"). The data now contained in SPIDR is the first half of the 16 bit word containing the temperature data. This SPIDR data is stored.
- Next, another dummy 8 bit data value is written to the SPIDR. The SPI master automatically clears the nBUSY bit, begins shifting the dummy data value and drives the SPCLK pin. Data on the SPDIN pin is sampled on each clock. The last 3 bits of this byte are used as a bus turnaround. The peripheral device sends '1' and tri-states its output for last two bits assuming that next data byte will be driven by the master.

USER'S NOTE: External pull-up or pull-down is required if the SPDIN is tri-stated by the slave device.

- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted. The data now contained in SPIDR is the last half of the 16 bit word containing the temperature data. SPIDR is read and stored.
- BIOEN is asserted '1' to indicate that data will now be driven by the master.
- The next SPI cycle is initiated when another 8 bit data value is written to the SPIDR. This value is the first half of a 16 bit command to be sent to temperature sensor peripheral. The SPI master automatically clears the nBUSY bit, begins shifting the data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is sampled on each clock.
- After 8 clocks, the SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted. The data now contained in SPIDR is ignored.
- The final SPI cycle is initiated when another 8 bit data value is written to the SPIDR. This value is the second half of a 16 bit command to be sent to temperature sensor peripheral. The SPI master automatically clears the nBUSY bit, begins shifting the data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 clocks, the final SPI cycle is complete, nBUSY is deasserted '1', and the SPIDONE interrupt is asserted. The data now contained in SPIDR is ignored.
- #CS is deasserted.

Chapter 17 Mailbox Register Interface

17.1 Overview

The Mailbox Registers Interface provides a standard run-time mechanism for the host to communicate with the 8051 and other logical components in the LPC47N350. The Mailbox Registers Interface includes a total of 52 index-addressable 8-bit registers (Table 17.1) and two 8-bit host access ports (Table 17.3). Thirty-two of these 52 registers are 8051 Mailbox registers.

The Mailbox Registers Interface host access ports are run-time registers that occupy two addresses in the system I/O space. The access ports are used by the host to read and write the 48 registers. The access ports base address is determined by the Mailbox Registers Interface Base Address that is initialized in Logical Device Number 9 in LPC47N350 configuration registers CR60 and CR61 (Table 17.2).

The 32 Mailbox registers as well as the PWM registers and Flash registers are directly addressable by the 8051 through Memory-Mapped Control Registers (see Table 7.7, “8051 On-Chip External Memory Mapped Registers,” on page 50).

In this specification, the registers in the Mailbox Registers Interface are identified by the prefix MBX in front of a hexadecimal index address. Table 17.1 summarizes the 52 registers in the Mailbox Registers Interface.

Table 17.1 Mailbox Registers Interface

REGISTER NAME	MAILBOX INDEX ADDR	SYSTEM R/W	8051 ADDR. (7F00+)	8051 R/W	POWER PLANE	VCC1 POR	VCC2 POR	NOTES
Flash Low Address	MBX80h	R/W	B1h	R/W	VCC1	00h	-	
Flash Data	MBX81h		B2h				-	
System-to-8051 Mailbox register 0-	MBX82h		08h	RC			-	
8051-to-system Mailbox register 1	MBX83h	RC	09h	R/W				Note 17.1
Mailbox register [2-F]	MBX 84h-91h	R/W	0Ah – 17h	R/W				Note 17.2
PWM0 Speed Control register	MBX92h		25h	R/W				
PWM1 Speed Control register	MBX93h		26h	R/W				
8051STP_CLK	MBX94h		-	-				
PWM2 register	MBX95h		29h	R/W	VCC2			
ESMI source register	MBX96h		-	-			00h	
ESMI mask register	MBX97h		-	-			00h	
PWM3 Speed Control Register	MBX98h		95h	R/W	VCC1	00h		
PWM3 Control Register	MBX99h		96h	R/W		04h		
Reserved	MBX9Ah	R	-	-	-		-	

Table 17.1 Mailbox Registers Interface (continued)

REGISTER NAME	MAILBOX INDEX ADDR	SYSTEM R/W	8051 ADDR. (7F00+)	8051 R/W	POWER PLANE	VCC1 POR	VCC2 POR	NOTES
UART1 FIFO Control Shadow register	MBX9Bh	R	-	-	VCC2		00h	
Reserved	MBX9Ch		-	-				Note 17.3
PWM Control Register	MBX9Dh	R/W	28h	R/W	VCC1	30h	-	
Flash Program Register	MBX9Eh		35h				-	
Flash High Address	MBX9Fh		B0h			00h	-	
Mailbox Register [10-1F]	MBX A0h-AFh		70h – 7Fh				-	
PWM0 Frequency Multiply	MBXB0h		97h				-	
PWM1 Frequency Multiply	MBXB1h		98h				-	
PWM2 Frequency Multiply	MBXB2h		99h		VCC2	-	00h	
PWM3 Frequency Multiply	MBXB3h		9Ah		VCC1	00h	-	

Note 17.1 Interrupt is cleared when read by the 8051.

Note 17.2 Interrupt is cleared when read by the host.

Note 17.3 This register is reserved and should not be accessed.

17.2 Mailbox Registers Interface Base Address

Logical Device 9 in the LPC47N350 configuration space supports the Mailbox Registers Interface. The three device configuration registers in LDN9 provide activation control and the base address for the Mailbox Registers Interface run-time registers (Table 17.2).

Register 0x30 is the Activate register. The activation control (LDN9:CR30.0) qualifies address decoding for the Mailbox Registers Interface; e.g., if the Activate bit D0 in the Activate register is “0”, the MBX access port addresses will not be decoded; if the Activate bit is “1”, MBX access port addresses will be decoded depending on the values programmed in the MBX Primary Base Address registers.

Registers 0x60 and 0x61 are the MBX Primary Base Address registers. Register 0x60 is the MBX Primary Base Address High Byte, register 0x61 is the MBX Primary Base Address Low Byte.

Note: Bit D0 in the MBX Primary Base Address Low Byte must be “0”. Valid Mailbox Registers Interface Base Address values are 0x0000 – 0x0FFE.

Table 17.2 Mailbox Registers Interface Configuration Controls (LDN9)

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1 & VCC0 POR	DESCRIPTION							
						D7	D6	D5	D4	D3	D2	D1	D0
0x30	R/W	0x00	0x00	0x00	-	Activate							

Table 17.2 Mailbox Registers Interface Configuration Controls (LDN9) (continued)

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1 & VCC0 POR	DESCRIPTION							
						RESERVED							Activate
0x60	R/W	0x00	0x00	0x00	-	MBX Primary Base Address High Byte							
						“0”	“0”	“0”	“0”	A11	A10	A9	A8
0x61	R/W	0x00	0x00	0x00	-	MBX Primary Base Address Low Byte							
						A7	A6	A5	A4	A3	A2	A1	“0”

17.3 Mailbox Registers Interface Access Ports

The Mailbox registers access ports are runtime registers that occupy two addresses in the Host I/O space (Table 17.3).

To access a Mailbox register once the Mailbox Registers Interface Base Address has been initialized, write the Mailbox register index address to the MBX Index port and read or write the Mailbox register data from the MBX data port.

Table 17.3 Mailbox Registers Interface Access Ports

ACCESS PORT NAME	HOST ADDRESS	HOST TYPE	POWER PLANE	VCC2 POR	VCC1 POR
MBX INDEX	MBX Base Address	R/W	VCC2	0x00	-
MBX DATA	MBX Base Address + 1			-	-

17.4 Mailbox Registers

There are 32 Mailbox Registers in the LPC47N350. The MBXA0–AF and MBX84– 91 Mailbox Registers are general purpose registers. There are no interrupts for these registers.

17.5 The System/8051 Interface Registers

Mailbox Register 0, System-to-8051, and Mailbox Register 1, 8051-to-System, are specifically designed to pass commands between the host and the 8051 (Figure 17.1). If enabled, these registers can generate interrupts.

Mailbox Register 0 and Mailbox Register 1 are not dual-ported, so the System BIOS and Keyboard BIOS must be designed to properly share these registers. When the host performs a write of the System-to-8051 mailbox register, an 8051 INT1 will be generated and seen by the 8051 if unmasked. When the 8051 writes to the System-to-8051 mailbox register, the data is blocked but the write forces the register to 0x00, providing a simple means for the 8051 to inform the host that an operation has been completed.

When the 8051 writes the 8051-to-System mailbox register, an SMI may be generated and seen by the host if unmasked. When the Host CPU writes to the 8051-to-System mailbox register, the data is blocked but the write forces the 8051-to-System register to clear to zero, providing a simple means for the host to inform that 8051 that an operation has been completed.

PROGRAMMER’S NOTE: The protocol used to pass commands back and forth through the Mailbox Registers Interface is left to the system designer. SMSC can provide an application example of working code in which the host uses the Mailbox registers to gain access to all of the 8051 registers.

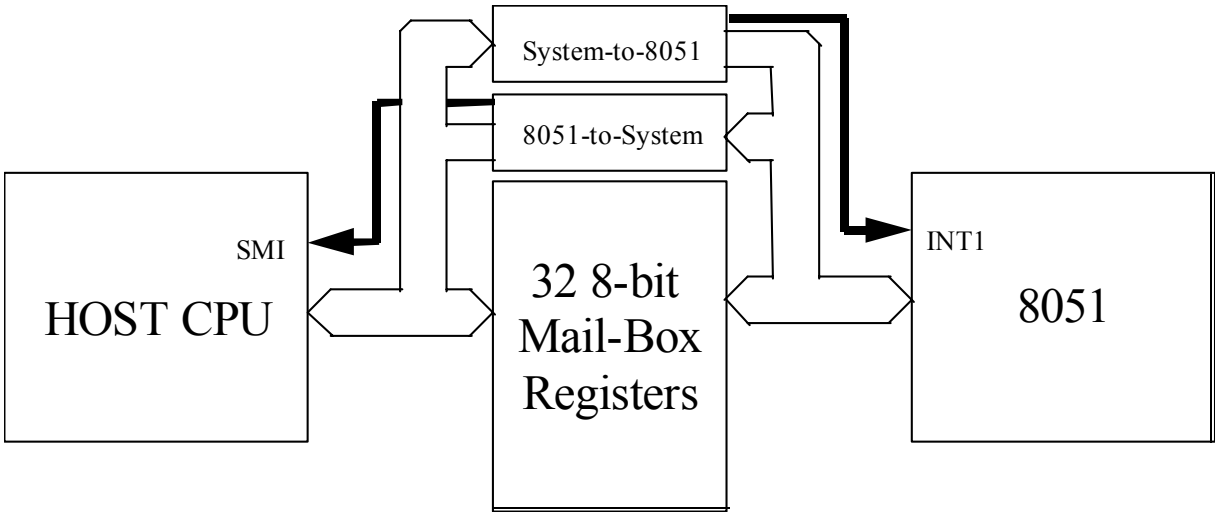


Figure 17.1 System-to-8051 Mailbox Interface Registers Block Diagram

17.5.1 Mailbox Register 0: System-to-8051

If enabled, an INT1 will be generated when the System writes to Mailbox Register 0 (Table 17.4). The interrupt source bit will be cleared when the 8051 reads this register.

After reading Mailbox Register 0, the 8051 can clear the register to “00H” by a dummy write to inform the host that the register contents have been read.

Table 17.4 Mailbox Register 0 (System-To-8051)

MAILBOX INDEX	0x82
8051 ADDRESS	0x7F08
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE (Note 17.4)	RC	RC	RC	RC	RC	RC	RC	RC
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0

Note 17.4 RC = Read-only register is cleared when written.

17.5.2 Mailbox Register 1: 8051-to-System

If enabled, an SMI will be generated when the 8051 writes to Mailbox Register 1 (Table 17.5). The SMI interrupt will be cleared when the host reads this register.

After reading Mailbox Register 1, the system can clear the register to “00H” by a dummy write to inform the 8051 that the register has been read.

Table 17.5 Mailbox Register 1 (8051-To-System)

MAILBOX INDEX	0x83
8051 ADDRESS	0x7F09
POWER	VCC1
DEFAULT	0x00

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MBX TYPE (Note 17.5)	RC	RC	RC	RC	RC	RC	RC	RC
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0

Note 17.5 RC = Read-only register is cleared when written.

17.6 8051 Stop Clock Register

The LPC Host can use the STP_CLK bit to stop the 8051 clock, for example when the LPC Bus Flash Program Access interface is used to update the 64k Embedded Flash.

Figure 17.2 illustrates the sequence the LPC Host must follow to stop the 8051 clock. The 8051 STP_CLK Register shown in Table 17.6 contains the STP_CLK bit.

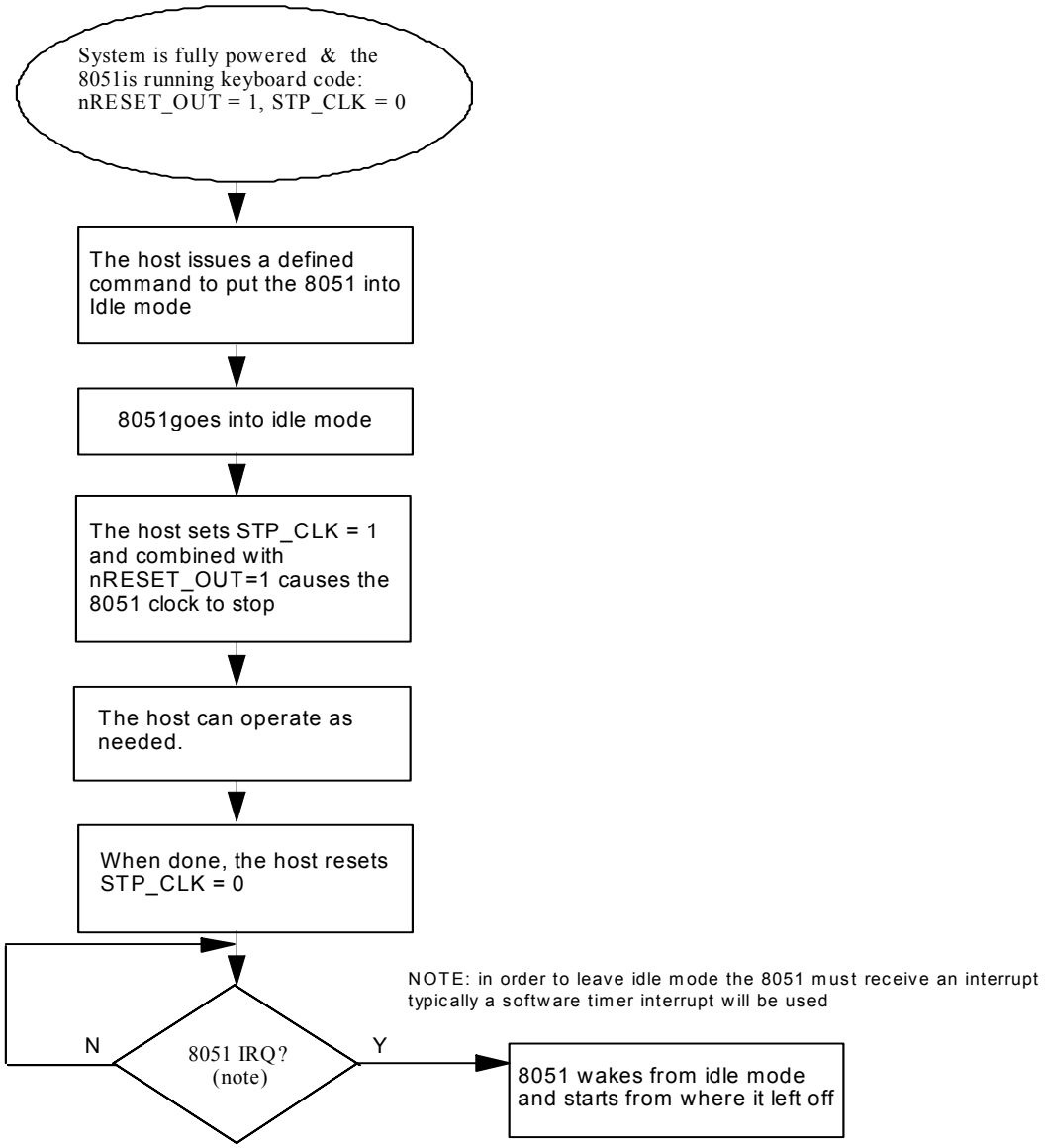


Figure 17.2 LPC Host Sequence to Stop the 8051

Table 17.6 8051 STP_CLK Register

HOST ADDRESS	MBX94h
8051 ADDRESS	N/A
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R	R/W
BIT NAME	IDLE	Reserved						STP_CLK

IDLE Bit – D7

When the IDLE bit is ‘0’, the 8051 is not in idle mode; when the IDLE bit is ‘1’, the 8051 is in idle mode. The IDLE bit is read-only.

STP_CLK Bit – D0

When the STP_CLK bit is ‘1’, the 8051 clock is stopped only when the nRESET_OUT pin is deasserted; when the STP_CLK bit is ‘0’, the 8051 clock can run. The STP_CLK bit is read/write. See Section 7.8.3.5, "Output Enable Register," on page 62.

17.7 ESMI Registers

The host can enable/disable the SMI interrupts generated as a result of the 8051 writing to Mailbox register 1. The host can read the ESMI source register to determine for the LPC47N350 Mailbox interface was the cause of the SMI.

Table 17.7 ESMI Source Register

HOST ADDRESS	MBX96
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R/W	R	R	R
BIT NAME	Reserved				8051_WR	Reserved		

8051_WR

This bit is set when a 8051-to-host mailbox has been written. This bit is cleared by a read of Mailbox Register 1 (MBX83).

Table 17.8 ESMI Mask Register

HOST ADDRESS	MBX97
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R/W	R	R	R
BIT NAME	Reserved				ESMI_MASK	Reserved		

ESMI_MASK

Setting this bit masks the 8051-to-host mailbox SMI.

Chapter 18 Pulse Width Modulators

18.1 Overview

The LPC47N350 has four independent programmable Pulse-Width Modulators (PWM0, PWM1 and PWM2) that can be used for controlling fan speed. The PWM0, PWM1, and PWM3 have 6-bit pulse-width resolution, have the ability to force the PWM output always high or low, and they can generate several fan speeds (F_{OUT}) as shown in Table 18.1. The PWM2 however, generates fewer fan speeds because there is no PWM2 STDBY CLOCK implementation, see Table 18.2.

PWM0, PWM1, and PWM3 can be driven by the system clock when VCC2 is active, or by the 32.768kHz standby clock (RTC) that is available when either VCC2 or VCC1 are active. PWM2 can only be driven by system clock when VCC2 is active. The PWM2 pin will tri-state when VCC2 = 0v (See Note 2.2).

PROGRAMMER'S NOTE: The availability of the 32kHz standby clock is subject to the affects of the RTC clock control bits.

The PWM Speed Control and PWM Control registers are accessible to both the Host and the 8051 through the Mailbox register interface (see Chapter 17, Mailbox Register Interface).

Table 18.1 PWM0, PWM1, and PWM3 Speed Control Summary

PWMX STDBY CLOCK BIT (Note 18.5)	PWMX CLOCK CONTROL BIT (Note 18.1)	PWMX CLOCK MULTI-PLIER BIT (Note 18.2)	PWMX CLOCK SELECT 1 BIT (Note 18.3)	PWMX CLOCK SELECT 0 BIT (Note 18.4)	FREQUENCY MULTIPLIER BITS (Note 18.7)				6-BIT DUTY CYCLE CONTROL(DCC)	DUTY CYCLE (%)
					00 (1X)	01 (2X)	10 (4X)	11 (8X)		
					F_{OUT} (KHZ) (Note 18.6)	F_{OUT} (KHZ) (Note 18.6)	F_{OUT} (KHZ) (Note 18.6)	F_{OUT} (KHZ) (Note 18.6)		
0	0	X	X	X	0 (low)	0 (low)	0 (low)	0 (low)	0	(DCC ÷ 64) × 100
0	0	0	0	0	15.625	31.25	62.5	125	1-63	
0	0	0	0	1	23.44	46.875	93.75	187.5		
0	0	0	1	0	0.407	0.0814	0.1628	0.326		
0	0	0	1	1	0.061	0.122	0.244	0.488		
0	0	1	0	0	31.25	62.5	125	250		
0	0	1	0	1	46.875	93.75	187.5	375		
0	0	1	1	0	0.0814	0.244	0.488	0.977		
0	0	1	1	1	0.122					
0	1	X	X	X	0 (high)	0 (high)	0 (high)	0 (high)	-	-
1	0	X	X		0 (low)	0 (low)	0 (low)	0 (low)	0	-

Table 18.1 PWM0, PWM1, and PWM3 Speed Control Summary (continued)

PWMX STDBY CLOCK BIT Note 18.5	PWMX CLOCK CONTROL BIT Note 18.1	PWMX CLOCK MULTI-PLIER BIT Note 18.2	PWMX CLOCK SELECT 1 BIT Note 18.3	PWMX CLOCK SELECT 0 BIT Note 18.4	FREQUENCY MULTIPLIER BITS (Note 18.7)				6-BIT DUTY CYCLE CONTROL(DCC)	DUTY CYCLE (%)
					00 (1X)	01 (2X)	10 (4X)	11 (8X)		
					F_{OUT} (KHZ) Note 18.6	F_{OUT} (KHZ) Note 18.6	F_{OUT} (KHZ) Note 18.6	F_{OUT} (KHZ) Note 18.6		
1	0	X	0	0	.032	.032	.032	.032	1-63	(DCC ÷ 64) × 100
1	0	X	0	1	.064	.064	.064	.064		
1	0	X	1	0	.128	.128	.128	.128		
1	0	X	1	1	Reserved	Reserved	Reserved	Reserved		
1	1	X	X	X	0 (high)	0 (high)	0 (high)	0 (high)	-	-

Note 18.1 This is PWM0/PWM1 Speed Control register bit 0.

Note 18.2 his is PWM Control register Bit 2 or Bit 3.

Note 18.3 This is PWM Control register Bit 0 or Bit 1.

Note 18.4 This is PWM0/PWM1 Speed Control register Bit 7.

Note 18.5 This is PWM Control register Bit 4 or Bit 5.

Note 18.6 The F_{out} frequency tolerance is ± 5%.

Note 18.7 This is PWM0/PWM1/PWM3 Frequency Multiply Register Bits 0 and Bits 1.

Table 18.2 PWM2 Speed Control Summary

PWM2 CLOCK CONTROL BIT Note 18.8	PWM2 CLOCK SELECT 1 BIT Note 18.10	PWM2 CLOCK MULTI-PLIER BIT Note 18.9	PWM2 CLOCK SELECT 0 BIT Note 18.11	FREQUENCY MULTIPLIER BITS (Note 18.7)				6-BIT DUTY CYCLE CONTROL (DCC)	DUTY CYCLE (%)
				00 (1X)	01 (2X)	10 (4X)	11 (8X)		
				F_{OUT} (KHZ) Note 18.12	F_{OUT} (KHZ) Note 18.12	F_{OUT} (KHZ) Note 18.12	F_{OUT} (KHZ) Note 18.12		
0	X	X	X	0 (low)	0 (low)	0 (low)	0 (low)	0	(DCC ÷ 64) × 100
	0	0	0	15.625	31.25	62.5	125	1-63	
			1	23.44	43.875	93.75	187.5		
		1	0	31.25	62.5	125	250		
			1	46.875	93.75	187.5	375		
	1	0	0	0.1831	0.3662	0.7324	1.4648		
		0	1	0.275	0.55	1.1	2.2		
		1	0	0.366	0.73332	1.46664	2.93328		
			1	0.55	1.1	2.2	4.4		
1	X	X	X	0 (high)	0 (high)	0 (high)	0 (high)	-	-

Note 18.8 This is PWM2 Speed Control register bit 0.

Note 18.9 This is PWM Control register Bit 7.

Note 18.10 This is PWM Control register Bit 6.

Note 18.11 This is PWM2 Speed Control register Bit 7.

Note 18.12 When the PWM2 Clock Control Bit = '0', Clock Select 0 = Clock Select 1 = '1', and the Clock Multiplier Bit = '0' (regardless of the Frequency Multiplier Bits selection), the frequency tolerance is ± 10 Hz. For all other combinations, the F_{out} frequency tolerance is ± 5%.

Note 18.13 This is PWM0/PWM1/PWM3 Frequency Multiply Register Bits 0 and Bits 1.

18.2 PWM Speed Control Registers

There are four PWM Speed Control registers: PWM0, PWM1, PWM2, and PWM3. These registers are located in the LPC47N350 Mailbox Registers Interface. PWM0 is MBX92, PWM1 is MBX93, PWM2 is MBX95, and PWM3 is MBX98 (see Table 17.1 on page 191).

The PWM Speed Control registers are in the LPC47N350 as shown in Table 18.3, Table 18.4 and Table 18.5.

The default values for all the PWM speed control registers are 0x00. These defaults take effect on VCC1 POR for PWM0, PWM1, and PWM3, and on VCC2 POR for PWM2 speed control register.

Table 18.3 PWM0 Speed Control Register

MAILBOX INDEX	0x92
8051 ADDRESS	0x7F25
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	PWM0 CLOCK SELECT 0	PWM0 DUTY CYCLE CONTROL						PWM0 CLOCK CONTROL

Table 18.4 PWM1 Speed Control Register

MAILBOX INDEX	0x93
8051 ADDRESS	0x7F26
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	PWM1 CLOCK SELECT 0	PWM1 DUTY CYCLE CONTROL						PWM1 CLOCK CONTROL

Table 18.5 PWM2 Speed Control Register

MAILBOX INDEX	0x95
8051 ADDRESS	0x7F29
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	PWM2 CLOCK SELECT 0	PWM2 DUTY CYCLE CONTROL						PWM2 CLOCK CONTROL

Table 18.6 PWM3 Speed Control Register

MAILBOX INDEX	0x98
8051 ADDRESS	0x7F85
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	PWM3 CLOCK SELECT 0	PWM3 DUTY CYCLE CONTROL						PWM3 CLOCK CONTROL

PWM Clock Select 0, D7

The PWM Clock Select 0 bit, D7 in the PWM Speed Control registers is used with the PWM Clock Select 1 and the PWM Clock Multiplier bits in the PWM Control register, and the Frequency Multiplier bits, to determine the fan speed FOUT.

Note: There are separate PWM0, PWM1 and PWM2 Clock Select 1 and Clock Multiplier bits in the PWM Control register (see Section 18.3). There is also a separate PWM3 Control Register for PWM3 Control Select 1 and Clock Multiplier bits

The affects of the PWM Clock Select[1:0] bits are shown in Table 18.1.

Duty Cycle Control, D6 – D1

The Duty Cycle Control (DCC) bits determine the PWM fan duty cycle. The LPC47N350 has ≈1.56% duty cycle resolution.

When DCC = “000000” (min. value), F_{OUT} is always low. When DCC is “111111” (max. value), F_{OUT} is almost always high; i.e., high for 63/64th and low for 1/64th of the F_{OUT} period.

Generally, the F_{OUT} duty cycle (%) is (DCC ÷ 64) × 100.

PWM Clock Control, D0

The PWM Clock Control bit, D0 is used to override the Duty Cycle Control bits and force F_{OUT} always high.

When D0 = “0”, the DCC bits determine the F_{OUT} duty cycle. When D0 = 1, F_{OUT} is always high, regardless of the state of the DCC bits.

18.3 PWM Control Register

The PWM Control register contains PWM Clock Select 1 and PWM Clock Multiplier for each of the three PWM Speed Controllers, PWM0, PWM1, and PWM2. The Standby Clock control bit is implemented only on PWM0 and PWM1.

The PWM Control register is MBX9D register (See Table 18.7). The default value for the PWM Control Register is 0x30. The default value takes effect on VCC1 POR.

For PWM3 Control Register, see Table 18.8.

Table 18.7 PWM Control Register

MAILBOX INDEX	0x9D
8051 ADDRESS	0x7F28
POWER	VCC1
DEFAULT	0x30

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	PWM2 CLOCK MULTI-PLIER	PWM2 CLOCK SELECT 1	PWM1 STDBY CLOCK	PWM0 STDBY CLOCK	PWM1 CLOCK MULTI-PLIER	PWM0 CLOCK MULTI-PLIER	PWM1 CLOCK SELECT 1	PWM0 CLOCK SELECT 1

PROGRAMMER’S NOTE: The PWMx STDBY CLOCK bits, D4 and D5, should not be switched when PWRGD is inactive; i.e., when VCC2 = 0V.

PWM2 Clock Multiplier, D7

The PWM2 Clock Multiplier bit, D7 is used with the PWM2 Clock Select 1 bit, D6, the PWM2 Clock Select 0 bit, MBX95.7, and the Frequency Multiplier bits, MBXB2.0 and MBXB2.1, to determine the PWM2 F_{OUT} .

When the PWM2 Clock Multiplier bit = “0”, no clock multiplier is used. When the PWM2 Clock Multiplier bit = “1”, the clock speed determined by the PWM2 Clock Select [1:0] bits is doubled (Table 18.2)

PWM2 Clock Select 1, D6

The PWM2 Clock Select 1 bit, D6 is used with the PWM2 Clock Multiplier bit, D7, the PWM2 Clock Select 0 bit, MBX95.7, and the Frequency Multiplier bits, MBXB2.0 and MBXB2.1, to determine the PWM2 F_{OUT} .

The affects of the Fan Clock Select [1:0] bits are shown in Table 18.2.

PWM1 STDBY Clock, D5

The PWM1 STDBY CLOCK bit D5 is used to determine the PWM1 controller clock source.

When the PWM1 STDBY CLOCK bit = “1”, the PWM1 controller clock source is the 32.768kHz RTC clock (VCC1/VCC2). The available PWM1 F_{OUT} frequencies when D5 = “1” are shown in Table 18.1.

When the PWM1 STDBY CLOCK bit = “0”, the PWM1 controller clock source is the system clock (VCC2). The available PWM1 F_{OUT} frequencies when D5 = “0” are shown in Table 18.1.

The PWM1 STDBY CLOCK bit default = “1”.

PWM0 STDBY Clock, D4

The PWM0 STDBY CLOCK bit, D4 is used to determine the PWM0 controller clock source.

When the PWM0 STDBY CLOCK bit = “1”, the PWM0 controller clock source is the 32.768kHz RTC clock (VCC1/VCC2). The available PWM0 F_{OUT} frequencies when D4 = “1” are shown in Table 18.1.

When the PWM0 STDBY CLOCK bit = “0”, the PWM0 controller clock source is the system clock (VCC2). The available PWM0 F_{OUT} frequencies when D4 = “0” are shown in Table 18.1.

The PWM0 STDBY CLOCK bit default = “1”.

PWM1 Clock Multiplier, D3

The PWM1 Clock Multiplier bit, D3 is used with the PWM1 Clock Select 1 bit, D1, the PWM1 Clock Select 0 bit, MBX93.7, and the Frequency Multiplier bits, MBXB1.0 and MBXB1.1, to determine the PWM1 F_{OUT} when the PWM1 STDBY CLOCK select bit is “0”.

When the PWM1 Clock Multiplier bit = “0”, no clock multiplier is used. When the PWM1 Clock Multiplier bit = “1”, the clock speed determined by the PWM1 Clock Select [1:0] bits is doubled (Table 18.1).

The PWM1 Clock Multiplier bit does not affect the PWM1 F_{OUT} when the PWM1 STDBY CLOCK select bit is “1”.

PWM0 Clock Multiplier, D2

The PWM0 Clock Multiplier bit, D2 is used with the PWM0 Clock Select 1 bit, D0, the PWM0 Clock Select 0 bit, MBX92.7, and the Frequency Multiplier bits, MBXB1.0 and MBXB1.1, to determine the PWM0 F_{OUT} when the PWM0 STDBY CLOCK select bit is “0”.

When the PWM0 Clock Multiplier bit = “0”, no clock multiplier is used. When the PWM0 Clock Multiplier bit = “1”, the clock speed determined by the PWM0 Clock Select [1:0] bits is doubled (Table 18.1).

The PWM0 Clock Multiplier bit does not affect the PWM0 F_{OUT} when the PWM0 STDBY CLOCK select bit is “1”.

PWM1 Clock Select 1, D1

The PWM1 Clock Select 1 bit, D1 is used with the PWM1 Clock Multiplier bit, D3, the PWM1 Clock Select 0 bit, MBX93.7, and the Frequency Multiplier bits, MBXB2.0 and MBXB2.1, to determine the PWM1 F_{OUT}.

The affects of the PWM1 Clock Select [1:0] bits are shown in Table 18.1.

PWM0 Clock Select 1, D0

The PWM0 Clock Select 1 bit, D0 is used with the PWM0 Clock Multiplier bit, D2, the PWM0 Clock Select 0 bit, MBX92.7, and the Frequency Multiplier bits, MBXB0.0 and MBXB0.1, to determine the PWM0 F_{OUT}.

The affects of the PWM1 Clock Select [1:0] bits are shown in Table 18.1.

Table 18.8 PWM3 Control Register

MAILBOX INDEX	0x99
8051 ADDRESS	0x7F96
POWER	VCC1
DEFAULT	0x.4

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R	R	R	R	R	R/W	R/W	R/W
8051 R/W	R	R	R	R	R	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	Reserved	PWM3 STDBY CLOCK	PWM3 CLOCK MULTIP LIER	PWM3 CLOCK SELECT 1

PROGRAMMER'S NOTE: The PWMx STDBY CLOCK bits, D4 and D5, should not be switched when PWRGD is inactive; i.e., when VCC2 = 0V.

PWM3 STDBY Clock, D2

The PWM3 STDBY CLOCK bit, D2 is used to determine the PWM3 controller clock source.

When the PWM3 STDBY CLOCK bit = "1", the PWM3 controller clock source is the 32.768kHz RTC clock (VCC1/VCC2). The available PWM3 F_{OUT} frequencies when D2 = "1" are shown in Table 18.1.

When the PWM3 STDBY CLOCK bit = "0", the PWM3 controller clock source is the system clock (VCC2). The available PWM3 F_{OUT} frequencies when D2 = "0" are shown in Table 18.1.

The PWM3 STDBY CLOCK bit default = "1".

PWM3 Clock Multiplier, D1

The PWM3 Clock Multiplier bit, D1, is used with the PWM3 Clock Select 1 bit, D0, the PWM3 Clock Select 0 bit, MBX98.7, and the Frequency Multiplier bits, MBXB3.0 and MBXB3.1, to determine the PWM3 F_{OUT} when the PWM3 STDBY CLOCK select bit is "0".

When the PWM3 Clock Multiplier bit = "0", no clock multiplier is used. When the PWM3 Clock Multiplier bit = "1", the clock speed determined by the PWM3 Clock Select [1:0] bits is doubled. See Table 18.1.

The PWM3 Clock Multiplier bit does not affect the PWM3 FOUT when the PWM3 STDBY CLOCK select bit is "1".

PWM3 Clock Select 1, D0

The PWM3 Clock Select 1 bit, D0 is used with the PWM3 Clock Multiplier bit, D1 and the PWM3 Clock Select 0 bit, MBX98.7, and the Frequency Multiplier bits, MBXB3.0 and MBXB3.1, to determine the PWM3 F_{OUT}.

18.4 Frequency Multiply Register

The Frequency Multiply bits are used with PWM Clock Select 0 bit, PWM Clock Select 1 bit, and PWM Clock Multiplier bit to select the frequency for PWM0, PWM1, PWM2, and PWM3. The PWM0, PWM1, and PWM3 also have PWM standby clock bits.

See Table 18.1 and Table 18.2.

Table 18.9 PWM0 Frequency Multiply Register

MAILBOX INDEX	0xB0
8051 ADDRESS	0x7F97
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R	R	R	R	R	R	R/W	R/W
8051 R/W	R	R	R	R	R	R	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Frequency Multiplier (See Table 18.13)	

Table 18.10 PWM1 Frequency Multiply Register

MAILBOX INDEX	0xB1
8051 ADDRESS	0x7F98
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R	R	R	R	R	R	R/W	R/W
8051 R/W	R	R	R	R	R	R	R/W	R/WS
BIT NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Frequency Multiplier (See Table 18.13)	

Table 18.11 PWM2 Frequency Multiply Register

MAILBOX INDEX	0xB2
8051 ADDRESS	0x7F99
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R	R	R	R	R	R	R/W	R/W
8051 R/W	R	R	R	R	R	R	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Frequency Multiplier (See Table 18.13)	

Table 18.12 PWM3 Frequency Multiply Register

MAILBOX INDEX	0xB3
8051 ADDRESS	0x7F9A
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R	R	R	R	R	R	R/W	R/W
8051 R/W	R	R	R	R	R	R	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Frequency Multiplier (See Table 18.13)	

Table 18.13 Frequency Multiplier Bits

BIT SELECTION FOR FREQUENCY MULTIPLIER BITS		DESCRIPTION
00	1x	1x the current frequency selected for PWM
01	2x	2x the current frequency selected for PWM
10	4x	4x the current frequency selected for PWM
11	8x	8x the current frequency selected for PWM

Chapter 19 Fan Tachometer Interface

19.1 Fan Tachometer Overview

The LPC47N350 implements a dual fan tachometer interface for systems with fans equipped with speed monitoring outputs. The fan tachometer input pins are FAN_TACH1 and FAN_TACH2 (Table 2.2). These pins are alternate functions of the GPIO15 and GPIO16 pins, respectively (See Table 2.4 and MICS[11 bit in Section 21.4, "Multiplexing_2 Register - MISC[16:9]"). The timebase for the fan tachometer interface is the 32.768kHz RTC oscillator (Figure 19.1). A fan tachometer input gates the 32.768 kHz RTC oscillator for one period of the input signal into an 8-bit counter. As shown in Figure 19.1, one fan revolution, $T_{R,}$ consists of two fan tachometer pulses, $T_{P.}$ The fan tachometer interface can generate an 8051 interrupt and wake event when the fan speed (RPM) drops below a predetermined value. The fan tachometer interface is available when VCC2 is active and on the suspend supply, VCC1.

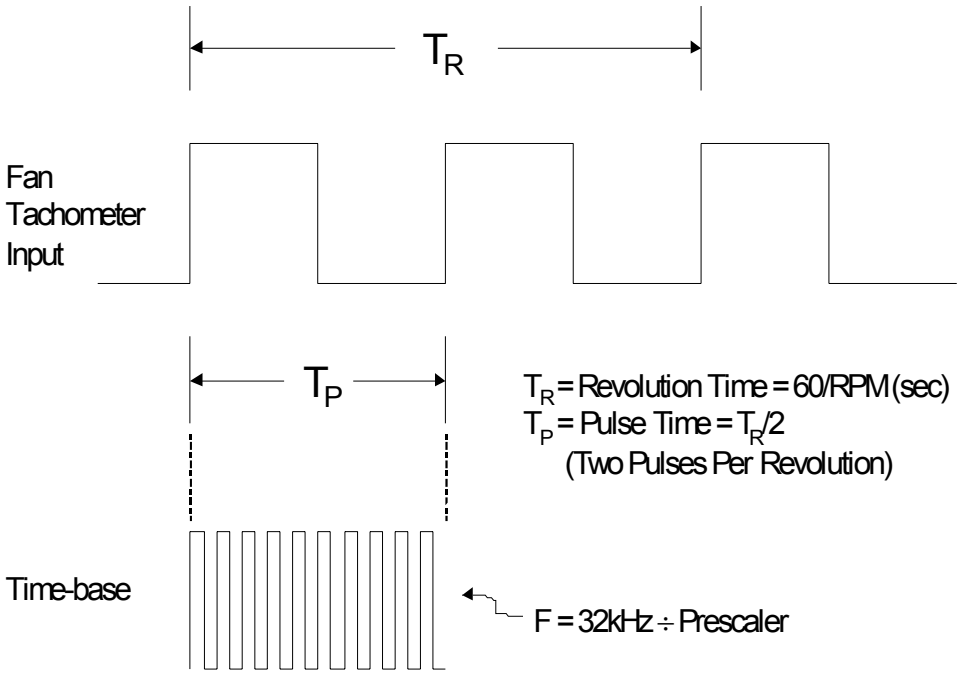


Figure 19.1 Fan Tachometer Input and Time-Base

19.2 Theory of Operation

Each fan tachometer in the dual fan tachometer interface contains a Timebase Prescaler, a Fan Pulse Counter, a Fan Pulse Counter Preload, a Fan Pulse Counter Read Latch, and a Fan Pulse Counter Threshold Detector (Figure 19.2). Detailed descriptions of these components follow in the subsections, below.

19.2.1 Timebase Prescaler

The timebase prescaler divides the fan tachometer timebase. The timebase prescaler can be used to account for several fan types (i.e., fans where the RPM values do not depend on two fan tachometer pulses per revolution) and a wide range of fan speeds. The prescaler for each fan tachometer is programmable via the FAN Tachometer Timebase Prescaler Register (see Section 19.8, "FAN Tachometer Timebase Prescaler Register"). The choices for the timebase prescaler are 1, 2, 4 and 8; the default is 2.

19.2.2 Fan Pulse Counter and Read Latch

The fan pulse counter measures the fan pulse time, $T_{p,}$ shown in Figure 19.1. The fan pulse counter is reset by the rising edge of each fan tachometer input pulse and by writing the counter preload register. The fan pulse counter does not wrap. For example, when the counter reaches 0xFF, it remains at 0xFF until the counter is reset by the next input pulse or by writing the Preload register. The host can read the last maximum fan pulse counter value using the FAN1 and FAN2 Read Latch registers (see Section 19.3, "Example" and Section 19.4, "FAN1 Read Latch Register", below). The fan pulse counter equation is shown in Table 19.1. The factor of ½ in first term of the equation accounts for the fan Revolution Time T_R (i.e., two pulses per revolution as shown in Figure 19.1). The numerator of the second term is derived by multiplying the 32.768kHz timebase by 60sec/min. The denominator of the second term is the product of the fan RPM and the timebase prescaler.

19.2.3 Fan Pulse Counter Threshold Detector

The fan pulse counter threshold detector consists of the two AND'ed MSB outputs of the fan pulse counter. This corresponds to an upper limit for the fan pulse counter of 192. The outputs of the fan pulse counter threshold detectors are always asserted when the fan pulse count equals or exceeds 192. The outputs of the fan pulse counter threshold detectors are always deasserted when the fan pulse count is less than 192. If enabled, the 8051 receives an interrupt when the outputs of the fan pulse counter threshold detectors are asserted. For a description of the FAN TACH1 and FAN TACH2 8051 interrupt registers see Section 19.9, "8051 FAN Tachometer Interrupt Registers".

Table 19.1 Fan Pulse Counter Equation

$$\text{FAN PULSE COUNT} = \frac{1}{2} \times \frac{1.966 \times 10^6}{\text{RPM} \times \text{PRESCALER}}$$

19.2.4 Fan Pulse Counter Preload

The fan pulse counter preload is the initial value for the fan pulse counter which is used to scale the count so that the value of 192 corresponds to the "lower limit" of the threshold RPM. The fan pulse counter is initialized with the preload on the rising edge of the fan tachometer input pulse. Typically, the fan pulse counter preload value will be 192 minus the fan pulse count of the desired RPM trigger threshold. The counter preload value is programmable for each fan tachometer via the FAN1 and FAN2 Preload Registers (see Section 19.5, "FAN2 Read Latch Register" and Section 19.7, "FAN2 Preload Register"). By setting the fan pulse counter preload value and the timebase prescaler appropriately, the 8051 can be interrupted when the fan speed reaches the desired percentage of the nominal RPM to indicate fan failures for a wide range of fan types and speeds (see Section 19.3, "Example").

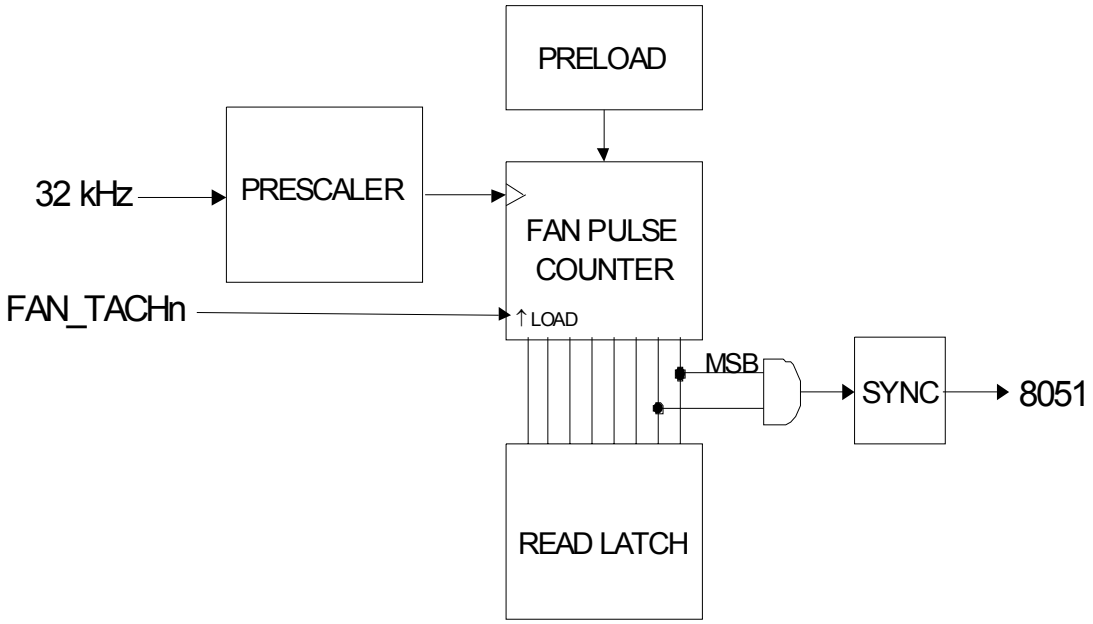


Figure 19.2 Fan Tachometer Block Diagram

19.3 Example

Table 19.2 illustrates a fan tachometer interface programming example for a 4400 RPM nominal fan. In this example, the system designer has specified a fan counter preload value of 33 so that the 8051 will be alerted when the fan speed drops below 70% nominal RPM.

Note: The values in Table 19.2 are based on a 2 pulse/revolution fan tachometer output with the default timebase prescaler of 2.

Table 19.2 4400 RPM Fan Tachometer Example

RPM (T_R)	PULSE TIME Note 19.1 (T_P)	FAN PULSE COUNT Note 19.2	PRELOAD	FAN PULSE COUNT + PRELOAD	DESCRIPTION	8051 INTERRUPT
4400	6.8 ms	111	33	144	Nominal RPM	NO
3960	7.6 ms	124		157	90% Nominal RPM	
3520	8.5 ms	139		172	80% Nominal RPM	
3080	9.7 ms	159		192	70% Nominal RPM	YES
2640	11.4 ms	186		219	60% Nominal RPM	
2200	13.6 ms	223		>255 (maximum count)	50% Nominal RPM	

Note 19.1 There are 2 fan tachometer pulses per fan revolution: $T_P = 60 \div (2 \times RPM)$.

Note 19.2 The timebase prescaler = 2.

19.4 FAN1 Read Latch Register

The FAN1 read latch register (Table 19.3) stores the maximum last fan pulse counter value before the rising edge of the next FAN1 tachometer input pulse. The fan pulse count is computed from the equation in Table 19.1. The FAN1 read latch register value may not be valid for up to 2 fan tachometer input pulses following a write to the preload register.

Table 19.3 FAN1 Read Latch Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F9B
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R	R
BIT NAME	D7	D6	D6	D6	D3	D2	D1	D0

19.5 FAN2 Read Latch Register

The FAN2 read latch register (Table 19.4) stores the last (maximum) fan pulse counter value before the rising edge of the FAN2 tachometer input pulse. The fan pulse count is computed from the equation in Table 19.1. The FAN2 read latch register value may not be valid for up to 2 fan tachometer input pulses following a write to the preload register.

Table 19.4 FAN2 Read Latch Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F9C
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R	R	R	R
BIT NAME	D7	D6	D6	D6	D3	D2	D1	D0

19.6 FAN1 Pulse Counter Preload Register

The FAN1 pulse counter preload register (Table 19.5) stores the preload value used in the computation of the FAN1 pulse count (see Section 19.2.4, "Fan Pulse Counter Preload"). The fan pulse count is computed from the equation in Table 19.1. Writing to the FAN1 pulse counter preload register resets the FAN1 pulse counter. The FAN1 read latch register value may not be valid for up to 2 fan tachometer input pulses following a write to the FAN1 pulse counter preload register.

Table 19.5 FAN1 Pulse Counter Preload Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F9D
POWER	VCC1
DEFAULT	0x00

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	D7	D6	D6	D6	D3	D2	D1	D0

19.7 FAN2 Preload Register

The FAN2 pulse counter preload register (Table 19.6) stores the preload value used in the computation of the FAN2 pulse count (see Section 19.2.4, "Fan Pulse Counter Preload"). The fan pulse count is computed from the equation in Table 19.1. Writing to the FAN2 pulse counter preload register resets the FAN2 pulse counter. The FAN2 read latch register value may not be valid for up to 2 fan tachometer input pulses following a write to the FAN2 pulse counter preload register.

Table 19.6 FAN2 Pulse Counter Preload Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F9E
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	D7	D6	D6	D6	D3	D2	D1	D0

19.8 FAN Tachometer Timebase Prescaler Register

The fan tachometer timebase prescaler register is shown below in Table 19.7. The timebase prescaler is described in Section 19.2.1, "Timebase Prescaler," on page 211.

Table 19.7 FAN Tachometer Timebase Prescaler Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F9F
POWER	VCC1
DEFAULT	0x05

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved				FAN2 PRESCALER 00: Prescaler = 1 01: Prescaler = 2 (DEFAULT) 10: Prescaler = 4 11: Prescaler = 8		FAN1 PRESCALER 00: Prescaler = 1 01: Prescaler = 2 (DEFAULT) 10: Prescaler = 4 11: Prescaler = 8	

19.9 8051 FAN Tachometer Interrupt Registers

The FAN TACH1 and FAN TACH 2 interrupts appear in the 8051 Wake Up SRC 7 and Wake Up MSK 7 registers See Figure 7.4, Figure 7.5, Table 7.25, and Table 7.32 in Section 7.9.

Chapter 20 GPIO Interface

20.1 Overview

The LPC47N350 includes four 8051 SFR-addressable GPIOs, twenty-nine 8051 non-SFR GPIOs, and eight LPC/8051-addressable GPIOs (Table 20.1).

The 8051 non-SFR GPIOs are described below in Section 20.2.

Sixteen of the twenty-four GPIOs can generate 8051 interrupts and wake events. See Figure 7.4, Figure 7.5, Figure 7.4, and Table 7.32 in Section 7.9.

Table 20.1 LPC47N350 GPIO Types

	TYPE	REGISTER CONTROL GROUP (Note 20.7)	PIN NAMES (Note 20.1)	WAKE CAPABLE (Note 20.2)	BUFFER MODES (Note 20.3)
1	8051 SFR	Group J	SGPIO30	N	PP
2			SGPIO31	N	PP
3			SGPIO32	N	PP
4			SGPIO33	N	PP
5	8051 SFR	Group D	OUT0	N	PP/OD
6			OUT1/nIRQ8	N	PP
7			OUT7/nSMI	N	PP
8	8051 (non-SFR)	Group E	OUT8/KBRST (Note 20.4)	N	PP
9			KSO12/OUT8/KBRST (Note 20.4)	N	OD
10			OUT9/PWM2	N	PP
11			OUT10/PWM0	N	PP
12			OUT11/PWM1	N	PP
13	8051 (non-SFR)	Group A	GPIO0 (WK_SE02)	Y	PP
14			GPIO1 (WK_SE03)	Y	PP
15			GPIO2 (WK_SE04)	Y	PP
16			GPIO3 (TRIGGER) (Note 20.5)	N	PP
17			GPIO4 (WK_SE07)/KSO14	Y	PP
18			GPIO5 (WK_SE10)/KSO15	Y	PP
19			GPIO6 (WK_SE11)	Y	PP
20			GPIO7 (WK_SE06)/PWM3	Y	PP/OD

Table 20.1 LPC47N350 GPIO Types (continued)

	TYPE	REGISTER CONTROL GROUP (Note 20.7)	PIN NAMES (Note 20.1)	WAKE CAPABLE (Note 20.2)	BUFFER MODES (Note 20.3)
21	8051 (non-SFR)	Group B	GPIO8 (WK_SE12)/RXD	Y	PP
22			GPIO9 (WK_SE13)/TXD	Y	PP
23			GPIO10 (WK_SE14)	Y	PP
24			GPIO11 (WK_SE15)/AB2A_DATA	Y	PP
25			GPIO12 (WK_SE16)/AB2A_CLK	Y	PP
26			GPIO13 (WK_SE17)/AB2B_DATA	Y	PP
27			GPIO14 (WK_SE20)/AB2B_CLK	Y	PP
28			GPIO15 (WK_SE21)/FAN_TACH1	Y	PP
29	8051 (non-SFR)	Group C	GPIO16 (WK_SE22)/FAN_TACH2	Y	PP
30			GPIO17 (WK_SE23)/A20M	Y	PP
31			KSO13/GPIO18 (WK_SE27) (Note 20.4)	Y	OD
32			GPIO19 (WK_SE24)	Y	PP
33			GPIO20 (WK_SE25)/PS2CLK	Y	OD
34			GPIO21 (WK_SE26)/PS2DAT	Y	OD
35	LPC/8051 (See Note 20.6)	Group G	LGPIO50	Y	PP
36			LGPIO51	Y	PP
37			LGPIO52	Y	PP
38			LGPIO53	Y	PP
39	LPC/8051 (See Note 20.6)	Group H	LGPIO60	N	PP/OD
40			LGPIO61	N	PP/OD
41			LGPIO62	N	PP/OD
42			LGPIO63	N	PP/OD

Note 20.1 The pin names for the pins are organized by primary pin function listed first. The alternate functions on the pin are separated by "/" (backslash).

Note 20.2 All non-SFR GPIOs that are wakeup capable can be configured for low-to-high, high-to-high, or either-edge wakeup. All alternate functions of wake-capable GPIO primary function pins can generate wake events.

Note 20.3 The buffer modes apply only to the GPIOs. PP = Push-Pull (Totem Pole) Outputs; PP/OD = Selectable Push-Pull or Open-Drain Outputs.

Note 20.4 The OUT8/KBRST functions are on KSO12/OUT8/KBRST pin and OUT8/KBRST pin.

Note 20.5 GPIO3 can be enabled to directly generate 8051 INT1.

Note 20.6 These pins can be controlled by the LPC Host or the 8051

20.2 8051 Non-SFR GPIOs

The 8051 non-SFR GPIO pins are listed in Table 20.1 Some 8051 non-SFR GPIOs are multiplexed with alternate functions (see Table 2.4).

All 8051 non-SFR registers are powered by VCC1. The following pins will tri-state to prevent back-biasing of external circuitry when they are configured as alternate function outputs and PWRGD is inactive (i.e. VCC2 is 0v): OUT1, OUT7, OUT8, OUT9, GPIO17, GPIO20, GPIO21, and KSO12.

PROGRAMMER'S NOTE: The direction of alternate function pins that are multiplexed with general purpose I/O pins (i.e., where the GPIO function is the default), is determined by the GPIO direction bit. For example, if the KSO14 function of GPIO4 is selected, bit 4 in GPIO Direction Register A must be set to "1". This rule does not apply to default non-GPIO pin functions that may have a GPIO as an alternate function.

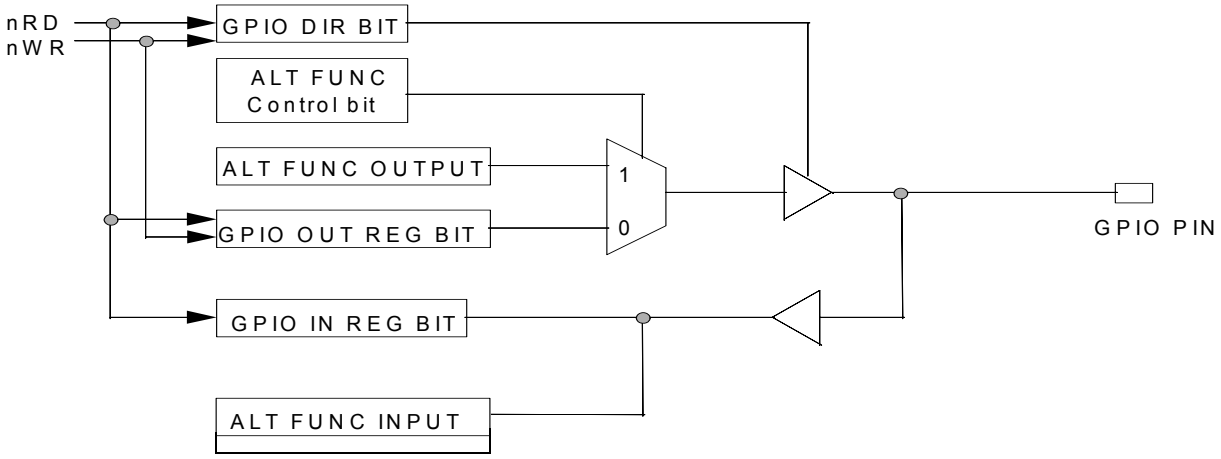


Figure 20.1 8051 Non-SFR GPIO Block Diagram

20.3 8051 Non-SFR Registers

Table 20.2 GPIO Direction Register A

HOST ADDRESS	N/A
8051 ADDRESS	0x7F18
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	GPIO7 1=output 0=input	GPIO6 1=output 0=input	GPIO5 1=output 0=input	GPIO4 1=output 0=input	GPIO3 1=output 0=input	GPIO2 1=output 0=input	GPIO1 1=output 0=input	GPIO0 1=output 0=input

Table 20.3 GPIO Output Register A

HOST ADDRESS	N/A
8051 ADDRESS	0x7F19
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 20.4 GPIO Input Register A

HOST ADDRESS	N/A
8051 ADDRESS	0x7F1A
POWER	VCC1
DEFAULT	N/A

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R
BIT NAME	status of pin GPIO7	status of pin GPIO6	status of pin GPIO5	status of pin GPIO4	status of pin GPIO3	status of pin GPIO2	status of pin GPIO1	status of pin GPIO0

Table 20.5 GPIO Direction Register B

HOST ADDRESS	N/A
8051 ADDRESS	0x7F1B
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	GPIO15 1=output 0=input	GPIO14 1=output 0=input	GPIO13 1=output 0=input	GPIO12 1=output 0=input	GPIO11 1=output 0=input	GPIO10 1=output 0=input	GPIO9 1=output 0=input	GPIO8 1=output 0=input

See Note 2.3.

Table 20.6 GPIO Output Register B

HOST ADDRESS	N/A
8051 ADDRESS	0x7F1C
POWER	VCC1
DEFAULT	0x00

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	GPIO 15	GPIO 14	GPIO 13	GPIO 12	GPIO 11	GPIO 10	GPIO 9	GPIO 8

Table 20.7 GPIO Input Register B

HOST ADDRESS	N/A
8051 ADDRESS	0x7F1D
POWER	VCC1
DEFAULT	N/A

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R
BIT NAME	status of pin GPIO15	status of pin GPIO14	status of pin GPIO13	status of pin GPIO12	status of pin GPIO11	status of pin GPIO10	status of pin GPIO9	status of pin GPIO8

Table 20.8 GPIO Direction Register C

HOST ADDRESS	N/A
8051 ADDRESS	0x7F1E
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	0	0	GPIO21 1=output 0=input	GPIO20 1=output 0=input	GPIO19 1=output 0=input	GPIO18 1=output 0=input	GPIO17 1=output 0=input	GPIO16 1=output 0=input

Table 20.9 GPIO Output Register C

HOST ADDRESS	N/A
8051 ADDRESS	0x7F1F
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	0	0	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16

Table 20.10 GPIO Input Register C

HOST ADDRESS	N/A
8051 ADDRESS	0x7F20
POWER	VCC1
DEFAULT	N/A

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R
BIT NAME	0	0	status of pin GPIO21	status of pin GPIO20	status of pin GPIO19	status of pin GPIO18	status of pin GPIO17	status of pin GPIO16

Table 20.11 Out Register D

HOST ADDRESS	N/A
8051 ADDRESS	0x7F22
POWER	VCC1
DEFAULT	0x00

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R					R/W	R/W
BIT NAME	OUT7	Reserved					OUT1	OUT0

Table 20.12 Out Register E

HOST ADDRESS	N/A
8051 ADDRESS	0x7F23
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	0	0	0	0	OUT11	OUT10	OUT9	OUT8

20.4 LPC/8051-Addressable GPIOs

The LPC47N350 includes eight LPC/8051-addressable LGPIO pins LGPIO50-LGPIO53, LGPIO60-LGPIO63 (See Table 2.1 and Table 2.2).

The output pin buffer type for LGPIO60-63 can be programmed by the 8051 as open-drain or push-pull (Section 20.4.3.4).

LGPIO50-LGPIO53 can generate 8051 interrupts and wake events. See Section 7.9, "8051 Interrupts". An interrupt will occur on either edge of signals connected to any LGPIO50-LGPIO53 pin configured as an input.

The LGPIO pins can be accessed either by the LPC host or the 8051 depending on the state of a group LPC SELECT bit (See Section 20.4.3.3). There are two 4-pin LGPIO groups. Host selection is determined by the 8051 per 4-pin group.

There are separate 8051 and LPC runtime register sets to control the LGPIO pins (See Section 20.4.2 and Section 20.4.3).

The 8051 is responsible for configuring the LGPIO interface including the LPC SELECT bits and the output pin buffer type.

When the LPC host is selected to control an LGPIO pin and PWRGD is deasserted, the pin is tristated (input). Otherwise, the LGPIO channel direction and logic state is determined by the runtime registers of the selected host (See Table 20.13, "LPC Addressable GPIO Direction Control" and Figure 20.2, "LPC Addressable GPIO Block Diagram").

Table 20.13 LPC Addressable GPIO Direction Control

	8051 DIR	LPC DIR	LPC SEL.	PWRGD	PIN DIR	COMMENTS
1.	X	X	1	0	IN	GPIO pin tristates (input) because GPIO is LPC type & VCC2 is invalid.
2.		1		1	OUT	GPIO pin is LPC type, follows LPC DIR bit & VCC2 is valid.
3.		0			IN	
4.	1	X	0	X	OUT	GPIO pin is 8051 type, follows 8051 DIR bit & VCC2 is not required.
5.	0				IN	

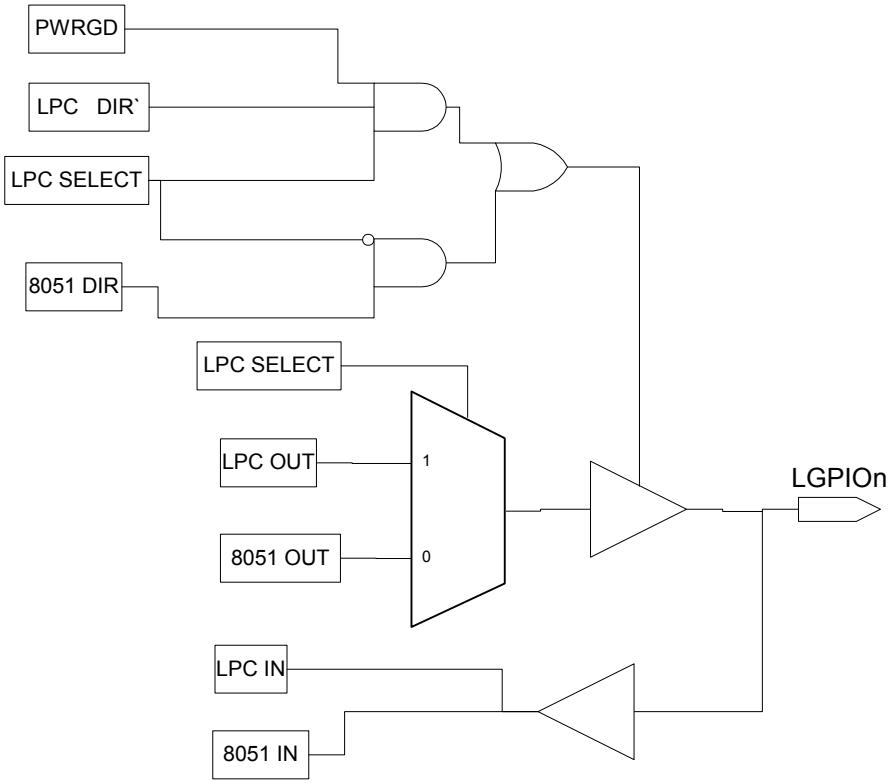


Figure 20.2 LPC Addressable GPIO Block Diagram

Note 20.7 This figure is for illustration purposes only and is not intended to suggest specific implementation details.

20.4.1 LPC LGPIO Base Address

Logical Device Number Ah in the LPC47N350 provides the base address and activation control for the 8 LPC/8051-addressable GPIO pins.

Register 0x30 is the Activate register. The activation control (LDNA:CR30.0) qualifies address decoding for the LPC LGPIO runtime registers; e.g., if the Activate bit D0 in the Activate register is “0”, the LPC LGPIO runtime register addresses will not be decoded; if the Activate bit is “1”, these addresses will be decoded depending on the values programmed in the LPC LGPIO Primary Base Address registers.

Registers 0x60 and 0x61 are the LPC LGPIO Primary Base Address register. Register 0x60 is the LPC LGPIO Primary Base Address High Byte, register 0x61 is the LPC LGPIO Primary Base Address Low Byte.

Note 20.8 The LPC LGPIO Base is relocatable on 16-byte boundaries; i.e., bits D0-D3 in the LPC LGPIO Primary Base Address Low Byte must be “0”. Valid LPC LGPIO runtime register base address values are between 0x0000-0x0FF0.

Table 20.14 LPC LGPIO Block Configuration Registers (LDN A)

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1 & VCC0 POR	DESCRIPTION							
						D7	D6	D5	D4	D3	D2	D1	D0
0x30	R/W	0x00	0x00	0x00	-	Activate							
						RESERVED							Activate
060	R/W	0x00	0x00	0x00	-	LPC LGPIO Block Primary Base Address High Byte							
						“0”	“0”	“0”	“0”	A11	A10	A9	A8
0x61	R/W	0x00	0x00	0x00	-	LPC LGPIO BLock Primary Base Address Low Byte							
						A7	A6	A5	A4	A3	“0”	“0”	“0”

20.4.2 LGPIO LPC Runtime Registers

The base address and activation control for these registers are located in the LPC Configuration Registers in Logical Device Ah.

Table 20.15 LPC LGPIO Runtime Registers

LPC SELECT REGISTER BIT	BASE ADDRESS OFFSET	REGISTER TYPE	REGISTER NAME
D0	0	R/W	LGPIO DIRECTION REGISTER G
	1	R	LGPIO INPUT REGISTER G
	2	R/W	LGPIO OUTPUT REGISTER G
D1	3		LGPIO DIRECTION REGISTER H
	4	R	LGPIO INPUT REGISTER H
	5	R/W	LGPIO OUTPUT REGISTER H

Note 20.9 The LPC SELECT bits determine the register source for the LGPIO pins (see Section 20.4.3.3, "LPC Select Register"). Register access is unaffected by the state of the LPC SELECT bits. For example, if the LPC GPIO runtime registers are active, the LGPIO Direction Register G can read and write even if the LPC SELECT register bit D0 is deasserted.

20.4.2.1 LGPIO Group G Registers

Table 20.16 LPC LGPIO Direction Register G

HOST ADDRESS	BASE ADDR. + 0
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO53 1=output 0=input	LGPIO52 1=output 0=input	LGPIO51 1=output 0=input	LGPIO50 1=output 0=input

Table 20.17 LPC LGPIO Input Register G

HOST ADDRESS	BASE ADDR. + 1
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	N/A

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R	R	R	R
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO53 IN	LGPIO52 IN	LGPIO51 IN	LGPIO50 IN

Table 20.18 LPC LGPIO Output Register G

HOST ADDRESS	BASE ADDR. + 2
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO53 OUT	LGPIO52 OUT	LGPIO51 OUT	LGPIO50 OUT

20.4.2.2 LGPIO Group H Registers

Table 20.19 LPC LGPIO Direction Register H

HOST ADDRESS	BASE ADDR. + 3
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO63 1=output 0=input	LGPIO62 1=output 0=input	LGPIO61 1=output 0=input	LGPIO60 1=output 0=input

Table 20.20 LPC LGPIO Input Register H

HOST ADDRESS	BASE ADDR. + 4
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	N/A

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R	R	R	R
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO63 IN	LGPIO62 IN	LGPIO61 IN	LGPIO60 IN

Table 20.21 LPC LGPIO Output Register H

HOST ADDRESS	BASE ADDR. + 5
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO63 OUT	LGPIO62 OUT	LGPIO61 OUT	LGPIO60 OUT

20.4.3 LGPIO MMCR (8051) Registers

These registers are accessible by the 8051 MMCR Address.

Table 20.22 LGPIO MMCR (8051) Registers Summary

8051 MMCR ADDRESS	REGISTER TYPE	8051 MMCR REGISTER NAME
0x7FA0	R/W	LGPIO DIRECTION REGISTER G
0x7FA1	R	LGPIO INPUT REGISTER G

Table 20.22 LGPIO MMCR (8051) Registers Summary

8051 MMCR ADDRESS	REGISTER TYPE	8051 MMCR REGISTER NAME
0x7FA2	R/W	LGPIO OUTPUT REGISTER G
0x7FA3		LGPIO DIRECTION REGISTER H
0x7FA4	R	LGPIO INPUT REGISTER H
0x7FA5	R/W	LGPIO OUTPUT REGISTER H
0x7FA9		LGPIO LPC SELECT
0x7FAA	R/W	LGPIO GROUP H BUFFER TYPE CONFIGURATION

20.4.3.1 LGPIO Group G Registers

Table 20.23 LPC LGPIO Direction Register G

HOST ADDRESS	0x7FA0
8051 ADDRESS	N/A
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO53 1=output 0=input	LGPIO52 1=output 0=input	LGPIO51 1=output 0=input	LGPIO50 1=output 0=input

Table 20.24 LPC LGPIO Input Register G

HOST ADDRESS	N/A
8051 ADDRESS	0x7FA1
POWER	VCC1
DEFAULT	N/A

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R	R	R
BIT NAME	Reserved	Reserved	Reserved	Reserved	status of pin LGPIO53	status of pin LGPIO52	status of pin LGPIO51	status of pin LGPIO50

Table 20.25 LPC LGPIO Output Register G

HOST ADDRESS	N/A
8051 ADDRESS	0x7FA2
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO53	LGPIO52	LGPIO51	LGPIO50

20.4.3.2 LGPIO Group H Registers

Table 20.26 LPC LGPIO Direction Register H

HOST ADDRESS	N/A
8051 ADDRESS	0x7FA3
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO63 1=output 0=input	LGPIO62 1=output 0=input	LGPIO61 1=output 0=input	LGPIO60 1=output 0=input

Table 20.27 LPC LGPIO Input Register H

HOST ADDRESS	N/A
8051 ADDRESS	0x7FA4
POWER	VCC1
DEFAULT	N/A

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R	R	R/	R
BIT NAME	Reserved	Reserved	Reserved	Reserved	status of pin LGPIO63	status of pin LGPIO62	status of pin LGPIO61	status of pin LGPIO60

Table 20.28 LPC LGPIO Output Register H

HOST ADDRESS	N/A
8051 ADDRESS	0x7FA5
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO63	LGPIO62	LGPIO61	LGPIO60

20.4.3.3 LPC Select Register

The LPC SELECT register is used to determine the host for the four LGPIO groups (Table 20.29, "LGPIO Pin Group LPC Select Register H").

There are two bits for LPGIO pin groups G and H. When an LPC SELECT bit is “1”, the LGPIO pins in that group are controlled by the LPC Host. When an LPC SELECT bit is “0”, the LGPIO pins in that group are controlled by the 8051.

Note 20.10 LPC and 8051 LGPIO runtime register access is unaffected by the LPC SELECT bits.

All of the LGPIO pin groups are controlled by the 8051 by default.

APPLICATION NOTE: For the LPC Host to “own” an LGPIO pin group, it should be configured by the 8051 before the BIOS can activate the LPC LGPIO logical device block.

Table 20.29 LGPIO Pin Group LPC Select Register H

HOST ADDRESS	N/A
8051 ADDRESS	0x7FA9
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R	R	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LPC SELECT GROUP H	LPC SELECT GROUP G

20.4.3.4 Programmable Buffer Type Registers

The buffer types for the LGPIO Group H pins are programmable as open-drain or push-pull depending on the bits in Table 20.30, "LGPIO Group H Buffer Type Configuration Register".

When the buffer type configuration bit is “1”, the LGPIO pin output buffer type is open-drain. When the buffer type configuration bit is “0”, the LGPIO pin output buffer type is push-pull.

The buffer types for the OUT0 and GPIO7 pins are programmable as open-drain or push–pull depending on the bits in Table 20.31, "GPIO Buffer Type Configuration Register".

Table 20.30 LGPIO Group H Buffer Type Configuration Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7FAA
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	LGPIO63	LGPIO62	LGPIO61	LGPIO60

“1” selected an open-drain buffer type; “0” selects a push-pull buffer type.

Table 20.31 GPIO Buffer Type Configuration Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7FAC
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R	R	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO7	OUT0

“1” selects an open-drain buffer type; “0” selects a push-pull buffer type.

20.5 Bit-Wise Addressable 8051 SFR GPIOs

The LPC47N350 includes a bit-wise addressable SFR register (0x80) for SGPIO30-SGPIO33.

The 8051 SETB bit and CLR bit instructions are utilized to directly access SGPIO bits where bit = address + bit.

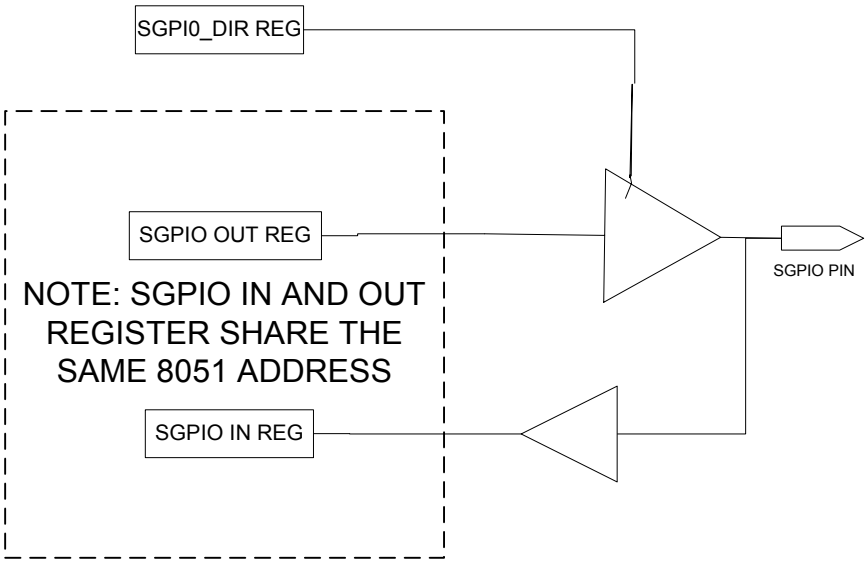


Figure 20.3 SGPIO Pin Block Diagram

Note: This figure is for illustration purposes only and is not intended to suggest specific implementation details.

Table 20.32 SGPIO Input/Output Register J

HOST ADDRESS	N/A
8051 ADDRESS	SFR 0x80
POWER	VCC1
DEFAULT	0x00

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	SGPIO33	SGPIO32	SGPIO31	SGPIO30

Table 20.33 SGPIO Direction Register J

HOST ADDRESS	N/A
8051 ADDRESS	0x7FAD
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	SGPIO33 1=output 0=input	SGPIO32 1=output 0=input	SGPIO31 1=output 0=input	SGPIO30 1=output 0=input

20.6 GPIO Pass-Through Ports

The LPC47N350 includes four GPIO Pass-Through Ports. GPIO Pass-Through Ports require two general purpose I/O pins and a multiplexer (See Figure 20.4). The GPIO Pass-Through Port (GPTP) can connect either the GPIOm pin or GPIOn to the GPIOn pin. The GPTPs are controlled by the PTMUX bits found in the GPIO Pass-Through Port Mux Register (See Section 20.6.1, "GPIO Pass-Through Port Mux Register"). The four GPTPs and their related PTMUX bits are shown in Figure 20.4.

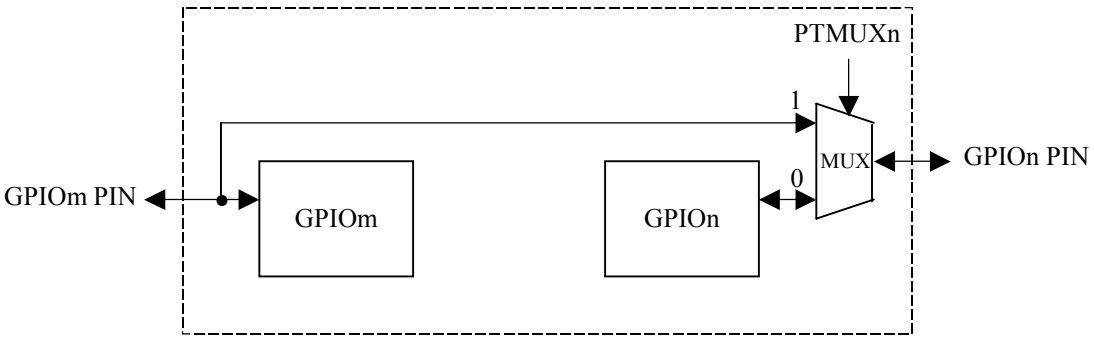


Figure 20.4 GPIO Pass-Through Port

Note: Figure 20.4 is for illustration purposes only and is not intended to suggest specific implementation details.

Table 20.34 Four GPIO Pass-Through Ports

GPIO PAIR (SEE Note 20.11)		MUX CONTROL (SEE Note 20.12)
GPIOM (SEE Note 20.13)	**GPION**	
LGPIO50	LGPIO60	PTMUX1

Table 20.34 Four GPIO Pass-Through Ports (continued)

GPIO PAIR (SEE Note 20.11)		MUX CONTROL (SEE Note 20.12)
GPIOM (SEE Note 20.13)	GPION	
LGPIO51	LGPIO61	PTMUX2
LGPIO52	LGPIO62	PTMUX3
LGPIO53	LGPIO63	PTMUX4

Note 20.11 See Figure 20.4

Note 20.12 Section 20.6.1, "GPIO Pass-Through Port Mux Register"

Note 20.13 These pins can generate 8051 interrupts and wake events. See Section 7.9, "8051 Interrupts".

20.6.1 GPIO Pass-Through Port Mux Register

The GPIO Pass-Through Port Mux Register contains the four PTMUX bits that are used to control the GPIO Pass-Through Ports (See Table 20.35). When a PTMUX is “0” (default), the pass-through mode is disabled and the GPIO pins function normally. When a PTMUX bit is “1”, the pass-through mode is enabled, GPIOn (See Figure 20.4) is disconnected and the signal at the GPIOm pin appears unmodified at the GPIOn pin (See Section 20.6.2, "GPTP Multiplexer").

The GPTM register is powered by VCC1 and is controlled solely by the 8051.

Table 20.35 GPIO Pass-Through Port Mux (GPTM) Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F85
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	PTMUX4	PTMUX3	PTMUX2	PTMUX1

20.6.2 GPTP Multiplexer

The GPIO Pass-Through Port Multiplexer determines connectivity for GPIOn pins as shown in Figure 20.4. GPIOn pins can be either an input or and output depending on the state of the PTMUX bit and the GPIOn direction register. In Pass-Through mode, GPIOn pins are always an output. In Normal mode, the GPIOn pins direction depends upon the GPIOn Direction Register (See Table 20.36).

Table 20.36 GPTP Multiplexor Direction Controls

GPIOM DIRECTION	GPION DIRECTION	PTMUX	GPION PIN TYPE	DESCRIPTION
IN	X	1	OUTPUT	PASS-THROUGH MODE
OUT				
X	IN	0	INPUT	NORMAL (GPIO) MODE
	OUT		OUTPUT	

Chapter 21 Multifunction Pin

21.1 Overview

Many of the LPC47N350's signal pins provide alternate functions which may be enabled by the 8051 firmware based on the system design requirements. See Table 2.4 on page 10 for a complete list of all of the multifunction pins. The 8051 firmware controls the multiplexing functions for each of the multiplexed pins through the registers described in this section. See the sub-sections that follow for a description of all of the MISC bits in the Multiplexing_1, Multiplexing_2, and Multiplexing_3 registers.

In the LPC47N350, the KBD Scan Interface Pins are multiplexed to support the 8051 Flash Interface. The multiplex functions for these pins are not controlled by the 8051. For information about the multiplexed KBD Scan Interface Pins see Section 9.6, "ATE Flash Program Access" and Section 9.7, "External Flash Interface".

21.2 Functions Available on More than One Pin

The KBRST and OUT8 functions can be made available on two pins: OUT8 and KSO12. The multiplex controls for these functions are described below. The OUT8, KSO12, KSO13 and GPIO17 pin functions all depend on the MISC17 and MISC6 multiplex control bits (Table 21.1). Note that OUT8 and KBRST cannot simultaneously exist on pins OUT8 and KSO12 (Figure 21.1).

Table 21.1 Multiplexing Register Bits Misc17 and Misc6

MISC17	MISC6	PIN OUT8	PIN KSO12	PIN KSO13	PIN GPIO17
0	0	OUT8	KSO12	KSO13	GPIO17
0	1	KBRST	KSO12	KSO13	GATEA20
1	0	OUT8	OUT8	GPIO18	GPIO17
1	1	KBRST	KBRST	GPIO18	GATEA20

Note: See "MISC6 – D6" and "MISC17 – D1" below.

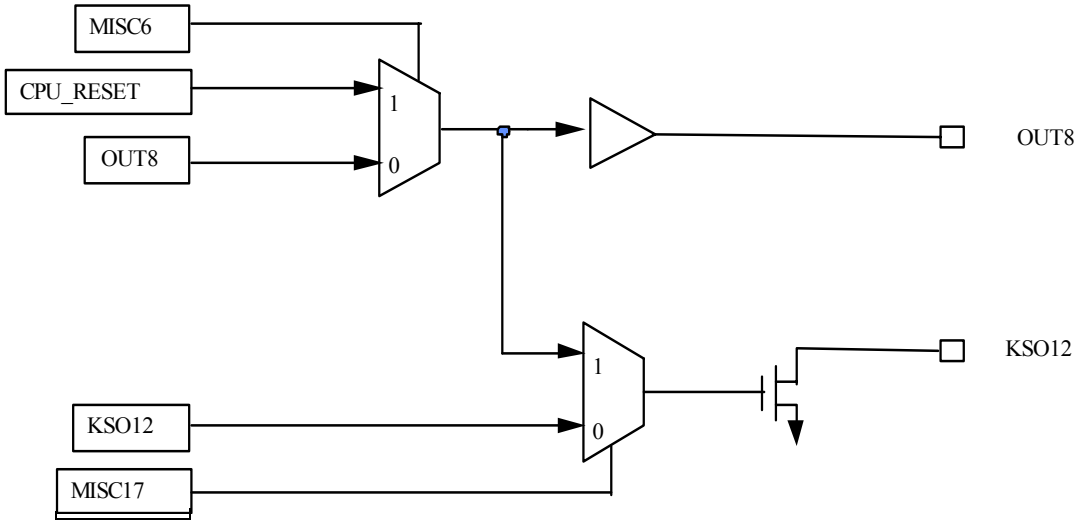


Figure 21.1 OUT8 and KSO12 Alternate Function Operation

21.3 Multiplexing_1 Register - MISC[7:0]

Table 21.2 Multiplexing_1 Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F3D
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
BIT NAME	MISC7	MISC6	Reserved	MISC4	MISC3	MISC2	MISC1	MISC0

MISC7 – LPC/8051 (SEE Note 20.6)

D7

The MISC7 bit is used in to select the pin function and the buffer mode between GPIO8 – GPIO9 and RXD/TXD (Table 21.3).

Table 21.3 Misc7 Bit

PIN	MISC7 = 0 (DEFAULT)	MISC7 = 1
GPIO8	GPIO8	RCD
GPIO9	GPIO9	TXD

MISC6 – D6

The MISC6 bit is used in the LPC47N350 to select the pin function and the buffer mode between GPIO17 and GATEA20 (Table 21.4). MISC6 also affects the multiplex functions of the OUT8, KSO12 pins (see Section 21.2, "Functions Available on More than One Pin" for Multiplexing control register interactive effects).

Table 21.4 Misc6 Bit

PIN	MISC6 = 0 (DEFAULT)	MISC6 = 1
GPIO17	GPIO17	GATEA20

MISC4 – D4

The MISC4 bit is used in the LPC47N350 to select the pin function and the buffer mode between OUT10 and PWM0 for the OUT10 pin (Table 21.5).

Table 21.5 Misc4 Bit

MISC4	DESCRIPTION
0	OUT10 Pin Function Selected (**DEFAULT**)
1	PWM0 Pin Function Selected

MISC3 – D3

The MISC3 bit is used to select between the nFDD_LED and the 8051RX alternate function and the buffer mode (Table 21.6).

Table 21.6 Misc3 Bit

MISC3	DESCRIPTION
0	nFDD_LED (**DEFAULT**)
1	8051RX

MISC2 – D2

The MISC2 bit is used in to select between the nPWR_LED and 8051TX function (Table 21.7).

Table 21.7 Misc2 Bit

MISC2	DESCRIPTION
0	nPWR_LED (**DEFAULT**)
1	8051TX

MISC1 – D1

The MISC1 bit is used to select the pin function and the buffer mode between GPIO20 and GPIO21, and the PS/2 CLK and DATA (Table 21.8).

Table 21.8 Misc1 Bit

MISC[1]	PIN GPIO20	PIN GPIO21
0 (DEFAULT)	GPIO20	GPIO21
1	PS2CLK	PS2DAT

The PS/2 pins on GPIO20 and GPIO21 are disabled (internally pulled high) when the non-PS/2 alternate functions are selected. The PS/2 inputs under this condition are seen as a high to the PS/2 Device Interface logic.

Whenever a PS/2 channel is not enabled, the input signals to that channel must be high. The LPC47N350 provides this through the use of weak pull-ups since the EM and KB channels share a common receive path and the IM and PS2 channels also share a common receive path.

MISC0 – D0

The MISC0 bit is used in the LPC47N350 to select the pin function and the buffer mode between OUT1 and nIRQ8 (Table 21.9)

Table 21.9 Misc0 Bit

MISC0	DESCRIPTION
0	OUT1 Pin Function Selected (**DEFAULT**)
1	nIRQ8 Pin Function Selected

21.4 Multiplexing_2 Register - MISC[16:9]

Table 21.10 Multiplexing_2 Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F40
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	MISC12	MISC11	MISC10	MISC9

MISC12 – D3

The MISC12 bit is used in the LPC47N350 to select the pin function and buffer mode between OUT11 and PWM1 for the OUT11 pin (Table 21.11).

Table 21.11 Misc12 Bit

MISC12	DESCRIPTION
0	OUT11 Pin Function Selected (**DEFAULT**)
1	PWM1 Pin Function Selected

MISC11

The MISC11 bit is used in the LPC47N350 to select the pin function and the buffer mode between OUT9 and PWM0 for the OUT9 pin (Table 21.12).

Table 21.12 Misc11 Bit

MISC11	DESCRIPTION
0	OUT9 Pin Function Selected (**DEFAULT**)
1	PWM2 Pin Function Selected

MISC9

The MISC9 bit is used in the LPC47N350 to select between the GPIO and Keyboard Scan Output alternate function and the buffer modes for the GPIO4 and GPIO5 pins (Table 21.13).

Table 21.13 Misc9 Bit

MISC9	PIN GPIO4	GPIO5
0 (DEFAULT)	GPIO4	GPIO5
1	KSO14	KSO15

Note 21.1 When the KSO14 and KSO15 functions are enabled, the direction bits for GPIO4 and GPIO5 in 8051 MMCR 0x7F18 have to be set to '1' for the KSO14 and KSO15 pins to function normally. When the KSO14 and KSO15 functions are enabled and the GPIO[5:4] direction bits are set to '0', the KSO14 and KSO15 output drivers are disabled; i.e., the KSO14 and KSO15 pins are inputs.

21.5 Multiplexing_3 Register - MISC[23:17]

Table 21.14 Multiplexing_3 Register

HOST ADDRESS	N/A
8051 ADDRESS	0x7F30
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	MISC23	MISC22	MISC21	MISC20	MISC19	MISC18	MISC17	Reserved

MISC23 – D7

The MISC23 bit is used to select the pin function and the buffer mode between GPIO15 and FAN_TACH1 for the GPIO15 pin (Table 21.15).

Table 21.15 Misc23 Bit

MISC23	DESCRIPTION
0	GPIO15 Function Selected (**DEFAULT**)
1	FAN_TACH1 Function Selected

MISC22 – D6

The MISC22 bit is used to select between GPIO7 and PWM3 functions (Table 21.16).

Table 21.16 Misc22 Bit

MISC22	DESCRIPTION
0 (DEFAULT)	GPIO7
1	PWM3

MISC21 – D5

The MISC21 bit is used to select the pin function and the buffer mode between GPIO16 and FAN_TACH2 for the GPIO16 pin (Table 21.17).

Table 21.17 Misc21 Bit

MISC21	DESCRIPTION
0	GPIO16 Function Selected (**DEFAULT**)
1	FAN_TACH2 Function Selected

MISC[20:19] D4 – D3

The MISC20 and MISC19 bits are used to select the pin function and the buffer mode between the switched I^2C/SMBus 2 interface and the GPIO11, GPIO12, GPIO13 and GPIO14 pins. The MISC20 and MISC19 bits control the number of pins allocated for I^2C/SMBus 2 interface alternate functions as follows: I^2C/SMBus 2 interface (4 pins), unswitched I^2C/SMBus 2 interface (2 pins), or no I^2C/SMBus 2 interface (0 pins). Pins not allocated to the I^2C/SMBus 2 interface are allocated to GPIO interface.

Table 21.18 Misc[20:19] Bits

MISC19	MISC20	PIN GPIO11	PIN GPIO12	PIN GPIO13	PIN GPIO14	DESCRIPTION
0	0	GPIO11	GPIO12	GPIO13	GPIO14	Four GPIO pins (Default)
0	1	AB2A_DATA	AB2A_CLK	GPIO13	GPIO14	Switched I^2C/SMBus 2 and Two GPIO pins
1	0	AB2A_DATA	AB2A_CLK	AB2B_DATA	AB2B_CLK	Switched I^2C/SMBus 2
1	1					Reserved

Note 21.2 The function of the GPIO[11:14] pin is RESERVED when MISC[20:19] = 1,1 (Table 21.18).

MISC18 – D2

The MISC18 bit is used in the LPC47N350, along with bit D3 in the ESMI Mask register to select the pin function and buffer mode for the OUT7 pin and the SMI transfer mechanism to the host. (Table 21.19). When MISC18 = '0', the primary function of the OUT7 pin is selected and the SMI is routed to the Serial IRQ interface. If the SMI is masked, SIRQ slot3 is available as IRQ2. When MISC18 = '1', the alternate nSMI function of the OUT7 pin is selected, the pad is driven open-drain, and the Serial IRQ slot3 is available as IRQ2. The ESMI Mask register IS MBX97h. See Section 17.7, "ESMI Registers".

Table 21.19 MISC18 and ESMI Mask Bits

ESMI MASK REGISTER		FUNCTION		DESCRIPTION
D3	MISC18	OUT7 PIN	SIRQ SLOT3	
0	0	OUT7	nSMI	SERIAL SMI (DEFAULT)
0	1	nSMI	IRQ2	PARALLEL SMI, SERIAL IRQ IRQ2 AVAILABLE
1	0	OUT7	IRQ2	MASKED SERIAL SMI, IRQ2 AVAILABLE
1	1	nSMI	IRQ2	PARALLEL SMI MASKED (INACTIVE), IRQ2 AVAILABLE

MISC17 – D1

The MISC17 bit is used in the LPC47N350 to select the pin function and buffer mode between KSO13 and GPIO18 on pin KSO13 (Table 21.20). MISC17 also affects the multiplex functions for the OUT8, KSO12 and KSO13 pins (see Section 21.2, "Functions Available on More than One Pin" for Multiplexing control register interactive effects).

Table 21.20 Misc17

MISC17	PIN KSO13
0	KSO13
1	GPIO18

Chapter 22 ACPI PM1 Block

22.1 ACPI PM1 Block Overview

The LPC47N350 supports ACPI as described in this section. These features comply with the ACPI Specification, Revision 1.0**/2.0**, through a combination of hardware and 8051 software.

The LPC47N350 implements the ACPI fixed registers but includes only those bits that apply to the power button sleep button and RTC alarm events. The ACPI WAK_STS, SLP_TYPx, and SLP_EN bits are also supported.

The registers in the LPC47N350 ACPI PM1 Block occupy eight addresses in the host I/O space and are specified as offsets from the ACPI PM1 Block base address. The ACPI PM1 Block base address is relocatable depending on the values programmed in LPC47N350 configuration registers CR60 and CR61 in Logical Device Number 1.

The functions described in the following sub-sections can generate a SCI event on the nEC_SCI pin. In the LPC47N350, an SCI event is considered the same as an ACPI wakeup or runtime event. The 8051 can also generate a SCI on the nEC_SCI pin by setting the 8051_SCI_STS bit in the 8051_PM_STS register (see Section 22.6, "nEC_SCI Pin Interface").

22.2 ACPI PM1 Block SCI Event-Generating Functions

Power Button With Override

The power button has a status and an enable bit in the PM1_BLK of registers to provide an SCI upon the button press. The status bit is software Read/Writeable by the 8051; the enable bit is Read-only by the 8051. It also has a status and enable bit in the PM1_BLK of registers to indicate and control the power button override (fail-safe) event. These bits are not required by ACPI. The power button override event status bit is software Read/Writeable by the 8051; the enable bit is software read-only by the 8051. The enable bit for the override event is located at bit 1 in the PM1_CNTRL2 register.

The power button enable bit is set by the Host to enable the generation of an SCI due to the power button event. The status bit is set by the 8051 when it generates a power button event and is cleared by the Host writing a ‘1’ to this bit (writing a ‘0’ has no effect); it can also be cleared by the 8051. If the enable bit is set, the 8051 will generate an SCI power management event.

Sleep Button

The sleep button has a status and an enable bit in the PM1_BLK of registers to provide an SCI upon the button press. The status bit is software Read/Writeable by the 8051; the enable bit is Read-only by the 8051.

The sleep button enable bit is set by the Host to enable the generation of an SCI due to the sleep button event. The status bit is set by the 8051 when it generates a sleep button event and is cleared by the Host writing a ‘1’ to this bit (writing a ‘0’ has no effect); it can also be cleared by the 8051. If the enable bit is set, the 8051 will generate an SCI power management event.

RTC Alarm

The ACPI specification requires that the RTC alarm generate a hardware wake-up event from the sleeping state. The RTC alarm can be enabled as an SCI event and its status can be determined through bits in the PM1_BLK of registers. The status bit is software Read/Writeable by the 8051; the enable bit is Read-only by the 8051.

The RTC enable bit is set by the Host to enable the generation of an SCI due to the RTC alarm event. The status bit is set by the 8051 when the RTC generates an alarm event and is cleared by the Host writing a ‘1’ to this bit (writing a ‘0’ has no effect); it can also be cleared by the 8051. If the enable bit is set, the 8051 will generate an SCI power management event.

22.3 ACPI PM1 Block Base Address

Logical Device 1 in the LPC47N350 configuration space supports the ACPI PM1 Block registers interface. Three device configuration registers in LDN1 provide activation control and the base address programming for the ACPI PM1 Block registers (Table 22.1).

Register 0x30 is the Activate register. The activation control (LDN1:CR30.0) qualifies address decoding for the ACPI PM1 Block registers; e.g., if the Activate bit D0 in the Activate register is “0”, the PM1 Block addresses will not be decoded; if the Activate bit is “1”, PM1 Block addresses will be decoded depending on the values programmed in the ACPI PM1 Block Primary Base Address registers.

Registers 0x60 and 0x61 are the ACPI PM1 Block Primary Base Address registers. Register 0x60 is the ACPI PM1 Block Primary Base Address High Byte, register 0x61 is the ACPI PM1 Block Primary Base Address Low Byte.

Note: The ACPI PM1 Block base address must be located on eight -byte boundaries; i.e., bits D0 – D2 in the ACPI PM1 Block Primary Base Address Low Byte must be “0”. Valid ACPI PM1 Block base address values are 0x0000 – 0x0FF8.

Table 22.1 ACPI PM1 Block Configuration Registers (LDN1)

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1& VCC0 POR	DESCRIPTION							
						D7	D6	D5	D4	D3	D2	D1	D0
0x30	R/W	0x00	0x00	0x00	-	Activate							
						RESERVED							Activate
0x60	R/W	0x00	0x00	0x00	-	ACPI PM1 Block Primary Base Address High Byte							
						“0”	“0”	“0”	“0”	A11	A10	A9	A8
0x61	R/W	0x00	0x00	0x00	-	ACPI PM1 Block Primary Base Address Low Byte							
						A7	A6	A5	A4	A3	“0”	“0”	“0”

22.4 ACPI PM1 Block

Description

The ACPI register model consists of a number of fixed register blocks that perform designated functions. A register block consists of a number of registers that perform Status, Enable and Control functions. The ACPI specification deals with events (which have an associated interrupt status and enable bits, and sometimes an associated control function) and control features. The status registers illustrate what defined function is requesting ACPI interrupt services (SCI). Any status bit in the ACPI specification has the following attributes:

- Status bits are only set through some defined hardware or 8051 event.
- Unless otherwise noted, status bits are cleared by the system writing a “1” to that bit position, and upon VCC1 POR. Writing a ‘0’ has no effect.
- Status bits only generate interrupts while their associated bit in the enable register is set.
- Function bit positions in the status register have the same bit position in the enable register (there are exceptions to this rule, special status bits have no enables).
- Note that this implies that if the respective enable bit is reset and the hardware event occurs, the respective status bit is set; however no interrupt is generated until the enable bit is set. This allows software to test the state of the event (by examining the status bit) without necessarily generating an interrupt. There are a special class of status bits that have no respective enable bit, these are

called out specifically, and the respective enable bit in the enable register is marked as reserved for these special cases.

- The enable registers allow the setting of the status bit to generate an interrupt (under 8051 control). As a general rule, there is an enable bit in the enable register for every status bit in the status register. The control register provides special controls for the associated event, or special control features that are not associated with an interrupt event. The order of a register block is the status registers, followed by enable registers, followed by control registers.

22.5 Registers

The registers in the LPC47N350 ACPI PM1 Block occupy eight addresses in the host I/O space and are specified as offsets from the ACPI PM1 Block base address (Table 22.2).

The registers in the PM1 Block are powered by VCC1.

Table 22.2 ACPI PM1 Block Registers

REGISTER	SIZE (BITS)	OFFSET	ADDRESS
PM1_STS 1	8	0	<ACPI PM1 Block Base Address>
PM1_STS 2		1	<ACPI PM1 Block Base Address>+1h
PM1_EN 1		2	<ACPI PM1 Block Base Address>+2h
PM1_EN 2		3	<ACPI PM1 Block Base Address>+3h
PM1_CNTRL 1		4	<ACPI PM1 Block Base Address>+4h
PM1_CNTRL 2		5	<ACPI PM1 Block Base Address>+5h
RESERVED		6	<ACPI PM1 Block Base Address>+6h
RESERVED		7	<ACPI PM1 Block Base Address>+7h

22.5.1 Power Management 1 Status Register 1 (PM1_STS 1)

Host Register Location: <ACPI PM1 Block Base Address> System I/O Space

8051 Register Location: n/a

Default Value: 00h on VCC1 POR

Host Attribute: Read

Size: 8-bits

Table 22.3 Power Management 1 Status Register 1

BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return a value of zero.

22.5.2 Power Management 1 Status Register 2 (PM1_STS 2)

Host Register Location: <ACPI PM1 Block Base Address>+1h System I/O Space

8051 Register Location: 0x7F80

Default Value: 00h on VCC1 POR

Host Attribute: Read/Write (Note 1)

8051 Attribute Read/Write

Size: 8-bits

Note: These bits are set/cleared by the 8051 directly i.e., writing '1' sets the bit and writing '0' clears it. These bits can also be cleared by the Host software writing a one to this bit position and by VCC1 POR. Writing a 0 by the Host has no effect.

An interrupt is generated to the 8051 when the Host writes to this register.

Table 22.4 Power Management 1 Status Register 2

BIT	NAME	DESCRIPTION
0	PWRBTN_STS	This bit can be set or cleared by the 8051 to simulate a Power button status if the power is controlled by the 8051. The Host writing a one to this bit can also clear this bit. The 8051 must generate the associated SCI interrupt under software control.
1	SLPBTN_STS	This bit can be set or cleared by the 8051 to simulate a Sleep button status if the sleep state is controlled by the 8051. The Host writing a one to this bit can also clear this bit. The 8051 must generate the associated SCI interrupt under software control.
2	RTC_STS	This bit can be set or cleared by the 8051 to simulate a RTC status. The Host writing a one to this bit can also clear this bit. The 8051 must generate the associated SCI interrupt under software control.
3	PWRBTNOR_STS	This bit can be set or cleared by the 8051 to simulate a Power button override event status if the power is controlled by the 8051. The Host writing a one to this bit can also clear this bit. The 8051 must generate the associated hardware event under software control.
4-6	Reserved	Reserved. These bits always return a value of zero.
7	WAK_STS	This bit can be set or cleared by the 8051. The Host writing a one to this bit can also clear this bit.

22.5.3 Power Management 1 Enable Register 1 (PM1_EN 1)

Host Register Location: <ACPI PM1 Block Base Address>+2 System I/O Space

8051 Register Location: n/a

Default Value: 00h on VCC1 POR

Host Attribute: Read

Size: 8-bits

Table 22.5 Power Management 1 Enable Register 1

BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return a value of zero.

22.5.4 Power Management 1 Enable Register 2 (PM1_EN 2)

Host Register Location: <ACPI PM1 Block Base Address>+3 System I/O Space

8051 Register Location: 0x7F81

Default Value: 00h on VCC1 POR

Host Attribute: Read/Write

8051 Attribute: Read

Size: 8-bits

An interrupt is generated to the 8051 when the Host writes this to register.

Table 22.6 Power Management 1 Enable Register 2

BIT	NAME	DESCRIPTION
0	PWRBTN_EN	This bit can be read or written by the Host. It can be read by the 8051.
1	SLPBTN_EN	This bit can be read or written by the Host. It can be read by the 8051.
2	RTC_EN	This bit can be read or written by the Host. It can be read by the 8051.
3-7	RESERVED	Reserved bits cannot be written and return “0” when read.

22.5.5 Power Management 1 Control Register 1 (PM1_CNTRL 1)

Host Register Location: <ACPI PM1 Block Base Address>+4 System I/O Space

8051 Register Location: n/a

Default Value: 00h on VCC1 POR

Host Attribute: Read

Size: 8-bits

Table 22.7 Power Management 1 Control Register 1

BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved bits cannot be written and return “0” when read.

22.5.6 Power Management 1 Control Register 2 (PM1_CNTRL 2)

Host Register Location: <ACPI PM1 Block Base Address>+5 System I/O Space

8051 Register Location: 0x7F82

Default Value: 00h on VCC1 POR

Host Attribute: Read/Write

8051 Attribute: Read. **Note:** Bit 5 is Read/Write

Size: 8-bits

An interrupt is generated to the 8051 when the Host writes to this register.

Table 22.8 Power Management 1 Control Register 2

BIT	NAME	DESCRIPTION
0	Reserved	Reserved. This field always returns zero.
1	PWRBTNOR_EN	This bit can be set or cleared by the Host, read by the 8051.
2-4	SLP_TYPx	These bits can be set or cleared by the Host, read by the 8051.

Table 22.8 Power Management 1 Control Register 2 (continued)

BIT	NAME	DESCRIPTION
5	SLP_EN	This bit is R/W by the Host; reads by the Host always return '0'. This bit can be set (written as '1') but not cleared by the Host (writing '0' has no effect). This bit is R/W by the 8051, and reads by the 8051 return the true value of the bit. When set by the Host, this bit is cleared by the 8051 writing a '1' to it; writing '0' has no effect.
6-7	RESERVED	Reserved bits cannot be written and return "0" when read.

22.6 nEC_SCI PIN INTERFACE

The nEC_SCI pin logic hardware is shown in Figure 22.1.

Any or all of the PWRBTN_STS, SLPBTN_STS, and RTC_STS bits in the PM1_STS 2 register can assert the nEC_SCI pin if enabled by the PWRBTN_EN, SLPBTN_EN, and RTC_EN bits in the PM1_EN 2 register. See descriptions of these registers, above.

The 8051_SCI_STS bit can assert the nEC_SCI pin at any time, without being enabled. The 8051_SCI_STS bit is located in the 8051_PM_STS register at MMCR address 0x7F83h (Table 22.9).

The 8051_SCI_STS bit is in the LPC47N350 and is read/write by the 8051. If the 8051_SCI_STS bit is "1", an interrupt is generated on the nEC_SCI pin.

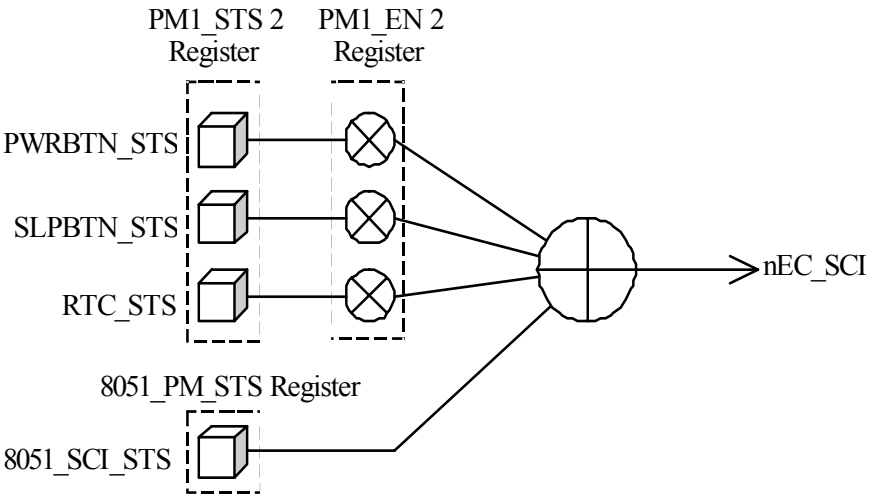


Figure 22.1 Hardware nEC_SCI Interface

Table 22.9 8051_Pm_Sts Register

HOST ADDRESS	-
8051 ADDRESS	0x7F83
POWER PLANE	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R/W
BIT NAME	RESERVED (RESERVED bits cannot be written and return “0” when read)							8051_SCI_STS

Chapter 23 Real-Time Clock

23.1 General Description

The Real-Time Clock Supercell (RTC) is a complete time of day clock with alarm, day of month alarm, one hundred year calendar, a century byte, and a programmable periodic interrupt. The RTC address space consists of two-128 byte banks of CMOS RAM (Bank0 and Bank1). Each bank is accessable via address and data ports. These access ports have relocatable addresses and are accessable by both the host and the 8051. Each bank's last addressable location accesses the Shared RTC Control. The remaining 127 bytes of Bank0 contain the following: eleven registers of time, calendar, century, and alarm data, four control and status registers, and 111 bytes of general purpose registers. The remaining 127bytes of Bank1 contain general purpose registers.

Features:

- Allows 32kHz clock input or a 32kHz crystal.
- Counts seconds, minutes, and hours of the day.
- Counts days of the week, date, month and year.
- Binary or BCD representation of time, calendar and alarm.
- 24 hour daily alarm.
- 30-day alarm.
- RTC/CMOS Bank Addresses are relocatable.
- The RTC CMOS Bank0 index register (70h) is shadowed
- RTC Interrupt (IRQ8) is available on the parallel nIRQ8 pin.
- RTC power source is switched internally between the VCC1 and VCC0 pins according to VCC1_PWRGD (See Figure 2.2, "VCC2 Power-Up Timing" and Figure 2.3, "VCC1_PWRGD Timing").
- Lockable CMOS Ram Address Ranges (See Table 8.4 on page 90.

23.2 Configuration Registers

The RTC configuration registers, in Logical Device Number 6, provide activation control and the base address for the run-time registers (See Table 23.1)

The activate bit register 0x30, Bit D0 enables RTC/CMOS Bank0.

The activate bit register 0x30, Bit D1 enables RTC/CMOS Bank1.

Table 23.1 RTC Configuration Registers

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1& VCC0 POR	DESCRIPTION							
						D7	D6	D5	D4	D3	D2	D1	D0
0x30	R/W	0x00	0x00	0x00	-	Activate							
						RESERVED						Activate CMOS Bank1	Activate RTC/ CMOS Bank0
0x60	R/W	0x00	0x00	0x00	-	RTC/CMOS Bank0 Primary Base Address High Byte							

Table 23.1 RTC Configuration Registers (continued)

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1& VCC0 POR	DESCRIPTION							
						“0”	“0”	“0”	“0”	A11	A10	A9	A8
0x61	R/W	0x70	0x70	0x70	-	RTC/CMOS Bank0 Primary Base Address Low Byte							
						A7	A6	A5	A4	A3	A2	A1	“0”
0x62	R/W	0x00	0x00	0x00	-	CMOS Bank1 Primary Base Address High Byte							
						“0”	“0”	“0”	“0”	A11	A10	A9	A8
0x63	R/W	0x74	0x74	0x74	-	CMOS Bank1 Primary Base Address Low Byte							
						A7	A6	A5	A4	A3	A2	A1	“0”
0xF1	R	-	-	-	-	Shadow RTC/CMOS Bank 0 Index register							

23.3 Host I/O Interface

Each bank has a CMOS Address Register and a CMOS Data Register. Each bank’s CMOS Address Register is located at the corresponding base address setup by the Configuration Registers in Table 23.1. Each bank’s CMOS Data Register is located at an offset of the corresponding base (see Table 23.2). Bit D7 of both CMOS Address Registers is not used for the CMOS RAM address decoding. All four CMOS Run Time registers are fully read/write.

Table 23.2 CMOS Run Time Registers

HOST ADDRESS*	BANK	FUNCTION
Bank0 * (R/W)	RTC/CMOS Bank0	CMOS Address Register
Bank0 * + 1(R/W)	RTC/CMOS Bank0	CMOS Data Register
Bank1 * (R/W)	CMOS Bank1	CMOS Address Register
Bank1 * + 2(R/W)	CMOS Bank1	CMOS Data Register

23.4 Internal Registers

Table 23.3 shows the address map of the RTC and CMOS RAM, eleven registers of time, calendar, century, and alarm data, four control and status registers, 239 bytes of CMOS registers and one Shared RTC Control register. Each bank’s last addressable location accesses the same register, the Shared RTC Control.

Table 23.3 RTC and CMOS RAM Address Map

BANK	BASE OFFEST	REGISTER TYPE	REGISTER FUNCTION
Bank0	0	R/W	Register 0: Seconds
	1		Register 1: Seconds Alarm
	2		Register 2: Minutes
	3		Register 3: Minutes Alarm
	4		Register 4: Hours
	5		Register 5: Hours Alarm
Bank0	6	R/W	Register 6: Day of Week
	7		Register 7: Day of Month
	8		Register 8: Month
Bank0	9		Register 9: Year
	A		Register A
	B		Register B: (Bit 0 is Read Only)
	C	R	Register C
	D	R/W	Register D: Day of Month Alarm
	32		Century Byte
	E-31, 33-7F		General purpose
	7F		Shared RTC Control
Bank1	0-7E		Bank 1: General purpose
	7F		Shared RTC Control

All 256 bytes are directly writable and readable by the host with the following exceptions:

- Registers C is read only.
- Bit 7 of Register D is read only which can only be set by a read of Register D.
- Bit 6 of Register D is read only.
- Bit 7 of Register A is read only.
- Bits 0 of Register B is read only.
- Bits 7-1 of the Shared RTC Control register are read only.

23.5 Time Calendar and Alarm

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar and alarm by writing to these locations. The contents of the twelve time, calendar and alarm registers can be in binary or BCD as shown in Table 23.4, "RTC Register Valid Range".

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the twelve locations in the binary or BCD format as defined by the DM bit in Register B. The SET bit may then be cleared to allow updates.

The 12/24 bit in Register B establishes whether the hour locations represent 1 to 12 or 0 to 23. The 12/24 bit cannot be changed without reinitializing the hour locations. When the 12 hour format is selected, the high order bit of the hours byte represents PM when it is a "1".

Once per second, the twelve time, calendar and alarm registers are updated, Incrementing by one second and checking for an alarm condition. During the update cycle all the registers in Table 23.4, except Register D, are not accessible by the processor program. The update cycle time is shown in Table 23.2. The update logic contains circuitry for automatic end-of-month recognition as well as automatic leap year compensation.

The three alarm registers may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarms registers. The "don't care" code is any hexadecimal byte from C0 to FF inclusive. That is the two most significant bits of each byte, when set to "1" create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Table 23.4 RTC Register Valid Range

ADD	REGISTER FUNCTION	BCD RANGE	BINARY RANGE
0	Register 0: Seconds	00-59	00-3B
1	Register 1: Seconds Alarm	00-59	00-3B
2	Register 2: Minutes	00-59	00-3B
3	Register 3: Minutes Alarm	00-59	00-3B
4	Register 4: Hours	01-12 am	01-0C
	(12 hour mode)	81-92 pm	81-8C
	(24 hour mode)	00-23	00-17
5	Register 5: Hours Alarm	01-12 am	01-0C
	(12 hour mode)	81-92 pm	81-8C
	(24 hour mode)	00-23	00-17
6	Register 6: Day of Week	01-07	01-07
7	Register 7: Day of Month	01-31	01-1F
8	Register 8: Month	01-12	01-0C
9	Register 9: Year	00-99	00-63
D	Day of Month Alarm	01-31	01-1F
32	Century Byte	00-99	00-63

23.6 Update Cycle

An update cycle is executed once per second if the SET bit in Register B is clear and the DV0-DV2 divider is not clear. The SET bit in the "1" state permits the program to initialize the time and calendar registers by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds register, check for overflow, increment the minutes register when appropriate and so forth through to the year of the century byte.

The update cycle also compares each alarm register with the corresponding time register and issues an alarm if a match or if a "don't care" code is present.

The length of an update cycle is shown in Table 23.5. During the update cycle, the time, calendar, and alarm registers are not accessible by the processor program. If the processor reads these locations before the update cycle is complete, the output will be undefined. The UIP (update in progress) status bit is set during the interval. When the UIP bit goes high, the update cycle will begin 244 μs later. Therefore, if a low is read on the UIP bit the user has at least 244 μs before time/calendar data will be changed.

Table 23.5 RTC Update Cycle Timing

INPUT CLOCK_ FREQUENCY	UIP BIT	UPDATE CYCLE TIME	MINIMUM TIME BEFORE START OF UPDATE CYCLE
32.768 kHz	1	1948 μs	-
	0	-	244 μs

23.7 Control and Status Registers

The RTC has four registers, which are accessible to the processor program at all times, even during the update cycle.

23.7.1 Register A

B7	B6	B5	B4	B3	B2	B1	B0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The update in progress bit is a status flag that may be monitored by the program. When UIP is a "1", the update cycle is in progress or will soon begin. When UIP is a "0", the update cycle is not in progress and will not be for at least 244 ms. The time, calendar, and alarm information is fully available to the program when the UIP bit is “0”. The UIP bit is a read only bit and is not affected by VCC1 POR. Writing the SET bit in Register B to a "1" inhibits any update cycle and then clears the UIP status bit.

DV2-0

Three bits are used to permit the program to select various conditions of the 22 stage divider chain. Table 23.6 shows the allowable combinations. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider chain at the precise time stored in the registers. When the divider reset is removed, the first update begins one-half second later. These three read/write bits are not affected by VCC1 POR.

Table 23.6 RTC Divider Selection Bits

OSCILLATOR FREQUENCY	REGISTER A BITS			MODE
32.768 kHz	DV2	DV1	DV0	
	0	0	0	Normal Operation
	0	0	1	Reset Divider
	0	1	0	Normal Operation
	0	1	1	Oscillator Disabled
	1	0	X	Test
	1	1	X	Reset Divider

RS3-0

The four rate selection bits select one of 15 taps on the divider chain or disable the divider output. The selected tap determines rate or frequency of the periodic interrupt. The program may enable or disable the interrupt with the PIE bit in Register B. Table 23.7 lists the periodic interrupt rates and equivalent output frequencies that may be chosen with the RS0-RS3 bits. These four bits are read/write bits which are not affected by VCC1 POR.

Table 23.7 RTC Periodic Interrupt Rates

RATE SELECT	32.768 KHZ TIME BASE	
RS3 RS2 RS1 RS0	PERIOD RATE OF INTERRUPT	FREQUENCY OF INTERRUPT
0 0 0 0	0.0	
0 0 0 1	3.90625 ms	256 Hz
0 0 1 0	7.8125 ms	128 Hz
0 0 1 1	122.070 µs	8.192 Hz
0 1 0 0	244.141 µs	4.096 kHz
0 1 0 1	488.281 µs	2.048 kHz
0 1 1 0	976.562 µs	1.024 kHz
0 1 1 1	1.953125 ms	512 Hz
1 0 0 0	3.90625 ms	256 Hz
1 0 0 1	7.8125 ms	128 Hz
1 0 1 0	15.625 ms	64 Hz
1 0 1 1	31.25 ms	32 Hz
1 1 0 0	62.5 ms	16 Hz
1 1 0 1	125 ms	8 Hz
1 1 1 0	250 ms	4 Hz
1 1 1 1	500 ms	2 Hz

23.7.2 Register B

B7	B6	B5	B4	B3	B2	B1	B0
SET	PIE	AIE	UIE	RES	DM	24/12	DSE

SET

When the SET bit is a "0", the update functions normally by advancing the counts once-per-second. When the SET bit is a "1", an update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the middle of initialization. SET is a read/write bit, which is not modified by VCC1 POR or any internal functions.

PIE

The periodic interrupt enable bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the IRQB port to be driven low. The program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3 - RS0 bits in Register A. A “0” in PIE blocks IRQB from being initiated by a periodic interrupt, but the periodic flag (PF) is still set at the periodic rate. PIE is not modified by any internal function, but is cleared to "0" by a VCC1 POR.

AIE

The alarm interrupt enable bit is a read/write bit, which when set to a "1" permits the alarm flag (AF) bit in Register C to assert IRQB. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an IRQB signal. The VCC1 POR port clears AIE to "0". The AIE bit is not affected by any internal functions.

UIE

The update-ended interrupt enable bit is a read/write bit which enables the update-end flag (UF) bit in Register C to assert IRQB. The VCC1 POR port or the SET bit going high clears the UIE bit.

RES

Reserved - read as zero

DM

The data mode bit indicates whether time and calendar updates are to use binary or BCD

Formats: The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or by VCC1 POR. A "1” in DM signifies binary data, while a "0" in DM specifies BCD data.

24/12

The 24/12 control bit establishes the format of the hours byte as either the 24 hour mode if set to a "1", or the 12 hour mode if cleared to a "0". This is a read/write bit that is not affected by VCC1 POR or any internal function.

DSE

The daylight savings enable bit is read only and is always set to a "0" to indicate that the daylight savings time option is not available.

23.7.3 Register C

REGISTER C IS A READ-ONLY REGISTER

B7	B6	B5	B4	B3	B2	B1	B0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The interrupt request flag is set to a "1" when one or more of the following are true:

PF = PIE = 1

AF = AIE = 1

UF = UIE = 1

Any time the IRQF bit is a "1", the IRQB signal is driven low. All flag bits are cleared after Register C is read or by the VCC1 POR port.

PF

The periodic interrupt flag is a read only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 -RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" sets the IRQF bit and initiates an IRQB signal when PIE is also a "1". The PF bit is cleared by VCC1 POR or by a read of Register C.

AF

The alarm interrupt flag when set to a "1" indicates that the current time has matched the alarm time. A "1" in AF causes a "1"to appear in IRQF and the IRQB port to go low when the AIE bit is also a "1". A VCC1 POR or a read of Register C clears the AF bit.

UF

The update-ended interrupt flag bit is set after each update cycle. When the UIE bit is also a "1", the "1" in UF causes the IRQF bit to be set and asserts IRQB. A VCC1 POR or a read of Register C causes UF to be cleared.

b3-0

The unused bits of Register C are read as “0” and cannot be written.

23.7.4 Register D

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	B0
VRT	0	Day of month					

VRT

The Valid RAM and Time (VRT) bit is cleared by VCC0 (Vbat) POR, only. This is the only case where the contents of the RAM, as well as the time and calendar registers, are not valid. The VRT bit can only be set by a read of Register D. The 8051 can set the VRT bit reading Register D after both of the following condition are met: VCC1_PWRGD =1 and the 8051 completes initialization. The Host can set the VRT bit reading Register D after PWRGD =1 See Section 23.11, "Power Management".

b6

Read as zero and cannot be written.

b5:b0

Day of month Alarm; these bits store the day of month alarm value. If set to 000000b, then a don't care state is assumed. The host must configure the Day of month alarm for these bits to do anything, yet they can be written at any time. If the Day of month alarm is not enabled, these bits will return zeros. These bits are not affected by RESET_DRV, VCC1_POR or VCC2_POR. The BCD Range for the Day of month of month alarm is 1-31 and the Binary Range is 01-1F.

23.7.5 Century Byte

The century byte is located at RTC/Bank0 register 0x32. The century byte is incremented by one when the year byte changes from 99 or 0x63 to 0. The BCD Range for the century byte is 00-99 and the Binary Range is 00-63.

23.7.6 General Purpose

Registers 0xEh-0x7EH, except 0x32 (The Century Byte) in Bank0 and 0x0-0x7E in Bank1 are general purpose "CMOS" registers. These registers can be used by the host or 8051 and are fully available during the time update cycle. The contents of these registers are preserved by VCC0 power. Registers Eh-7Eh are in bank0 and registers 80h-FEh are in bank1.

23.7.7 Shared RTC Control

Each bank's last addressable location (0x7F) accesses the Shared RTC Control. The Shared RTC Control Register implements an interface that allows the 8051 to read/write the RTC and CMOS registers by use of the smart host protocol. Refer to 8051 RTC CMOS access, Section 23.9, "8051 RTC CMOS access," on page 266 for the definition of this register.

23.8 Interrupts

The RTC includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 122.070 ms. The update ended interrupt may be used to indicate to the program that an update cycle is completed. Each of these independent interrupts are described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive by writing a "1" to the appropriate enable bits in Register B. A "0" in an enable bit prohibits the IRQB port from being asserted due to that interrupt cause. When an interrupt event occurs a flag bit is set to a "1" in Register C, which are set independent of the state of the corresponding enable bits in Register B. Each of the three interrupt sources have separate flag bits in Register C. The flag bits may be used with or without enabling the corresponding enable bits. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included in Register C to ensure the bits that are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts are held until after the read cycle. If an interrupt flag is already set when the interrupt becomes enabled, the IRQB port is immediately activated, though the interrupt initiating the event may have occurred much earlier.

When an interrupt flag bit is set and the corresponding interrupt-enable bit is also set, the IRQB port is driven low. IRQB is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a "1" whenever the IRQB port is being driven low.

23.8.1 Frequency Divider

The RTC has 22 binary divider stages following the clock input. The output of the divider is a one Hertz signal to the update-cycle logic. The divider is controlled by the three divider bits (DV3-DV0) in Register A. As shown in Table 23.6 the divider control bits can select the operating mode, or be used to hold the divider chain reset that allows precision setting of the time. When the divider chain is changed from reset to the operating mode, the first update cycle is one-half second later.

23.8.2 Periodic Interrupt Selection

The periodic interrupt allows the IRQB port to be triggered from once every 500 ms to once every 122.07 µs. As Table 23.7 shows, the periodic interrupt is selected with the RS0-RS3 bits in Register A. The periodic interrupt is enabled with the PIE bit in Register B.

23.9 8051 RTC CMOS access

The LPC47N350FR implements an interface that allows the 8051 to read/write the RTC and CMOS registers under the following conditions: When nRESET_OUT is active, or when VCC2 is off, or by use of the smart host protocol.

RTCCNTRL (RTC Control) Register

HOST	N/A
8051	0x7FF5
POWER	VCC1
DEFAULT	0x80

The RTC Control register is mirrored in CMOS register 0x7Fh in both bank0 and bank1.

D7	D6	D5	D4	D3	D2	D1	D0
nSH	0	0	0	KREQH	HREQH	KREQL	HREQL

nSH

nSmart Host - This bit is controlled by the 8051. When set to a “1”, the host is not a smart host and does not recognize the sharing protocol. When set to a “0”, the host is smart and can recognize the sharing protocol. When set to “1”, this bit will clear HREQH and HREQL. Clearing this bit to “0” will allow the 8051 to regain access to the CMOS RAM.

KREQL

Keyboard Request Low - The 8051 can set this bit when HREQL IS '0'. If the request is not granted, this bit is read back as a zero and the request must be tried again.

Note: After regaining control of the CMOS, the 8051 must re-write the RTC Low Address Register before accessing the RTC Data Register. This bit selects access to the CMOS RAM Addresses 0-7F.

HREQL

Host Request Low - This bit can be set by the host when KREQL is “0”. If the request is not granted, this bit is read back as a “0” and the request must be tried again.

KREQH

Keyboard Request High - This bit can be set by the 8051 when HREQH is “0” If the request is not granted, this bit is read back as a “0” and the request must be tried again. Note: After regaining control of the CMOS, the 8051 must re-write the RTC High Address Register before accessing the RTC Data Register. This bit selects access to the CMOS RAM Addresses 80-FF.

HREQH

Host Request High - This bit can be set by the host when KREQH is “0”. If the request is not granted, this bit is read back as a “0” and the request must be tried again.

NSH	KREQX	HREQX	BUS ACCESS
1	X	X	Host
0	0	0	None
0	1	0	8051
0	0	1	Host

RTC Address Register (High and Low)

HOST	N/A
8051	0x7FF8 & 0x7FF6
POWER	VCC1
DEFAULT	0x00 & 0x00

When KREQ=1 in the RTC Control register, the Low Address Register and the High Address Register are used to access the 256 CMOS RAM registers. The Low Address Register is used to provide the address to access the 128 CMOS RAM registers in bank0 and the High Address Register is used to provide the address to access the 128 CMOS RAM registers in bank1. Bit D7 of the Low Address Register and the High Address Register are not used for the address decode and are don't care bits.

RTC Data Register (High and Low)

HOST	N/A
8051	0x7FF9 & 0x7FF7
POWER	VCC1
DEFAULT	0x00 & 0x00

The low register is used to access the first bank of 128 bytes, in CMOS RAM the high register is used to access the second bank of 128 registers. This register is used to read or write the selected CMOS register when KREQ=1.

23.10 32kHz Clock Input

The LPC47N350 uses the XOSEL pin to select either a 32.768kHz input clock or a 32.768kHz crystal to drive the Real Time Clock Interface (Table 2.2, "Pin Function Description").

When XOSEL = '0', the RTC uses a 32.768kHz crystal connected between the XTAL1 and XTAL2 pins. When XOSEL = '1', the RTC is driven by a 32.768kHz single-ended clock source connected to the XTAL2 pin.

Note: $I_{CC0} \geq 10\mu A$ for time-keeping operations under V_{CC0} using a single-ended clock source. $I_{CC1} = 30\mu A$ under V_{CC1} using a single-ended clock source.

23.11 Power Management

The RTC and CMOS RAM utilize VCC0 power plane (see Section 2.3, "Power Configuration"). See Figure 2.2, "VCC2 Power-Up Timing" and Figure 2.3, "VCC1_PWRGD Timing".

The VCC1 POR does not affect the clock, calendar, or RAM functions. When VCC1 POR is active the following occurs:

- Periodic Interrupt Enable (PIE) is cleared to “0”.
- Alarm Interrupt Enable (AIE) bit is cleared to “0”.
- Update Ended Interrupt Enable (UIE) bit is cleared to “0”.
- Update Ended Interrupt Flag (UF) bit is cleared to “0”.
- Interrupt Request status Flag (IRQF) bit is cleared to “0”.
- Periodic Interrupt Flag (PIF) is cleared to “0”.
- The RTC and CMOS registers are not accessible.
- Alarm Interrupt Flag (AF) is cleared to “0”.
- nIRQ pin is in high impedance state.

If both the main power (VCC1) and the battery power (VCC0) are both low at the same time and then re-applied (for example, a new battery is installed) the following occurs:

- Initialize all registers 00-0D to a “00” when VCC1 is applied.
- The oscillator is disabled immediately.

When PWRGD = 0, all host inputs are locked out so that the internal registers cannot be modified by the host system. The Host lockout condition continues for 500usec (min) to 1msec (max) after PWRGD =1. The Host lockout condition does not occur when either of the following occur:

- RTC Divider Selection mode is not in normal mode in Table 23.6.

Chapter 24 PCI Clock Run Support

24.1 Overview

The LPC47N350 supports the PCI CLKRUN# signal. CLKRUN# is used to indicate the PCI clock status as well as to request that a stopped clock be started. See Figure 24.1, an example of a typical system implementation using CLKRUN#.

CLKRUN# support is required because the LPC47N350 interrupt interface relies entirely on Serial IRQs and PCI clock is required to drive the SER_IRQ signal (see Section 25.1, "SERIRQ Mode Bit Function").

The LPC47N350 SerIRQ Mode control is in bit D2 of the Device Mode register CR25 (see Section 27.3, "Chip-Level (Global) Control/Configuration Registers [0x00-0x2F]"]. When the SerIRQ Mode bit is '0', Serial IRQs are disabled and the CLKRUN# pin is disabled. When the SerIRQ Mode bit is '1', Serial IRQs are enabled, the CLKRUN# pin is enabled, and the CLKRUN# support related to nLDRQ as described in the section below is enabled.

24.2 Using CLKRUN#

The CLKRUN# pin is an open drain output and input. Refer to the *PCI Mobile Design Guide Rev 1.0* for a description of the CLKRUN# function. If CLKRUN# is sampled "high", the PCI clock is stopped or stopping. If CLKRUN# is sampled "low", the PCI clock is starting or started (running). CLKRUN# in the LPC47N350 supports Serial IRQ.

24.2.1 CLKRUN# Support for Serial IRQ Cycle

If a device in the LPC47N350 asserts or de-asserts an interrupt and CLKRUN# is sampled "high", the LPC47N350 can request the restoration of the clock by asserting the CLKRUN# signal asynchronously (Table 24.1). The LPC47N350 holds CLKRUN# low until it detects two rising edges of the clock. After the second clock edge, the LPC47N350 must disable the open drain driver (Figure 24.2).

The LPC47N350 must not assert CLKRUN# if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR in Figure 24.1. The LPC47N350 will not assert CLKRUN# under any conditions if the Serial IRQs are disabled.

The LPC47N350 must not assert CLKRUN# unless the line has been deasserted for two successive clocks; i.e., before the clock was stopped (Figure 24.2).

Table 24.1 LPC47N350 CLKRUN# Function

SIRQ_MODE (BIT 2 OF CR25)	INTERNAL INTERRUPT	CLKRUN#	ACTION
0	X	X	None
1	NO CHANGE	X	
	CHANGE/ASSERTION	0	
		1	Assert CLKRUN#

Note: "Change" means either-edge change on any or all parallel IRQs routed to the Serial IRQ block. "Assertion" means assertion of DMA request by a device in the LPC47N350. The "change" detection logic must run asynchronously to the PCI Clock and regardless of the Serial IRQ mode; i.e., "continuous" or "quiet".

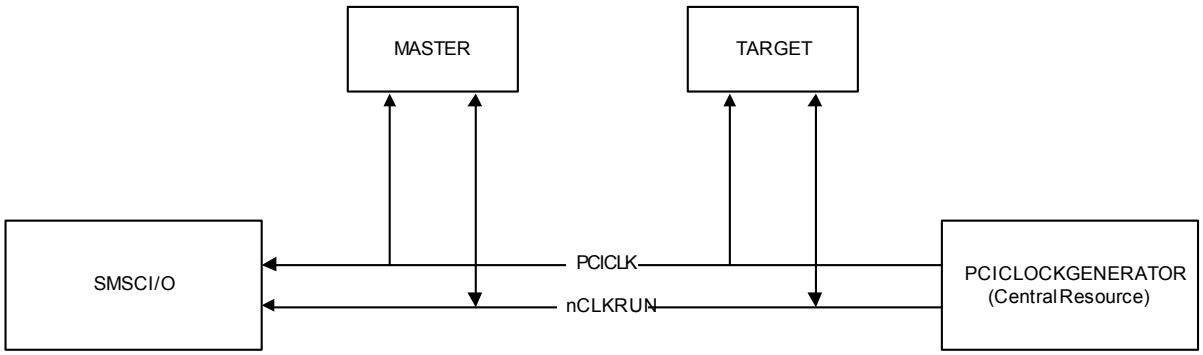


Figure 24.1 CLKRUN# System Implementation Example

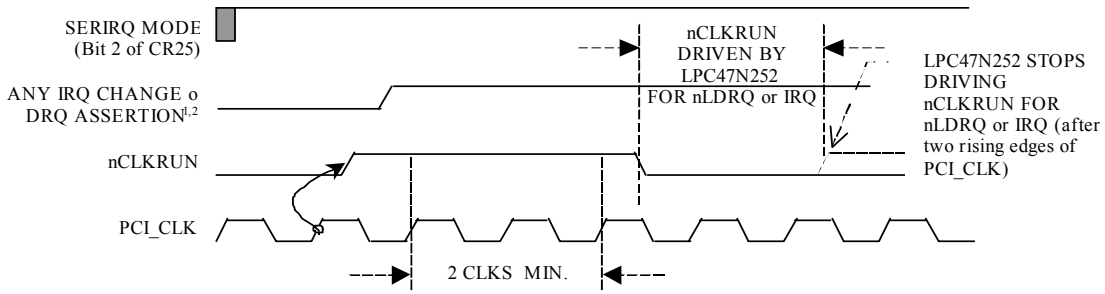


Figure 24.2 Clock Start Illustration

Notes:

1. The signal “ANY IRQ CHANGE or DRQ ASSERTION” is the same as “CHANGE/ASSERTION” in Table 24.1.
2. The LPC47N350 must continually monitor the state of CLKRUN# to maintain the PCI Clock until an active “any IRQ change” condition has been transferred to the host in a Serial IRQ cycle. For example, if “any IRQ change or DRQ assertion” is asserted before CLKRUN# is de-asserted (not shown in Figure 24.2), the LPC47N350 must assert CLKRUN# as needed until the Serial IRQ cycle has completed.

Chapter 25 Serial Interrupts

MSIO will support the serial interrupt scheme, which is adopted by several companies, to transmit interrupt information to the system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems Version 6.0.

Timing Diagrams for IRQSER Cycle

PCICLK = 33 MHz_IN pin

IRQSER = SIRQ pin

Start Frame Timing with Source Sampled a Low Pulse on IRQ1

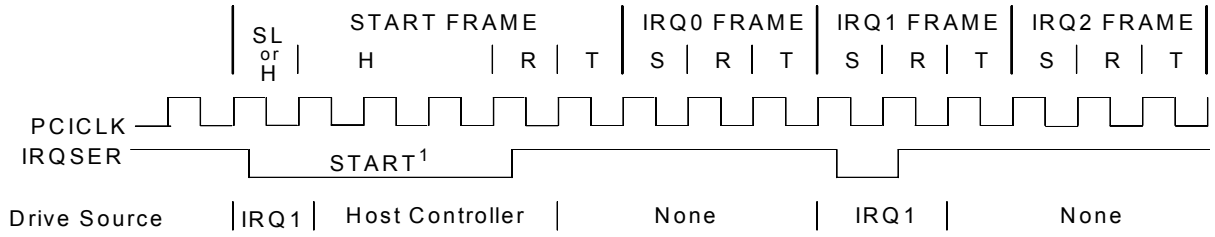


Figure 25.1 Serial Interrupts Waveform "Start Frame"

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Start Frame pulse can be 4-8 clocks wide.

Stop Frame Timing with Host Using 17 IRQSER Sampling Period

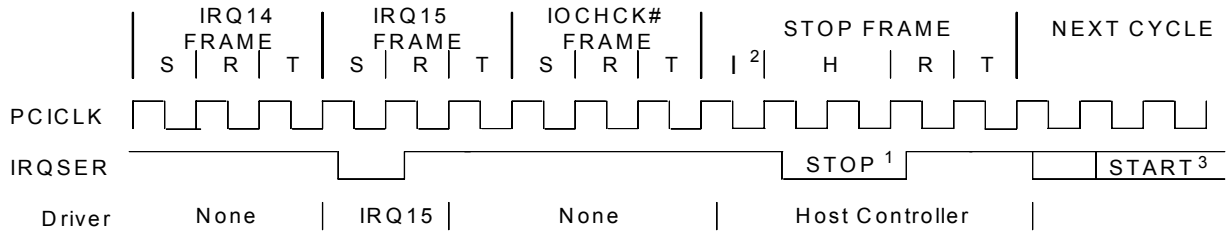


Figure 25.2 Serial Interrupt Waveform "Stop Frame"

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle

- Stop pulse is two clocks wide for Quiet mode, three clocks wide for Continuous mode.
- There may be none, one, or more Idle states during the Stop Frame.
- The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

25.1 SERIRQ Mode Bit Function

Table 25.1 SERIRQ_EN Configuration Control

CR25 BIT[2]	NAME	DESCRIPTION
0	SERIRQ_EN	Serial IRQ Disabled
1		Serial IRQ Enabled (Default)

IRQSER Cycle Control

There are two modes of operation for the IRQSER Start Frame:

1. Quiet (Active) Mode

Any device may initiate a Start Frame by driving the IRQSER low for one clock, while the IRQSER is Idle. After driving low for one clock, the IRQSER must immediately be tri-stated without at any time driving high. A Start Frame may not be initiated while the IRQSER is active. The IRQSER is Idle between Stop and Start Frames. The IRQSER is active between Start and Stop Frames. This mode of operation allows the IRQSER to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated, the host controller will take over driving the IRQSER low in the next clock and will continue driving the IRQSER low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the host controller will drive the IRQSER back high for one clock then tri-state.

Any IRQSER Device (i.e., The LPC47N350) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the host controller unless the IRQSER is already in an IRQSER Cycle and the IRQ/Data transition can be delivered in that IRQSER Cycle.

2. Continuous (Idle) Mode

Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other IRQSER agents become passive and may not initiate a Start Frame. IRQSER will be driven low for four to eight clocks by host controller. This mode has two functions. It can be used to stop or idle the IRQSER or the host controller can operate IRQSER in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An IRQSER mode transition can only occur during the Stop Frame. Upon reset, IRQSER bus is defaulted to continuous mode, therefore only the host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next IRQSER Cycle's mode.

IRQSER Data Frame

Once a Start Frame has been initiated, the LPC47N350 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the sample phase, the LPC47N350 must drive the IRQSER (SIRQ pin) low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, IRQSER must be left tri-stated. During the recovery phase, the LPC47N350 must drive the SERIRQ high, if and only if, it had driven the IRQSER low during the previous sample phase. During the turn-around phase, the LPC47N350 must tri-state the SERIRQ. The LPC47N350 drives the IRQSER line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the start frame.

The Sample phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one, e.g. the IRQ5 Sample clock is the sixth IRQ/Data Frame, then the sample phase is {(6 x 3) - 1 = 17} the seventeenth clock after the rising edge of the Start Pulse.

Table 25.2 IRQSER Sampling Periods

IRQSER PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	Not Used	2
2	IRQ1	5
3	nSMI/IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SIRQ data frame will now support IRQ2 from a logical device; previously IRQSER Period 3 was reserved for use by the System Management Interrupt (nSMI). When using Period 3 for IRQ2, the user should mask off the LPC47N350's SMI via the ESMI Mask Register. Likewise, when using Period 3 for nSMI, the user should not configure any logical devices as using IRQ2.

IRQSER Period 14 is used to transfer IRQ13. Logical devices 4 (Ser Port), 6 (RTC), and 7 (KBD) will have IRQ13 as a choice for their primary interrupt.

Stop Cycle Control

Once all IRQ/Data Frames have completed, the host controller will terminate IRQSER activity by initiating a Stop Frame. Only the host controller can initiate the Stop Frame. A Stop Frame is indicated when the IRQSER is low for two or three clocks. If the Stop Frame's low time is two clocks, then the next IRQSER cycle's sampled mode is the Quiet mode; and any IRQSER device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks, then the next IRQSER cycle's sampled mode is the continuous mode, and only the host controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

Latency

Latency for IRQ/Data updates over the IRQSER bus in bridge-less systems with the minimum IRQ/Data Frames of seventeen will range up to 96 clocks (3.84μS with a 25 MHz PCI Bus or 2.88μs with a 33 MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

EOI/ISR Read Latency

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the IRQSER Cycle latency in order to ensure that these events do not occur out of order.

AC/DC Specification Issue

All IRQSER agents must drive/sample IRQSER synchronously related to the rising edge of the PCI bus clock. IRQSER (SIRQ) pin uses the electrical specification of the PCI bus. Electrical parameters will follow the PCI specification section 4, sustained tri-state.

Reset and Initialization

The IRQSER bus uses nPCIRST as its reset signal (nPCIRST is equivalent to using nRESET_OUT) and follows the PCI bus reset mechanism. The IRQSER pin is tri-stated by all agents while nPCIRST is active. With reset, IRQSER slaves and bridges are put into the (continuous) Idle mode. The host controller is responsible for starting the initial IRQSER cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent IRQSER cycles. It is the host controller's responsibility to provide the default values to the 8259's and other system logic before the first IRQSER cycle is performed. For IRQSER system suspend, insertion, or removal application, the host controller should be programmed into Continuous (IDLE) mode first. This is to guarantee IRQSER bus is in Idle state before the system configuration changes.

Chapter 26 XNOR Chain Test Mode

An XNOR-Chain test structure is in to the LPC47N350 to allow users to confirm that all pins are in contact with the motherboard during assembly and test operations (Figure 26.1).

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the LPC47N350 pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

26.1 Pins in XNOR Chain Structure

All pins are inputs into the XNOR-Chain with the exception of the following pin:

- VCC0 pins
- VCC1 pins
- VCC2 pins
- AGND pin
- VSS pin
- XTAL1 pin
- XTAL2 pin
- XOSEL pin
- nRESET_OUT pin (this is the XNOR-Chain output)
- TEST_PIN (this is the XNOR-Chain enable input)

26.2 Entering and Exiting the XNOR Chain

The XNOR-Chain test is entered as follows in the LPC47N350:

- Apply first rising edge on TEST_PIN. In this mode, KDAT, KCLK, IMDAT, and IMCLK are turned into inputs.
- Set KDAT = KCLK = IMDAT = 0 and IMCLK = 1. Apply another rising edge of TEST_PIN, the part enters the XNOR-Chain test mode.

When activated, the test mode allows one single input pin, when switched, to toggle the nRESET_OUT output.

The XNOR-Chain is exited as follows in the LPC47N350:

- Set KDAT = KCLK = IMDAT = 0 and IMCLK = 0. Apply another rising edge of TEST_PIN, the part exits the XNOR-Chain test mode.

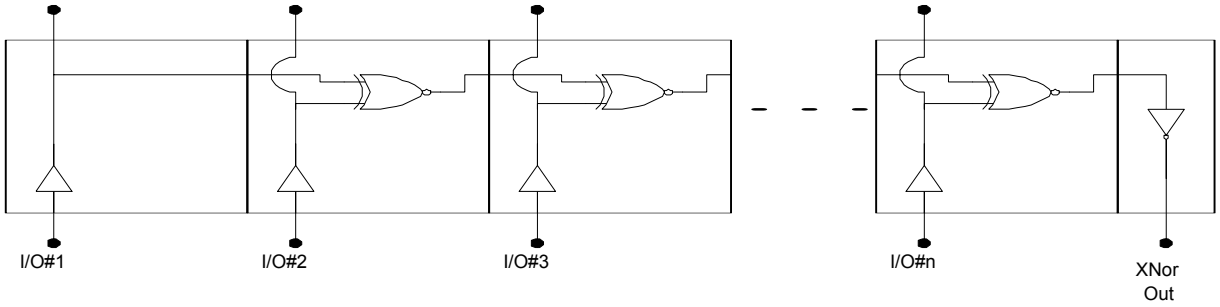


Figure 26.1 XNOR Chain Test Structure

Chapter 27 LPC47N350 Configuration

27.1 Overview

The Configuration of the LPC47N350 is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components.

The LPC47N350 is designed for motherboard designs in which the resources required by their components are known. With its flexible resource allocation architecture, the LPC47N350 allows the BIOS to assign resources at POST.

27.2 Configuration Register Access

Only two states are defined (Run and Configuration). In the Run State, the chip will always be ready to enter the Configuration State.

The desired configuration registers are accessed in two steps:

a. Write the index of the Logical Device Number Configuration Register (i.e., 0x07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT.

b. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

Note: If accessing the Global Configuration Registers, step (a) is not required.

27.2.1 Primary Configuration Address Decoder

The logical devices are configured through three Configuration Access Ports (CONFIG, INDEX and DATA). The BIOS uses these ports to initialize the logical devices at POST (Table 27.1).

The MODE pin is a hardware configuration pin that sets the default Configuration Access Port base address at power-up. The status of the mode pin can be read by the 8051 through the Led Register (MMCR 7F21h). See Section 7.8.4, "LED Controls," on page 63. The Configuration Ports base address can also be changed using the configuration ports base address register (see Section 27.2.3, "Base Address Configuration Registers").

Table 27.1 LPC47N350 Configuration Access Ports

PORT NAME	MODE PIN = 0 (10K PULL-DOWN RESISTOR OR TIE TO GND)	MODE PIN = 1 (10K PULL-UP RESISTOR OR TIE TO VCC1)	TYPE
CONFIG PORT	0x02E	0x04E	Write
INDEX PORT			Read/Write
DATA PORT	INDEX PORT + 1		

Note 27.1 This address can be changed by configuration registers 26h and 27h.

27.2.1.1 Entering the Configuration State

The INDEX and DATA ports are effective only when the chip is in the Configuration State. The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = < 0x55>

27.2.1.2 Exiting the Configuration State

The device exits the Configuration State when the following Config Key is successfully written to the CONFIG PORT address.

Config Key = < 0xAA>

27.2.1.3 Read Accessing Configuration Port

The Configuration Port reads back a float condition when not in the Configuration State. The Configuration Port reads back 0x00, after the Configuration Key 0x55 has been written to the Configuration Port, but prior any further writes to the Configuration Port. After the Configuration Index Register has been written to at least once (in the Configuration State), then the last value written to the Configuration Index Register (via the Configuration Port) can be read back.

27.2.2 Configuration Sequence Example

To program the configuration registers, the following sequence must be followed:

Enter Configuration Mode

Configure the Configuration Registers

Exit Configuration Mode

The following is an example of a configuration program in Intel 8086 assembly language.

```
;----------------------------.
; ENTER CONFIGURATION MODE   |
;----------------------------'
MOV DX,02EH
MOV AX,055H
OUT DX,AL
;-----------------------------------.
; CONFIGURE REGISTER CRE0,    |
; LOGICAL DEVICE 8            |
;-----------------------------------'
MOV DX,02EH
MOV AL,07H
OUT DX,AL ;Point to LD# Config Reg
MOV DX,02FH
MOV AL, 08H
OUT DX,AL;Point to Logical Device 8
;
MOV DX,02EH
MOV AL,E0H
OUT DX,AL      ; Point to CRE0
MOV DX,02fH
MOV AL,02H
OUT DX,AL      ; Update CRE0
;----------------------------.
; EXIT CONFIGURATION MODE     |
;----------------------------'
MOV DX,02EH
MOV AX,0AAH
OUT DX,AL.
```

27.2.3 Base Address Configuration Registers

The LPC47N350 configuration ports base address is relocatable beyond the two addressing options provided by the MODE pin. The ability to relocate the configuration ports base address can prevent address conflicts. Registers CR26 and CR27 enable the relocatable configuration ports base address function. CR26 is the configuration ports base address least significant byte; CR27 is the most significant byte (Table 27.2). The configuration ports base address is relocatable on even-byte boundaries; i.e., A0 = “0”. Valid configuration ports base address values are 0x0000 – 0x0FFE.

Prior to Vcc2 POR, the configuration ports base address are undefined. At Vcc2 POR, the configuration ports base address is determined by the MODE pin.

To relocate the configuration ports base address after power-up, first write the lower address byte (LSB) of the new base address to CR26 and then write the upper address bits to CR27.

Note: Writing CR27 changes the configuration ports base address.

Table 27.2 Configuration Port Address Registers

INDEX	TYPE	HARD RESET (SEE Note 27.2)	REGISTER NAME	DESCRIPTION							
				D7	D6	D5	D4	D3	D2	D1	D0
GLOBAL CONFIGURATION REGISTERS											
0x26 (See Note 27.3)	R/W	MODE = 0: 0x2E MODE = 1: 0x4E	Configuration Port Base Address Byte 0 (LSB)	A7	A6	A5	A4	A3	A2	A1	“0”
0x27 (See Note 27.4)	R/W	MODE = 0: 0x00 MODE = 1: 0x00	Configuration Port Base Address Byte 1 (MSB)	“0”	“0”	“0”	“0”	A11	A10	A9	A8

Note 27.2 The MODE pin determines the configuration port base address following Hard Reset Configuration Register (See Section Hard Reset Configuration Register). Soft Reset Configuration Register has no effect on CR26 and CR27

Note 27.3 The configuration ports base address is relocatable on even-byte boundaries; i.e., A0 = “0”.

Note 27.4 Writing CR27 changes the configuration ports base address.

27.2.4 Configuration Register Reset Conditions

27.2.4.1 Hard Reset Configuration Register

HARD RESET = VCC2 POR or nRESET_OUT pin asserted.

(See Section 7.8.3.5, "Output Enable Register" for description 8051 control of nRESET_OUT)

27.2.4.2 Soft Reset Configuration Register

SOFT RESET = Configuration Control Register Bit0 set to a one by host.

27.2.5 Configuration Register Map

The LPC47N350 Configuration register map is shown below in Table 27.1.

Table 27.3 LPC47N350 Configuration Register Map

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER NAME
GLOBAL CONFIGURATION REGISTERS				
0x02	W	0x00	0x00	Config Control
0x03	-	-	-	RESERVED
0x07	R/W	0x00	0x00	Logical Device Number
0x17	-	-	-	RESERVED

Table 27.3 LPC47N350 Configuration Register Map (continued)

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER NAME
GLOBAL CONFIGURATION REGISTERS				
0x20	R	0x15	0x15	LPC47N350 Device ID
0x21	R	**0x00**	0x00	Device Rev – hard wired
0x22	R/W	0x00	n/a	Power Control
0x23	R/W	0x00	n/a	Power Mgmt
0x24	R/W	0x04	n/a	OSC
0x25	R/W	0x04	n/a	Device Mode
0x26	R/W	See Note 27.2		Configuration Port Base Address (LSB)
0x27	R/W			Configuration Port Base Address (MSB)
0x28 – 0x2F	-	0x00	0x00	RESERVED (Test Mode Registers)
LOGICAL DEVICE 0 CONFIGURATION REGISTERS (RESERVED)				
LOGICAL DEVICE 1 CONFIGURATION REGISTERS (PM1) - OPTIONAL				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
LOGICAL DEVICE 2 CONFIGURATION REGISTERS (RESERVED)				
LOGICAL DEVICE 3 CONFIGURATION REGISTERS (RESERVED)				
LOGICAL DEVICE 4 CONFIGURATION REGISTERS (SERIAL PORT)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	UART Register Base I/O Address
0x70	R/W	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	n/a	Serial Port Mode Register
LOGICAL DEVICE 5 CONFIGURATION REGISTERS (RESERVED)				
LOGICAL DEVICE 6 CONFIGURATION REGISTERS (RTC)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x70	0x00, 0x70	RTC Bank 0 Primary Base Address
0x62, 0x63	R/W	0x00, 0x74	0x00, 0x74	RTC Bank 1 Primary Base Address
0x70	R/W	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	n/a	Real Time Clock Mode Register
0xF1	R	-	-	Shadowed RTC/CMOS Bank 0 Index Register

Table 27.3 LPC47N350 Configuration Register Map (continued)

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER NAME
GLOBAL CONFIGURATION REGISTERS				
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (KBD)				
0x30	R/W	0x00	0x00	Activate
0x70		0x00	0x00	Primary Interrupt Select
0x72		0x00	0x00	Second Interrupt Select
0xF0	R/W	0x00	0x00	KRST_GA20
LOGICAL DEVICE 8 CONFIGURATION REGISTERS (EC)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61		0x00, 0x62	0x00, 0x62	ECI Register Base I/O Address
LOGICAL DEVICE 9 CONFIGURATION REGISTERS (MAILBOX)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61		0x00, 0x00	0x00, 0x00	Mailbox Register Base I/O Address
LOGICAL DEVICE A CONFIGURATION REGISTERS (LGPIO)				
0x30	R/W	0x00	0x00	Activate
0x60		0x00	0x00	LPC GPIO Base I/O Address High Byte
0x61		0x00	0x00	LPC GPIO Base I/O Address Low Byte
LOGICAL DEVICE C CONFIGURATION REGISTERS (Docking LPC)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61		0x00, 0x00	0x00, 0x00	DLPC Runtime Registers Base I/O Address

27.3 Chip-Level (Global) Control/Configuration Registers [0x00-0x2F]

The chip-level (global) registers lie in the address range [0x00-0x2F]. All unimplemented registers and bits ignore writes and return zero when read.

The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessible only in the Configuration State.

Table 27.4 Global Configuration Registers

REGISTER	ADDRESS	DESCRIPTION
CHIP (GLOBAL) CONTROL REGISTERS		
	0x00 –0x01	Reserved, Writes are ignored, reads return 0.

Table 27.4 Global Configuration Registers (continued)

REGISTER	ADDRESS	DESCRIPTION
CHIP (GLOBAL) CONTROL REGISTERS		
Config Control	0x02 W	The hardware automatically clears this bit after the write; there is no need for software to clear the bits. Bit [0] = 1: Soft Reset; Refer to Table 27.3 for the soft reset value for each register.
Card Level Reserved	0x03W	Reserved - Writes are ignored, reads return 0.
	0x04 - 0x06	Reserved - Writes are ignored, reads return 0.
Logical Device #	0x07 R/W	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. Note: The Activate command operates only on the selected logical device.
Card Level Reserved	0x08 - 0x1F	Reserved - Writes are ignored, reads return 0.
Device ID Hard Wired	0x20 R	A read-only register which provides device identification.: Bits[7-0] = 0x15 when read
Device Rev Hard Wired	0x21 R	A read-only register which provides device revision information. Bits[7-0] = 0x01 when read
Power Control	0x22 R/W	Bit[0:3] Reserved (read as 0) Bit[4] Serial Port Power Bit[5:7] Reserved (read as 0) =0 Power off or disabled =1 Power on or Enabled
Power Mgmt	0x23 R/W	Bit[0:3] Reserved (read as 0) Bit[4] Serial Port 1 Bit[5:7] Reserved (read as 0) =0 Power off or disabled =1 Power on or Enabled
OSC	0x24 R/W	Bit[1:0] Reserved, set to “0” Bit[3:2] OSC **=01 (default) OSC and BRG clock are on when PWRGD is active, otherwise, OSC is off and BRG clock disabled.** =10 Same as above (01) case **=00 OSC is on and BRG clock enabled, both regardless of the PWRGD input pin.** =11 OSC is off, BRG Clock is disabled Bit[6:4] CLK_OUT Select for 24MHz_OUT pin =[0,0,0] Off =[0,0,1] CLK_OUT = 14.318 MHz =[0,1,0] CLK_OUT = 16 MHz =[0,1,1] CLK_OUT = 24 MHz =[1,0,0] CLK_OUT = 48 MHz =[1,0,1] Reserved =[1,1,X] Reserved Bit[7] nIRQ8 Polarity =0 nIRQ8 is active high =1 nIRQ8 is active low **Note:** This polarity bit not only affects the nIRQ8 pin, but is also reflected in the Serial IRQ sample phase for the IRQ8 Frame for the Serial IRQ Bus.

Table 27.4 Global Configuration Registers (continued)

REGISTER	ADDRESS	DESCRIPTION
CHIP (GLOBAL) CONTROL REGISTERS		
Device Mode	0x25 R/W	Bit [1-0] Reserved – writes ignored, reads return “0”. Bit[2] SerIRQ Mode (Note 27.5) = 0: Serial IRQ Disabled. = 1: Serial IRQ Enabled (Default). Bit [7:3] Reserved – writes ignored, reads return “0”.
Registers Base Address	0x26-0x27	See Section 27.2.3, "Base Address Configuration Registers".
Test Registers	0x28-0x2B	SMSC Test Mode Registers, Reserved for SMSC.
TEST 0	0x2C	Test Modes - Reserved for SMSC. Users should not write to this register, may produce undesired results.
TEST 1	0x2D R/W	Test Modes: Reserved for SMSC. Users should not write to this register; may produce undesired results.
TEST 2	0x2E R/W	Test Modes - Reserved for SMSC. Users should not write to this register; may produce undesired results.
TEST 3	0x2F R/W	Test Modes - Reserved for SMSC. Users should not write to this register; may produce undesired results.

Note 27.5 The SerIRQ Mode bit controls the SER_IRQ pin and the CLKRUN# pin. (see Section 24.2, "Using CLKRUN#").

27.4 Logical Device Configuration/Control Registers [0x30-0xFF]

Used to access the registers that are assigned to each logical unit. This chip supports ten logical units and has ten sets of logical device registers:

- PM1
- Serial
- Real Time Clock
- Keyboard Controller
- Embedded Controller
- Mailbox Interface

A separate set (bank) of control and configuration registers exists for each Logical Device and is selected with the Logical Device # Register (0x07). The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT. The Logical Device registers are accessible only when the device is in the Configuration State The logical register addresses are listed in Table 27.5.

Table 27.5 Logical Device Configuration Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION
Activate	(0x30)	Bits[7:1] Reserved, set to “0”. Bit[0] = 1 Activates the logical device currently selected through the Logical Device # register. = 0 Logical device currently selected is inactive.
Logical Device Control	(0x31-0x37)	Reserved - Writes are ignored, reads return “0”.

Table 27.5 Logical Device Configuration Registers (continued)

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION
Logical Device Control	(0x38-0x3F)	Vendor Defined – Reserved - Writes are ignored, reads return “0”.
Memory Base Address	(0x40-0x5F)	Reserved - Writes are ignored, reads return “0”.
I/O Base Address (see Table 27.6)	(0x60-0x6F) 0x60= addr[15:8] 0x61= addr[7:0]	All logical devices contain 0x60, 0x61. Unused registers will ignore writes and return “0” when read.
Interrupt Select	(0x70,0x72)	0x70 is implemented for each logical device. Refer to Interrupt Configuration Register description. Only the KYBD controller uses Interrupt Select register 0x72. Unused register (0x72) will ignore writes and return “0” when read. Interrupts default to edge high (ISA compatible).
	(0x71,0x73)	Reserved - not implemented. These register locations ignore writes and return “0” when read.
	(0x74, 0x75)	Reserved - not implemented and ignores writes and returns “0” when read.
32-Bit Memory Space Configuration	(0x76-0xA8)	Reserved - not implemented. These register locations ignore writes and return “0” when read.
Logical Device	(0xA9-0xDF)	Reserved - not implemented. These register locations ignore writes and return “0” when read.
Logical Device Configuration	(0xE0-0xFE)	Reserved - Vendor Defined (see SMSC defined Logical Device Configuration Registers).
Reserved	0xFF	Reserved

Note 27.6 A logical device will be active and powered up according to the following equation:

DEVICE ON (ACTIVE) = (Activate Bit SET AND Pwr/Control Bit SET) AND (8051 Disable Bit SET)

The Logical device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other. The Serial Port bit in the 8051’s Disable Register (see Table 7.8 on page 59) is capable of overriding the Activate and PWR/Control bit settings for logical device 4. Thus clearing bit D6 of the Disable register will disable the Serial Port regardless of the Serial Port’s Activate and PWR/Control bits. When D6 of the Disable register is set, the Serial Port’s Activate and PWR/Control bits will determine the on/off state of the Serial Port. If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

27.5 I/O Base Address Configuration Register Description

Table 27.6 Logical Device, Base I/O Addresses

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (SEE Note 27.7)	FIXED BASE OFFSETS
0x00	Reserved			

Table 27.6 Logical Device, Base I/O Addresses (continued)

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (SEE Note 27.7)	FIXED BASE OFFSETS
0x01	PM1	0x60,0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0: PM1_STS1 +1: PM1_STS2 +2: PM1_EN1 +3: PM1_EN2 +4: PM1_CNTRL1 +5: PM1_CNTRL2 +6: Reserved +7: Reserved
0x02	Reserved			
0x03	Reserved			
0x04	Serial Port 1	0x60,0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0: RB/TB | LSB div +1: IER | MSB div +2: IIR/FCR +3: LCR +4: MCR +5: LSR +6: MSR +7: SCR
0x05	Reserved			
0x06	RTC	0x60, 0x61 0x62, 0x63	[0x100:0x0FFE] [0x100:0x0FFD]	Bank 0 Base address +0: Address Register +1: Data Register Bank 1 Base address +0: Address Register +2: Data Register
0x07	KYBD	N/A	Not Relocatable Fixed Base Address	0x60: Data Register 0x64: Command/Status Reg.
0x08	ECI	0x60, 0x61 (See Note 27.8)	[0x0000:0xFFA] Relocatable	+0: Data Register (See Note 27.9) +4: Command Register
0x09	Mailbox Register	0x60, 0x61	[0x0000:0x0FFE]	+0: Index +1: Data
0x0A	Reserved			

Note 27.7 This chip uses all LPC address bits to decode the base address of each of its logical devices.

Note 27.8 Please refer to Table 61 – ECI Configuration Registers (LDN8) for further description.

Note 27.9 Please refer to Table 62 – ECI Run-Time Registers for further description.

27.6 Interrupt Select Configuration Register Description

Table 27.7 Interrupt Select Configuration Registers

NAME	REG INDEX	DEFINITION
Interrupt request level select 0	0x70 (R/W)	Bit [3-0] Select which interrupt level is used for Interrupt 0. 0x00=no interrupt selected. 0x01=IRQ1 0x02=IRQ2 0x0E= IRQ14 0x0F= IRQ15 All pin-type interrupts are edge high (except ECP/EPP). Each Logical Device's interrupts selected through this register physically select the interrupts to be used by the LPC47N350 for either the Serial IRQ interface or for the individual pin-type ISA interrupts if selected.

Note: An interrupt is activated by setting the Interrupt Request Level Select 0 register to a non-zero value AND:

1. for the Serial Port logical device by setting any combination of bits D0-D3 in the IER and by setting the OUT2 bit in the UART's Modem Control (MCR) Register.
2. for the RTC by (refer to the RTC section of this specification).
3. for the KYBD by (refer to the KYBD controller section of this specification).

27.7 Interrupt and DMA Enable and Disable

Any time the interrupt for a logical block is disabled by a register bit in that logical block, the interrupt output must be disabled. This is in addition to the interrupt disabled by the Configuration Registers (activate bit cleared or address outside of valid range or the Interrupt Select register set to 0x00).

27.7.1 Logical Device 4 (Serial Port)

Modem Control Register (MCR) Bit D2 (OUT2) –

When OUT2 is a logic "0", the serial port interrupt is disabled.

27.7.2 Real Time Clock (RTC)

See Chapter 23, "Real-Time Clock," on page 257.

27.7.3 Keyboard Controller (KYBD)

See Chapter 13, "Keyboard Controller," on page 143.

27.8 SMSC-Defined Logical Device Configuration Registers

The SMSC Specific Logical Device Configuration Registers reset to their default values only on hard resets. These registers are not effected by soft resets. See Section 27.2.4, "Configuration Register Reset Conditions".

Table 27.8 Serial Port, Logical Device 4 [Logical Device Number = 0x04]

NAME	REG INDEX	DEFINITION
Serial Port 1 Mode Register Default = 0x00	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled (default) = 1 High Speed Enabled Bit[7:2] Reserved, set to “0”

Table 27.9 RTC, LOGICAL DEVICE 6 [LOGICAL DEVICE NUMBER = 0X06]

NAME	REG INDEX	DEFINITION	STATE
RTC Mode Register Default = 0x00	0xF0 R/W	Bit[0] = 1: Lock CMOS RAM 80-9Fh Bit[1] = 1: Lock CMOS RAM A0-BFh Bit[2] = 1: Lock CMOS RAM C0-DFh Bit[3] = 1: Lock CMOS RAM E0-FEh Bit[7:4] Reserved, set to “0” Once set, bit[3:0] can not be cleared by a write; bits[3:0] are cleared on VCC2 Power On Reset, VCC2 Power Off, or upon a Hard Reset (nRESET_OUT asserted). Once lock bits are set, both the Host and the 8051 are locked out of accessing the locked locations as long as VCC1 and VCC2 are active. When VCC2 goes to 0V, the lock bits are cleared and the 8051 can access this RAM while nRESET_OUT is asserted.	C

Table 27.10 KYBD, Logical Device 7 [Logical Device Number = 0x07]

NAME	REG INDEX	DEFINITION	STATE
KRST_GA20	0xF0 R/W	Bit[0]: ENAB_P92 = 0: Port 92 Disabled = 1: Port 92 Enabled Bit[7:0]: Reserved, set to “0”.	

Note: See Section 13.4.4, "GATEA20" for descriptions of these registers.

Chapter 28 Electrical Specifications

28.1 Maximum Guaranteed Ratings*

Operating Temperature Range . . . . . 0°C to +70°C

Storage Temperature Range . . . . . -55° to +150°C

Lead Temperature Range (soldering, 10 seconds) . . . . . +325°C

Positive Voltage on any pin, with respect to Ground . . . . . +5.5V

Negative Voltage on any pin, with respect to Ground 0.3V

Supply Voltage Range $V_{CC}1$ and $V_{CC}2$ . . . . . .5 VDC

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Table 28.1 Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Vcc0	Vbat for RTC	2.**0**	3.0	3.3	V
Vcc1	Vcc for 8051	2.97	3.3	3.63	
Vcc2	System Vcc			3.63	
PCI_CLK	PCI Clock		33		MHz
XTAL1/XTAL2	RTC Crystal		32.768		kHz
CLOCKI	14.318 Clock Input		14.318		MHz
T_A	Operating Temperature	0		70	°C

28.1.1 DC Specifications

Table 28.2 DC Electrical Characteristics (T_A = 0°C - 70°C, $V_{CC}1$ and $V_{CC}2$= 3.3 VDC ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{IL}			0.8	V	TTL Levels
High Input Level	V_{IH}	2.0			V	

Table 28.2 DC Electrical Characteristics (T_A = 0°C - 70°C, $V_{CC}1$ and $V_{CC}2$= 3.3 VDC ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IPD Type Buffer **Low Input Level** **High Input Level** **Pull Down**	 **V_{IL}** **V_{IH}** **PD**	 **2.0**	 **30**	 **0.8**	 **V** **V** **uA**	
ISP Type Input Buffer with 90 µA weak pull-up Low Input Level High Input Level Schmitt Trigger Hysteresis	 V_{ILIS} V_{IHIS} V_{HYS}	 2.2 	 250	 0.8 	 V V mV	 Schmitt Trigger Schmitt Trigger
ICLK Input Buffer Low Input Level High Input Level	 VILCK VIHCK	 **2**.0	 	 0.**8** 	 V V	
ICLK2/OCLK2 Crystal Oscillator	Use a 32 Khz parallel resonant crystal oscillator. The load capacitors are seen by the crystal as two capacitors in series and should be approximately **CL = X/Y, X = CL1* CL2, Y = CL1 + CL2.** For example, a 7.5pF crystal should use two 15pF capacitors for proper loading.					
OD4 Type Buffer Low Output Level	 V_{OL}	 	 	 0.4	 V	 V_{OL} = 4 mA
O8 Type Buffer Low Output Level High Output Level	 V_{OL} V_{OH}	 2.4	 	 0.4 	 V V	 I_{OL} = 8 mA I_{OH} = -4 mA
OD8 Type Buffer Low Output Level	 V_{OL}	 	 	 0.4	 V	 V_{OL} = 8 mA
O12 Type Buffer Low Output Level High Output Level	 V_{OL} V_{OH}	 2.4	 	 0.4 	 V V	 I_{OL} = 12mA I_{OH} = -6mA
OD12 Type Buffer Low Output Level Output Leakage	 V_{OL} I_{OL}	 -10	 	 0.4 +10	 V µA	 I_{OL} = 12mA V_{IN} = 0 to 5V
O24 Type Buffer Low Output Level High Output Level	 V_{OL} V_{OH}	 2.4	 	 0.4 	 V V	 I_{OL} = 24 mA I_{OH} = -12 mA
IO4 Type Buffer Low Output Level High Output Level	 V_{OL} V_{OH}	 2.4	 	 0.4 	 V V	 I_{OL} = 4mA I_{OH} = -2mA

Table 28.2 DC Electrical Characteristics (T_A = 0°C - 70°C, $V_{CC}1$ and $V_{CC}2$= 3.3 VDC ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IO8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
IOD8 Type Buffer						
Low Input Level	V_{IL}			0.8	V	
High Input Level	V_{IH}	2.0			V	
Low Output Level	V_{OL}			0.4	V	I_{OL}=8 mA
IO12 Type Buffer						
Low Input Level	V_{IL}			0.8	V	
High Input Level	V_{IH}	2.0			V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IOD12 Type Buffer						
Low Input Level	V_{IL}			0.8	V	
High Input Level	V_{IH}	2.0			V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
Input Leakage (All except PWRGD and VCC1_PWRGD)						
Low Input Leakage	$ILEAK_{IL}$			-10	µA	V_{IN} = 0
High Input Leakage	$ILEAK_{IH}$			+10	µA	$V_{IN} = V_{CC}$ or V_{IN} = 5 V
Input Current	I_{OH}				µA	V_{IN} = 0
PCI type buffers PCI_I, PCI_O, PCI_IO, PCI_CLK	3.3V PCI 2.1 Compatible					

Table 28.3 Power Consumption in Various States

V_{CC2} (VDC)	V_{CC1} (VDC)	8051 STATE	CLOCK STATE	SUPPLY CURRENT (AMPS)				COMMENTS
					MIN	TYP	MAX	
3.3	3.3	Run	Ring OSC	I_{CC2} I_{CC1}		>1ma 8 ma	2 ma 10 ma	PLL On I^2C/SMBus Off
		Idle		I_{CC2} I_{CC1}		>1ma 5ma	2 ma 7 ma	PLL Off
			32 Mhz	I_{CC2} I_{CC1}		TBD	TBD	Flash program cycle
0		Run	Ring OSC	I_{CC2} I_{CC1}		8 ma	10ma	PLL Off I^2C/SMBus Off
		Idle		I_{CC2} I_{CC1}		6 ma	8ma	PLL Off I^2C/SMBus Off
		Sleep	Stop	I_{CC1}			160 µa	XOSEL=1
				I_{CC1}		50 µa	80 µa	XOSEL=0
	0			ICC0		40µa	60 µa	2.**0** < Vcc0 < 4 VDC, XOSEL=1,
				ICC0		0.4µa	1.5 µa	2.**0** < Vcc0 < 4 VDC, XOSEL = 0

Note: When a single-ended 32.768kHz clock source is selected (see Section 23.10, "32kHz Clock Input". The LPC47N350 uses the XOSEL pin to select either a 32.768kHz input clock or a 32.768kHz crystal to drive the Real Time Clock Interface (Table 2.2 on page 4). When XOSEL = '0', The RTC uses a 32.768kHz crystal connected between the XTAL1 and XTAL2 pins. When XOSEL = '1', the RTC is driven by a 32.768kHz single-ended clock source connected to the XTAL2 pin.

28.2 AC Specifications

AC Test Conditions

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{cc} = 3.3 VDC

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10		
Output Capacitance	C_{OUT}			20		

Chapter 29 Timing Diagrams

29.1 Clock and Reset Timing

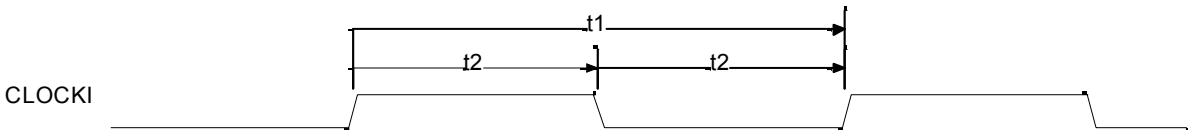


Figure 29.1 Input Clock Timing

Table 29.1 Input Clock Timing Parameters

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318 MHz (See Note)		69.84		ns
t2	Clock High Time/Low Time for 14.318 MHz	15			
tr, tf	Clock Rise Time/Fall Time (not shown)			5	

Note: Tolerance is ± 0.01%.

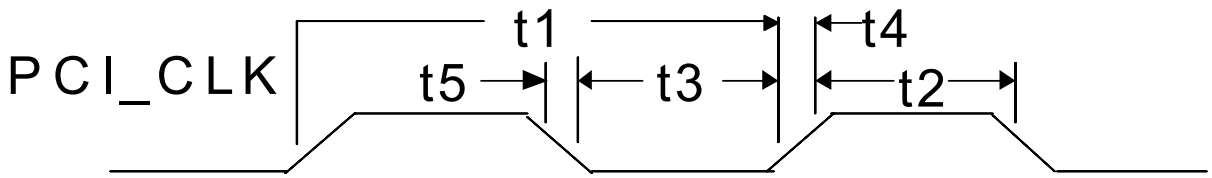


Figure 29.2 PCI Clock Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Period	30		33.3	nsec
t2	High Time	12			
t3	Low Time	12			
t4	Rise Time			3	
t5	Fall Time				

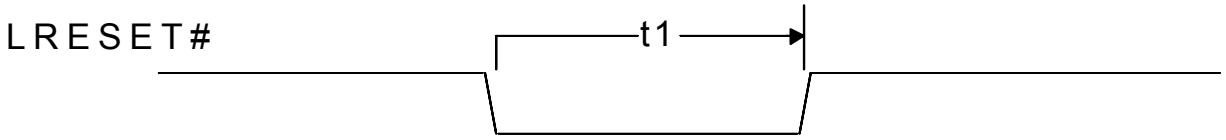


Figure 29.3 Reset Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	LRESET# width	1			ms

29.2 LPC Timing

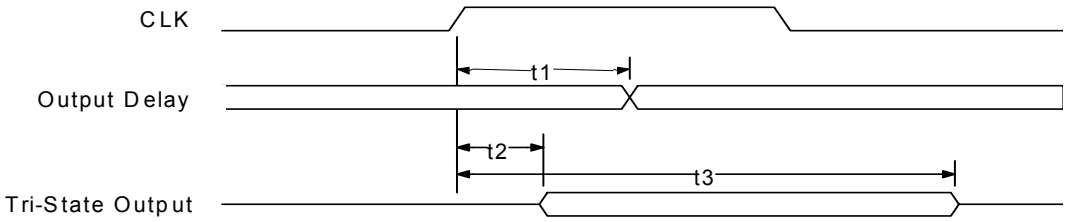


Figure 29.4 Output Timing Measurement Conditions, LPC Signals

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	CLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay				
t3	Active to Float Delay			28	

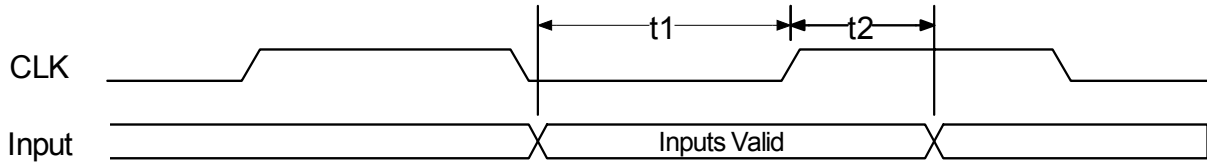


Figure 29.5 Input Timing Measurement Conditions, LPC Signals

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Input Set Up Time to CLK – Bused Signals	7			ns
t2	Input Hold Time from CLK	0			

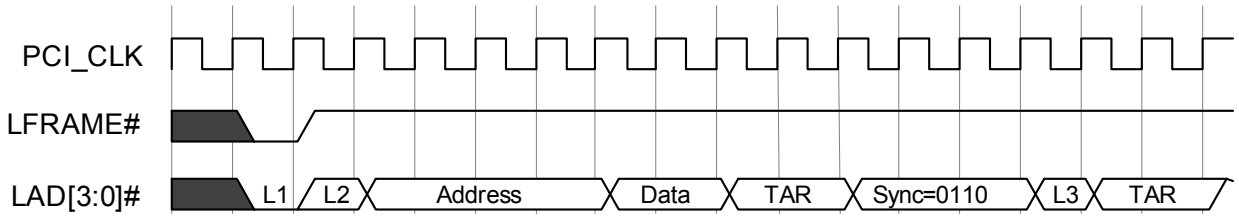


Figure 29.6 I/O Write

Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

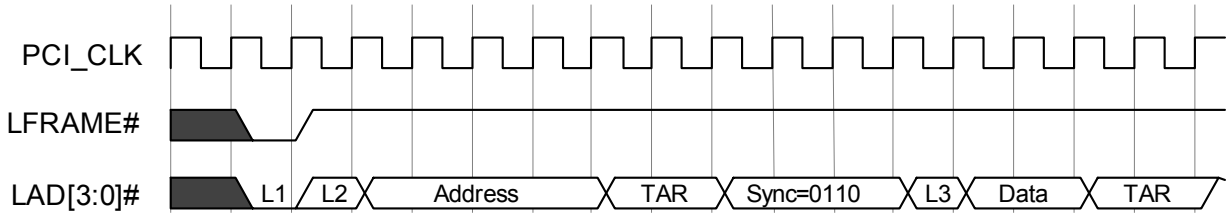


Figure 29.7 I/O Read

Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

29.3 Serial IRQ Timing

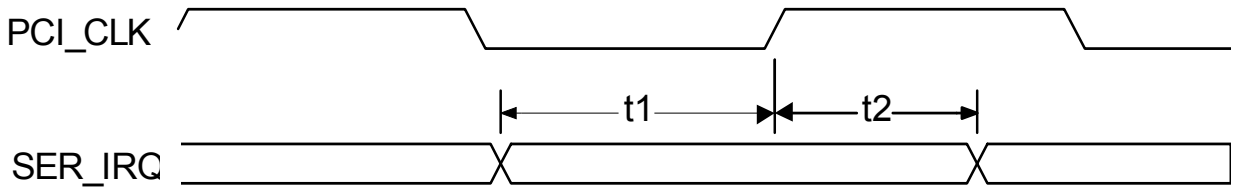


Figure 29.8 Setup and Hold Time

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			

29.4 Serial Port Data Timing

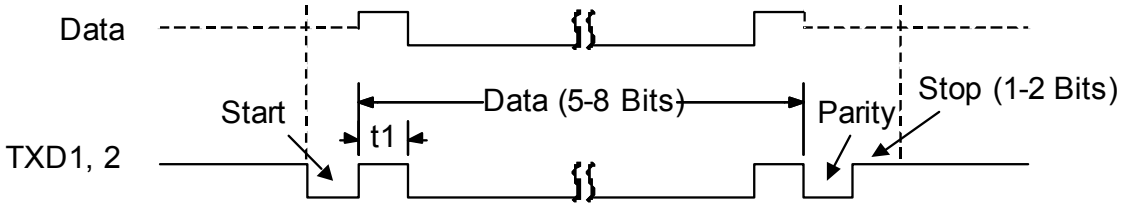


Figure 29.9 Serial Port Data

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Serial Port Data Bit Time		t_{BR} (Note 29.1)		nsec

Note 29.1 t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the “Baud Rate” table in the “Serial Port” section.

29.5 I2C_SMBus Timing

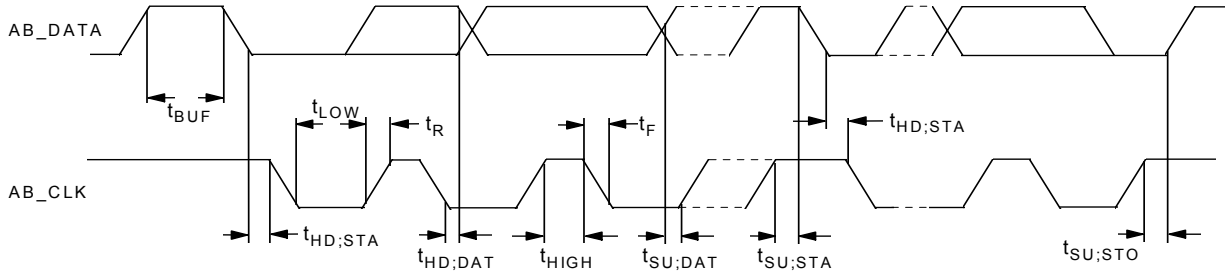


Figure 29.10 I²C/SMBus Timing

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{SCL}	SCL Clock Frequency			100	kHz
t_{BUF}	Bus Free Time	4.7			µs
$t_{SU;STA}$	START Condition Set-Up Time				
$t_{HD;STA}$	START Condition Hold Time	4.0			
t_{LOW}	SCL LOW Time	4.7			
t_{HIGH}	SCL HIGH Time	4.0			
t_R	SCL and SDA Rise Time			1.0	
t_F	SCL and SDA Fall Time			0.3	
$t_{SU;DAT}$	Data Set-Up Time	0.25			
$t_{HD;DAT}$	Data Hold Time	0			
$t_{SU;STO}$	STOP Condition Set-Up Time	4.0			

29.6 Fan and Fan Tachometer Timing

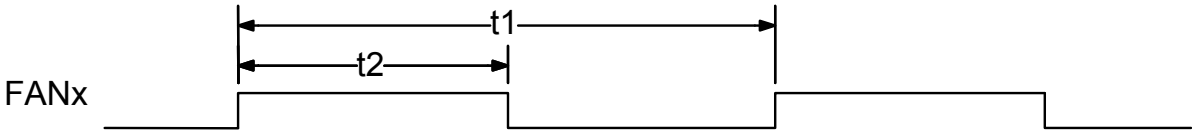


Figure 29.11 Fan Output Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PWM Period (Note 29.2)	0.0254		5.75	msec
t2	PWM High Time (Note 29.3)	0.00039		5.75	

Note 29.2 The period is $1/f_{out}$,where f_{out} is programmed through the PWM Speed Control register, the PWM Control registers, and the PWM Frequency Multiplier Register. The tolerance on f_{out} is +/- 5% and is accounted for in the timing.

Note 29.3 When Bit 0 of the PWMx registers is 0, then the duty cycle is programmed through Bits[6:1] of these registers. If Bits[6:1] = "000000", then the PWMx pin is low. The duty cycle is programmable through Bits[6:1] to be between 1.56% and 98.44%. When Bit 0 is 1, the PWMx pin is high.

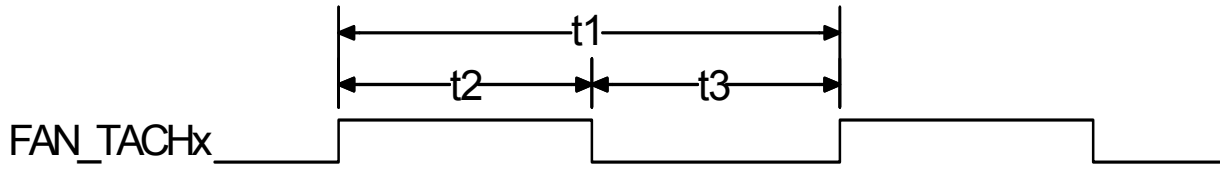


Figure 29.12 Fan Tachometer Input Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Pulse Time (1/2 Revolution Time=30/RPM)	$4T_{TACH}$ (Note 29.4)			µsec
t2	Pulse High Time	$3T_{TACH}$ (Note 29.4)			
t3	Pulse Low Time	T_{TACH}			

Note 29.4 t_{TACH} is the clock used for the tachometer counter. It is 30.52* prescaler, where the prescaler is programmed in the Fan Tachometer Timebase Prescaler register.

29.7 PS/2 Timing

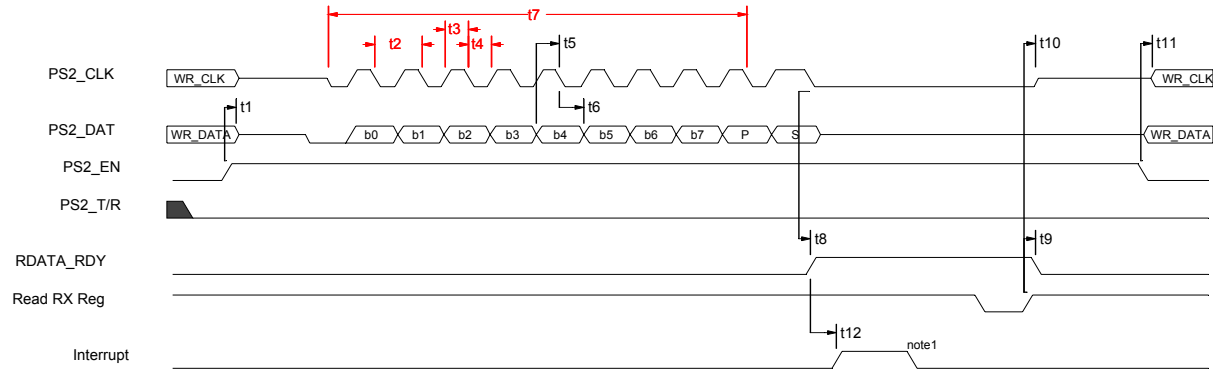


Figure 29.13 PS/2 Channel Receive Timing Diagram

Table 29.2 PS/2 Channel Receive Timing Parameters

PARAMETER		MIN	TYP	MAX	UNITS
t1	The PS2 Channel's CLK and DATA lines are floated following PS2_EN=1 and PS2_T/R=0.			100	ns
t2	Period of CLK	60		302	us
t3	Duration of CLK high (active)	30		151	
t4	Duration of CLK low (inactive)				
t5	DATA setup time to falling edge of CLK. LPC47N350 samples the data line on the falling CLK edge.	1			
t6	DATA hold time from falling edge of CLK. LPC47N350 samples the data line on the falling CLK edge.	2			
t7	Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).			2.002	ms
t8	Falling edge of 11th CLK to RDATA_RDY asserted.			1.6	µs
t9	Trailing edge of the 8051's RD signal of the Receive Register to RDATA_RDY bit deasserted.			100	ns
t10	Trailing edge of the 8051's RD signal of the Receive Register to the CLK line released to high-Z.				
t11	The PS2 Channel's CLK and DATA lines are driven to the values stored in the WR_CLK and WR_DATA bits of the Control Register when PS2_EN is written to 0.				
t12	RDATA_RDY asserted to interrupt generated. Note1- Interrupt is cleared by reading the 8051 INT0 Source Register.				

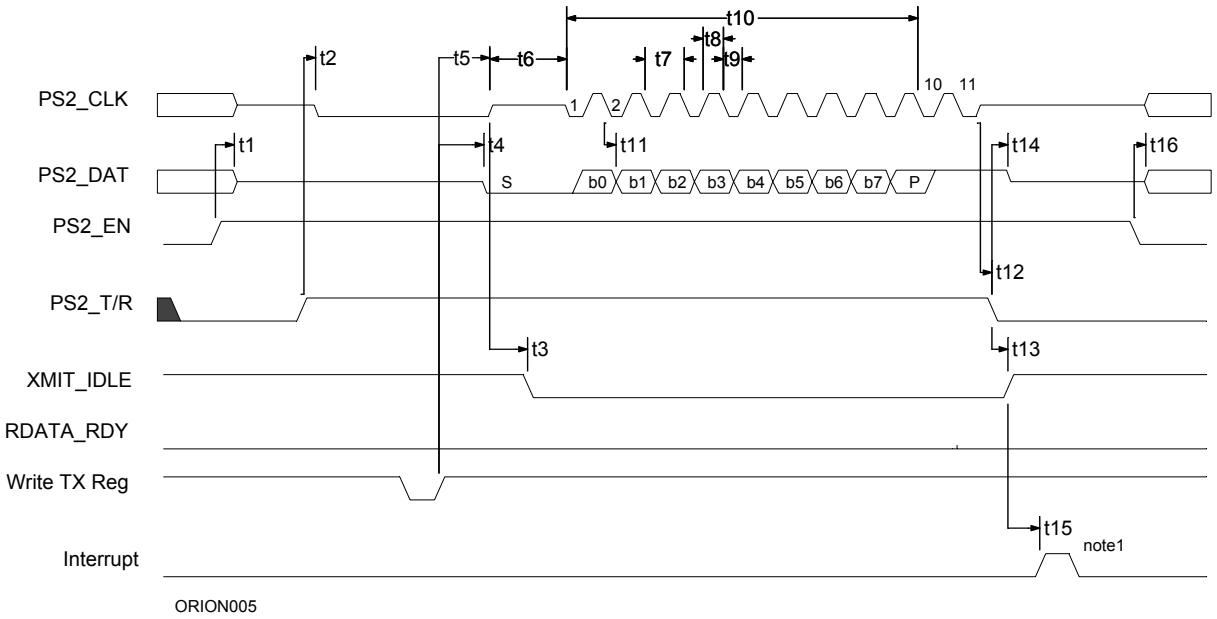


Figure 29.14 PS/2 Channel Transmit Timing Diagram

Table 29.3 PS/2 Channel Transmission Timing Parameters

PARAMETER		MIN	TYP	MAX	UNITS
t1	The PS2 Channel's CLK and DATA lines are floated following PS2_EN=1 and PS2_T/R=0.			100	ns
t2	PS2_T/R bit set to CLK driven low preparing the PS2 Channel for data transmission.			100	
t3	CLK line floated to XMIT_IDLE bit deasserted.			1.7	us
t4	Trailing edge of 8051 WR of Transmit Register to DATA line driven low.	45		90	ns
t5	Trailing edge of 8051 WR of Transmit Register to CLK line floated.	90		130	
t6	Initiation of Start of Transmit cycle by the PS2 channel controller to the auxiliary peripheral's responding by latching the Start bit and driving the CLK line low.	0.002		25.003	ms
t7	Period of CLK	60		302	us
t8	Duration of CLK high (active)	30		151	
t9	Duration of CLK low (inactive)				
t10	Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).			2.002	ms
t11	DATA output by LPC47N350 following the falling edge of CLK. The auxiliary peripheral device samples DATA following the rising edge of CLK.	3.5		7.1	us
t12	Rising edge following the 11th falling clock edge to PS_T/R bit driven low.	400		800	ns

Table 29.3 PS/2 Channel Transmission Timing Parameters (continued)

PARAMETER		MIN	TYP	MAX	UNITS
t13	Trailing edge of PS_T/R to XMIT_IDLE bit asserted.			100	ns
t14	DATA released to high-Z following the PS2_T/R bit going low.				
t15	XMIT_IDLE bit driven high to interrupt generated. Note1- Interrupt is cleared by reading the 8051 INT0 Source Register.				
t16	The PS2 Channel's CLK and DATA lines are driven to the values stored in the WR_CLK and WR_DATA bits of the Control Register when PS2_EN is written to 0.				

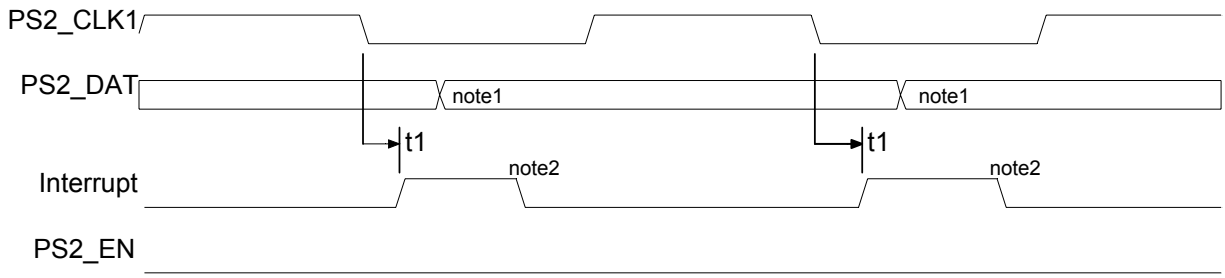


Figure 29.15 PS/2 Channel "Bit-Bang" Transmit Timing Diagram

Table 29.4 PS/2 Channel "Bit-Bang" Transmit Timing Parameters

PARAMETER		MIN	TYP	MAX	UNITS
t1	Falling Edge of CLK to Interrupt generated.			1.1	µs

Note 29.5 8051 firmware responds to interrupt and drives data line before rising edge of PS2_CLK line.

Note 29.6 8051 firmware clears Interrupt by reading the 8051 INT0 Source Register.

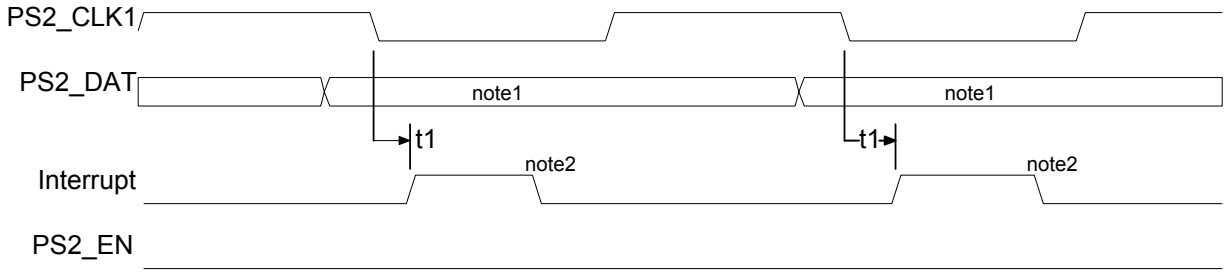


Figure 29.16 PS/2 Channel "Bit-Bang" Receive Timing Diagram

Table 29.5 PS/2 Channel "Bit-Bang" Receive Timing Parameters

PARAMETER		MIN	TYP	MAX	UNITS
t1	Falling Edge of CLK to Interrupt generated.			100	ns

Note 29.7 8051 firmware responds to interrupt and latches data line before rising edge of PS2_CLK line.

Note 29.8 8051 firmware clears Interrupt by reading the 8051 INT0 Source Register.

29.8 Serial Peripheral Interface (SPI) Timings

29.8.1 SPI Clock Timing

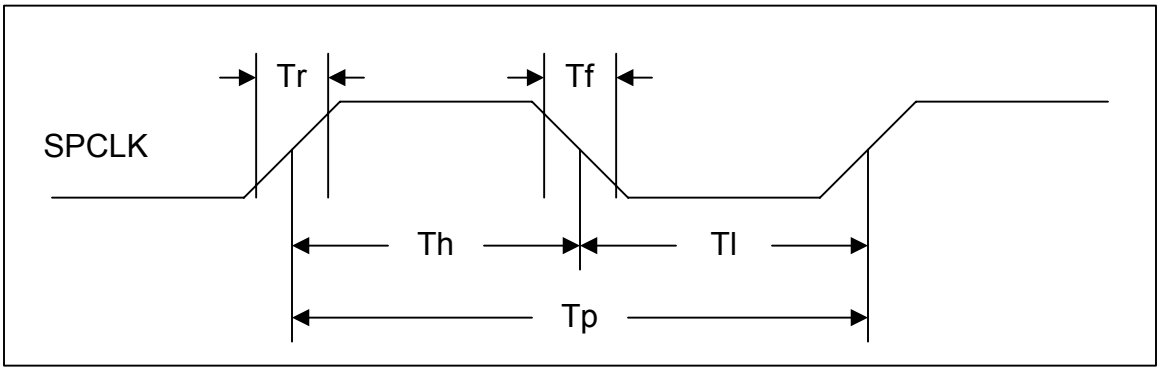


Figure 29.17 SPI Clock Timing

Table 29.6 SPI Clock Timing Parameters

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
Tr	SPI Clock Rise Time. Measured from 10% to 90%.			10% of SPCLK Period	ns
Tf	SPI Clock Fall Time. Measured from 90% to 10%.			10% of SPCLK Period	
Th/Tl	SPI Clock High Time/SPI Clock Low Time	40% of SPCLK Period	50% of SPCLK Period (See Note)	60% of SPCLK Period	
Tp	SPI Clock Period – As selected by SPIBR register.	83.33		31948.88	

Note: If divide by 1 is used on the ring oscillator, the duty cycle may not be 50%. The actual duty cycle of divide by 1 will be provided after characterization.

29.8.2 SPI Setup and Hold Times

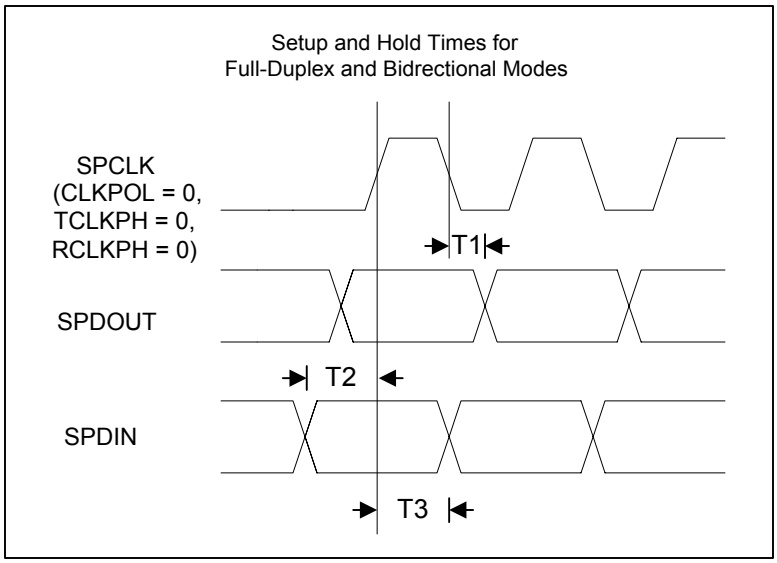


Figure 29.18 SPI Setup and Hold Times

Table 29.7 SPI Setup and Hold Times Parameters

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
T1	Data Output Delay			10	ns
T2	Data IN Setup Time	20			
T3	Data IN Hold Time				

29.8.3 SPI Interface Timings

The following timing diagrams represent a single-byte transfer over the SPI interface using different SPCLK phase settings. Data bits are transmitted in bit order starting with the MSB (LSBF='0') or the LSB (LSBF='1'). See Section 16.7.1.1, "D0 - LSBF - Least Significant Bit First" for information on the LSBF bit. The CS signal in each diagram is a generic bit-controlled chip select signal required by most peripheral devices. This signal and additional chip selects can be GPIO controlled. Note that these timings for Full Duplex Mode are also applicable to Bi-directional mode.

29.8.3.1 SPI Interface Timing – Full Duplex Mode (TCLKPH = 0, RCLKPH = 0)

In this mode, data is available immediately when a device is selected and is sampled on the first and following odd SPCLK edges by the master and slave.

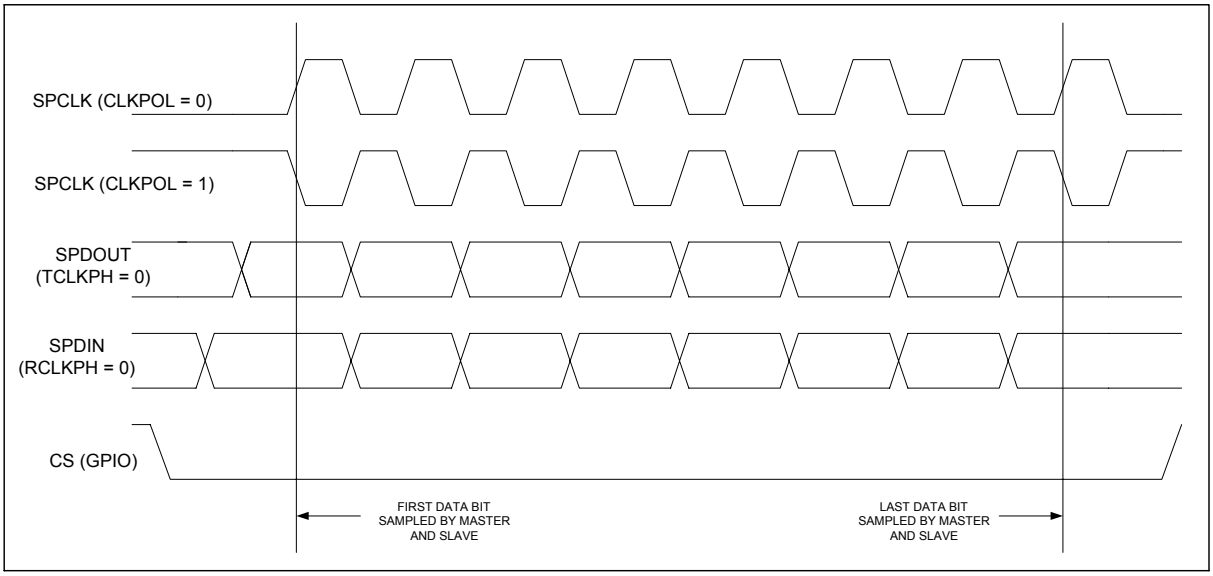


Figure 29.19 SPI Interface Timing, Full Duplex Mode (TCLKPH = 0, RCLKPH = 0)

29.8.3.2 SPI Interface Timing - Full Duplex Mode (TCLKPH = 1, RCLKPH = 0)

In this mode, the master requires an initial SPCLK edge before data is available. The data from slave is available immediately when the slave device is selected. The.data is sampled on the first and following odd edges by the master. The data is sampled on the second and following even SPCLK edges by the slave.

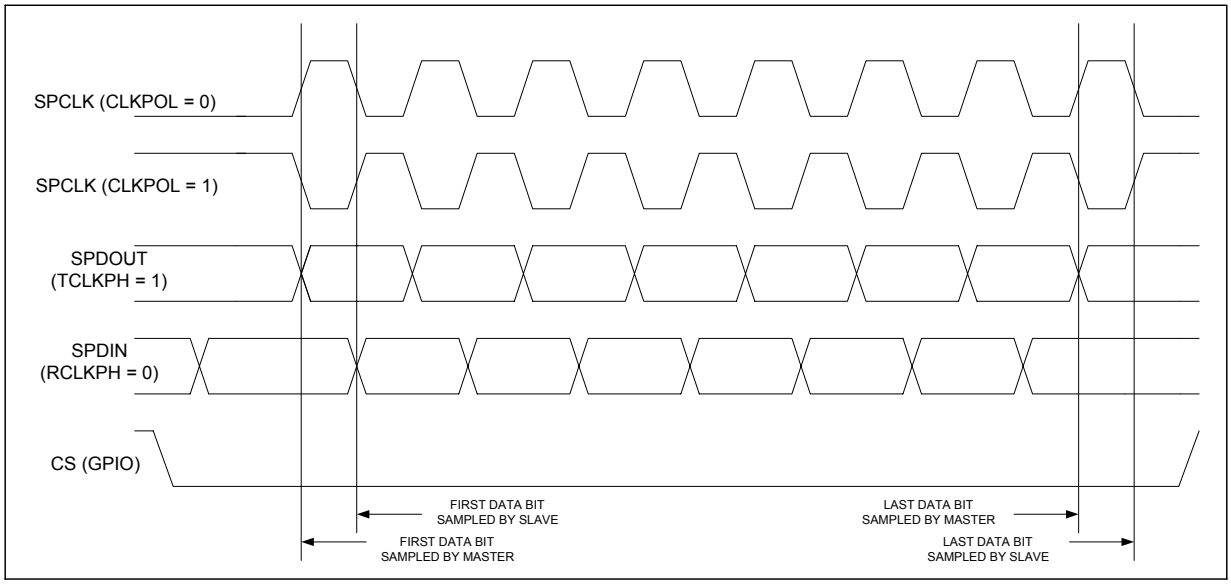


Figure 29.20 SPI Interface Timing, Full Duplex Mode (TCLKPH = 1, RCLKPH = 0)

29.8.3.3 SPI Interface Timing - Full Duplex Mode (TCLKPH = 0, RCLKPH = 1)

In this mode, the data from slave is available immediately when the slave device is selected. The slave device requires an initial SPCLK edge before data is available. The data is sampled on the second and following even SPCLK edges by the master. The data is sampled on the first and following odd edges by the slave.

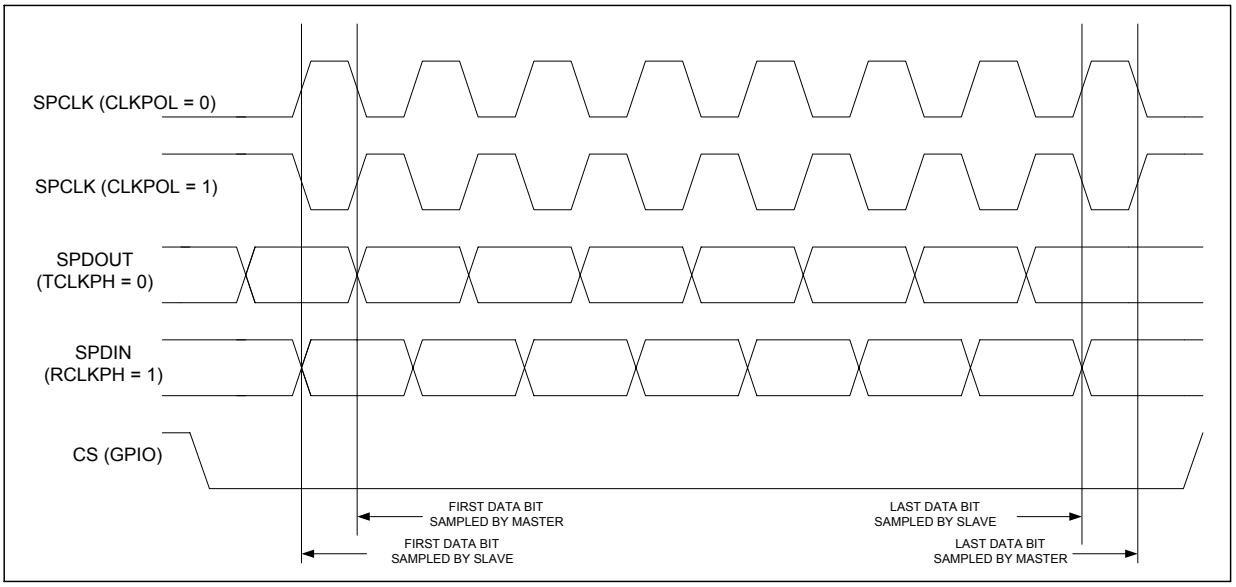


Figure 29.21 SPI Interface Timing, Full Duplex Mode (TCLKPH = 0, RCLKPH = 1)

29.8.3.4 SPI Interface Timing - Full Duplex Mode (TCLKPH = 1, RCLKPH = 1)

In this mode, the master and slave require an initial SPCLK edge before data is available. Data is sampled on the second and following even SPCLK edges by the master and slave.

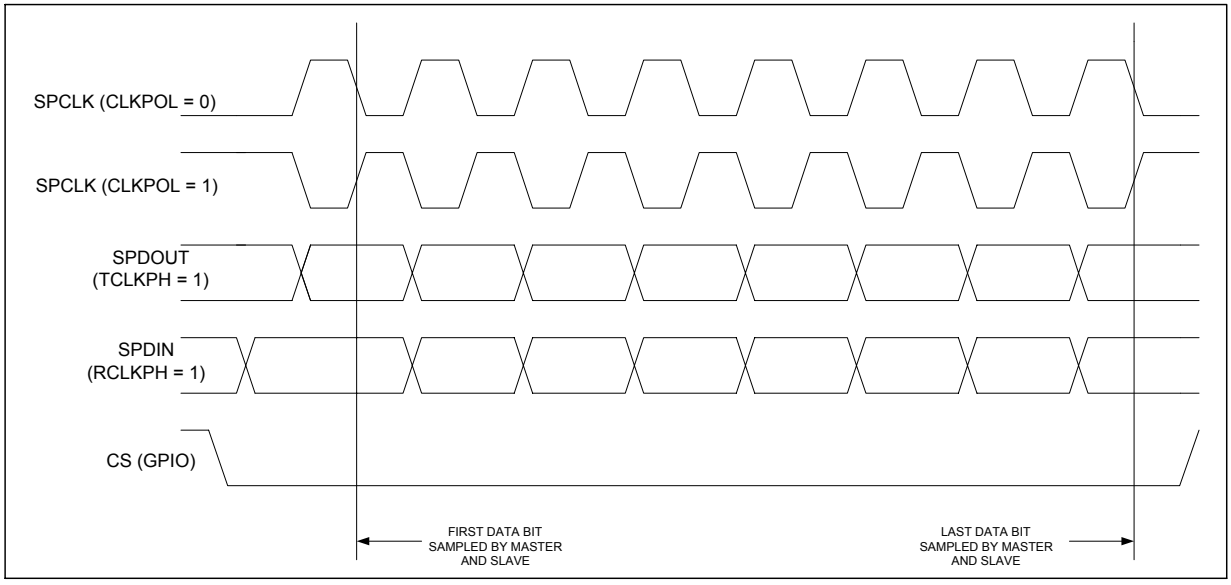


Figure 29.22 SPI Interface Timing - Full Duplex Mode (TCLKPH = 1, RCLKPH = 1)

Chapter 30 Package Outline Data

30.1 128-Pin QFP Package Outline, 14X20X2.7 Body, 3.9mm Footprint

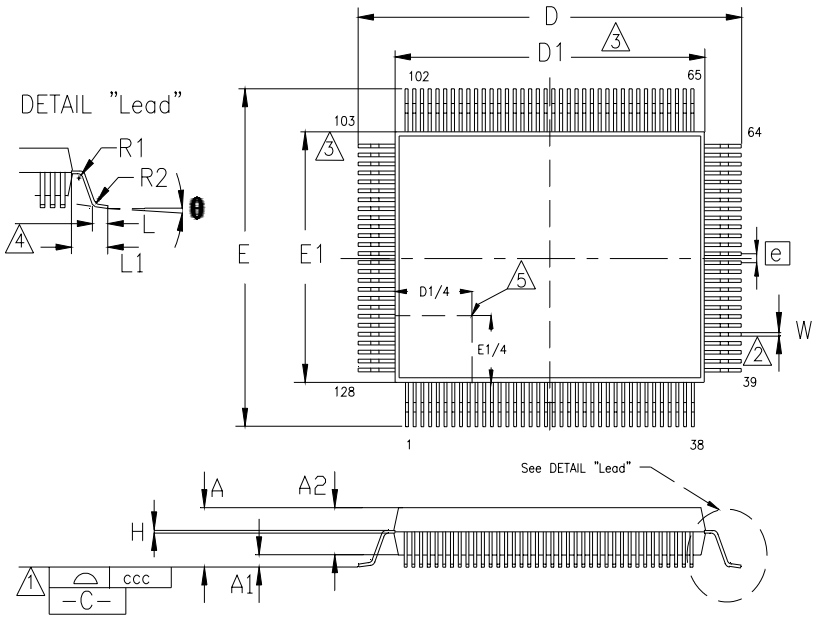


Figure 30.1 128-Pin QFP Package Outline

Table 30.1 128-Pin QFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.55	~	3.05	Body Thickness
D	23.70	~	24.10	X Span
D1	19.90	~	20.10	X Body Size
E	17.70	~	18.10	Y Span
E1	13.90	~	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.95	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0^o	~	7^o	Lead Foot Angle

Table 30.1 128-Pin QFP Package Parameters (continued)

	MIN	NOMINAL	MAX	REMARK
W	0.10	0.22	0.30	Lead Width
R1	0.13	~	~	Lead Shoulder Radius
R2	0.13	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter
2. Tolerance on the true position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

30.2 128-Pin VTQFP Package Outline, 14X14X1.0 Body, 2mm Footprint

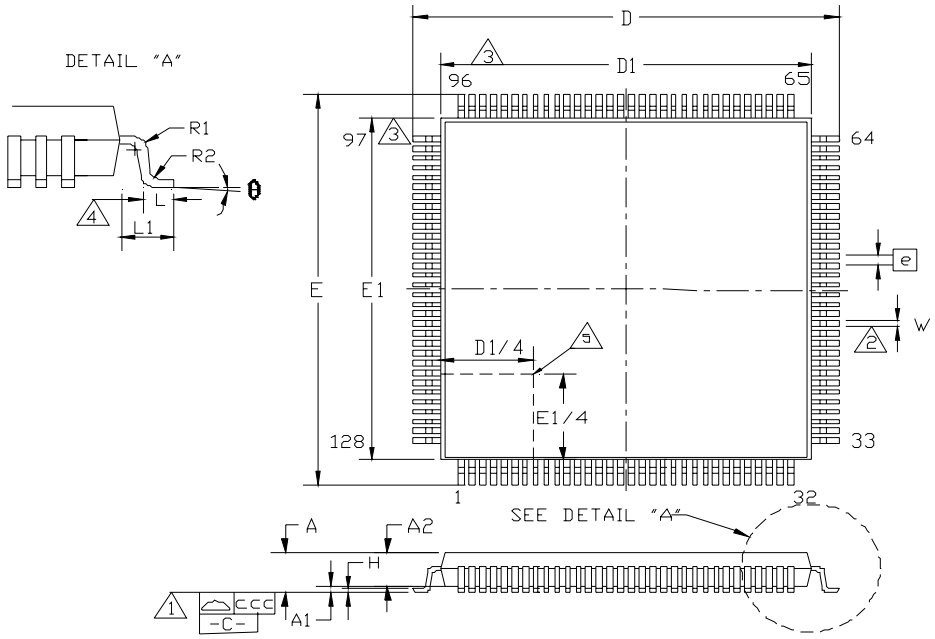


Figure 30.2 128-Pin VTQFP Package Outline

Table 30.2 128-Pin VTQFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.20	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	~	1.05	Body Thickness
D	15.80	~	16.20	X Span
D1	13.80	~	14.20	X Body Size
E	15.80	~	16.20	Y Span
E1	13.80	~	14.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.40 Basic			Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width

Table 30.2 128-Pin VTQFP Package Parameters (continued)

	MIN	NOMINAL	MAX	REMARK
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter
2. Tolerance on the true position of the leads is ± 0.035 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

Appendix A High-Performance 8051 Cycle Timing and Instruction Set

The high-performance 8051 processor offers increased performance by executing instructions in a 4-clock cycle, as opposed to the standard 8051. The shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectures.

Some instructions require a different number of instruction cycles on the high-performance 8051than they do on the standard 8051. In the standard 8051, all instructions except for MUL and DIV take one or two instruction cycles to complete. In the high-performance 8051 architecture, instructions can take between one and five instructions to complete. The average speed improvement for the entire instruction set is approximately 2.5X.

Table A.1 Legend for Instruction Set Table

SYMBOL	FUNCTION
A	Accumulator
Rn	Register R7-R0
direct	Internal register address
@Ri	Internal register pointed to by R0 or R1 (except MOVX)
rel	Two's complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

Table A.2 8051 Instruction Set

INSTRUCTION	DESCRIPTION	BYTE COUNT	INSTRUCTION CYCLES	HEX CODE
ARITHMETIC				
ADD A, Rn	Add register to A	1	1	28-2F
ADD A, direct	Add direct byte to A	2	2	25
ADD A, @Ri	Add data memory to A	1	1	26-27
ADD A, #data	Add immediate to A	2	2	24
ADDC A, Rn	Add register to A with carry	1	1	38-3F
ADDC A, direct	Add direct byte to A with carry	2	2	35
ADDC A, @Ri	Add data memory to A with carry	1	1	36-37
ADDC A, #data	Add immediate to A with carry	2	2	34

Table A.2 8051 Instruction Set (continued)

INSTRUCTION	DESCRIPTION	BYTE COUNT	INSTRUCTION CYCLES	HEX CODE
SUBB A, Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A, direct	Subtract direct byte from A with borrow	2	2	95
SUBB A, @Ri	Subtract data memory from A with borrow	1	1	96-97
SUBB A, #data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	1	04
INC Rn	Increment register			08-0F
INC direct	Increment direct byte	2	2	05
INC @Ri	Increment data memory	1	1	06-07
DEC A	Decrement A			14
DEC Rn	Decrement register		1	18-1F
DEC direct	Decrement direct byte	2	2	15
DEC @Ri	Decrement data memory	1	1	16-17
INC DPTR	Increment data pointer		3	A3
MUL AB	Multiply A by B		5	A4
DIV AB	Divide A by B		5	84
DA A	Decimal adjust A		1	D4
LOGICAL				
ANL A, Rn	AND register to A	1	1	58-5F
ANL A, direct	AND direct byte to A	2	2	55
ANL A, @Ri	AND data memory to A	1	1	56-57
ANL A, #data	AND immediate to A	2	2	54
ANL direct, A	AND A to direct byte			52
ANL direct, #data	AND immediate data to direct byte	3	3	53
ORL A, Rn	OR register to A	1	1	48-4F
ORL A, direct	OR direct byte to A	2	2	45
ORL A, @Ri	OR data memory to A	1	1	46-47
ORL A, #data	OR immediate to A	2	2	44
ORL direct, A	OR A to direct byte			42
ORL direct, #data	OR immediate data to direct byte	3	3	43
XORL A, Rn	Exclusive-OR register to A	1	1	68-6F

Table A.2 8051 Instruction Set (continued)

INSTRUCTION	DESCRIPTION	BYTE COUNT	INSTRUCTION CYCLES	HEX CODE
XORL A, direct	Exclusive-OR direct byte to A	2	2	65
XORL A, @Ri	Exclusive-OR data memory to A	1	1	66-67
XORL A, #data	Exclusive-OR immediate to A	2	2	64
XORL direct, A	Exclusive-OR A to direct byte	3	3	63
XORL direct, #data	Exclusive-OR immediate to direct byte	3	3	63
CLR A	Clear A	1	1	E4
CPL A	Complement A			F4
RL A	Rotate A left			23
RLC A	Rotate A left through carry			33
RR A	Rotate A right			03
RRC A	Rotate A right through carry			13
DATA TRANSFER				
MOV A, RN	Move register to A	1	1	E8-EF
MOV A, direct	Move direct byte to A	2	2	E5
MOV A, @Ri	Move data memory to A	1	1	E6-E7
MOV A, #data	Move immediate to A	2	2	74
MOV Rn, A	Move A to register	1	1	F8-FF
MOV Rn, direct	Move direct byte to register	2	2	A8-AF
MOV Rn, #data	Move immediate to register			78-7F
MOV direct, A	Move A to direct byte			F5
MOV direct, Rn	Move register to direct byte			88-8F
MOV direct, direct	Move direct byte to direct byte	3	3	85
MOV direct, @Ri	Move data memory to direct byte	2	2	86-87
MOV direct, #data	Move immediate to direct byte	3	3	75
MOV @Ri, A	Move A to data memory	1	1	F6-F7
MOV @Ri, direct	Move direct byte to data memory	2	2	A6-A7
MOV @Ri, #data	Move immediate to data memory			76-77
MOV DPTR, #data	Move immediate to data pointer	3	3	90
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1		93
MOVC A, @A+PC	Move code byte relative PC to A			83
MOVX A, @Ri	Move external data (A8) to A		2-9	E2-E3

Table A.2 8051 Instruction Set (continued)

INSTRUCTION	DESCRIPTION	BYTE COUNT	INSTRUCTION CYCLES	HEX CODE
MOVX A, @DPTR	Move external data (A16) to A	1	2-9	E0
MOVX @Ri, A	Move A to external data (A8)			F2-F3
MOVX @DPTR, A	Move A to external data (A16)			F0
PUSH direct	Push direct byte onto stack	2	2	C0
POP direct	Pop direct byte from stack			D0
XCH A, Rn	Exchange A and register	1	1	C8-CF
XCH A, direct	Exchange A and direct byte	2	2	C5
XCH A, @Ri	Exchange A and data memory	1	1	C6-C7
XCHD A, @Ri	Exchange A and data memory nibble			D6-D7
BOOLEAN				
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set Carry	1	1	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	2	B2
ANL C, bit	AND direct bit to carry			82
ANL C, /bit	AND direct bit inverse to carry			B0
ORL C, bit	OR direct bit to carry			72
ORL C, /bit	OR direct bit inverse to carry			A0
MOV C, bit	Move direct bit to carry			A2
MOV bit, C	Move carry to direct bit			92
BRANCHING				
ACALL addr 11	Absolute call to subroutine	2	3	11-F1
LCALL addr 16	Long call to subroutine	3	4	12
RET	Return from subroutine	1		22
RETI	Return from interrupt			32
AJMP addr 11	Absolute jump unconditional	2	3	01-E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	3	80
JC rel	Jump on carry = 1			40

Table A.2 8051 Instruction Set (continued)

INSTRUCTION	DESCRIPTION	BYTE COUNT	INSTRUCTION CYCLES	HEX CODE
JNC rel	Jump on carry = 0	2	3	50
JB bit, rel	Jump on direct bit = 1	3	4	20
JNB bit, rel	Jump on direct bit = 0			30
JMP @A+DPTR	Jump indirect relative DPTR	1	3	73
JZ rel	Jump on accumulator = 0	2		60
JNZ rel	Jump on accumulator /= 0			70
CJNE A, direct, rel	Compare A, direct JNE relative	3	4	B5
CJNE A, #d, rel	Compare A, immediate JNE relative			B4
CJNE Rn, #d, rel	Compare reg, immediate JNE relative			B8-BF
CJNE @Ri, #d, rel	Compare Ind, immediate JNE relative			B6-B7
DJNZ Rn, rel	Decrement register, JNZ relative	2	3	D8-DF
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	4	D5
MISCELLANEOUS				
NOP	No operation	1	1	00

Appendix B High-Performance 8051 Extended Interrupt Unit

B.1 Interrupts

The EXIF, EICON, EIE, and EIP registers provide flags, enable control, and priority control for the extended interrupt unit in the LPC47N350 high-performance 8051.

B.1.1 Interrupt Processing

When an enabled interrupt occurs, the CPU vectors to the address of the interrupt service routine (ISR) associated with that interrupt (See Table 7.15 on page 66). The CPU executes the ISR to completion unless another interrupt of higher priority occurs. Each ISR ends with a RETI (return from interrupt) instruction. After executing the RETI, the CPU returns to the next instruction that would have been executed if the interrupt had not occurred.

An ISR can only be interrupted by a higher priority interrupt. That is, an ISR for a low-level interrupt can only be interrupted by high-level interrupt. An ISR for a high-level interrupt can only be interrupted by the power-fail interrupt (extended interrupt unit only).

The 8051 always completes the instruction in progress before servicing an interrupt. If the instruction in progress is RETI, or a write access to any of the IP, IE, EIP, or EIE SFRs, the 8051 completes one additional instruction before servicing the interrupt.

B.1.2 Interrupt Masking

The EA bit in the IE SFR (IE.7) is a global enable for all interrupts except the power-fail interrupt. When EA = 1, each interrupt is enabled/masked by its individual enable bit. When EA = 0, all interrupts are masked. The only exception is the power-fail interrupt, which is not affected by the EA bit. When EPFI = 1, the power-fail interrupt is enabled, regardless of the state of the EA bit. Table 7.15 on page 66 provides a summary of interrupt sources, flags, enables, and priorities.

B.1.3 Interrupt Priorities

There are two stages of interrupt priority assignment, interrupt level and natural priority. The interrupt level (highest, high, or low) takes precedence over natural priority. The power-fail interrupt, if enabled, always has highest priority and is the only interrupt that can have highest priority. All other interrupts can be assigned either high or low priority.

In addition to an assigned priority level (high or low), each interrupt also has a natural priority, as listed in Table 7.15 on page 66. Simultaneous interrupts with the same priority level (for example, both high) are resolved according to their natural priority. For example, if int0_n and int2 are both programmed as high priority, int0_n takes precedence.

Once an interrupt is being serviced, only an interrupt of higher priority level can interrupt the service routine of the interrupt currently being serviced.

B.1.4 Interrupt Sampling

The internal timers and serial ports generate interrupts by setting their respective SFR interrupt flag bits. External interrupts are sampled once per instruction cycle.

int0_n and int1_n are both active low and can be programmed to be either edge-sensitive or level-sensitive, through the IT0 and IT1 bits in the TCON SFR. For example, when IT0 = 0, int0_n is level-sensitive and the 8051 sets the IE0 flag when the int0_n pin is sampled low. When IT0 = 1, int0_n is edge-sensitive and 8051 sets the IE0 flag when the int0_n pin is sampled high then low on consecutive samples.

The remaining four external interrupts are edge-sensitive only. int2 and int4 are active high, int3_n and int5_n are active low. The power-fail (pfi) interrupt is edge-sensitive, active high, and sampled once per instruction cycle. To ensure that edge-sensitive interrupts are detected, the corresponding ports should be held high for 4 clk cycles and then low for 4 clk cycles. Level-sensitive interrupts are not latched and must remain active until serviced.

B.1.5 Interrupt Latency

Interrupt response time depends on the current state of the 8051. The fastest response time is 5 instruction cycles: 1 to detect the interrupt, and 4 to perform the LCALL to the ISR. The maximum latency (13 instruction cycles) occurs when the 8051 is currently executing a RETI instruction followed by a MUL or DIV instruction. The 13 instruction cycles in this case are: 1 to detect the interrupt, 3 to complete the RETI, 5 to execute the DIV or MUL, and 4 to execute the LCALL to the ISR. For the maximum latency case, the response time is 13 x 4 = 52 clk cycles.

B.1.6 Dual Data Pointers

The high-performance 8051 in the LPC47N350 employs dual data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit value used to address external RAM or peripherals. The LPC47N350 maintains the standard data pointer as DPTR0 at SFR locations 82h and 83h. It is not necessary to modify code to use DPTR0.

The LPC47N350 adds a second data pointer (DPTR1) at SFR locations 84h and 85h. The SEL bit in the DPTR Select Register, DPS (SFR 86h), selects the active pointer (see Section B.3.1, "DPL1", Section B.3.2, "DPH1" and Section B.3.3, "DPS").

All DPTR-related instructions use the currently selected data pointer. To switch the active pointer, toggle the SEL bit. The fastest way to do so is to use the increment instruction (INC DPS). This requires only one instruction to switch from a source address to a destination address, saving application code from having to save source and destination addresses when doing a block move.

B.2 Timer 2

B.2.1 Overview

The high-performance 8051 in the LPC47N350 includes a third timer/counter (Timer 2). Timer 2 runs only in 16-bit mode and offers several capabilities not available with Timers 0 and 1. The modes available with Timer 2 are 16-bit auto-reload timer/counter and baud rate generator. The SFRs associated with Timer 2 are:

T2CON (SFR C8h)

RCAP2L (SFR CAh) – Used as the 16-bit LSB reload value when Timer 2 is configured for auto-reload mode.

RCAP2H (SFR CBh) – Used as the 16-bit MSB reload value when Timer 2 is configured for auto-reload mode.

TL2 (SFR CCh) – Lower 8 bits **Table 332**-bit count.

TH2 (SFR CDh) – Upper 8 bits of 16-bit count.

Table B.1 summarizes how the T2CON SFR bits (Table B.11) determine the Timer 2 operating mode.

Table B.1 Timer 2 Mode Control Summary

RCLK	TCLK	TR2	MODE
0	0	1	16-bit Timer/Counter w/Auto-reload
1	X		Baud Rate Generator

Table B.1 Timer 2 Mode Control Summary (continued)

RCLK	TCLK	TR2	MODE
X	1	1	Baud Rate Generator
	X	0	Off

B.2.2 16-Bit Timer/Counter Mode with Auto-Reload

Figure B.1 illustrates how Timer 2 operates in timer/counter mode with auto-reload. The 16-bit timer counts CLK cycles (divided by 4 or 12). The TR2 bit enables the counter. When the count increments from FFFFh, the overflow occurs. The overflow causes the TF2 flag is set, and t2_out goes high for one CLK cycle. The overflow also causes the preloaded start value in the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers.

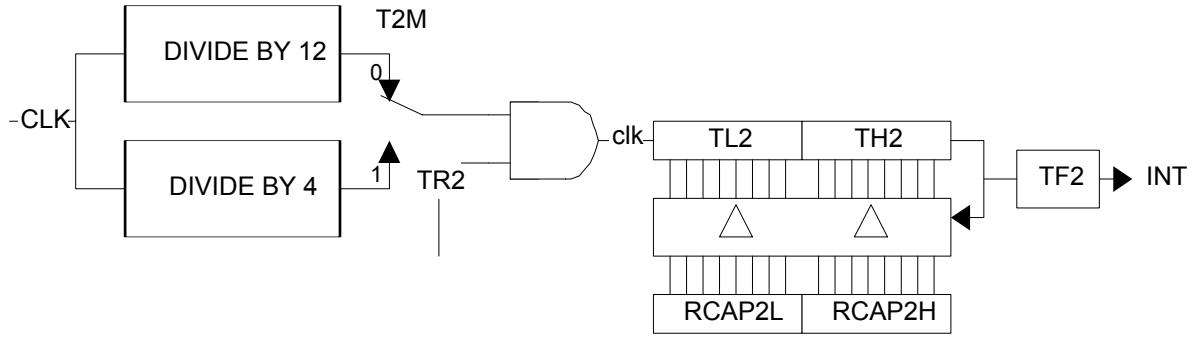


Figure B.1 Timer 2 Timer/Counter with Auto-Reload

B.2.3 Baud Rate Generator Mode

Setting either RCLK or TCLK to 1 configures Timer 2 to generate baud rates for Serial Port 0 in serial mode 1 or 3. In baud rate generator mode, Timer 2 functions in auto-reload mode. However, instead of setting the TF2 flag, the counter overflow is used to generate a shift clock for the serial port function. As in normal auto-reload mode, the overflow also causes the preloaded start value in the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers.

When either TCLK = 1 or RCLK = 1, Timer 2 is forced into auto-reload operation. The counter time base in baud rate generator mode is clk/2.

B.3 Special Function Registers

The following SFRs are not part of the standard 8051 architecture.

B.3.1 DPL1

The DPL1 register (Table B.2) is the LSB of DPTR1.

Table B.2 DPL1 Register - SFR 84H

SFR ADDRESS	N/A
POWER	0x 7F38
DEFAULT	VCC1

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	A7	A6	A5	A4	A3	A2	A1	A0

B.3.2 DPH1

The DPH1 register (Table B.3) is the MSB of DPTR1

Table B.3 DPH1 Register - SFR 85H

SFR ADDRESS	85h
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	A15	A14	A13	A12	A11	A10	A9	A8

B.3.3 DPS

The DPS register (Table B.4) is used to select the active DPTR

Table B.4 DPS Register - SFR 86h

SFR ADDRESS	86h
POWER	VCC1
DEFAULT	0x00

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TYPE	R		R	R	R	R	R	R
BIT NAME	RESERVED							SEL (Note B.1

Note B.1 When SEL = ‘0’, instructions that use the DPTR will use DPL0 and DPH0. When SEL = ‘1’, instructions that use the DPTR will use DPL1 and DPH1.

B.3.4 CKCON

The default timer clock scheme for the DW8051 timers is 12 clk cycles per increment, the same as in the standard 8051. However, in the DW8051, the instruction cycle is 4 clk cycles. Using the default rate (12 clocks per timer increment) allows existing application code with real-time dependencies, such as baud rate, to operate properly. However, applications that require fast timing can set the timers to increment every 4 clk cycles by setting bits in the Clock Control register (CKCON) at SFR location 8Eh (Table B.5 and Table B.6)

The CKCON bits that control the timer clock rates are:

CKCON BIT	COUNTER/TIMER
5	Timer 2
4	Timer 1
3	Timer 0

When a CKCON register bit is set to 1, the associated counter increments at 4-clk intervals. When a CKCON bit is cleared, the associated counter increments at 12-clk intervals. The timer controls are independent of each other. The default setting for all three timers is 0 (12-clk intervals). These bits have no effect in counter mode.

Table B.5 CKCON Register - SFR 8EH

SFR ADDRESS	8EH
POWER	VCC1
DEFAULT	0x01

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TYPE	R	R	R	R/W	R/W	R/W	R/W	R/W
BIT NAME	Reserved		T2M	T1M	T0M	MD2	MD1	MD0

Table B.6 CKCON Register Bit Descriptions

BIT	FUNCTION
CKCON.7-6	Reserved
CKCON.5	T2M. Timer 2 clock select. When T2M = 0, Timer 2 uses clk/12 (for compatibility with 80C32); when T2M = 1, Timer 2 uses clk/4. This bit has no effect when Timer 2 is configured for baud rate generation.
CKCON.4	T1M. Timer 1 clock select. When T1M = 0, Timer 1 uses clk/12 (for compatibility with 80C32); when T1M = 1, Timer 1 uses clk/4.
CKCON.3	T0M. Timer 0 clock select. When T0M = 0, Timer 0 uses clk/12 (for compatibility with 80C32); when T0M = 1, Timer 0 uses clk/4.
CKCON.2-0	MD2, MD1, MD0 -- Control the number of cycles to be used for external MOVX instructions.

B.3.5 SPC_FNC

Table B.7 SPC_FNC Register - SFR 8FH

SFR ADDRESS	8FH
POWER	VCC1
DEFAULT	0x00

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TYPE	R	R	R	R	R	R	R	R/W
BIT NAME	Reserved							WRS

Table B.8 CKCON Register Bit Descriptions

BIT	FUNCTION
SPC_FNC.7-1	Reserved
SPC_FNC.0	WRS. Select RAM write strobe 0 = mem_wr_n 1 = mem_pswr_n This bit allows writes to 8051 code space using the alternate write strobe mem_pswr_n.

B.3.6 MPAGE

The MPAGE special function register (Table B.9) replaces the function of the Port 2 latch in the LPC47N350. During MOVX A, @Ri and MOVX @Ri, A instructions, the 8051 places the contents of the MPAGE register on the upper eight address bits. This provides the paging function that is normally provided by the Port 2 latch.

Table B.9 MPAGE Register - SFR 92H

SFR ADDRESS	92H
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	A15	A14	A13	A12	A11	A10	A9	A8

B.3.7 T2CON

The T2CON register is used to configure Timer 2

Table B.10 T2CON Register - SFR C8H

SFR ADDRESS	C8h
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	TF2	Reserved	RCLK	TCLK	Reserved	TR2	Reserved	

Table B.11 T2CON Register Bit Descriptions

BIT	FUNCTION
T2CON.7	TF2 Timer 2 overflow flag. Hardware will set TF2 when the Timer 2 overflows from FFFFh. TF2 must be cleared to 0 by the software. TF2 will only be set to a 1 if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.
T2CON.6	Reserved. This bit should be written as '0'.
T2CON.5	RCLK Receive clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of received data in serial mode 1 or 3. RCLK =1 selects Timer 2 overflow as the receive clock. RCLK =0 selects Timer 1 overflow as the receive clock.
T2CON.4	TCLK Transmit clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of transmit data in serial mode 1 or 3. RCLK =1 selects Timer 2 overflow as the transmit clock. RCLK =0 selects Timer 1 overflow as the transmit clock.
T2CON.3	Reserved. This bit should be written as '0'.
T2CON.2	TR2. Timer 2 run control flag. TR2 = 1 starts Timer 2. TR2 = 0 stops Timer 2.
T2CON.1-0	Reserved. This bit should be written as '0'.

B.3.8 RCAP2L

The RCAP2L register is the 16-bit LSB reload value (RV[7:0]) when Timer 2 is configured for auto-reload mode.

Table B.12 RCAP2L Register - SFR CAH

SFR ADDRESS	CAh
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0

B.3.9 RCAP2H

The RCAP2H register is the 16-bit MSB reload value (RV[15:8]) when Timer 2 is configured for auto-reload mode.

Table B.13 RCAP2H Register - SFR CBH

SFR ADDRESS	CBh
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	RV15	RV14	RV13	RV12	RV11	RV10	RV9	RV8

B.3.10 TL2

The TL2 register (Table B.14) is the 16-bit LSB Timer 2 count value (CV[7:0]).

Table B.14 TL2 Register - SFR CCH

SFR ADDRESS	CCh
POWER	VCC1
DEFAULT	0x00

BIT	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	CV7	CV6	CV5	CV4	CV3	CV2	CV1	CV0

B.3.11 TH2

The TH2 register (Table B.15) is the 16-bit MSB Timer 2 count value (CV[15:8]).

Table B.15 TH2 Register - SFR CDH

SFR ADDRESS	CDh
POWER	VCC1
DEFAULT	0x00

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	CV15	CV14	CV13	CV12	CV11	CV10	CV9	CV8

B.3.12 EXIF

The EXIF register contains the external interrupt flags for the extended interrupt unit.

Table B.16 EXIF Register - SFR 91H

SFR ADDRESS	91h
POWER	VCC1
DEFAULT	0x08

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	IE5	IE4	IE3	IE2	Reserved			

Table B.17 EXIF Register Bit Descriptions

BIT	FUNCTION
EXIF.7	IE5 External Interrupt 5 flag. IE5 = 1 indicates a falling edge was detected at the int5_n pin. IE5 must be cleared by software. Setting IE5 in software generates an interrupt, if enabled.
EXIF.6	IE4 External Interrupt 4 flag. IE4 = 1 indicates a rising edge was detected at the int4 pin. IE4 must be cleared by software. Setting IE4 in software generates an interrupt, if enabled.
EXIF.5	IE3 External Interrupt 3 flag. IE3 = 1 indicates a falling edge was detected at the int3_n pin. IE3 must be cleared by software. Setting IE3 in software generates an interrupt, if enabled.
EXIF.4	IE2 External Interrupt 2 flag. IE2 = 1 indicates a rising edge was detected at the int2 pin. IE2 must be cleared by software. Setting IE2 in software generates an interrupt, if enabled.

Table B.17 EXIF Register Bit Descriptions (continued)

BIT	FUNCTION
EXIF.3	Reserved. Read as '1'.
EXIF.2-0	Reserved. Read as '0'.

B.3.13 EICON

The EICON register contains pfi and serial port 1 controls for the extended interrupt unit.

Table B.18 EICON Register - SFR D8H

SFR ADDRESS	D8h
POWER	VCC1
DEFAULT	0x40

BIT	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	SMOD1	Reserved	EPFI	PFI	Reserved			

Table B.19 EICON Register Bit Descriptions

BIT	FUNCTION
EICON.7	SMOD1 Serial Port 1 baud rate doubler enable. When SMOD1 = 1, the baud rate for Serial Port 1 is doubled.
EICON.6	Reserved. Read as '1'.
EICON.5	EPFI Enable power-fail interrupt. EPFI = 0 disables power-fail interrupt (pfi). EPFI = 1 enables interrupts generated by the pfi pin.
EICON.4	PFI Power-fail interrupt flag. PFI = 1 indicates a power-fail interrupt was detected at the pfi pin. PFI must be cleared by software before exiting the interrupt service routine. Otherwise, the interrupt occurs again. Setting PFI in software generates a power-fail interrupt, if enabled.
EICON.3-0	Reserved. Read as '0'.

B.3.14 EIE

The EIE register contains the external interrupt enables for the extended interrupt unit.

Table B.20 EIE Register - SFR E8H

SFR ADDRESS	E8h
POWER	VCC1
DEFAULT	0xE0

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved				EX5	EX4	EX3	EX2

Table B.21 EIE Register Bit Descriptions

BIT	FUNCTION
EIE.7-5	Reserved. Read as ‘1’.
EIE.4	Reserved. Read and Write as ‘0’.
EIE.3	EX5 Enable external interrupt 5. EX5 = 0 disables external interrupt 5 (int5_n). EX5 = 1 enables interrupts generated by the int5_n pin.
EIE.2	EX4 Enable external interrupt 4. EX4 = 0 disables external interrupt 4 (int4). EX4 = 1 enables interrupts generated by the int4 pin.
EIE.1	EX3 Enable external interrupt 3. EX3 = 0 disables external interrupt 3 (int3_n). EX3 = 1 enables interrupts generated by the int3_n pin.
EIE.0	EX2 Enable external interrupt 2. EX2 = 0 disables external interrupt 2 (int2). EX2 = 1 enables interrupts generated by the int2 pin.

B.3.15 EIP

The EIP register contains the external interrupt priority controls for the extended interrupt unit.

Table B.22 EIP Register - SFR F8H

SFR ADDRESS	F8h
POWER	VCC1
DEFAULT	0xE0

BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved				PX5	PX4	PX3	PX2

Table B.23 EIP Register Bit Descriptions

BIT	FUNCTION
EIP.7-5	Reserved. Read as ‘1’.
EIP.4	Reserved. Read and Write as ‘0’.
EIP.3	PX5 External interrupt 5 priority control. PX5 = 0 sets external interrupt 5 (int5_n) to low priority. PX5 = 1 sets external interrupt 5 to high priority.
EIP.2	PX4 External interrupt 4 priority control. PX4 = 0 sets external interrupt 4 (int4) to low priority. PX2 = 1 sets external interrupt 4 to high priority.
EIP.1	PX3 External interrupt 3 priority control. PX3 = 0 sets external interrupt 3 (int3_n) to low priority. PX3 = 1 sets external interrupt 3 to high priority.
EIP.0	PX2 External interrupt 2 priority control. PX2 = 0 sets external interrupt 2 (int2) to low priority. PX2 = 1 sets external interrupt 2 to high priority.