

LTC1346A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage	
V_{CC}	6.5V
V_{EE}	-6.5V
Input Voltage	
Transmitters	-0.3V to ($V_{CC} + 0.3V$)
Receivers	-18V to 18V
S0, S1, S2	-0.3V to ($V_{CC} + 0.3V$)
Output Voltage	
Transmitters	-18V to 18V
Receivers	-0.3V to ($V_{CC} + 0.3V$)
Short-Circuit Duration	
Transmitter Output	Indefinite
Receiver Output	Indefinite
Operating Temperature Range	
LTC1346AC	0°C to 70°C
LTC1346AI	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION





	ORDER PART NUMBER
	LTC1346ACSW LTC1346AISW

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V \pm 5\%$, $V_{EE} = -5V \pm 5\%$ (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V_{OD}	Transmitter Differential Output Voltage	$-4V \leq V_{OS} \leq 4V$ (Figure 1)	●	0.44	0.55	0.66	V
V_{OC}	Transmitter Common Mode Output Voltage	$V_{OS} = 0V$ (Figure 1)	●	-0.6	0	0.6	V
I_{OH}	Transmitter Output High Current	$V_{Y,Z} = 0V$	●	-12.6	-11	-9.4	mA
I_{OL}	Transmitter Output Low Current	$V_{Y,Z} = 0V$	●	9.4	11	12.6	mA
I_{OZ}	Transmitter Output Leakage Current	$-5V \leq V_{Y,Z} \leq 5V$, $S1 = S2 = 0V$	●		±1	±20 ±100	μA μA
R_O	Transmitter Output Impedance	$-2V \leq V_{Y,Z} \leq 2V$			100		kΩ
V_{TH}	Differential Receiver Input Threshold Voltage	$-7V \leq (V_A + V_B)/2 \leq 12V$	●		25	200	mV
ΔV_{TH}	Receiver Input Hysteresis	$-7V \leq (V_A + V_B)/2 \leq 12V$			50		mV
I_{IN}	Receiver Input Current (A, B)	$-7V \leq V_{A,B} \leq 12V$	●			0.7	mA
R_{IN}	Receiver Input Impedance	$-7V \leq V_{A,B} \leq 12V$	●	17.5	30		kΩ
V_{OH}	Receiver Output High Voltage	$I_O = 4mA$, $V_{A,B} = 0.2V$	●	3	4.5		V
V_{OL}	Receiver Output Low Voltage	$I_O = 4mA$, $V_{A,B} = -0.2V$	●		0.2	0.4	V
I_{OSR}	Receiver Output Short-Circuit Current	$0V \leq V_O \leq V_{CC}$	●	7	40	85	mA
I_{OZR}	Receiver Three-State Output Current	$S0 = V_{CC}$, $0V \leq V_O \leq V_{CC}$	●			±10	μA
V_{IH}	Logic Input High Voltage	T, S0, S1, S2	●	2			V
V_{IL}	Logic Input Low Voltage	T, S0, S1, S2	●			0.8	V
I_{IN}	Logic Input Current	T, S0, S1, S2	●			±10	μA

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V \pm 5\%$, $V_{EE} = -5V \pm 5\%$ (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	V_{CC} Supply Current	$V_{OS} = 0V$, $S0 = \text{Low}$, $S1 = S2 = \text{High}$ (Figure 1)	●	40	50	mA
		No Load, $S0 = \text{Low}$, $S1 = S2 = \text{High}$	●	6	9	mA
		Shutdown, $S0 = V_{CC}$, $S1 = S2 = 0V$	●	0.1	100	μA
I_{EE}	V_{EE} Supply Current	$V_{OS} = 0V$, $S0 = \text{Low}$, $S1 = S2 = \text{High}$ (Figure 1)	●	-40	-50	mA
		No Load, $S0 = \text{Low}$, $S1 = S2 = \text{High}$	●	-6	-9	mA
		Shutdown, $S0 = V_{CC}$, $S1 = S2 = 0V$	●	-0.1	-100	μA
t_r, t_f	Transmitter Rise or Fall Time	$V_{OS} = 0V$ (Figures 1, 3)	●	7	40	ns
t_{PLH}	Transmitter Input to Output 	$V_{OS} = 0V$ (Figures 1, 3)	●	25	70	ns
t_{PHL}	Transmitter Input to Output 	$V_{OS} = 0V$ (Figures 1, 3)	●	30	70	ns
t_{SKEW}	Transmitter Output to Output	$V_{OS} = 0V$ (Figures 1, 3)		5		ns
t_{PLH}	Receiver Input to Output 	$V_{OS} = 0V$ (Figures 1, 4)	●	50	100	ns
t_{PHL}	Receiver Input to Output 	$V_{OS} = 0V$ (Figures 1, 4)	●	55	100	ns
t_{SKEW}	Differential Receiver Skew, $ t_{PLH} - t_{PHL} $	$V_{OS} = 0V$ (Figures 1, 4)		5		ns
t_{ZL}	Receiver Enable to Output Low (Active Mode)	$C_L = 15pF$, SW1 Closed (Figures 2, 5)	●	40	70	ns
	Receiver Enable to Output Low (from Shutdown, Note 3)	$C_L = 15pF$, SW1 Closed (Figures 2, 5)		2		μs
t_{ZH}	Receiver Enable to Output High (Active Mode)	$C_L = 15pF$, SW2 Closed (Figures 2, 5)	●	35	70	ns
	Receiver Enable to Output High (from Shutdown, Note 3)	$C_L = 15pF$, SW2 Closed (Figures 2, 5)		2		μs
t_{LZ}	Receiver Disable from Low	$C_L = 15pF$, SW1 Closed (Figures 2, 5)	●	30	70	ns
t_{HZ}	Receiver Disable from High	$C_L = 15pF$, SW2 Closed (Figures 2, 5)	●	35	70	ns

The ● denotes specifications which apply over the full operating temperature range.

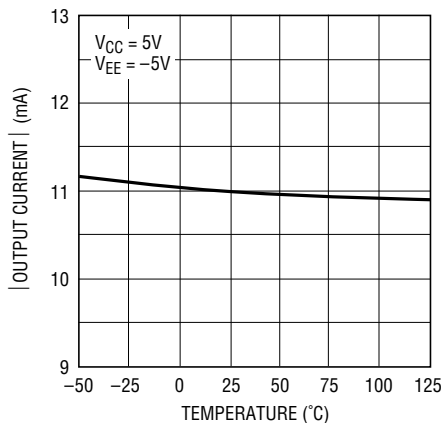
Note 1: The Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are termed negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: Receiver enable to output valid high or low from shutdown is typically 2 μs .

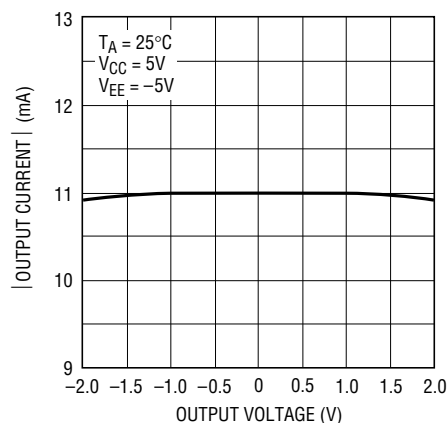
TYPICAL PERFORMANCE CHARACTERISTICS

Transmitter Output Current vs Temperature



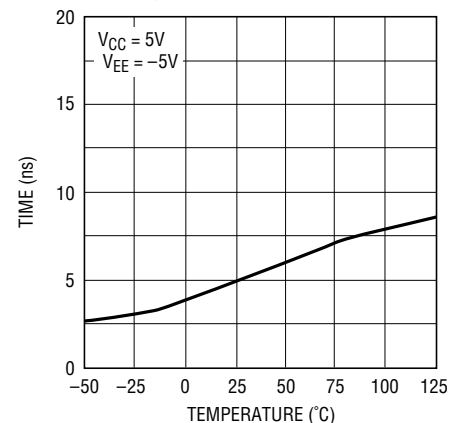
1346A G01

Transmitter Output Current vs Output Voltage



1346A G02

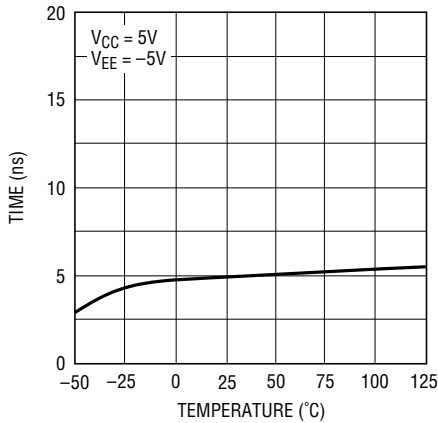
Transmitter Output Skew vs Temperature



1346A G03

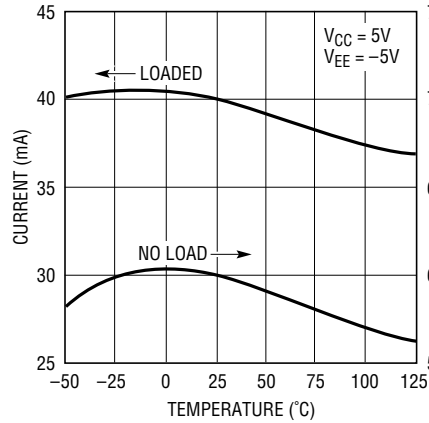
TYPICAL PERFORMANCE CHARACTERISTICS

Receiver $t_{PLH} - t_{PHL}$ vs Temperature



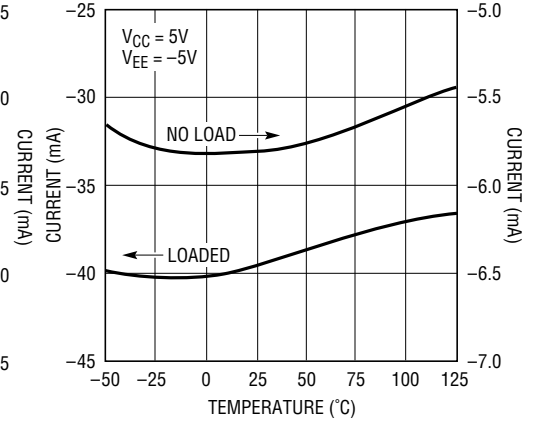
1346A G04

I_{CC} Supply Current vs Temperature



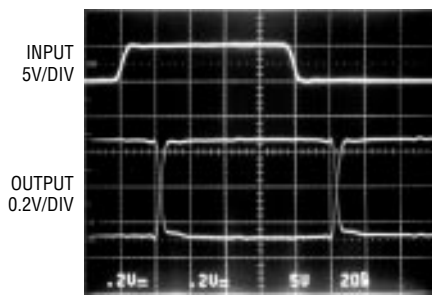
1346A G05

I_{EE} Supply Current vs Temperature



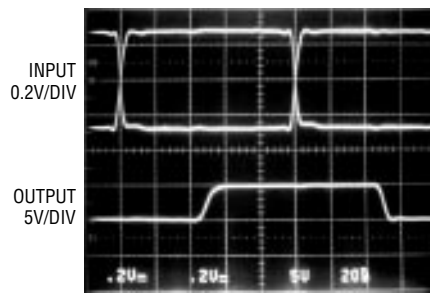
1346A G06

Transmitter Output Waveforms



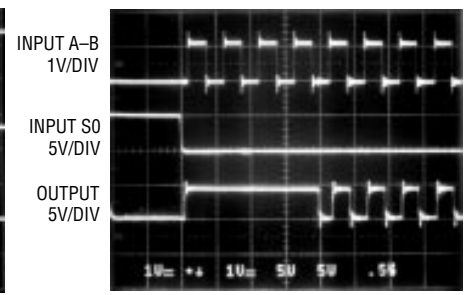
1346A G07

Receiver Output Waveforms



1346A G08

Receiver Enable from Shutdown



1346A G09

PIN FUNCTIONS

V_{EE} (Pin 1): Negative Supply, $-4.75V \geq V_{EE} \geq -5.25V$

V_{CC} (Pin 2): Positive Supply, $4.75V \leq V_{CC} \leq 5.25V$

GND (Pin 3): Ground

T1 (Pin 4): Transmitter 1 Input, TTL Compatible

T2 (Pin 5): Transmitter 2 Input, TTL Compatible

T3 (Pin 6): Transmitter 3 Input, TTL Compatible

S1 (Pin 7): Select Input 1, TTL Compatible

S2 (Pin 8): Select Input 2, TTL Compatible

R3 (Pin 9): Receiver 3 Output, TTL Compatible

R2 (Pin 10): Receiver 2 Output, TTL Compatible

R1 (Pin 11): Receiver 1 Output, TTL Compatible

S0 (Pin 12): Select Input 0, TTL Compatible

B1 (Pin 13): Receiver 1 Inverting Input

A1 (Pin 14): Receiver 1 Noninverting Input

B2 (Pin 15): Receiver 2 Inverting Input

A2 (Pin 16): Receiver 2 Noninverting Input

B3 (Pin 17): Receiver 3 Inverting Input

A3 (Pin 18): Receiver 3 Noninverting Input

Z3 (Pin 19): Transmitter 3 Inverting Output

Y3 (Pin 20): Transmitter 3 Noninverting Output

Z2 (Pin 21): Transmitter 2 Inverting Output

Y2 (Pin 22): Transmitter 2 Noninverting Output

Z1 (Pin 23): Transmitter 1 Inverting Output

Y1 (Pin 24): Transmitter 1 Noninverting Output

FUNCTION TABLES

Transmitter and Receiver Configuration

S0	S1	S2	DX ON	RX ON	Description
0	0	0	—	1, 2, 3	All RX ON, All DX OFF
1	0	0	—	—	All OFF, Shutdown
0	1	0	1, 2, 3	1, 2	DCE Mode
1	1	0	1, 2, 3	—	DCE Mode, All RX OFF
0	0	1	1, 2	1, 2, 3	DTE Mode
1	0	1	1, 2	—	DTE Mode, All RX OFF
0	1	1	1, 2, 3	1, 2, 3	All ON
1	1	1	1, 2, 3	—	All DX ON, All RX OFF

Transmitter

CONFIGURATION	INPUTS				OUTPUTS			
	S0	S1	S2	T	Y1 AND Y2	Z1 AND Z2	Y3	Z3
All OFF	0	0	0	X	Z	Z	Z	Z
Shutdown	1	0	0	X	Z	Z	Z	Z
DCE or All ON	X	1	X	0	0	1	0	1
DCE or All ON	X	1	X	1	1	0	1	0
DTE	X	0	1	0	0	1	Z	Z
DTE	X	0	1	1	1	0	Z	Z

Receiver

CONFIGURATION	INPUTS				OUTPUTS	
	S0	S1	S2	A - B	R1 AND R2	R3
All Rx ON	0	0	0	$\leq -0.2V$	0	0
All Rx ON	0	0	0	$\geq 0.2V$	1	1
Shutdown	1	0	0	X	Z	Z
DCE	0	1	0	$\leq -0.2V$	0	Z
DCE	0	1	0	$\geq 0.2V$	1	Z
Disabled	1	1	0	X	Z	Z
DTE or All ON	0	X	1	$\leq -0.2V$	0	0
DTE or All ON	0	X	1	$\geq 0.2V$	1	1
Disabled	1	X	1	X	Z	Z

TEST CIRCUITS

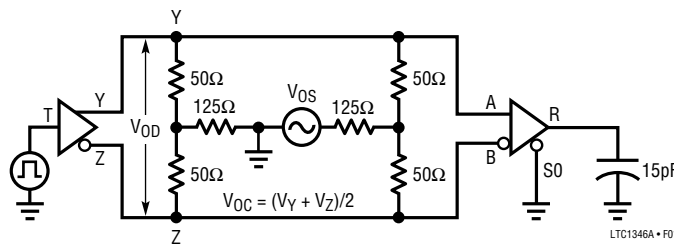


Figure 1. V.35 Transmitter/Receiver Test Circuit

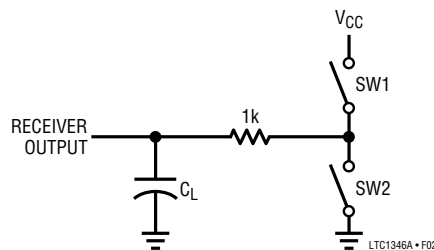


Figure 2. Receiver Output Enable and Disable Timing Test Load

APPLICATIONS INFORMATION

Review of CCITT Recommendation V.35 Electrical Specifications

V.35 is a CCITT recommendation for synchronous data transmission via modems. Appendix 2 of the recommendation describes the electrical specifications which are summarized below:

1. The interface cable is a balanced twisted pair with 80Ω to 120Ω impedance.
2. The transmitter's source impedance is between 50Ω and 150Ω .
3. The transmitter's resistance between shorted terminals and ground is $150\Omega \pm 15\Omega$.
4. When terminated by a 100Ω resistive load, the terminal-to-terminal voltage should be $0.55V \pm 20\%$.
5. The transmitter's rise time should be less than 1% of the signal pulse or $40ns$, whichever is greater.
6. The common mode voltage at the transmitter output should not exceed $0.6V$.
7. The receiver impedance is $100\Omega \pm 10\Omega$.
8. The receiver impedance to ground is $150\Omega \pm 15\Omega$.
9. The transmitter or receiver should not be damaged by connection to earth ground, short-circuiting or cross connection to other lines.

10. No data errors should occur with $\pm 2V$ common mode change at either the transmitter/receiver or $\pm 4V$ ground potential difference between transmitter and receiver.

Cable Termination

Each end of the cable connected to an LTC1346A must be terminated by an external Y- or Δ -resistor network for proper operation. The Y-termination has two series connected 50Ω resistors and a 125Ω resistor connected between ground and the center tap of the two 50Ω resistors as shown in Figure 6.

The alternative Δ -termination has a 120Ω resistor across the twisted wires and two 300Ω resistors between each wire and ground. Standard $1/8W$, 5% surface mount resistors can be used for the termination network. To maintain the proper differential output swing, the resistor tolerance must be 5% or better. A termination network that combines all the resistors into an SO-14 package is available from:

BI Technologies (Formerly Beckman Industrial)
Resistor Networks
4200 Bonita Place
Fullerton, CA 92635
Phone: (714) 447-2357
FAX: (714) 447-2500
Part #: BI Technologies 627T500/1250 (SOIC)
899TR50/125 (DIP)

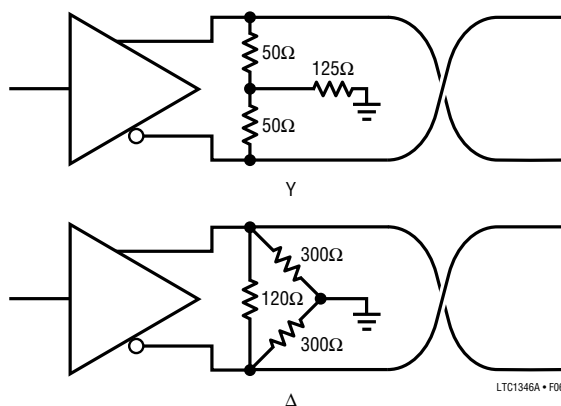


Figure 6. Y- and Δ -Termination Networks

APPLICATIONS INFORMATION

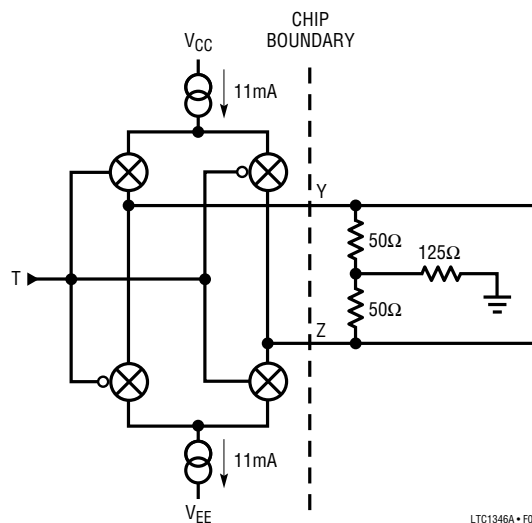


Figure 7. Simplified Transmitter Schematic

Theory of Operation

The transmitter outputs consist of complementary switched-current sources as shown in Figure 7.

With a logic zero at the transmitter input, the inverting output Z sources 11mA and the noninverting output Y sinks 11mA. The differential transmitter output voltage is then set by the termination resistors. With two differential 50Ω resistors at each end of the cable, the voltage is set to $(50\Omega)(11\text{mA}) = 0.55\text{V}$. With a logic 1 at the transmitter input, output Z sinks 11mA and Y sources 11mA. The common mode voltage of Y and Z is 0V when both current sources are matched and there is no ground potential difference between the cable terminations. The transmitter current sources have a common mode range of $\pm 2\text{V}$, which allows for a ground difference between cable terminations of $\pm 4\text{V}$.

Each receiver input has a 30k resistance to ground and requires external termination to meet the V.35 input impedance specification. The receivers have an input hysteresis of 50mV to improve noise immunity.

Three Select pins, S0, S1 and S2, configure the chip as described in Function Tables. When the transmitters and

receivers are OFF, all outputs are forced into high impedance. The S0 pin can be used as receiver output enable. In shutdown mode, I_{CC} drops to $1\mu\text{A}$ with all transmitters and receivers OFF. When the LTC1346A is enabled from shutdown the transmitters and receivers require $2\mu\text{s}$ to stabilize.

Complete V.35 Port

Figure 8 shows the schematic of a complete surface mounted, $\pm 5\text{V}$ DTE and DCE V.35 port using only three ICs and six capacitors per port. The LTC1346A is used to transmit the clock and data signals and the LT1134A to transmit the control signals. If test signals 140, 141 and 142 are not used, the transmitter inputs should be tied to V_{CC} .

RS422/RS485 Applications

The receivers on the LTC1346A can be used for RS422 and RS485 applications. Using the test circuit in Figure 9, the LTC1346A receivers are able to successfully extract the data stream from the common mode voltage, meeting RS422 and RS485 requirements as shown in Figures 10 and 11.

APPLICATIONS INFORMATION

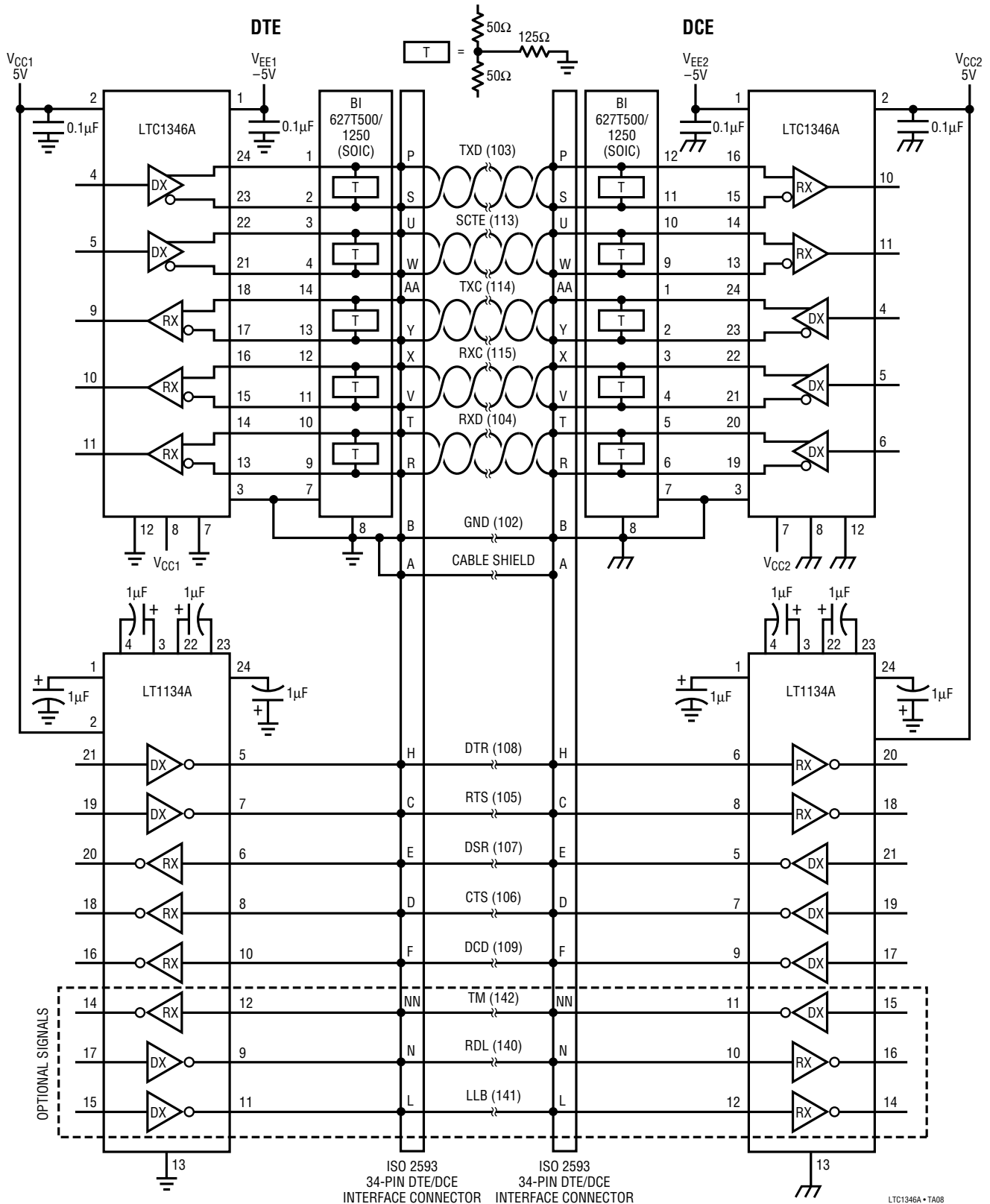


Figure 8. Complete Single $\pm 5V$ V.35 Interface

APPLICATIONS INFORMATION

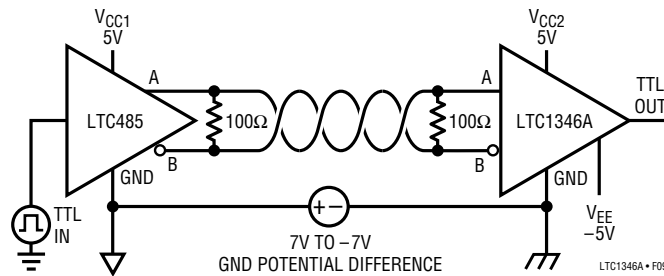


Figure 9. RS422/RS485 Receiver Interface

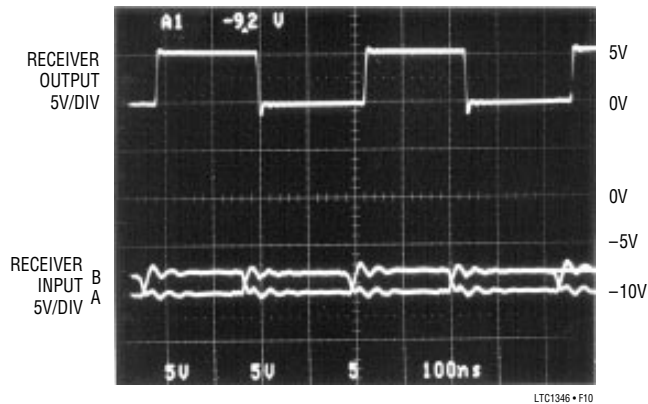


Figure 10. -7V Common Mode

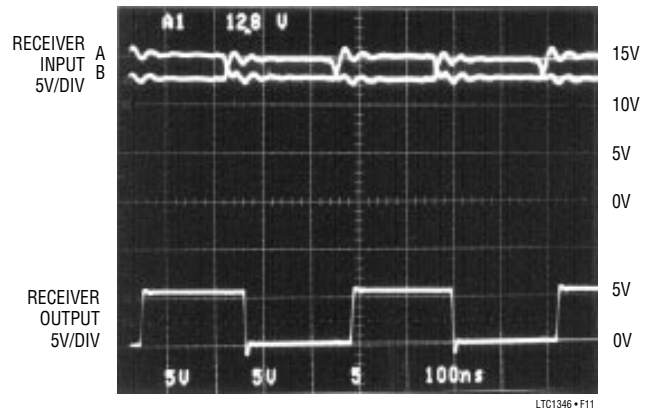


Figure 11. 12V Common Mode

Multiprotocol Application

The LTC1346A can be used in multiprotocol applications where V.35, RS232 and RS422 (used in RS530, RS449 among others) signals may appear at the same port. The LTC1346A switched current source driver is not compatible with RS232 or RS422. However, the outputs when disabled can share lines with RS232 drivers with a shutdown feature such as the LT1030 and RS422 drivers with a disable feature such as the LTC486/LTC487 (Figure 12a).

The LTC1346A driver will not be damaged or load the shared lines when disabled. The LTC1346A receiver can receive V.35, RS232 and RS422 signals as shown in Figure 12b. The LTC1346A receiver is directly compatible with V.35 and RS422. For RS232 signal, the noninverting input of the receiver should be grounded. Because the line termination for each of the protocols is different, some form of termination switching should be included, either the connector (as shown in Figures 12a and 12b) or on the PCB.

APPLICATIONS INFORMATION

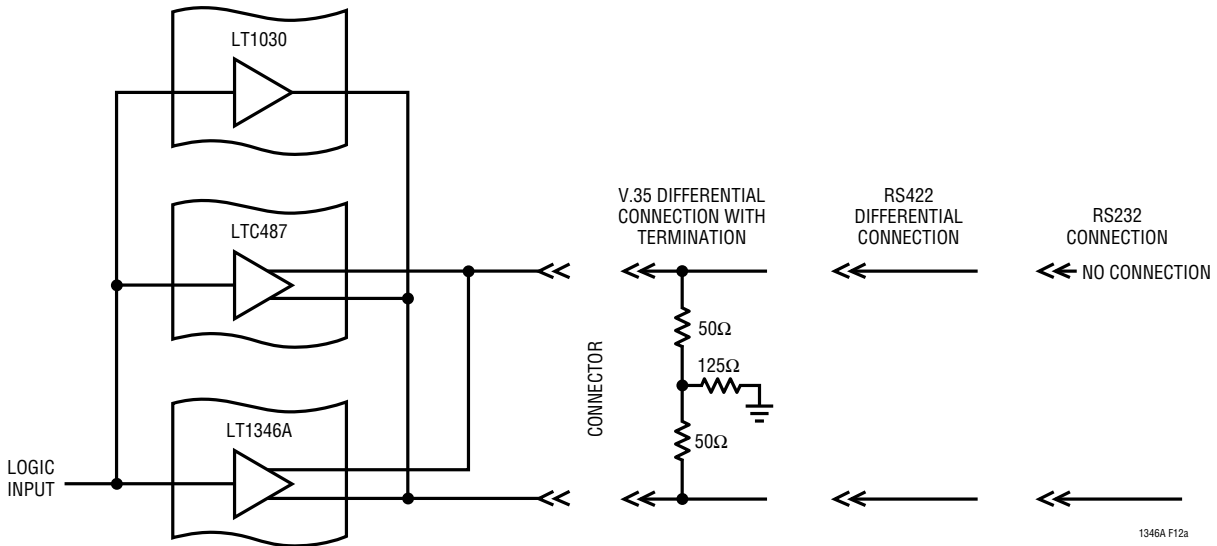


Figure 12a. Multiprotocol Transmitter

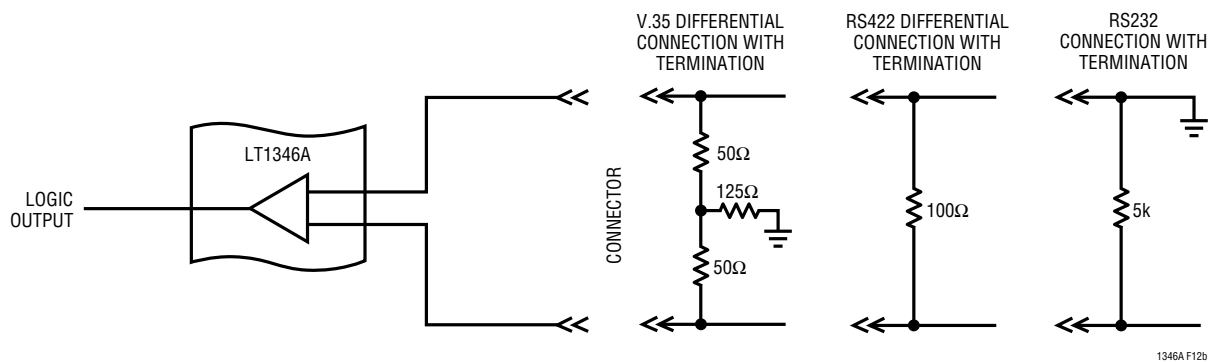
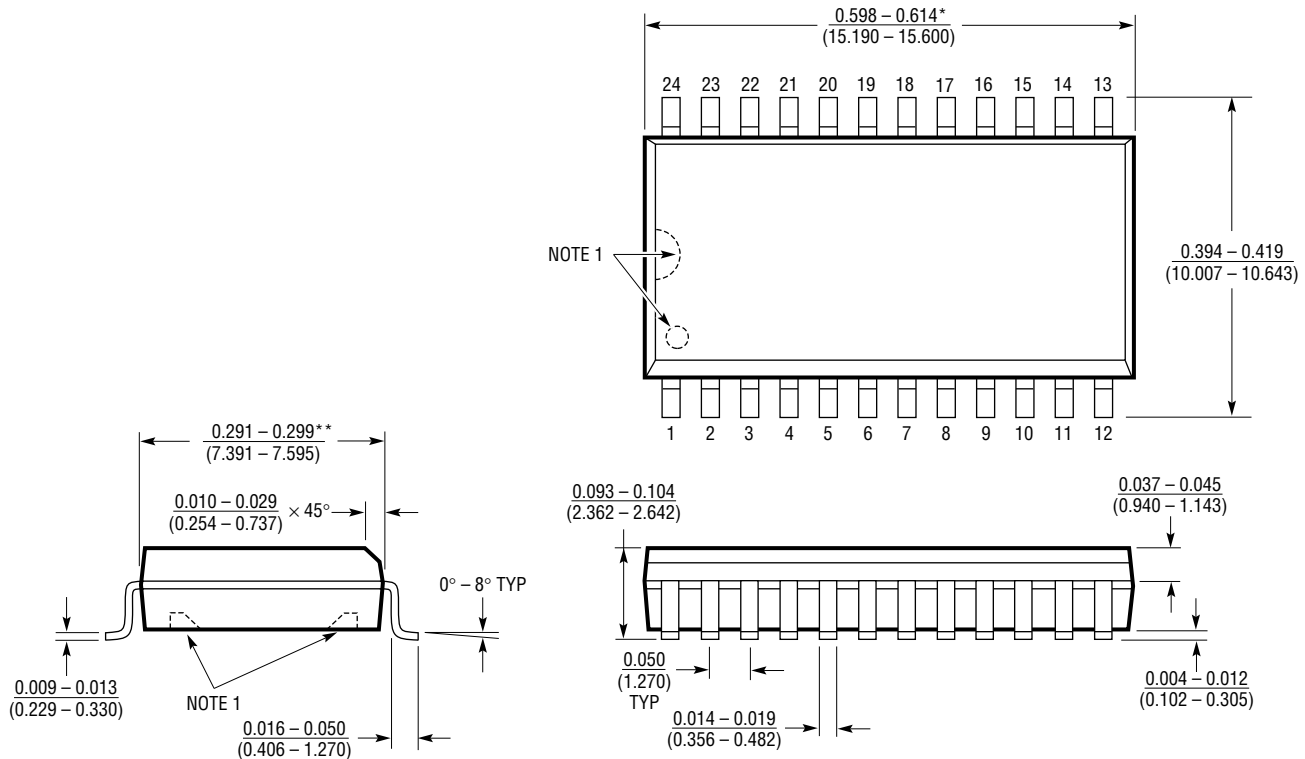


Figure 12b. Multiprotocol Receiver

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
24-Lead Plastic Small Outline (Wide 0.300)
 (LTC DWG # 05-08-1620)



NOTE:
 1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
 *DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
 **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S24 (WIDE) 0695

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1134A	5V Only, 4-Driver/4-Receiver RS232 Transceiver	Forms Complete V.35 Interface with LTC1346A
LTC1334	5V Only, Configurable RS232/RS485 Transceiver	Includes On-Chip Charge Pump
LTC1345	Single Supply V.35 Transceiver	Single 5V Only, Includes On-Chip Charge Pump