MOTOROLA

MC54/74F164

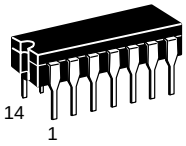
8-BIT SERIAL-IN, PARALLEL-OUT SHIFT REGISTER

The MC54/74F164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock.

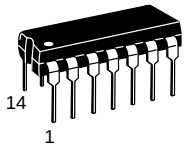
- Typical Shift Frequency of 90 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers

8-BIT SERIAL-IN, PARALLEL-OUT SHIFT REGISTER

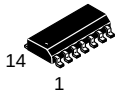
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

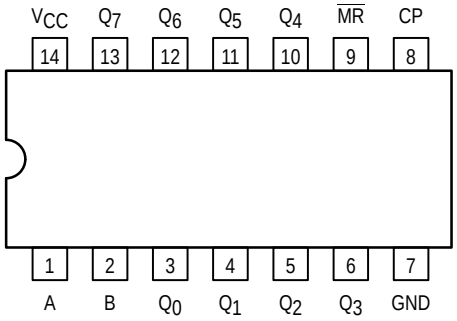


D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

CONNECTION DIAGRAM

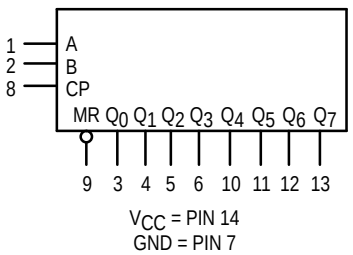


MODE SELECT TABLE

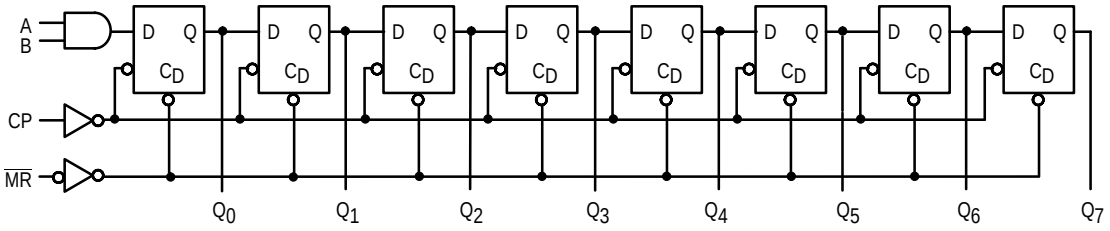
Operating Mode	Inputs			Outputs	
	$\overline{MR}$	A	B	Q_0	$Q_1 - Q_7$
Reset (Clear)	L	X	X	L	L–L
Shift	H	l	l	L	q_0–q_6
	H	l	h	L	q_0–q_6
	H	h	l	L	q_0–q_6
	H	h	h	H	q_0–q_6

H(h) = HIGH Voltage Levels
L(l) = LOW Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The F164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs ($A \bullet B$) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	–55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			–1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = –1.0 mA	V_{CC} = MIN
		74	2.7			V	I_{OH} = –1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				–0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			35	55	mA	A, B = GND, V_{CC} = MAX CP = HIGH, $\overline{MR}$ = GND	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F T_A = + 25°C V_{CC} = + 5.0 V C_L = 50 pF			54F T_A = –55°C to +125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		74F T_A = 0°C to + 70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		Unit
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	80	90		70		80		MHz
t_{PLH}	Propagation Delay	3.0	6.0	8.0	3.0	11	3.0	9.0	ns
t_{PHL}	CP to Q_n	5.0	7.5	10	5.0	13	5.0	11	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.5	10.5	13	5.5	16	5.5	14	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F T_A = + 25°C V_{CC} = + 5.0 V			54F T_A = –55°C to +125°C V_{CC} = 5.0 V ± 10%		74F T_A = 0°C to + 70°C V_{CC} = + 5.0 V ± 10%		Unit
		Min	Typ	Max	Min	Max	Min	Max	
t_s(H)	Setup Time, HIGH or LOW	7.0			7.0		7.0		
t_s(L)	D_n to CP	7.0			7.0		7.0		ns
t_h(H)	Hold Time, HIGH or LOW	1.0			1.0		1.0		
t_h(L)	D_n to CP	1.0			1.0		1.0		
t_w(H)	CP Pulse Width, HIGH or LOW	4.0			4.0		4.0		ns
t_w(L)		7.0			7.0		7.0		
t_w(L)	$\overline{MR}$ Pulse Width, LOW	7.0			7.0		7.0		ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	7.0			7.0		7.0		ns