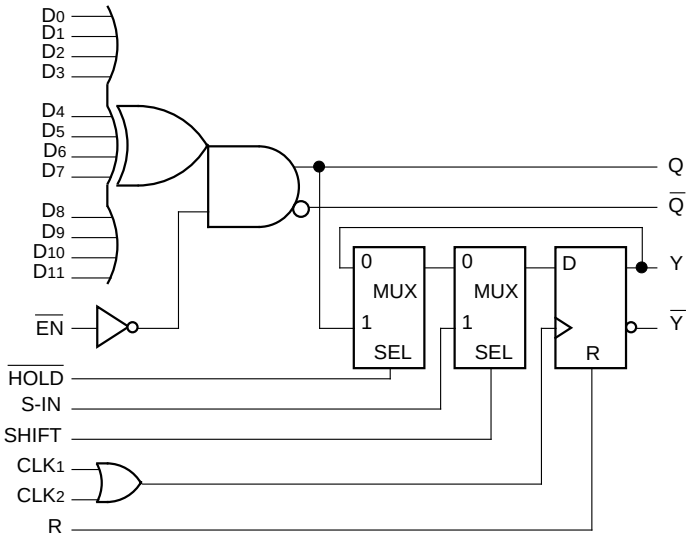
12-BIT PARITY GENERATOR/CHECKER

FEATURES

- Provides odd-HIGH parity of 12 inputs
- Extended 100E V_{EE} range of –4.2V to –5.5V
- Output register with Shift/Hold capability
- 900ps max. D to Q, /Q output
- Enable control
- Asynchronous Register Reset
- Differential outputs
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E160
- Available in 28-pin PLCC package

BLOCK DIAGRAM



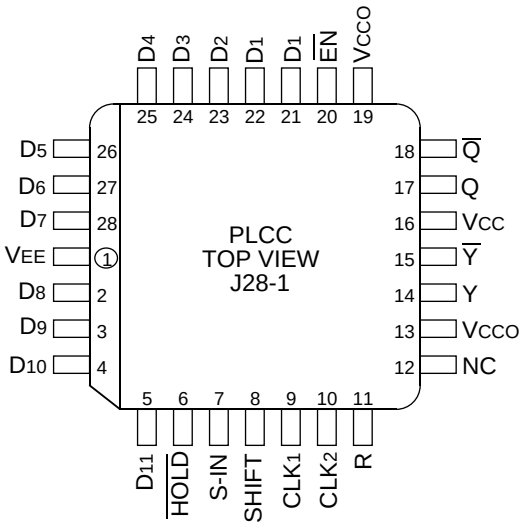
DESCRIPTION

The SY10/100E160 are high-speed, 12-bit parity generator/checkers with differential outputs, for use in new, high-performance ECL systems. The output Q takes on a logic HIGH value only when an odd number of inputs are at a logic HIGH. A logic HIGH on the enable input (EN) forces the output Q to a logic LOW.

An additional feature of the E160 is the output register. Two multiplexers and their associated signals control the register input by providing the option of holding present data, loading the new parity data or shifting external data in. To hold the present data, the Hold signal (HOLD) must be at a logic LOW level. If the HOLD signal is at a logic HIGH, the data present at the Q output is passed through the first multiplexer. Taking the Shift signal (SHIFT) to a logic HIGH will shift the data at the S-IN pin into the output register. If the SHIFT signal is at a logic LOW, the output of the first multiplexer is then passed through to the register.

The register itself is clocked on the rising edge of CLK_1 or CLK_2 (or both). The presence of a logic HIGH on the reset pin (R) forces the register output Y to a logic LOW.

PIN CONFIGURATION



Rev.: D Amendment: /0
Issue Date: February, 1998

PIN NAMES

Pin	Function
D_0–D_{11}	Data Inputs
S-IN	Serial Data Input
EN	Enable, active LOW
HOLD	Hold, active LOW
SHIFT	Shift, active HIGH
CLK_1, CLK_2	Clock Inputs
R	Reset Input
Q, $\overline{Q}$	Direct Output
Y, $\overline{Y}$	Register Output
V_{CCO}	V_{CC} to Output

TRUTH TABLE

Number of HIGH Inputs	Output Q
Even	LOW
Odd	HIGH

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current										µA	—
	CLK_1, CLK_2	—	—	200	—	—	200	—	—	200		
	R	—	—	300	—	—	300	—	—	300		
	All Other Inputs	—	—	150	—	—	150	—	—	150		
I_{EE}	Power Supply Current										mA	—
	10E	—	82	98	—	82	98	—	82	98		
	100E	—	82	98	—	82	98	—	94	113		

AC ELECTRICAL CHARACTERISTICS

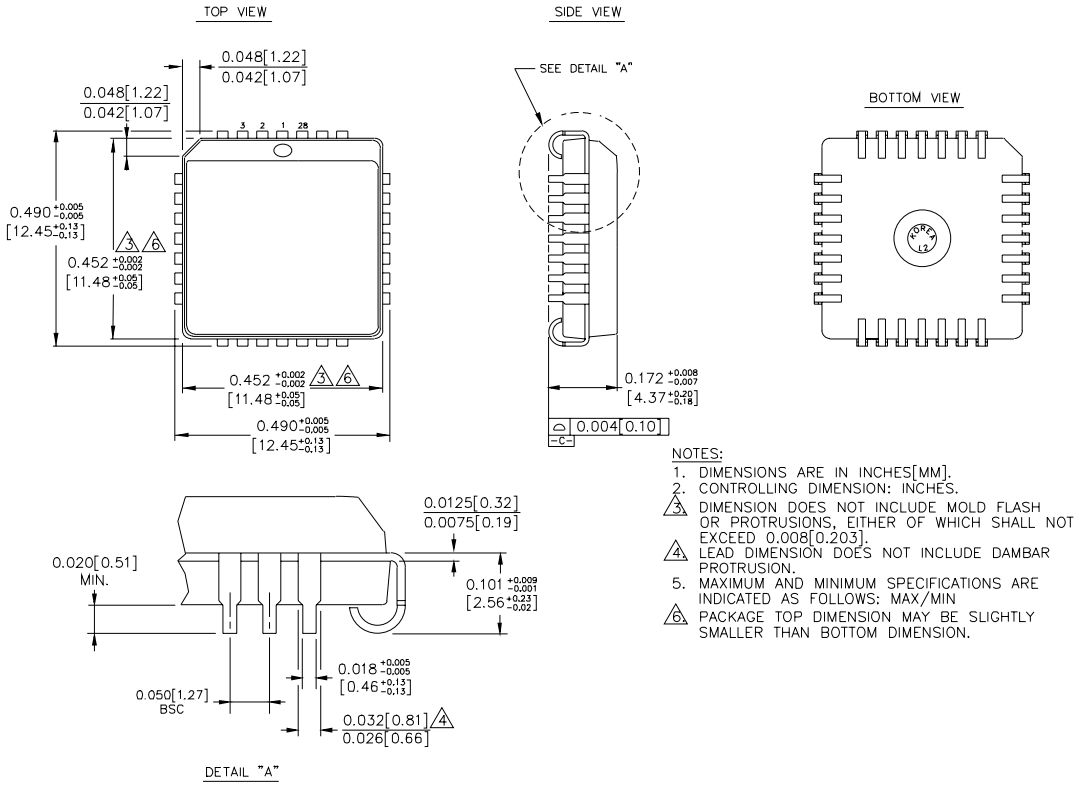
V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q EN to Q CLK to Y R to Y	 400 300 275 275	 650 550 500 500	 950 750 700 725	 400 300 275 275	 650 550 500 500	 950 750 700 725	 400 300 275 275	 650 550 500 500	 950 750 700 725	ps	—
t_S	Set-up Time D HOLD S-IN SHIFT	 1200 600 350 500	 900 300 150 250	 — — — —	 1200 600 350 500	 900 300 150 250	 — — — —	 1200 600 350 500	 900 300 150 250	 — — — —	ps	—
t_H	Hold Time D HOLD S-IN SHIFT	 –400 100 300 200	 –900 –300 –150 –250	 — — — —	 –400 100 300 200	 –900 –300 –150 –250	 — — — —	 –400 100 300 200	 –900 –300 –150 –250	 — — — —	ps	—
t_r t_f	Rise/Fall Time 20% to 80%	300	450	650	300	450	650	300	450	650	ps	—

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E160JC	J28-1	Commercial
SY10E160JCTR	J28-1	Commercial
SY100E160JC	J28-1	Commercial
SY100E160JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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