

# AN5195K-C

Single chip IC for PAL/NTSC color TV  
(built-in I<sup>2</sup>C bus interface)

## ■ Overview

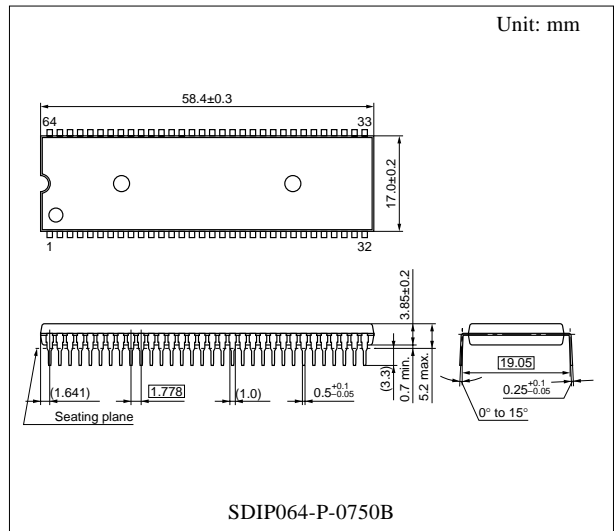
The AN5195K-C is an IC in which all of the PAL/NTSC system color television signal processing circuits are integrated on one chip. The rationalization of set production line can be realized by the incorporation of I<sup>2</sup>C bus interface.

## ■ Features

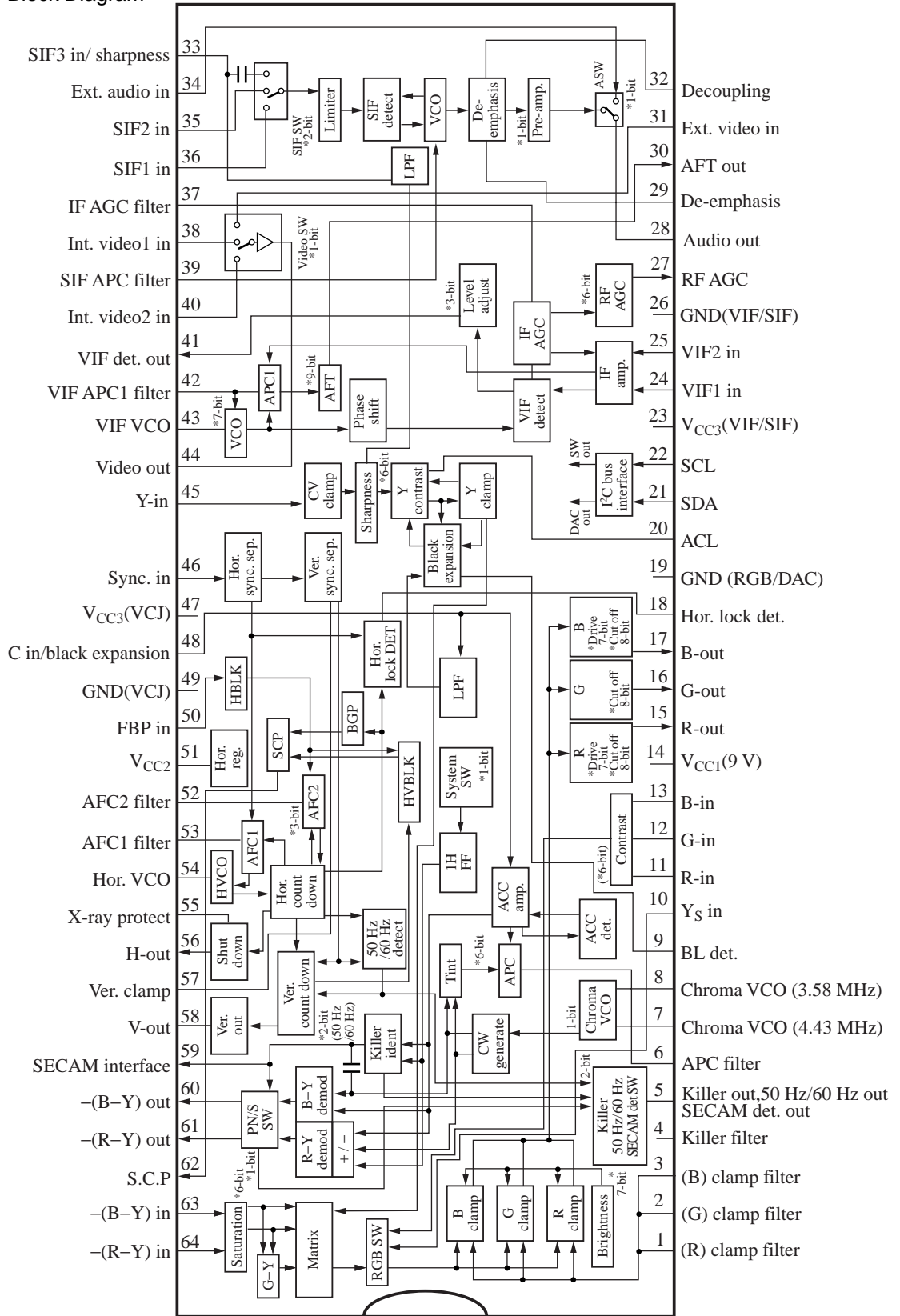
- Built-in video IF circuit, sound IF circuit, video signal processing circuit, color signal processing circuit, and sync. signal processing circuit
- Rationalization of set production line can be realized by the incorporation of I<sup>2</sup>C bus interface
- Can be applied to PAL/NTSC/AV-NTSC/M-NTSC system
- Package: 64-SDIP, supply voltage: 5 V, 9 V

## ■ Applications

- TV, TV-video combination



■ Block Diagram



### ■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	(R) clamp	33	SIF3 input/ sharpness
2	(G) clamp	34	External audio input
3	(B) clamp	35	SIF2 input
4	Killer filter	36	SIF1 input
5	Killer out, 50 Hz/60 Hz out, SECAM det. out	37	IF AGC filter
6	Chroma APC filter	38	Internal video1 input
7	Chroma VCO (4.43 MHz)	39	SIF APC filter
8	Chroma VCO (3.58 MHz)	40	Internal video2 input
9	Black level det.	41	VIF detect output
10	$Y_S$ input	42	VIF APC1 filter
11	External R input	43	VIF VCO ( $f_P/2$ )
12	External G input	44	Video output
13	External B input	45	Y input
14	$V_{CC1}$	46	HV sync. input
15	R output	47	$V_{CC3-2}$ (chroma/jungle/DAC)
16	G output	48	Chroma input/black expansion start
17	B output	49	GND (video/chroma/jungle)
18	Hor. lock detect	50	FBP input
19	GND (RGB/I <sup>2</sup> C/DAC)	51	$V_{CC2}$ (hor. stability supply)
20	ACL	52	AFC2 filter
21	SDA	53	AFC1 filter
22	SCL	54	Hor. VCO ( $32 f_H$ )
23	$V_{CC3-1}$ (VIF/SIF)	55	X-ray protection input
24	VIF1 input	56	Hor. pulse output
25	VIF2 input	57	Ver. sync. clamp
26	GND (VIF/SIF)	58	Ver. pulse output
27	RF AGC output	59	SECAM interface
28	Audio output	60	-(B-Y) output
29	De-emphasis	61	-(R-Y) output
30	AFT output	62	Sandcastle pulse output
31	External video input	63	-(B-Y) input
32	DC decoupling filter	64	-(R-Y) input

### ■ Absolute Maximum Ratings

Parameter	Symbol		Rating	Unit
Supply voltage	$V_{CC}$	$V_{CC1}(14)$	10.5	V
		$V_{CC3}(23, 47)$	6.0	
Supply current	$I_{CC}$	$I_{14}$	67	mA
		$I_{23+47}$	126	
		$I_{51}$	27	
Power dissipation*2	$P_D$		1,480	mW
Operating ambient temperature*1	$T_{opr}$		-20 to + 70	°C
Storage temperature *1	$T_{stg}$		-55 to + 150	°C

Note) \*1 : Except for the operating ambient temperature and storage temperature, all ratings are for  $T_a = 25^\circ\text{C}$ .

\*2 : The power dissipation shown is the value for  $T_a = 70^\circ\text{C}$ .

### ■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	$V_{CC1}$	8.1 to 9.9	V
	$V_{CC3}$	4.5 to 5.5	
Supply current	$I_{51}$	10 to 25	mA

### ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply						
Supply current 1	$I_{14}$	Current at $V_{14} = 9\text{ V}$	39	48	57	mA
Supply current 2	$I_{23}$	Current at $V_{23} = 5\text{ V}$	7	10	13	mA
Supply current 3	$I_{47}$	Current at $V_{47} = 5\text{ V}$	49	63	77	mA
Stabilized power supply voltage	$V_{51}$	Voltage at $I_{51} = 15\text{ mA}$	5.8	6.5	7.2	V
Stabilized power supply current	$I_{51}$	Current at $V_{51} = 5\text{ V}$	2	5	7	mA
Stabilized power supply input resistance	$R_{51}$	DC measurement, gradient at $I_{51} = 10\text{ mA}$ and $25\text{ mA}$	1	5	10	$\Omega$

VIF circuit Typical input:  $f_p = 38.9\text{ MHz}$ ,  $V_{IN} = 90\text{ dB}\mu$

Video detection output (typ.)	$V_{PO}$	Modulation $m = 87.5\%$ , data $0B = 44$	1.7	2.1	2.5	V[p-p]
Video detection output (max.)	$V_{POmax}$	$0B = 74$	1.9	2.6	3.3	V[p-p]
Video detection output (min.)	$V_{POmin}$	$0B = 04$	1.1	1.6	2.1	V[p-p]
Video detection output f characteristics	$f_{PC}$	Frequency to become $-3\text{ dB}$ for $1\text{ MHz}$	5.5	8	12	MHz
Sync. peak value voltage	$V_{SP}$	Sync. peak voltage at V[p-0] measurement	1.6	2.0	2.4	V
APC pull-in range (H)	$f_{PPH}$	High band side pull-in range (difference from $f_p = 38.9\text{ MHz}$ )	1.0	2.0	—	MHz
APC pull-in range (L)	$f_{PPL}$	Low band side pull-in range (difference from $f_p = 38.9\text{ MHz}$ )	—	-2.0	-1.0	MHz
RF AGC delay point adjusting range	$\Delta V_{RFDP}$	Delay point (input to become $V_{27} = \text{approx. } 6.5\text{ V}$ ) at data $0A = 00$ to $3F$	75	—	95	$\text{dB}\mu$

**■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF circuit (continued) Typical input: $f_p = 38.9\text{ MHz}$ , $V_{IN} = 90\text{ dB}\mu$						
VCO free-running frequency	$\Delta f_p$	Dispersion without input $V_{IN}$ , $V_{37}$ (IF AGC) = 0 V (measurement of difference from 38.9 MHz)	-1.2	0	1.2	MHz
RF AGC maximum sink current	$IRF_{max}$	Maximum current IC can sink when pin 27 is low	1.5	3.0	—	mA
RF AGC minimum sink current	$IRF_{min}$	Leakage current of IC, when pin 27 is high	-50	0	50	$\mu\text{A}$
AFT discrimination sensitivity	$\mu_{AFT}$	$\Delta f = \pm 25\text{ kHz}$	40	57	75	mV/kHz
AFT center voltage	$V_{AFT}$	$V_{30}$ without input $V_{IN}$	4.0	4.5	5.0	V
AFT maximum output voltage	$V_{AFTmax}$	$V_{30}$ at $f = f_p - 500\text{ kHz}$	7.8	8.1	8.7	V
AFT minimum output voltage	$V_{AFTmin}$	$V_{30}$ at $f = f_p + 500\text{ kHz}$	0.3	0.8	1.0	V
Detection output resistance	$R_{O41}$	DC measurement $I_O = -0.4\text{ mA}$ to $-1.0\text{ mA}$	70	120	170	$\Omega$
SIF circuit Typical input: $f_s = 6.0\text{ MHz}$ , $f_M = 400\text{ Hz}$ , $V_{IN} = 90\text{ dB}\mu$						
Audio detection output (PAL, SIF1)	$V_{SOP36}$	$\Delta f = \pm 50\text{ kHz}$ $0B-D3 = 0$	0.90	1.15	1.40	V[rms]
Audio detection output (PAL, SIF2)	$V_{SOP35}$	$\Delta f = \pm 50\text{ kHz}$ $0B-D3 = 0$	0.90	1.15	1.40	V[rms]
Audio detection output (PAL, SIF3)	$V_{SOP33}$	$\Delta f = \pm 50\text{ kHz}$ $0B-D3 = 0$	0.90	1.15	1.40	V[rms]
Audio detection output NTSC/PAL	$R_{SN/P}$	$\Delta f = \pm 25\text{ kHz}$ , $0B-D3 = 1$ , ratio to PAL ( $V_{SOP36}$ )	-2.5	-0.5	1.5	dB
Audio detection output linearity	$\Delta V_{SOP}$	Ratio between $f_s = 5.5\text{ MHz}$ and $6.0\text{ MHz}$ , and $6.5\text{ MHz}$	-3	0	3	dB
SIF pull-in range NTSC (4.5 MHz)	$f_{SNH}$ (4.5 MHz)	Pull-in range of high frequency side	4.8	5.0	—	MHz
SIF pull-in range NTSC (4.5 MHz)	$f_{SNL}$ (4.5 MHz)	Pull-in range of low frequency side	—	4.0	4.2	MHz
SIF pull-in range PAL (5.5 MHz)	$f_{SPH}$ (5.5 MHz)	Pull-in range of high frequency side	5.8	6.0	—	MHz
SIF pull-in range PAL (5.5 MHz)	$f_{SPL}$ (5.5 MHz)	Pull-in range of low frequency side	—	5.0	5.2	MHz
SIF pull-in range PAL (6.0 MHz)	$f_{SPH}$ (6.0 MHz)	Pull-in range of high frequency side	6.3	6.5	—	MHz
SIF pull-in range PAL (6.0 MHz)	$f_{SPL}$ (6.0 MHz)	Pull-in range of low frequency side	—	5.5	5.7	MHz
SIF pull-in range PAL (6.5 MHz)	$f_{SPH}$ (6.5 MHz)	Pull-in range of high frequency side	6.8	7.0	—	MHz
SIF pull-in range PAL (6.5 MHz)	$f_{SPL}$ (6.5 MHz)	Pull-in range of low frequency side	—	6.0	6.2	MHz
De-emphasis pin output resistance (PAL)	$R_{29P}$	Impedance of pin 29 at PAL	32	40	48	k $\Omega$
De-emphasis pin output resistance (NTSC)	$R_{29N}$	Impedance of pin 29 at NTSC	48	60	72	k $\Omega$

■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AV SW circuit						
Video SW voltage gain	$G_{VSW}$	$f = 1\text{MHz}$ , $V_{IN} = V[p-p]$	5.7	6.7	7.7	dB
Video SW f characteristics	$f_{VSW}$	Frequency to become $-3\text{ dB}$ from $f = 1\text{ MHz}$ , $V_{IN} = 0.714\text{ V}[0-p]$	8	10	—	MHz
Video SW external input pin voltage	$V_{31}$	DC measurement	1.7	2.0	2.3	V
Video SW external output DC voltage	$V_{44E}$	DC measurement, 03-D7 = 1, 0B-D7 = 1	4.2	4.8	5.4	V
Video SW external input resistance	$R_{I31}$	DC measurement	44	56	68	$k\Omega$
Video SW output resistance	$R_{O44}$	DC measurement, $I_O = -0.6\text{ mA}$ to $-1.0\text{ mA}$	100	140	180	$\Omega$
Video SW internal clamp pin voltage	$V_{38,40}$	DC measurement, $I_{IN} = -1.0\text{ mA}$	1.3	1.6	1.9	V
Video SW internal output DC voltage	$V_{44I}$	DC measurement	3.7	4.3	4.9	V
Audio SW voltage gain	$G_{ASW}$	Data 03-D7 = 1, 0B-D7 = 1 (external input) $f = 400\text{ Hz}$ , $V_{IN} = 1\text{ V}[p-p]$	-1	0	1	dB
Audio SW input pin voltage	$V_{34}$	DC measurement	3.7	4.2	4.7	V
Audio SW output DC voltage	$V_{28}$	DC measurement	3.7	4.2	4.7	V
Audio SW input resistance	$R_{I34}$	DC measurement	55	65	75	$k\Omega$
Audio SW output resistance	$R_{O28}$	DC measurement	200	400	600	$\Omega$
Video signal processing circuit Typical input: $0.6\text{ V}[p-p]$ ( $V_{WB} = 0.42\text{ V}[p-p]$ stair-step), at G-out						
Video output (typ.)	$V_{YO}$	Data 03 = 20 (typ.) (contrast)	1.9	2.4	2.9	$V[0-p]$
Video output (max.)	$V_{YOmax}$	Data 03 = 3F (max.)	4.1	5.0	5.9	$V[0-p]$
Video output (min.)	$V_{YOmin}$	Data 03 = 00 (min.)	0.15	0.50	1.00	$V[0-p]$
Contrast variable range	$Y_{Cmax/min}$	$\frac{03 = 3F}{03 = 00}$	15	20	25	dB
Video frequency characteristics	$f_{YC}$	Pin 33 = $5\text{ V}$ (sharpness), frequency to become $-3\text{ dB}$ from $f = 0.2\text{ MHz}$	5.5	6.0	—	MHz
Picture quality variable range	$Y_{Smax/min}$	$\frac{V_{33} = 7\text{ V}}{V_{33} = 5\text{ V}}$ , $f = 3.8\text{ MHz}$	9	13	17	dB
Pedestal level (typ.)	$V_{PED}$	Data 02 = 40 (typ.) (brightness)	2.0	2.5	3.0	V
Pedestal level variable width	$\Delta V_{PED}$	Difference between data 02 = 00 and 7F	2.0	2.6	3.2	V
Brightness control sensitivity	$\Delta V_{BRT}$	Average amount of change at data 02 = 30 and 50 per 1 step	14	20	26	mV/Step
Video input clamp voltage	$V_{YCLP}$	Clamp voltage of pin 45	3.2	3.7	4.2	V
ACL sensitivity	ACL	Change of Y-out, when $V_{20} = 3.0\text{ V} \rightarrow 3.5\text{ V}$	2.4	3.0	3.6	V/V
Blanking off threshold voltage	$V_{YBL}$	DC voltage of blanking pulse	—	1.0	1.5	V
Blanking level Service SW threshold voltage <sup>*1</sup>	$V_{STH}$	Stop voltage of vertical output, when lowering pin 20 (ACL) voltage	—	—	0.3	V
DC restoration ratio	$T_{DC}$	APL 10% to 90% $T_{DC} = \frac{\Delta AC - \Delta DC}{\Delta AC} \times 100$	90	100	110	%
Video input clamp current	$I_{YCLP}$	DC measurement: IC inside sink current	8	13	18	$\mu\text{A}$

Note) \*1: Take great care for not to become  $V_{20} < 0.9\text{ V}$  at set design so that the pin 20 is combined use for service SW when it is used as the ACL.

**■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video signal processing circuit (continued) Typical input: 0.6 V[p-p] ( $V_{WB} = 0.42$ V[p-p] stair-step), at G-out						
Pedestal difference voltage	$\Delta V_{IPL}$	Difference voltage of R,G,B-out pedestal	-0.2	0	0.2	V
Brightness voltage tracking	$\Delta T_{BL}$	R,G,B-out fluctuation level ratio of data 02 (brightness) = 20 to 60	0.9	1.0	1.1	Times
Video voltage gain relative ratio	$\Delta G_{YC}$	Output ratio of R,B-out against G-out	0.8	1.0	1.2	Times
Video voltage gain tracking	$\Delta T_{CONT}$	Gain ratio of R,G,B-out at data 03 (contrast) = 10 to 30	0.9	1.0	1.1	Times/ Times
Chroma signal processing circuit Burst 150 mV[p-p] (PAL), reference is B-out						
Color-difference output (typ.)	$V_{CO}$	Input: Color bar data 00 = 20 (typ.), 03 = 20 (typ.)	2.9	3.7	4.5	V[p-p]
Color-difference output (max.)	$V_{COmax}$	Data 00 = 3F, amplitude of one side, 03 = 20	2.6	3.3	—	V[0-p]
Color-difference output (min.)	$V_{COmin}$	Data 00 = 00, 03 = 20	—	—	100	mV[p-p]
Contrast variable range	$C_{Cmax/min}$	$03 = 3F$ $03 = 00$ , 00 = 20	15	20	25	dB
ACC characteristics 1	ACC1	Burst 150 mV[p-p] → 300 mV[p-p]	0.9	1.0	1.2	Times
ACC characteristics 2	ACC2	Burst 150 mV[p-p] → 30 mV[p-p]	0.8	1.0	1.2	Times
NTSC tint center	$\Delta\theta_C$	Difference from data 01 = 20 (tint), when adjusted at tint center	-7	0	7	Step
NTSC tint variable range 1	$\Delta\theta_1$	Input: Rainbow, data 01 = 3F	30	50	65	deg
NTSC tint variable range 2	$\Delta\theta_2$	Input: Rainbow, data 01 = 00	-65	-50	-30	deg
Color-difference output ratio (R)	R/B	Input: Rainbow for both PAL/NTSC	0.46	0.56	0.66	Times
Color-difference output ratio (G)	G/B	Input: Rainbow for both PAL/NTSC	0.28	0.34	0.40	Times
Color-difference output angle (R)	$\angle R$	Input: Rainbow for both PAL/NTSC	78	90	102	deg
Color-difference output angle (G)	$\angle G$	Input: Rainbow for both PAL/NTSC	224	236	248	deg
PAL color killer tolerance	$V_{KILLP}$	0 dB = 150 mV[p-p]	-57	-44	-34	dB
NTSC color killer tolerance	$V_{KILLN}$	0 dB = 150 mV[p-p]	-57	-44	-34	dB
APC pull-in range (H)	$f_{CPH}$	For both PAL/NTSC	450	700	—	Hz
APC pull-in range (L)	$f_{CPL}$	For both PAL/NTSC	—	-700	-450	Hz
Color killer detection output voltage (color)	$V_{KC}$	$V_5$ , when chroma input Data 0A-D6 = 0, 0A-D7 = 1, killer out	4.5	5.0	—	V
Color killer detection output voltage (B&W)	$V_{KBW}$	$V_5$ , when chroma input Data 0A-D6 = 0, 0A-D7 = 1, killer out	0	0.1	0.5	V
Demodulation output -(B-Y)	$V_{DB}$	Input: Measurement at pin 60 for both color bar PAL/NTSC	555	695	835	mV[p-p]
Demodulation output -(R-Y)	$V_{DR}$	Input: Measurement at pin 61 for both color bar PAL/NTSC	430	540	650	mV[p-p]
Demodulation output angle $\angle(B-Y)$	$\angle R_{DB}$	Phase shift of B-Y axis	-6	0	6	deg
Demodulation output angle $\angle(R-Y)$	$\angle R_{DR}$	Phase difference from B-Y axis	84	90	96	deg
CW output level (4.43 MHz)	$V_{CWP}$	AC component, when $V_{CO}$ is set at 4.43 MHz	250	350	450	mV[p-p]

**■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Chroma signal processing circuit (continued) Burst 150 mV[p-p] (PAL), reference is B-out						
CW output level (3.58 MHz)	$V_{\text{CWN}}$	AC component, when $V_{\text{CO}}$ is set at 3.58 MHz	—	—	50	mV[p-p]
CW output level period (SECAM)	$T_{\text{CW}}$	CW output period at SECAM and PAL	1.31	1.41	1.51	ms
SECAM discrimination current	$I_{\text{SECAM}}$	Minimum value for taking out current from pin 59 and discriminating as SECAM	50	100	150	$\mu\text{A}$
SECAM discrimination output	$V_{\text{SE}}$	$V_5$ data, when SECAM signal inputted 0A-D6 = 1, 0A-D7 = 0, SECAM det. out	4.5	5.0	—	V
PAL/NTSC DC level	$V_{59\text{PN}}$	$V_{59}$ DC level at PAL/NTSC	0.8	1.3	1.65	V
SECAM DC level	$V_{59\text{S}}$	$V_{59}$ DC level at SECAM	4.1	4.6	5.1	V
RGB processing circuit DAC data are typical						
Drive adjustment range	$G_{\text{DV}}$	AC change amount of R, B-out, when drive adjustment max. and min.	5	6	7	dB
Cut-off adjustment range	$V_{\text{CUTOFF}}$	DC change amount of R,G,B-out, when cutoff adjustment max. and min.	2.1	2.4	2.7	V
$Y_S$ threshold voltage	$V_{\text{YSON}}$	Minimum DC voltage, when $Y_S$ turns on	1.0	—	—	V
$Y_S$ threshold voltage	$V_{\text{YSOFF}}$	Maximum DC voltage, when $Y_S$ turns off	—	—	0.4	V
External RGB pedestal difference voltage	$\Delta V_{\text{EPL}}$	$Y_S = 5\text{ V}$	-200	0	200	mV
Internal and external pedestal difference voltage	$\Delta V_{\text{PL/IE}}$	Internal-external	200	0	200	mV
External RGB output voltage	$V_{\text{ERGB}}$	Input 0.7 V[p-p], contrast 03 = 20 (typ.)	1.8	2.2	2.7	V[p-p]
External RGB output difference voltage	$\Delta V_{\text{ERGB}}$	Output ratio of external R,G,B-out	0.8	1.0	1.2	Times
External RGB contrast variable range	$E_{\text{Cmax/min}}$	$\frac{03 = 3F}{03 = 00}$	12	17	22	dB
External RGB frequency characteristics	$f_{\text{RGBC}}$	Input 0.2 V[p-p]	8	10	—	MHz
Internal and external RGB output voltage ratio	$V_{\text{E/I}}$	External 0.7 V[p-p]/internal 0.6 V[p-p] input, contrast 03 = 20 (typ.)	0.78	0.92	1.06	Times
Synchronizing signal processing circuit						
Horizontal free-running oscillation frequency	$f_{\text{HO}}$	Without sync. signal input	15.33	15.63	15.93	kHz
Horizontal output pulse duty cycle	$\tau_{\text{HO}}$	Upward going pulse duty cycle	31	37	43	%
Horizontal pull-in range	$f_{\text{HP}}$	Difference from $f_{\text{H}} = 15.625\text{ kHz}$	$\pm 500$	$\pm 650$	—	Hz
PAL vertical free-running oscillation frequency	$f_{\text{VO-P}}$	Data 01-D7 = 1, 02-D7 = 0 Forced 50 Hz mode, no sync. signal input	48	50	52	Hz
NTSC vertical free-running oscillation frequency	$f_{\text{VO-N}}$	Data 01-D7 = 1, 02-D7 = 1 Forced 60 Hz mode, no sync. signal input	58	60	62	Hz
Vertical output pulse width	$\tau_{\text{VO}}$	For both PAL/NTSC	9	10	11	1/fH
PAL vertical pull-in range	$f_{\text{VP-P}}$	$f_{\text{H}} = 15.625\text{ kHz}$ , forced 50 Hz mode	46	—	54	Hz
NTSC vertical pull-in range	$f_{\text{VP-N}}$	$f_{\text{H}} = 15.75\text{ kHz}$ , forced 60 Hz mode	56	—	64	Hz
Horizontal output voltage (H)	$V_{56\text{H}}$	High-level DC voltage	2.9	3.2	3.5	V
Horizontal output voltage (L)	$V_{56\text{L}}$	Low-level DC voltage	—	—	0.3	V



**■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Synchronizing signal processing circuit (continued)						
Vertical output voltage (H)	$V_{58H}$	High-level DC voltage	3.9	4.2	4.5	V
Vertical output voltage (L)	$V_{58L}$	Low-level DC voltage	—	—	0.3	V
Picture center variable range	$\Delta T_{HC}$	Change amount of phase difference of H sync. and H-out of data 0B = 40 to 47	2.6	3.2	4.4	$\mu\text{s}$
Overvoltage protective operation voltage	$V_{XRAY}$	Minimum voltage of pin 55 at which H-out stops to appear	0.60	0.68	0.76	V
Vertical frequency discrimination 50	$f_{50}$	Vertical frequency to become $V_5 = \text{low} (< 0.5 \text{ V})$	47	—	55	Hz
Vertical frequency discrimination 60	$f_{60}$	Vertical frequency to become $V_5 = \text{high} (> 4.5 \text{ V})$	57	—	63	Hz
Sync. signal clamp voltage	$V_{46}$	$V_{46}$ clamp voltage	1.0	1.3	1.6	V
Horizontal output start voltage	$V_{IHS}$	Minimum $V_{50}$ to become $f_0 > 10 \text{ kHz}$ , when horizontal oscillation output is more than 1 V[p-p]	3.4	4.2	5.0	V

**I<sup>2</sup>C interface**

Sink current at ACK	$I_{ACK}$	Maximum value of pin 21 sink current when ACK	1.8	2.5	5.0	mA
SCL, SDA signal input high-level	$V_{IHI}$		3.1	—	—	V
SCL, SDA signal input low-level	$V_{ILO}$		—	—	0.9	V
Maximum frequency allowable to input	$f_{Imax}$		—	—	100	kbit/s

**• Design reference data**

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF circuit Typical input: $f_p = 38.9 \text{ MHz}$ , $V_{IN} = 90 \text{ dB}\mu$						
Input sensitivity	$V_{PS}$	Input level to become $V_{PO1} = -3 \text{ dB}$	—	45	—	$\text{dB}\mu$
Maximum allowable input	$V_{Pmax}$	Input level to become $V_{PO1} = +1 \text{ dB}$	—	110	—	$\text{dB}\mu$
SN ratio	$SN_P$		50	—	—	dB
Differential gain	$DG_P$		—	—	5	%
Differential phase	$DP_P$		—	—	5	deg
Black noise detection level	$\Delta V_{BN}$	Deference from sync. peak value	—	-45	—	IRE
Black noise clamp level	$\Delta V_{BNC}$	Deference from sync. peak value	—	45	—	IRE
RF AGC operation sensitivity	$G_{RF}$	Input level difference to become $V_{27} = 1 \text{ V} \rightarrow 7 \text{ V}$	0.5	—	3.0	dB
VCO switch on drift	$\Delta f_{PD}$	Frequency drift from 5 seconds to 5 mins. after SW on	—	—	200	kHz
Intermodulation	IM	$V_{fC} - V_{fP} = -2 \text{ dB}$ , $V_{fC} - V_{fP} = -12 \text{ dB}$	46	—	—	dB
RF AGC adjustment sensitivity	$S_{RF}$	Average amount of change of output voltage $V_{27}$ at data 1 step	2	—	5	V/Step

## ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

### • Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF circuit (continued) Typical input: $f_P = 38.9\text{ MHz}$ , $V_{IN} = 90\text{ dB}\mu$						
AFT offset adjustment sensitivity	$S_{AFT}$	Average amount of change of output voltage $V_{30}$ at data 1 step	0.1	—	0.3	V/Step
Video detection output fluctuation with $V_{CC}$	$\Delta V_{P/V}$	$V_{CC} = \pm 10\%$	—	—	$\pm 15$	%
Video detection output-temperature characteristics	$\Delta V_{P/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	—	—	$\pm 10$	%
Input resistance (pin 24, pin 25)	$R_{I24,25}$	$f = 38.9\text{ MHz}$	—	1.2	—	$\text{k}\Omega$
Input capacitance (pin24, pin 25)	$C_{I24,25}$	$f = 38.9\text{ MHz}$	—	4.0	—	$\text{pF}$
Sound IF output level	$V_{SIF}$	$f_S = 38.9\text{ MHz}$ – $6.0\text{ MHz}$ , P/S = 20 dB	90	—	110	$\text{dB}\mu$
VCO control sensitivity	$\beta_P$	$\Delta V_{42} = \pm 0.1\text{ V}$	2.0	—	3.5	$\text{kHz/mV}$
VCO control range	$f_{VCO}$	Free-running frequency change width at data 0C = 00 to 7F	3	—	5	$\text{MHz}$
RF AGC delay-point temperature characteristics	$\Delta V_{DP/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	—	—	5	$\text{dB}$
VCO free-running frequency temperature characteristics	$\Delta f_{P/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	—	300	—	$\text{kHz}$
AFT center frequency temperature characteristics	$\Delta f_{AFT/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$ , input frequency at which AFT output voltage becomes 4.5 V	—	300	—	$\text{kHz}$
External mode output DC voltage	$V_{41EXT}$	Output DC voltage at AV SW external mode	0.5	1.0	1.8	V
SIF circuit Typical input: $f_S = 6.0\text{ MHz}$ , $f_M = 400\text{ Hz}$ , $V_{IN} = 90\text{ dB}\mu$						
Input limiting level	$V_{LIM}$	Input level to become $V_{SOP} = -3\text{ dB}$	—	—	50	$\text{dB}\mu$
AM rejection ratio	AMR	AM = 30%	55	—	—	$\text{dB}$
Total harmonic distortion	THD	$\Delta f = \pm 50\text{ kHz}$	—	—	1.0	%
SN ratio	$SN_A$	$\Delta f = \pm 50\text{ kHz}$ , $f_M = 400\text{ Hz}$ , on/off	55	—	—	$\text{dB}$
Audio output with $V_{CC}$ fluctuation	$\Delta V_{S/V}$	$V_{CC} = \pm 10\%$	—	—	$\pm 10$	%
Audio output temperature characteristics	$\Delta V_{S/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	—	—	$\pm 10$	%
SIF input resistance	$R_{I35}$	DC measurement	—	30	—	$\text{k}\Omega$
SIF input resistance	$R_{I36}$	DC measurement	—	30	—	$\text{k}\Omega$
AV SW circuit						
Video SW cross-talk (Internal → Internal)	$CT_{VII}$	$f = 1\text{ MHz}$ , $V_{IN} = 1\text{ V[p-p]}$ Internal → Internal	—	—	-55	$\text{dB}$
Video SW cross-talk (External → Internal)	$CT_{VEI}$	$f = 1\text{ MHz}$ , $V_{IN} = 1\text{ V[p-p]}$ Internal → External, External → Internal	—	—	-55	$\text{dB}$
Audio SW cross-talk (Internal → Internal)	$CT_{AII}$	$f_S = 6.5\text{ MHz}$ , $f_M = 400\text{ Hz}$ , $V_{IN} = 1\text{ V[p-p]}$ $f_S = 6.5\text{ MHz}$ , $f_M = 1.0\text{ kHz}$ , $V_{IN} = 1\text{ V[p-p]}$	—	—	-60	$\text{dB}$

### ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

#### • Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AV SW circuit (continued)						
SIF SW cross-talk (External → Internal)	$CT_{AEI}$	$f_S = 6.5 \text{ MHz}$ , $f_M = 400 \text{ Hz}$ , $V_{IN} = 1 \text{ V[p-p]}$ Inside $f = 400 \text{ Hz}$ , $V_{IN} = 1 \text{ V[p-p]}$	—	—	-60	dB
Video signal processing circuit Typical input: 0.6 V[p-p] ( $V_{BW} = 0.42 \text{ V[0-p]}$ ) stair-step) at G-out						
Black level extension 1	$V_{BL1}$	Input: Total black, difference between the voltage at pin 9 = 9 V and open (with RC filter)	-100	0	100	mV
Black level extension 2	$V_{BL2}$	Input: Total black, difference between the voltage at pin 9 = 3 V and 9 V	400	700	1 000	mV
Black level extension 3	$V_{BL3}$	Input: approx. 20IRE, difference between the voltage at pin 9 = open and 9 V, 03 (contrast) = 3F (max.)	100	300	500	mV
Contrast variation with sharpness	$\Delta V_{CS}$	Y-out output level difference, when sharpness max. and min.	-300	0	300	mV
Brightness variation with sharpness	$\Delta V_{BS}$	Pedestal level DC difference, when sharpness max. and min.	-250	0	250	mV
Input dynamic range	$V_{Imax}$	03 (contrast) = 20 (typ.)	—	—	1.6	V[p-p]
Y signal SN ratio	$SN_Y$	03 (contrast) = 3F (max.)	53	—	—	dB
Black level extension start point	$V_{BLS}$	Start point at $V_{48} = 4.5 \text{ V}$	37	42	47	IRE
Video output with $V_{CC}$ fluctuation	$\Delta V_{Y/V}$	$V_{CC1} = 9 \text{ V}$ (allowance: $\pm 10\%$ )	—	—	$\pm 15$	%
Video output-temperature characteristics	$\Delta V_{Y/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	—	—	$\pm 10$	%
ACL start point	$V_{ACL}$	$V_{20}$ at which output amplitude becomes 90% when ACL pin ( $V_{20}$ ) is decreased from 5 V	3.4	3.7	4.0	V
Color signal processing circuit Burst 150 mV[p-p] (PAL), reference is B-out						
Demodulation output residual carrier	$V_{CAR1}$	$2 f_{SC}$ level of pin 60 and pin 61	—	—	30	mV
Color difference output residual carrier	$V_{CAR2}$	$2 f_{SC}$ level of pin 15, pin 16, and pin 17	—	—	50	mV
VCO free-running frequency (PAL)	$f_{CP}$	Difference from $f = 4.433619 \text{ MHz}$	-300	—	300	Hz
VCO free-running frequency (NTSC)	$f_{CN}$	Difference from $f = 3.579545 \text{ MHz}$	-300	—	300	Hz
$f_{CO}$ fluctuation with $V_{CC}$	$\Delta f_C/V_{CC}$	$V_{CC1} = 9 \text{ V}$ (allowance: $\pm 10\%$ ), $V_{CC3} = 5 \text{ V}$ (allowance: $\pm 10\%$ )	-300	—	300	Hz
Static phase error (PAL)	$\Delta\theta_P$	Tint shift, when $\Delta f_C = -300 \text{ Hz}$ to $+300 \text{ Hz}$ change	—	—	5	deg/ 100 Hz
Static phase error (NTSC)	$\Delta\theta_N$	Tint shift, when $\Delta f_C = -300 \text{ Hz}$ to $+300 \text{ Hz}$ change	—	—	5	deg/ 100 Hz
PAL/NTSC	$R_{P/N}$	Output amplitude ratio between PAL and NTSC	0.7	1.0	1.3	Times
Line crawling	$\Delta V_{PAL}$	Pin 61: Output amplitude difference per 1H for - (R-Y) pin	—	—	50	mV
Color difference output bandwidth	$f_{CC}$	Band to become -3 dB	1.0	—	—	MHz

## ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

### • Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing circuit (continued) Burst 150 mV[p-p] (PAL), reference is B-out						
Color-difference output fluctuation with $V_{CC}$	$\Delta V_{C/V}$	$V_{CC1} = 9\text{ V}$ (allowance: $\pm 10\%$ ), $V_{CC3} = 5\text{ V}$ (allowance: $\pm 10\%$ )	—	—	$\pm 15$	%
Color-difference output temperature characteristics	$\Delta V_{C/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	—	—	$\pm 15$	%
PAL/NTSC output impedance	$R_{O60,61PN}$	DC measurement	390	480	570	$\Omega$
SECAM output impedance	$R_{O60,61S}$	DC measurement	100	—	—	$\text{k}\Omega$
Color/B&W DC difference voltage	$\Delta V_{CBW}$	Pedestal level DC difference, when burst signal with or without	-60	0	60	mV
(C-Y)/Y	$R_{C/Y}$	Color bar input, B-out Contrast typ., color data 00 = 30	0.9	1.2	1.5	$V[0-p]/V[0-p]$
RGB processing circuit						
$Y_S$ changeover speed	$f_{YS}$	$f_{YS}$ , when $Y_S$ input is 3 V[0-p], output level -3 dB	7	—	—	MHz
External RGB input dynamic range	$V_{DEXT}$	Contrast max., data 03 = 3F	1.0	—	—	V[p-p]
Internal/external crosstalk	$CT_{RGB}$	Leakage, when $f = 1\text{ MHz}$ , 1 V[p-p], $Y_S = 5\text{ V}$	—	—	-50	dB
Synchronizing signal processing circuit						
Lock detection output voltage	$V_{LD}$	$V_{18}$ , when horizontal AFC lock	5.7	6.3	6.9	V
Lock detection charge and discharge current	$I_{LD}$	DC measurement	$\pm 0.6$	$\pm 0.8$	$\pm 1.1$	mA
EBP (RGB) slice level	$V_{FBP}$	Minimum voltage of pin 50, when blanking is applied to RGB output	0.4	0.75	1.1	V
EBP (AFC2) slice level	$V_{FBPH}$	Minimum voltage of pin 50 at which AFC2 operates	1.5	1.9	2.3	V
Horizontal AFC $\mu$	$\mu_H$	DC measurement	30	37	44	$\mu\text{A}/\mu\text{s}$
Horizontal VCO $\beta$	$\beta_H$	$\beta$ curve gradient near $f = 15.75\text{ kHz}$	1.4	1.9	2.4	$\text{Hz}/\text{mV}$
Burst gate pulse position	$P_{BGP}$	For both PAL/NTSC, delay from H. sync. rise	0.2	0.4	0.6	$\mu\text{s}$
PAL burst gate pulse width	$W_{BGPP}$		3.4	4.0	4.6	$\mu\text{s}$
NTSC burst gate pulse width	$W_{BGPN}$		2.5	3.0	3.5	$\mu\text{s}$
Burst gate pulse output voltage	$V_{BGP}$	DC voltage of pin 62 in BGP period	4.5	4.7	4.9	V
H blanking pulse output voltage	$V_{HBLK}$	DC voltage in H-blanking pulse period of pin 62	2.1	2.4	2.7	V
V blanking pulse output voltage	$V_{VBLK}$	DC voltage in V-blanking pulse period of pin 62	2.1	2.4	2.7	V
PAL V blanking pulse width	$W_{VP}$	Pulse width at $f = 15.625\text{ kHz}$	1.31	1.41	1.51	ms
NTSC blanking pulse width	$W_{VN}$	Pulse width at $f = 15.75\text{ kHz}$	1.01	1.11	1.21	ms
FBP allowable range	$T_{FBP}$	Time from H-out rise to FBP center	12	—	19	$\mu\text{s}$

## ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

### • Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Synchronizing signal processing circuit (continued)						
FBP max. allowable input voltage	$V_{AFBP}$		2.5	—	5.0	V
I <sup>2</sup> C Interface						
Bus free before start	$t_{BUF}$		4.0	—	—	$\mu\text{s}$
Start condition set-up time	$t_{SU,STA}$		4.0	—	—	$\mu\text{s}$
Start condition hold time	$t_{HD,STA}$		4.0	—	—	$\mu\text{s}$
Low period SCL, SDA	$t_{LOW}$		4.0	—	—	$\mu\text{s}$
High period SCL	$t_{HIGH}$		4.0	—	—	$\mu\text{s}$
Rise time SCL, SDA	$t_r$		—	—	1.0	$\mu\text{s}$
Fall time SCL, SDA	$t_f$		—	—	0.35	$\mu\text{s}$
Data set-up time (write)	$t_{SU,DAT}$		0.25	—	—	$\mu\text{s}$
Data hold time (write)	$t_{HD,DAT}$		0	—	—	$\mu\text{s}$
Acknowledge set-up time	$t_{SU,ACK}$		—	—	3.5	$\mu\text{s}$
Acknowledge hold time	$t_{HD,ACK}$		0	—	—	$\mu\text{s}$
Stop condition set-up time	$t_{SU,STO}$		4.0	—	—	$\mu\text{s}$
DAC						
3, 6, 7-bit DAC DNLE	$L_{3,6,7}$	$1\text{LSB} = \{\text{data (max.)} - \text{data (00)}\} / 7, 63, 127$	0.1	1.0	1.9	$\frac{\text{LSB}}{\text{Step}}$
8-bit DAC DNLE	$L_8$	$1\text{LSB} = \{\text{data (FF)} - \text{data (00)}\} / 255$ (except 7F $\rightarrow$ 80)	0.1	1.0	1.9	$\frac{\text{LSB}}{\text{Step}}$
8-bit DAC DNLE 80	$L_{8-80}$	$1\text{LSB} = \{\text{data (FF)} - \text{data (00)}\} / 255$ (7F $\rightarrow$ 80)	0.1	1.0	2.9	$\frac{\text{LSB}}{\text{Step}}$
AFT DAC overlap	$\Delta\text{Step}$	Overlap of AFT 8-bit 2-stage changeover	27	32	37	Step

### • Typical conditions when testing

#### 1. Input signal

- 1) VIF:  $f_p = 38.9\text{ MHz}$ ,  $V_{IN} = 90\text{ dB}\mu$

Video modulation : modulated signal is 10-staircase. Modulation  $m = 87.5\%$

$V_{IN} = 90\text{ dB}\mu$ , pin 25 input level approx.  $84\text{ dB}\mu$

- 2) SIF:  $f_s = 6.0\text{ MHz}$ ,  $V_{IN} = 90\text{ dB}\mu$ , modulated signal  $f_M = 400\text{ MHz}$ , deviation: PAL $\pm 50\text{ kHz}$ , NTSC $\pm 25\text{ kHz}$
- 3) Video: 10-stair-step  $0.6\text{ V[p-p]}$  ( $V_{BW} = 0.42\text{ V[0-p]}$ )
- 4) Chroma: Color bar signal: Burst level  $150\text{ mV[p-p]}$   
Rainbow signal: Burst level  $150\text{ mV[p-p]}$
- 5) Sync. signal:  $0.6\text{ V[p-p]}$

■ Electrical Characteristics (continued)

• Typical conditions when testing (continued)

2. I<sup>2</sup>C bus conditions: (PAL)

Sub Address	Data (H)
00	20
01	20
02	40
03	20
04	00
05	00
06	00
07	40
08	40
09	01
0A	20
0B	44
0C	C0

DAC typical condition

Color	Center
Tint	Center
Brightness	Center
Contrast	Center
Cut-off R	Minimum
Cut-off G	Minimum
Cut-off B	Minimum
Drive R, B	Center
Video output	Center
Picture center position	Center
AFT	Center
RF AGC	Center
VIF VCO	Center

SW typical condition

PAL mode

RF being inputted state (Video1 in, SIF1 in)

■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	DC (V)
1 2 3	<p>9 V (V<sub>CC1</sub>) 300 Ω 300 Ω 0.01 μF Pins 1,2,3 BGP 150 μA Brightness control</p>	<p>Pin 1: Primary color signal clamp pin (R): Pin 2: Primary color signal clamp pin (G): Pin 3: Primary color signal clamp pin (B):</p> <ul style="list-style-type: none"> <li>Clamp pulse uses internal clamp pulse (BGP)</li> </ul>	<p>DC approx. 7 V</p>
4	<p>5 V (V<sub>CC3</sub>) 3.3 V 1 V 2.5 V 9 V 137 kΩ 270 Ω 1.0 MΩ 0.47 μF Killer det. circuit BGP 2.8 V 100 μA</p>	<p>Killer filter pin:</p> <ul style="list-style-type: none"> <li>Filter pin for killer detection circuit (operates for BGP period)</li> <li>Killer turns on (without color output) at 2.8 V or less</li> </ul>	<p>DC approx. 3.3 V</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC (V)
5		<p>Killer, 50 Hz/60 Hz and SECAM det. output pin:</p> <ul style="list-style-type: none"> <li>• Output selecting by SW (I<sup>2</sup>C bus)</li> <li>• Connect 33 kΩ load resistor of pin 5 to microcomputer V<sub>CC</sub></li> </ul>	<p>DC low-level 0.2 V high-level 5 V</p>
6		<p>Pin for APC filter:</p> <ul style="list-style-type: none"> <li>• Filter pin for APC detection circuit (operates for BGP period)</li> <li>• Detection sensitivity becomes large when external R → large (Tends to pull-in easily. Tends to be affected by noise)</li> </ul> <ul style="list-style-type: none"> <li>• At SECAM, APC circuit is stopped by short circuiting 40 kΩ resistor</li> </ul>	<p>DC approx. 2.5 V</p>
7 8		<p>Pin 7: Chroma oscillation pin (4.43 MHz): Pin 8: Chroma oscillation pin (3.58 MHz):</p> <ul style="list-style-type: none"> <li>• Oscillation pin for chroma. Either one of 4.43 MHz or 3.58 MHz is oscillated</li> <li>• Oscillation frequency changeover is performed by 08–D7 bit of I<sup>2</sup>C bus</li> <li>• At 08–D7=0 IP<sub>1</sub> and IP<sub>2</sub> turn-on and at 4.43 MHz, oscillation starts At 08–D7=1 IN<sub>1</sub> and IN<sub>2</sub> turn-on and at 3.58 MHz, oscillation starts</li> <li>• Pattern design of pin and oscillator element should be as short as possible.</li> </ul>	<p>AC f = f<sub>C</sub> approx. 0.7 V[p-p]</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC (V)
9		<p>Black level detection pin: Blanking off SW pin</p> <ul style="list-style-type: none"> <li>• Black level detection filter pin for black extension circuit</li> <li>• Holds the most black Y level except blanking period</li> <li>• Changes operating sensitivity (area judged as black) of black extension by external R</li> </ul> <p>Responds with small area when R goes large.</p> <ul style="list-style-type: none"> <li>• To stop the black extension, set pin 9 to <math>V_{CC}</math> (9 V).</li> <li>• Connected to GND, blanking comes off. (also the black extension is off)</li> </ul>	<p>DC approx. 5.1 V</p>
10		<p><math>Y_S</math> input pin:</p> <ul style="list-style-type: none"> <li>• Fast blanking pulse input pin for external analog RGB</li> <li>• Turns on at a voltage of 1 V[0-p] or more and off at 0.4 V[0-p] or less.</li> </ul>	<p>AC (Pulse)</p>
11 12 13		<p>Pin 11: External R input pin: Pin 12: External G input pin: Pin 13: External B input pin:</p> <ul style="list-style-type: none"> <li>• Output changes linearly according to input level.</li> </ul>	<p>AC</p>
14	<p>—</p>	<p><math>V_{CC1}</math> (typ. 9 V):</p> <ul style="list-style-type: none"> <li>• Output part of VIF and SIF circuit</li> <li>• AV SW circuit</li> <li>• Video circuit</li> <li>• RGB circuit</li> </ul>	<p>DC 9 V</p>
15 16 17		<p>Pin 15: R-out pin: Pin 16: G-out pin: Pin 17: B-out pin:</p> <ul style="list-style-type: none"> <li>• BLK level: Approx. 0.9 V</li> <li>• Black (pedestal) level: Approx. 2.2 V</li> <li>• Blanking can be released when pin 9 (black level detection pin) is set at 0 V.</li> </ul>	<p>AC</p>



■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC (V)
18		<p>Horizontal sync. detection pin:</p> <ul style="list-style-type: none"> <li>Phase of horizontal synchronizing signal and horizontal output pulse is detected and outputted.</li> <li>Pin 18 is low at out of phase.</li> <li>In asynchronous state, color control becomes min. and chroma output disappears.</li> <li>Pay attention to impedance when voltage of pin18 is used by micro-computer (<math>Z_O \geq 500 \text{ k}\Omega</math> is required)</li> </ul> <ul style="list-style-type: none"> <li>HV<sub>SYNC</sub> Period</li> <li>When pin 56 is high: I<sub>1</sub> on</li> <li>When pin 56 is low: I<sub>2</sub> on</li> </ul>	<p>DC</p> <p>at synchronous approx. 6 V</p> <p>at asynchronous approx. 0.3 V</p>
19	<p>—</p>	<p>GND:</p> <ul style="list-style-type: none"> <li>RGB circuit</li> <li>DAC I<sup>2</sup>C circuit</li> </ul>	<p>—</p>
20		<p>ACL pin:</p> <ul style="list-style-type: none"> <li>Contrast can be reduced when DC voltage of pin 20 is decreased from the outside.</li> <li>Service SW</li> </ul> <p>Note) When pin 20 is used as ACL, set design must be done not to become <math>V_{20} &lt; 0.9 \text{ V}</math> so that pin 20 operates also as the service SW.</p>	<p>DC</p> <p>approx. 3 V</p>
21		<p>I<sup>2</sup>C bus data input pin:</p>	<p>AC (pulse)</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC (V)
22		I <sup>2</sup> C clock input pin:	AC (Pulse)
23	—	V <sub>CC3-1</sub> (typ. 5 V): • For VIF and SIF circuit	DC 5 V
24 25		Pin 24: VIF input pin-1: Pin 25: VIF input pin-2: • Input for VIF amp. and balanced input	AC f = f <sub>p</sub> DC level approx. 2.7 V
26	—	GND: • For VIF and SIF circuit	DC
27		RF AGC output pin: • Open collector output. Can be used at given bias (max. 12 V)	DC
28		Audio output pin:	AC 0 kHz to 20 kHz

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC (V)
29		<p>De-emphasis pin</p> <ul style="list-style-type: none"> <li>De-emphasis filter pin for sound detection signal.</li> <li>External C is the same for PAL and NTSC (internal impedance changes)</li> <li>PAL: <math>120\text{ k}\Omega/60\text{ k}\Omega \times 1\text{ }200\text{ pF} = 48\text{ }\mu\text{s}</math></li> <li>NTSC: <math>60\text{ k}\Omega \times 1\text{ }200\text{ pF} = 72\text{ }\mu\text{s}</math></li> </ul>	<p>AC</p> <p>0 kHz to 20 kHz</p>
30		<p>AFT output pin</p> <ul style="list-style-type: none"> <li>Center voltage offset should be adjusted by using bus.</li> <li>If AFT defeat SW is turned on (09 = 00), <math>V_{30}</math> comes to a value determined by the value of externally attached resistor dividing.</li> <li>AFT <math>\mu</math> is variable by impedance of externally attached resistor.</li> </ul>	<p>DC</p>
31		<p>External video input pin</p> <ul style="list-style-type: none"> <li>Input pin for external video signal. DC cut input.</li> <li>Typical 1 V[p-p]</li> </ul>	<p>AC</p> <p>1 V[p-p] (composite)</p> <p>DC approx. 2.0 V</p>
32		<p>Decoupling pin</p> <ul style="list-style-type: none"> <li>S curve inside IC is wide band but DC feedback is applied so that DC voltage of output signal becomes constant.</li> <li>DC level (typ. 4.5 V)</li> <li><math>f_s \rightarrow</math> high: <math>V_{32} \rightarrow</math> low</li> </ul>	<p>DC</p>
33		<p>SIF signal input pin</p> <ul style="list-style-type: none"> <li>Common use with DC input pin for sharpness control</li> <li>DC bias is applied from external (DC: 5 V to 7 V for sharpness control)</li> </ul>	<p>AC+DC</p> <p>AC</p> <p><math>f = f_s</math></p>



■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC (V)
41		<p>VIF detection output pin:</p> <ul style="list-style-type: none"> <li>Adjust to 2 V[p-p] by I<sup>2</sup>C bus (uses upper rank 4-bit of 0 A)</li> </ul>	<p>AC 2 V[p-p]</p>
42		<p>APC1 filter pin:</p> <ul style="list-style-type: none"> <li>Filter pin of VIF APC1 circuit</li> <li>VCO lock detection circuit is incorporated in the IC, and it changes over the time constant of APC filter.</li> <li>Lock: SW: 0 Unlock: SW: 1</li> </ul>	<p>DC approx. 2.5 V</p>
43		<p>VIF oscillation pin:</p> <ul style="list-style-type: none"> <li>Change the oscillation coil according to VIF frequency.</li> <li>Oscillation frequency is <math>\frac{1}{2} \times f_p</math></li> </ul>	<p>AC <math>f = f_p/2</math> approx. 0.7 V[p-p] DC level approx. 3.9 V</p>
44		<p>Video output pin:</p> <ul style="list-style-type: none"> <li>Int. video1, int. video2 or ext. video signal selected by AV SW is outputted.</li> </ul>	<p>AC 2 V[p-p]</p> <p>DC level approx. 4.5 V</p>
45		<p>Video input pin:</p> <ul style="list-style-type: none"> <li>Input pin of video signal (possible also for composite video)</li> <li>Typical input 0.6 V[p-p]</li> <li>Sync. top is clamped to 3.5 V</li> <li>Video signal should be inputted with low impedance.</li> </ul>	<p>AC 0.6 V[p-p]</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC (V)
46		<p>Vertical and horizontal sync. separation input pin:</p> <ul style="list-style-type: none"> <li>• Sync. top is clamped to 1.3 V.</li> </ul>	<p>AC</p> <p>2 V[p-p]</p>
47	—	<p><math>V_{CC3-2}</math> (typ. 5 V):</p> <ul style="list-style-type: none"> <li>• Chroma and Jungle circuit use</li> </ul>	<p>DC</p> <p>5 V</p>
48		<p>Chroma signal input pin:</p> <p>Black extension start point adjustment pin</p> <ul style="list-style-type: none"> <li>• Pin 48 is chroma signal input pin and black extension start point is adjusted by DC voltage applied externally.</li> </ul>	<p>AC+DC</p> <p>Burst typ.</p> <p>150 mV[p-p]</p> <p>DC typ.</p> <p>4.5 V</p>
49	—	<p>GND:</p> <p>Video, chroma and jungle circuit use</p>	<p>DC</p> <p>0 V</p>
50		<p>FBP input:</p> <ul style="list-style-type: none"> <li>• FBP input pin for horizontal blanking and APC circuit</li> <li>• Threshold level HBLK: 0.7 V AFC: 1.9 V</li> <li>• If DC 1.3 V is applied from outside, the state comes to all blanking</li> </ul>	<p>AC</p> <p>FBP</p>
51		<p>Horizontal stabilized power supply pin:</p> <ul style="list-style-type: none"> <li>• Stabilized power supply for horizontal circuit start up. Zener circuit is included inside.</li> </ul>	<p>DC</p> <p>6.3 V</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC (V)
52	<p>6.3 V (<math>V_{CC2}</math>) To hor. out <math>V_{52}</math> 1.9V 3.3V From DAC (hor. position) 2 k<math>\Omega</math> 2 k<math>\Omega</math> 1 k<math>\Omega</math> 1 k<math>\Omega</math> max. 500 <math>\mu</math>A 0.022 <math>\mu</math>F 50 <math>\mu</math>A</p>	<p>Horizontal AFC2 filter pin:</p> <ul style="list-style-type: none"> <li>• Pulse phase of FBP and IC inside are compared and capacitor connected to pin 52 is charged or discharged.</li> <li>• Screen center position adjustment is executed by charge or discharge of DC current with DAC.</li> <li>• According to the time from H-out to FBP-in, <math>V_{52}</math> is changed, and slice level of inside saw-tooth waveform is changed.</li> </ul>	<p>DC 1.5 V to 3.5 V</p>
53	<p>6.3 V (<math>V_{CC2}</math>) 4.3 V 27 k<math>\Omega</math> R1 27 k<math>\Omega</math> 1.5 V Hor. sync. 22 <math>\mu</math>F C2 820 <math>\Omega</math> R2 200 <math>\mu</math>A 0.033 <math>\mu</math>F C1 1 000 <math>\mu</math>A Hor. OSC <math>f_H</math> Horizontal <math>\beta</math> curve <math>V_{53}</math></p>	<p>Horizontal AFC1 filter pin:</p> <ul style="list-style-type: none"> <li>• Pulse phase of horizontal sync. signal and IC inside are compared and capacitor connected to pin 53 is charged or discharged.</li> <li>• R1, R2, C1 and C2 are lag-lead filters for AFC1</li> </ul>	<p>DC typ. 4.3 V</p>
54	<p>6.3 V (<math>V_{CC2}</math>) 22 k<math>\Omega</math> 300 <math>\Omega</math> 100 <math>\mu</math>A 200 <math>\mu</math>A 10 k<math>\Omega</math> 10 k<math>\Omega</math> 80 <math>\mu</math>A 220 pF</p>	<p>Horizontal oscillation pin:</p> <ul style="list-style-type: none"> <li>• Oscillation is done at <math>32 \times f_H \cong 503</math> kHz by ceramic resonator.</li> <li>• Horizontal and vertical pulse are made by count-down circuit of IC inside.</li> </ul>	<p>AC <math>f = 32 f_H</math> (approx. 503 kHz)</p>
55	<p>6.3 V (<math>V_{CC2}</math>) 4.3 V 20 k<math>\Omega</math> 20 k<math>\Omega</math> 40 k<math>\Omega</math> 3 V To count down 20 k<math>\Omega</math></p>	<p>Overvoltage protection input pin:</p> <ul style="list-style-type: none"> <li>• Input pin for protection circuit against X-ray caused by overvoltage.</li> <li>• Shut-down is started by inside logic circuit when H-out is low. (break-down protection of horizontal drive <math>T_R</math>)</li> </ul>	<p>DC Normally 0 V</p>
56	<p>6.3 V (<math>V_{CC2}</math>) 4.3 V 19 k<math>\Omega</math> 50 <math>\Omega</math> 10 k<math>\Omega</math> 40 k<math>\Omega</math> 2.8 V 0 V Hor. out</p>	<p>Horizontal pulse output pin:</p> <ul style="list-style-type: none"> <li>• Pulse duty approx. 36%</li> </ul>	<p>AC Pulse</p>

■ Terminal Equivalent Circuits (continued)

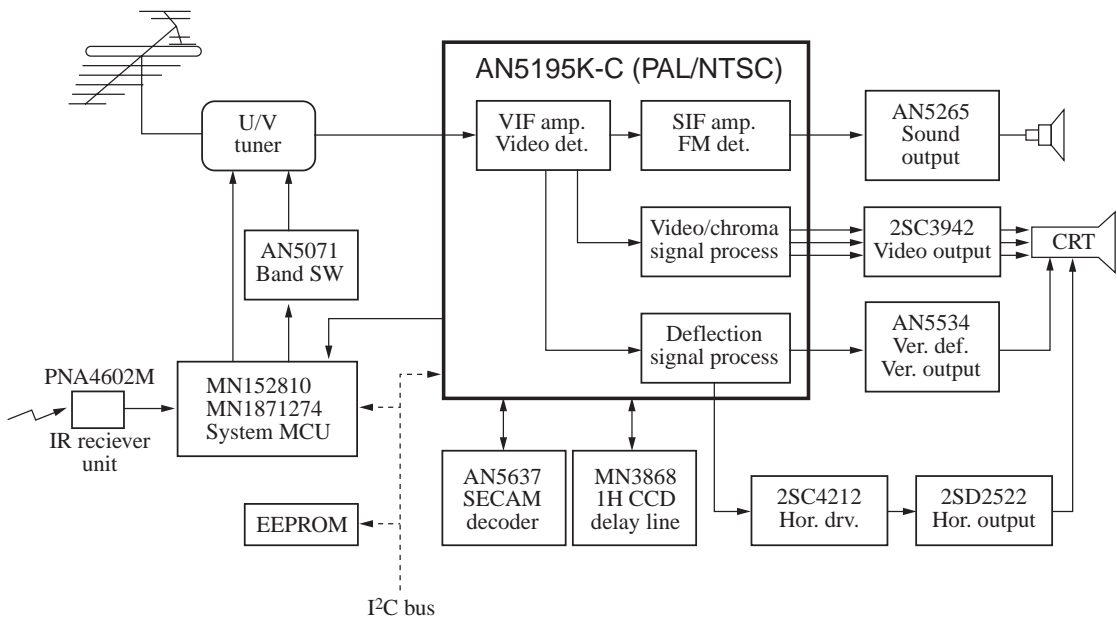
Pin No.	Equivalent circuit	Description	DC (V)
57		<p>Vertical sync. signal clamp pin:</p> <ul style="list-style-type: none"> <li>• Peak clamp pin in order to separate vertical sync. signal</li> <li>• Integrating amount of vertical sync. signal itself is determined by time constant of inside but triggering timing is determined by selecting R1 and C1 of external time constant.</li> <li>• Uses with R1 &gt; 200 kΩ</li> <li>• R2 is for emitter current limiting resistor</li> </ul>	<p>AC</p> <p><math>f = f_V</math></p>
58		<p>Vertical pulse output pin:</p> <ul style="list-style-type: none"> <li>• Negative polarity, pulse width 10 H</li> </ul>	<p>AC</p> <p>Pulse</p>
59		<p>SECAM interface pin:</p> <ul style="list-style-type: none"> <li>• Inpu/output pin for interface with SECAM IC</li> <li>• SECAM mode is made by taking the curr. of 100 μA or more from pin 59.</li> <li>• At SECAM DC4.4 V+AC250 mV[p-p]</li> <li>• At non-SECAM DC1.1 V+AC250 mV[p-p]: 4.43 MHz or 0 mV[p-p]: 3.58 MHz</li> </ul>	<p>AC+DC</p> <p>AC</p> <p>250 mV[p-p]</p> <p>or</p> <p>0 mV[p-p]</p> <p>DC</p> <p>4.4 V</p> <p>or</p> <p>1.1 V</p>
60		<p>Pin 60: -(B-Y) output pin:</p> <p>Pin 61: -(R-Y) output pin:</p> <ul style="list-style-type: none"> <li>• At SECAM, output circuit is off and comes to high impedance.</li> <li>• Output to IHDL</li> </ul>	<p>AC</p> <p>-(B-Y)</p> <p>-(R-Y)</p> <p>DC level approx. 2.1 V</p>
62		<p>Sandcastle pulse output pin:</p> <ul style="list-style-type: none"> <li>• Sandcastle pulse is outputted to IHDL and SECAM IC.</li> </ul>	<p>AC</p> <p>Pulse</p> <p>4.7 V</p> <p>2.4 V</p>



■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC (V)
63 64		<p>Pin 63: -(B-Y) input pin: Pin 64: -(R-Y) input pin:</p> <ul style="list-style-type: none"> <li>Input color difference signal from IHDL output .</li> <li>Pedestal level is clamped to 4 V by clamp circuit.</li> </ul>	<p>AC -(B-Y) -(R-Y) DC level 4 V</p>

■ System Application Example



Application Circuit Example

