SONY

CXP80712B/80716B/80720B/80724B

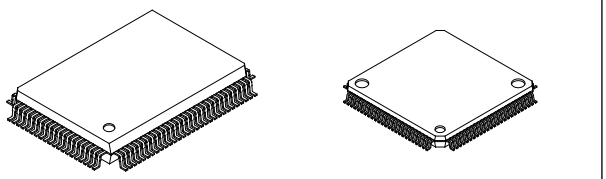
CMOS 8-bit Single Chip Microcomputer

Description

The CXP80712B/80716B/80720B/80724B is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, high precision timing pattern generation circuit, PWM output, VISS/VASS circuit, 32kHz timer/counter, remote control receiving circuit, VSYNC separator and the measurement circuit which measures signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also CXP80712B/80716B/80720B/80724B provides sleep/stop function which enables to lower power consumption.

100 pin QFP (PIastic) 100 pin LQFP (PIastic)



Structure

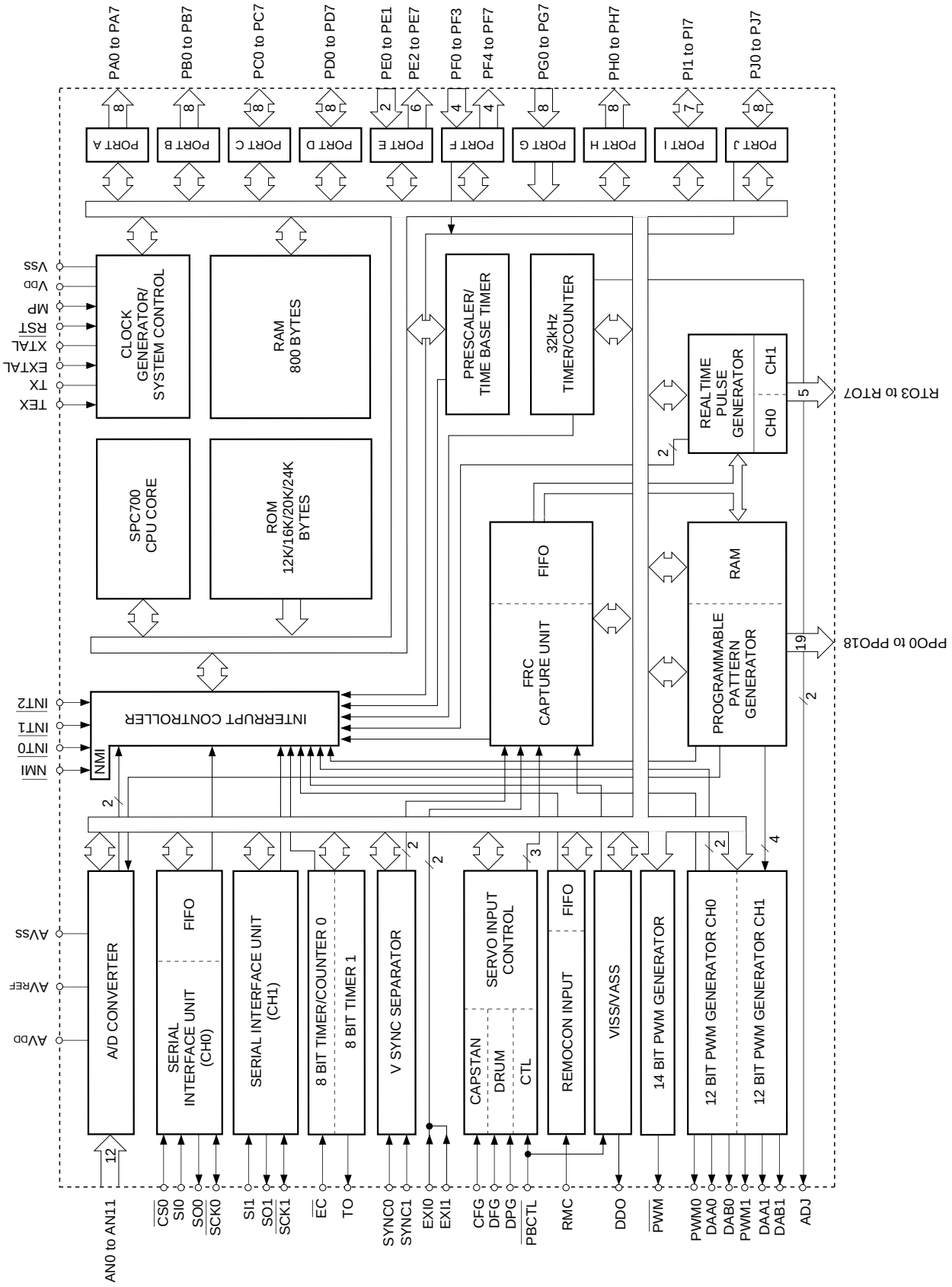
Silicon gate CMOS IC

Features

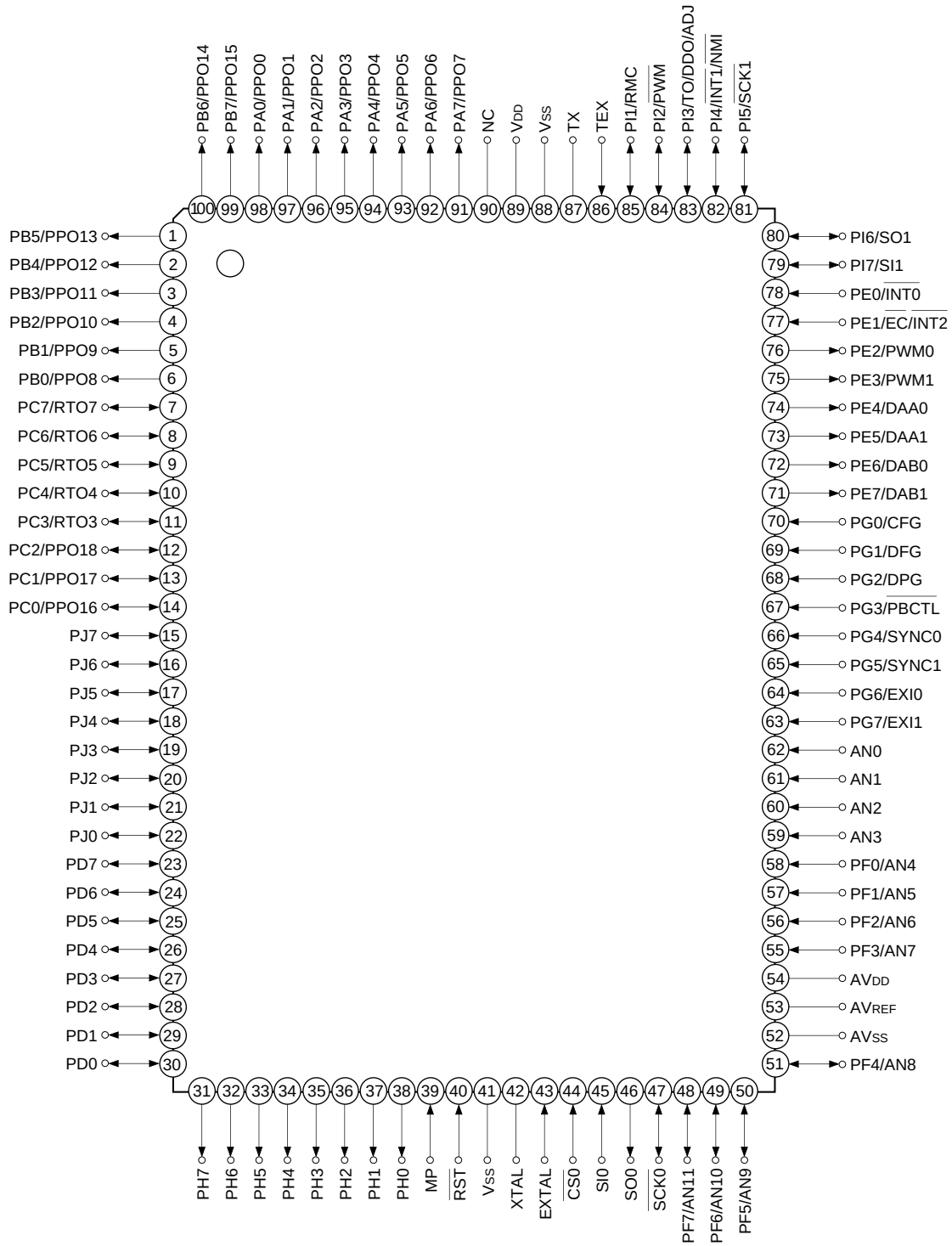
- A wide instruction set (213 instructions) which cover various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle 250ns at 16MHz operation
  122µs at 32kHz operation
- Incorporated ROM capacity 12K bytes (CXP80712B)
  16K bytes (CXP80716B)
  20K bytes (CXP80720B)
  24K bytes (CXP80724B)
- Incorporated RAM capacity 800 bytes
- Peripheral functions
  - — A/D converter: 8 bits, 12 channels, successive approximation system (Conversion time of 20.0µs/16MHz)
  - — Serial Interface: Incorporated 8-bit and 8-stage FIFO, 1 channel (1 to 8 bytes auto transfer)
    8-bit serial I/O, 1 channel
  - — Timer: 8-bit timer
    8-bit timer/counter
    19-bit time base timer
    32kHz timer/counter
  - — High precision timing pattern generator: PPG for 19 pins, 32-stage programmable
    RTG for 5 pins, 2 channels
  - — PWM/DA gate output: 12 bits, 2 channels (Repetitive frequency of 62.5kHz/16MHz)
  - — Servo input control: Capstan FG, Drum FG/PG, CTL input
  - — VSYNC separator
  - — FRC capture unit: Incorporated 26-bit and 8-stage FIFO
  - — PWM output: 14 bits, 1 channel
  - — VISS/VASS circuit: Pulse duty auto detection circuit
  - — Remote control receiving circuit: 8-bit pulse measurement counter, 6-stage FIFO
- Interruption: 21 factors, 15 vectors, multi-interruption possible
- Standby mode: SLEEP/STOP
- Package: 100-pin plastic QFP/LQFP
- Piggyback/evaluation chip: CXP87700 100-pin ceramic PQFP

E95Z43A71

Block Diagram

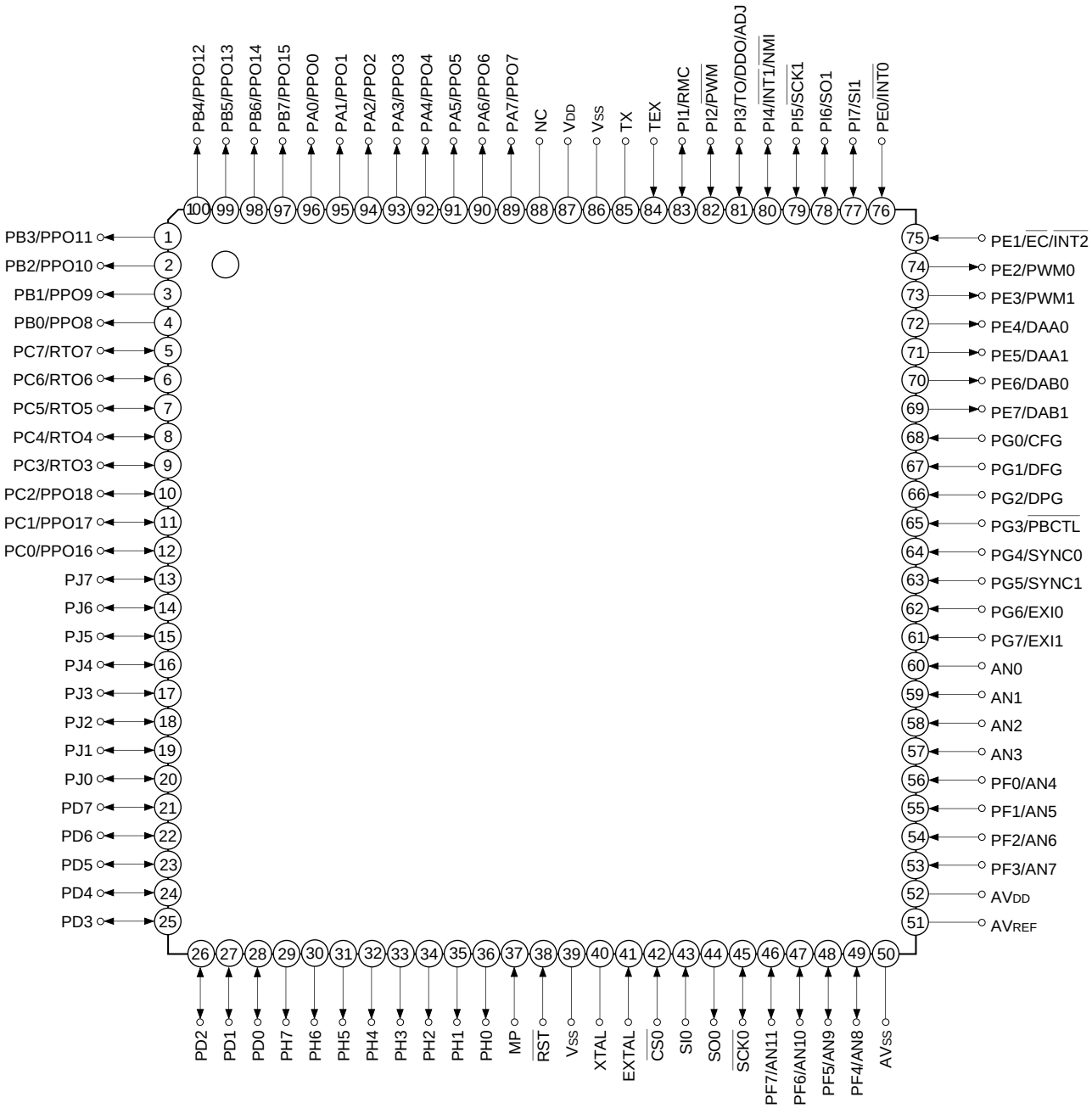


Pin Assignment 1 (Top View) 100 pin QFP package



Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. Vss (Pins 41 and 88) are both connected to GND.
3. MP (Pin 39) is always connected to GND.

Pin Assignment 2 (Top View) 100 pin LQFP package



Note) 1. NC (Pin 88) is always connected to V_{DD}.
2. Vss (Pins 39 and 86) are both connected to GND.
3. MP (Pin 37) is always connected to GND.

Pin Description

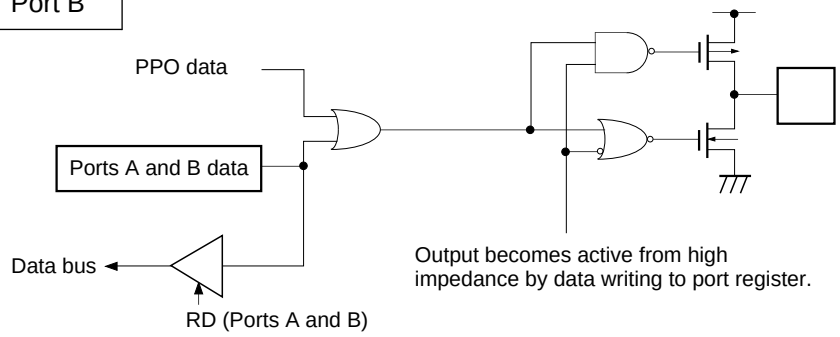
Symbol	I/O	Description	
PA0/PPO0 to PA7/PPO7	Output/ Real-time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port. (19 pins)
PB0/PPO8 to PB7/PPO15	Output/ Real-time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	
PC0/PPO16 to PC2/PPO18	I/O/ Real-time output	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)	
PC3/RTO3 to PC7/RTO7	I/O/ Real-time output		Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins)
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of 4 bits. Can 12mA sink current. (8 pins)	
PE0/$\overline{\text{INT0}}$	Input/Input	(Port E) 8-bit port. Lower 2 bits are for inputs; upper 6 bits are for outputs. (8 pins)	Input pin to request external interruption. Active when falling edge.
PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$	Input/Input/Input		External event input pin for timer/counter. / Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/Output		PWM output pins. (2 pins)
PE3/PWM1	Output/Output		
PE4/DAA0	Output/Output		DA gate pulse output pins. (4 pins)
PE5/DAA1	Output/Output		
PE6/DAB0	Output/Output		
PE7/DAB1	Output/Output		
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)	
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are for inputs; upper 4 bits are for outputs. Lower 4 bits also serve as standby release input pin. (8 pins)	
PF4/AN8 to PF7/AN11	Output/Input		
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.	
SO0	Ouput	Serial data (CH0) output pin.	
SI0	Input	Serial data (CH0) input pin.	
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.	

Symbol	I/O	Description	
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.
PG1/DFG	Input/Input		Drum FG input pin.
PG2/DPG	Input/Input		Drum PG input pin.
PG3/$\overline{\text{PBCTL}}$	Input/Input		Playback CTL pulse input pin.
PG4/SYNC0	Input/Input		Composite sync signal input pin. (2 pins)
PG5/SYNC1	Input/Input		
PG6/EXI0	Input/Input		External input pin to FRC capture unit. (2 pins)
PG7/EXI1	Input/Input		
PH0 to PH7	Output	(Port H) 8-bit output port; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be set in a unit of single bits. (7 pins)	Remote control receiving circuit input pin.
PI2/$\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.
PI3/TO/ DDO/ADJ	I/O/Output/ Output/Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.
PI4/$\overline{\text{INT1}}$/ $\overline{\text{NMI}}$	I/O/Input/Input		Input pin to request external interruption and non maskable interruption. Active when falling edge.
PI5/$\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/Output		Serial data (CH1) output pin.
PI7/SI1	I/O/Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be set in a unit of single bits. I/O can be set in a unit of single bits.	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
$\overline{\text{RST}}$	Input	System reset pin of active Low level.	
MP	Input	Test mode input pin. Always connect to GND.	
AV_{DD}		Positive power supply pin of A/D converter.	
AV_{REF}	Input	Reference voltage input pin of A/D converter.	
AVss		GND pin of A/D converter.	
V_{DD}		Positive power supply pin.	
NC		NC pin. Connect this pin to V_{DD} for normal operation.	
Vss		GND pin. Connect both Vss pins to GND.	

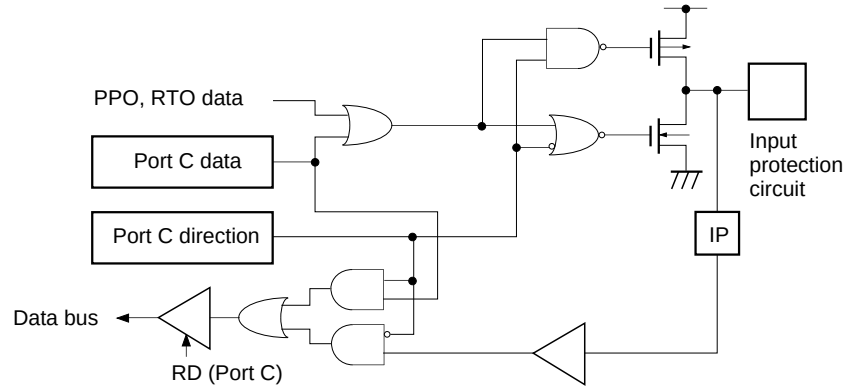
Input/Output Circuit Formats for Pins

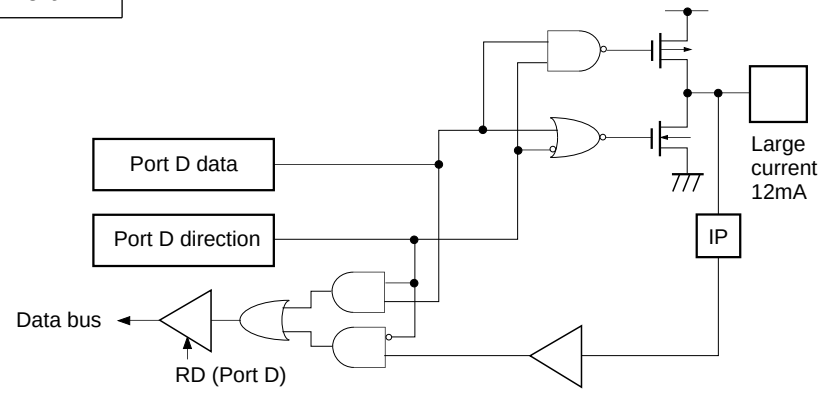
<table>
<tr><th>Pin</th><th>Circuit format</th><th>When reset</th></tr>
<tr><td>PA0/PPO0
to
PA7/PPO7

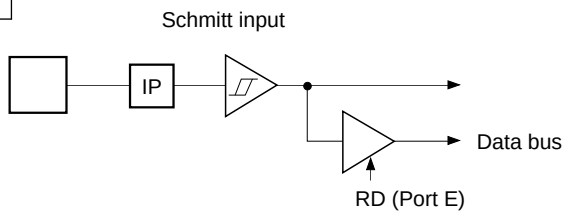
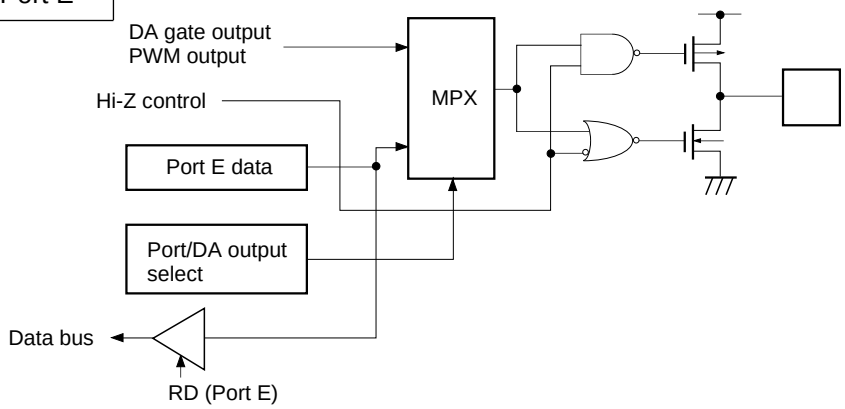
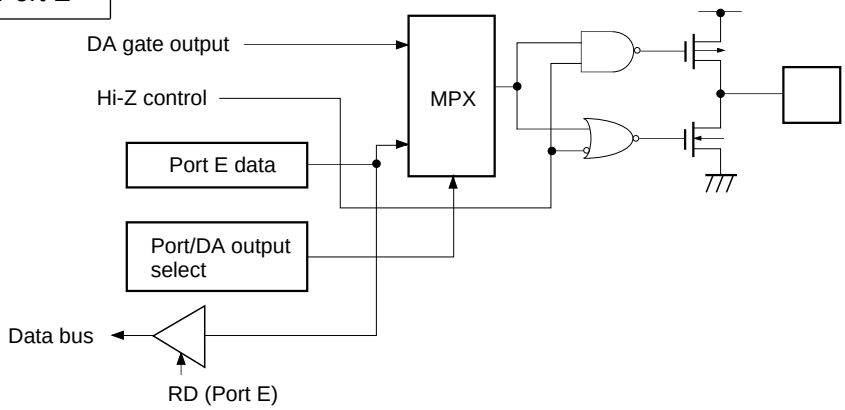
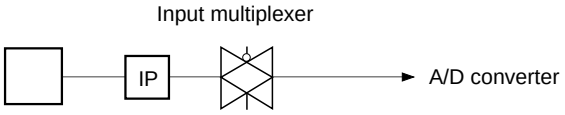
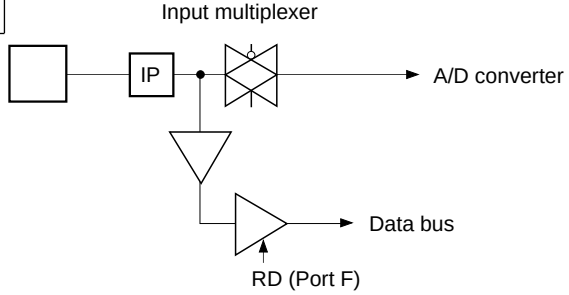
PB0/PPO8
to
PB7/PPO15

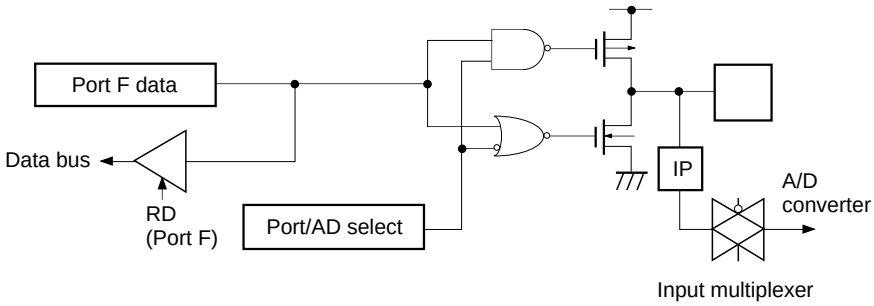
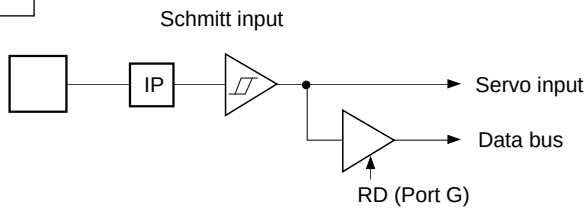
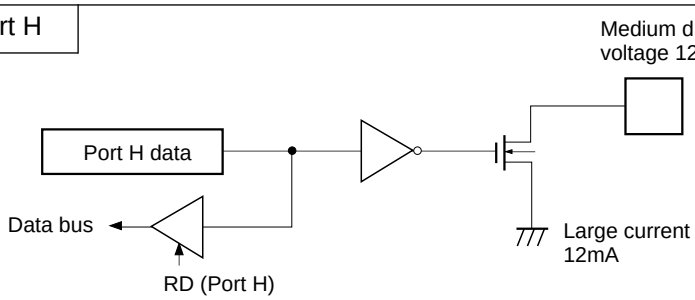
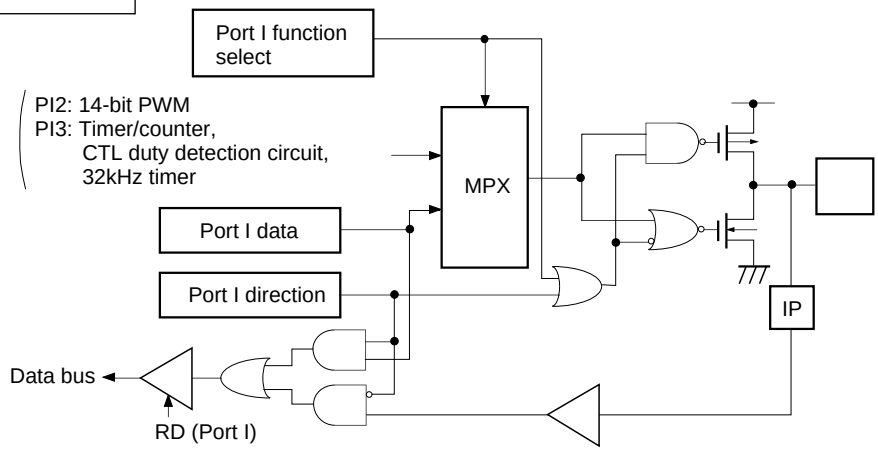
16 pins</td><td>Port A
Port B
 
</td><td>Hi-Z</td></tr>
<tr><td>PC0/PPO16
to
PC2/PPO18

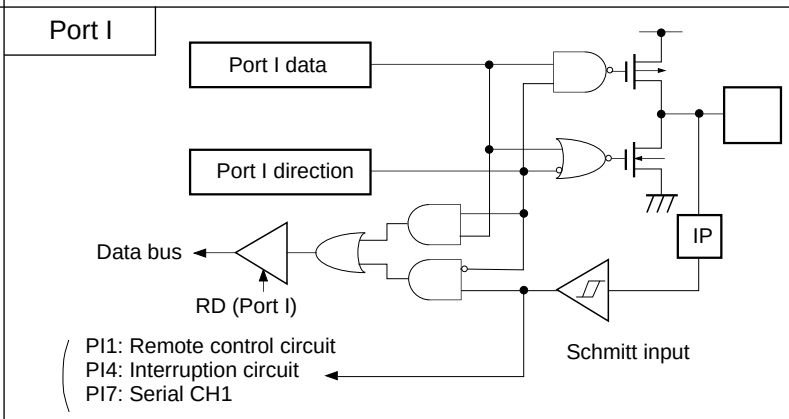
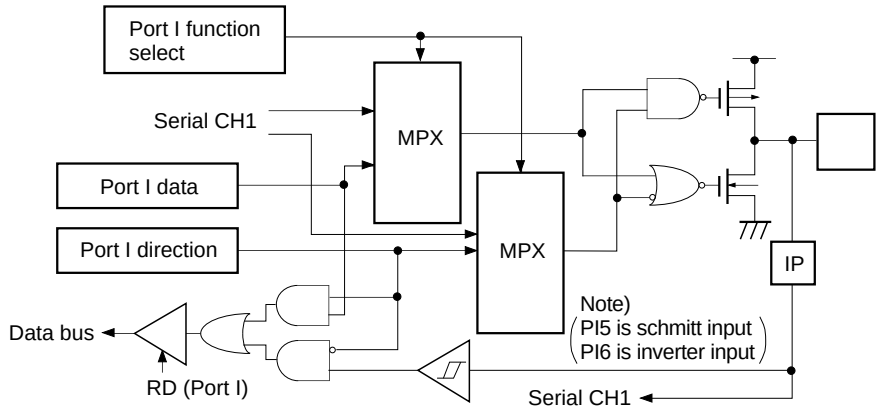
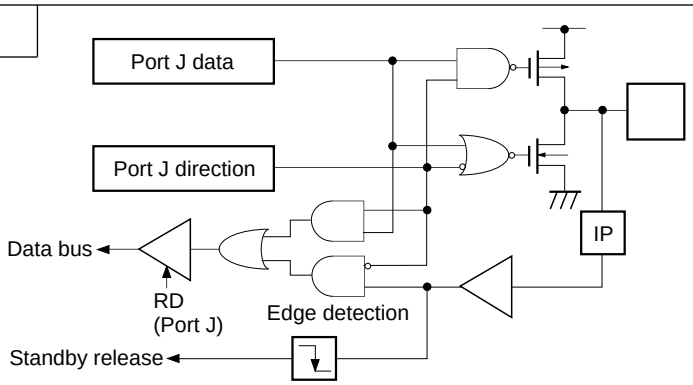
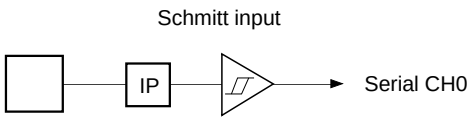
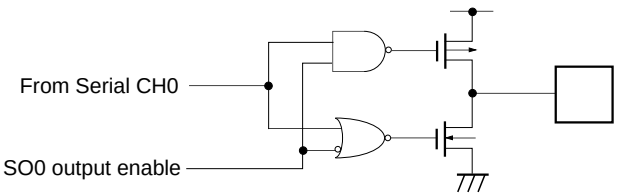
PC3/RTO3
to
PC7/RTO7

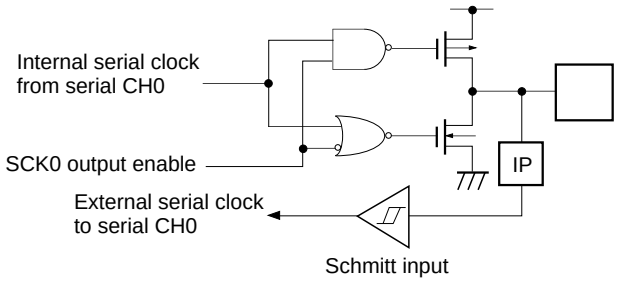
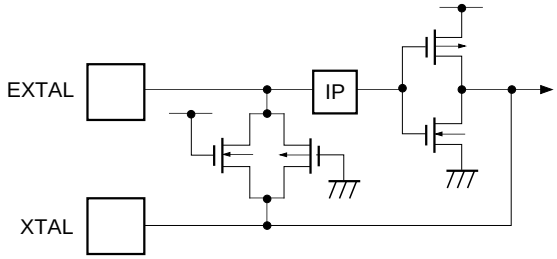
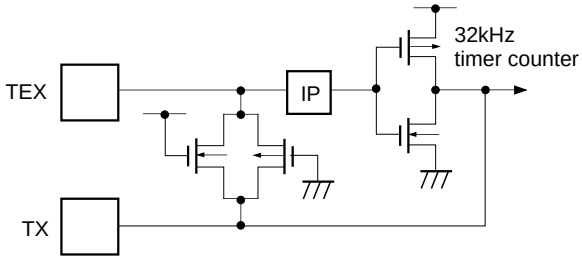
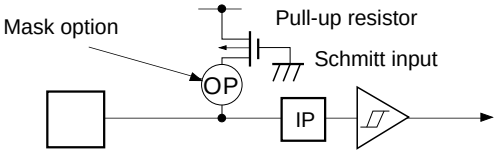
8 pins</td><td>Port C
 
</td><td>Hi-Z</td></tr>
<tr><td>PD0
to
PD7

8 pins</td><td>Port D
 
</td><td>Hi-Z</td></tr>
</table>

Pin	Circuit format	When reset
PE0/$\overline{INT0}$ PE1/$\overline{EC}$/$\overline{INT2}$ 2 pins	Port E 	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E 	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E 	High level
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z

Pin	Circuit format	When reset
PF4/AN8 to PF7/AN11 4 pins	Port F 	Hi-Z
PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1 8 pins	Port G  Note) For PG4/SYNC0 and PG5/SYNC1, CMOS schmitt input or TTL schmitt input can be selected with the mask option.	Hi-Z
PH0 to PH7 8 pins	Port H 	Hi-Z
PI2/PWM PI3/TO/ DDO/ADJ 2 pins	Port I 	Hi-Z

PIn	Circuit format	When reset
PI1/RMC PI4/$\overline{INT1}$/$\overline{NMI}$ PI7/SI1 3 pins	Port I 	Hi-Z
PI5/$\overline{SCK1}$ PI6/SO1 2 pins	Port I 	Hi-Z
PJ0 to PJ7 8 pins	Port J 	Hi-Z
$\overline{CS0}$ SI0 2 pins		Hi-Z
SO0 1 pin		Hi-Z

PIn	Circuit format	When reset
$\overline{\text{SCK0}}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed and XTAL becomes High level during stop.	Oscillation
TEX TX 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs Low level and TX pin outputs High level.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	AV_{DD}	AVss to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Medium drive output voltage	V_{OUTP}	–0.3 to +15.0	V	Port H (PH)
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than large current output port (value per pin)
	I_{OLC}	20	mA	Large current port*2 (value per pin)
Low level total output current	$\sum I_{OL}$	130	mA	Total of output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package type
		380		LQFP package type

*1 AV_{DD}, V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The large current output ports are Port D (PD) and Port H (PH).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for 1/2, 1/4 frequency dividing clock
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or during SLEEP mode.
		2.7	5.5	V	Guaranteed operation range by TEX clock
		2.5	5.5	V	Guaranteed data hold operation range during STOP
Analog power supply	AV_{DD}	4.5	5.5	V	*1
HIgh level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*2
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	CMOS schmitt input*3
	V_{IHTS}	2.2	V_{DD}	V	TTL schmitt input*4
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL pin*5 TEX pin*6
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	*2
	V_{ILS}	0	$0.2V_{DD}$	V	CMOS schmitt input*3
	V_{ILTS}	0	0.8	V	TTL schmitt input*4
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*5 TEX pin*6
Operating temperature	Topr	–20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to the same voltage.

*2 Normal input port (each pin of PC, PD, PE0, PE1, PF0 to PF3, PG, PI and PJ), MP pin.

*3 Each pin of $\overline{CS0}$, SI0, $\overline{SCK0}$, $\overline{RST}$, PE0/$\overline{INT0}$, PE1/$\overline{EC}$/$\overline{INT2}$, PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option), PI1/RMC, PI4/$\overline{INT1}$/$\overline{NMI}$, PI5/$\overline{SCK1}$ and PI7/SI1.

*4 Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

*5 Specifies only during external clock input.

*6 Specifies only during event count clock input.

Electrical Characteristics

DC Characteristics

(Ta = –20 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only) PI1 to PI7, PJ, SO0, SCK0	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*1		–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, $\overline{CS0}$, SI0, SO0 $\overline{SCK0}$, $\overline{RST}$*1	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-CH Tr off state)	I_{LOH}	PH	V_{DD} = 5.5V V_{OH} = 12V			50	µA
Supply current*2	I_{DD1}	V_{DD}	16MHz crystal oscillation (C_1 = C_2 = 15pF), V_{DD} = 5.5V		20	45	mA
	I_{DDS1}		16MHz crystal oscillation (C_1 = C_2 = 15pF), V_{DD} = 5.5V, SLEEP mode		1.1	8	mA
	I_{DD2}		32kHz crystal oscillation (C_1 = C_2 = 47pF), V_{DD} = 3.3V		35	100	µA
	I_{DDS2}		32kHz crystal oscillation (C_1 = C_2 = 47pF), V_{DD} = 3.3V, SLEEP mode		7	30	µA
	I_{DDS3}		V_{DD} = 5.5V, STOP mode (termination of 32kHz and 16MHz crystal oscillation)			10	µA
Input capacity	C_{IN}	PC, PD, PE0 to 1, PF0 to 3, PG, PI, PJ, AN, $\overline{SCK0}$, SI0, $\overline{CS0}$, EXTAL, XTAL, TEX, TX, $\overline{RST}$, MP	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 $\overline{RST}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when no resistance is selected.

*2 When entire output pins are open.

*3 When setting upper 2 bits (CPU clock selection) of clock control register (CLC: 00FE$_H$) to "00" and operating in high speed mode (1/2 frequency dividing clock).

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)	28			ns
System clock input rise and fall times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)			200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	4tsys*1			ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ns
System clock frequency	f_C	TEX TX	Fig. 2 V_{DD} = 2.7 to 5.5V (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1 tsys indicates three values according to the contents of the clock control register (CLC; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

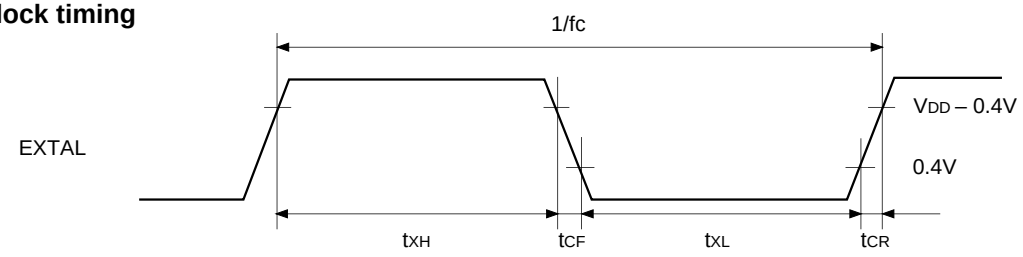


Fig. 2. Clock applied condition

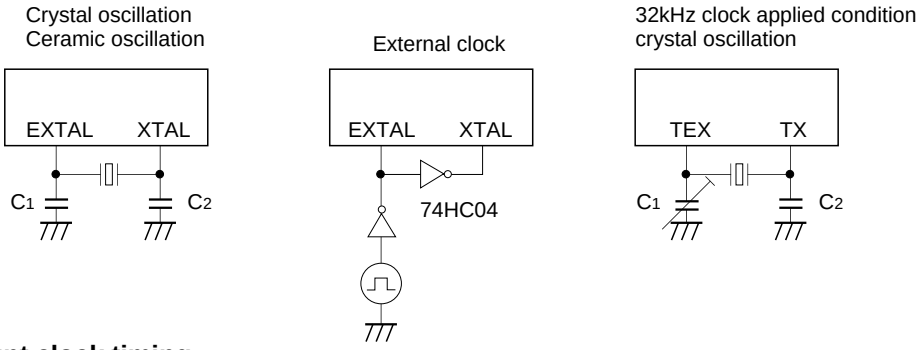
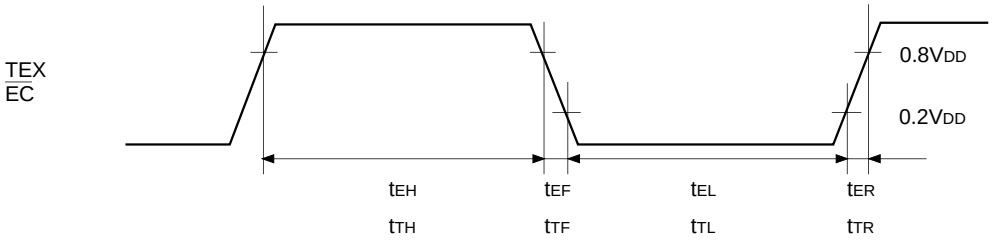


Fig. 3. Event count clock timing



(2) Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

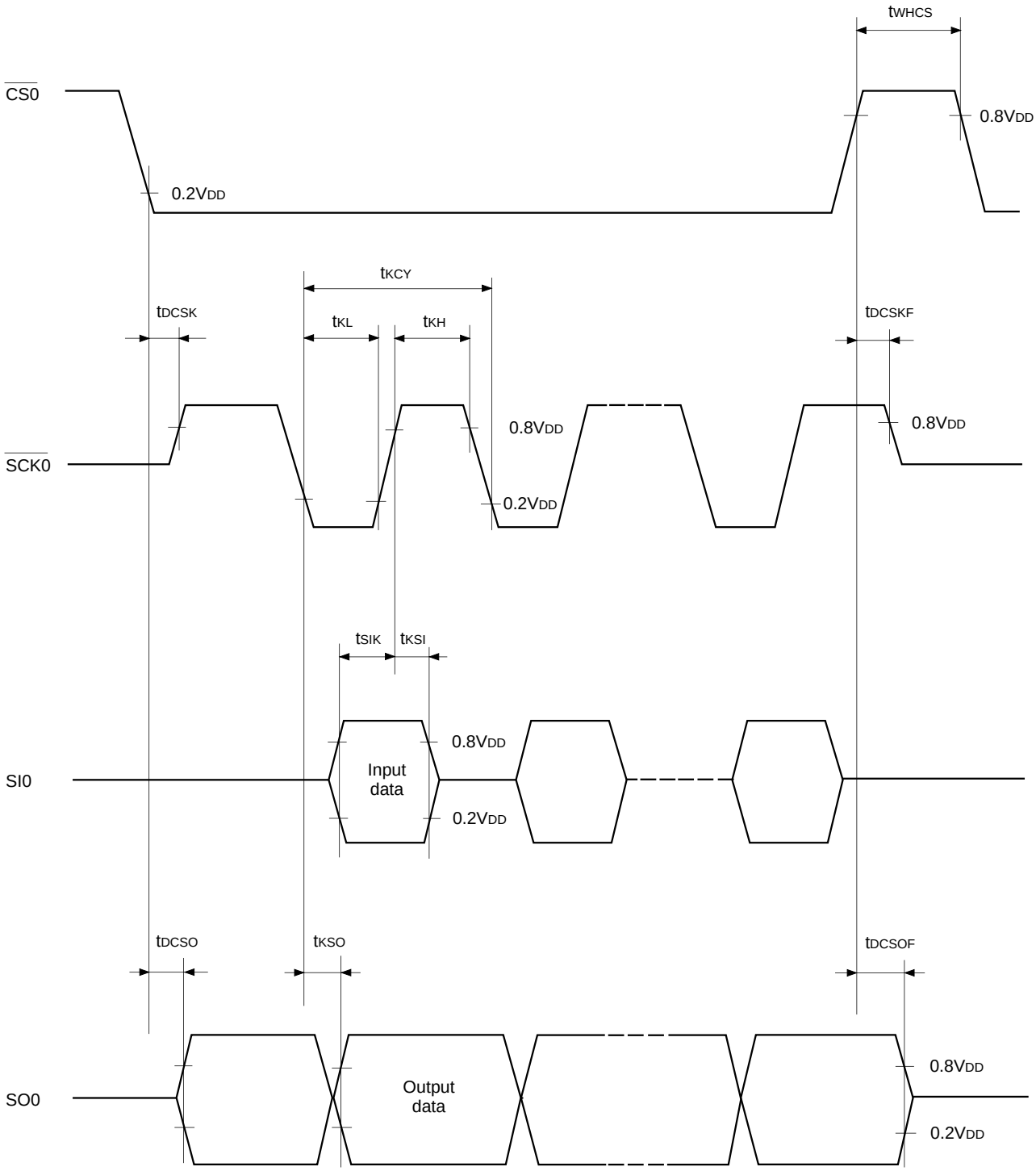
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0}\downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0}\downarrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0}\downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}\downarrow \rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI0 input setup time (for $\overline{SCK0}\uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0}\uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0}\downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC; $00FE_H$) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing (CH0)

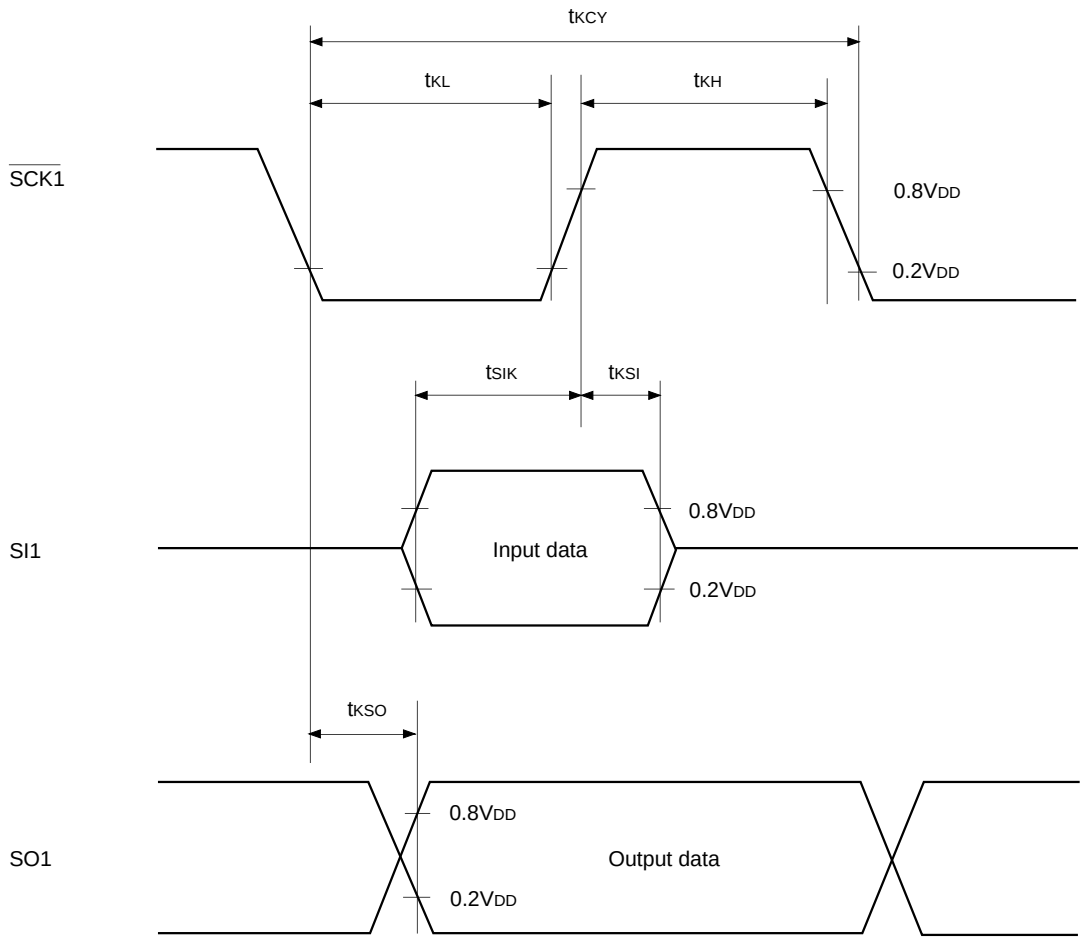


Serial transfer (CH1) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	8000/fc – 50		ns
SI1 input setup time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ output mode		100	ns

Note) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.

Fig. 5. Serial transfer timing (CH1)

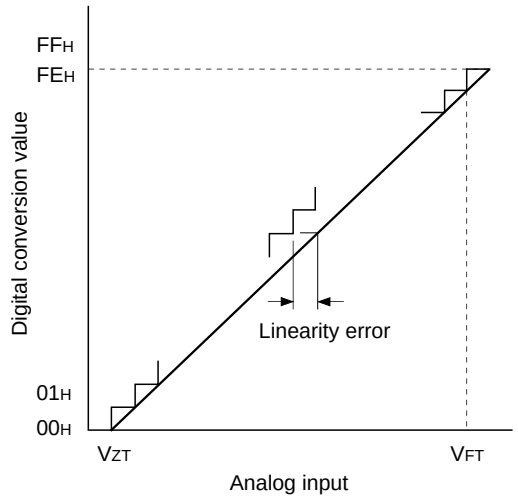


(3) A/D converter characteristics

(Ta = –20 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}*1			µs
Sampling time	t_{SAMP}			12/f_{ADC}*1			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD} – 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	µA

Fig. 6. Definitions of A/D converter terms



*1 f_{ADC} indicates the below values due to the contents of bit 0 (ADCCK) of the ADC operation clock selection (MSC: 01FF$_H$), bits 7 (PCK1) and 6 (PCK0) of the clock control register.

PCK1, PCK0 \ ADCCK	0 (ϕ/2 selection)	1 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$ PJ0 to PJ7		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 7. Interruption input timing

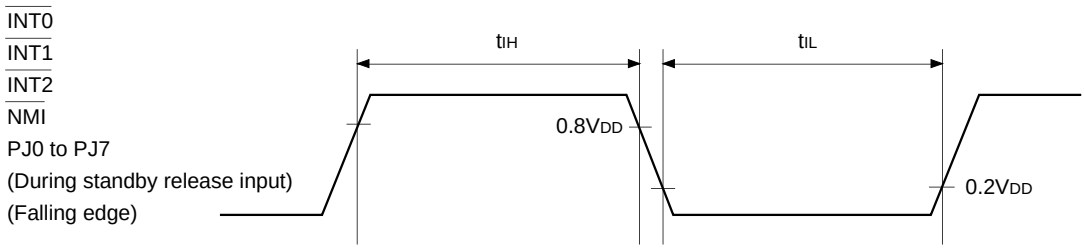
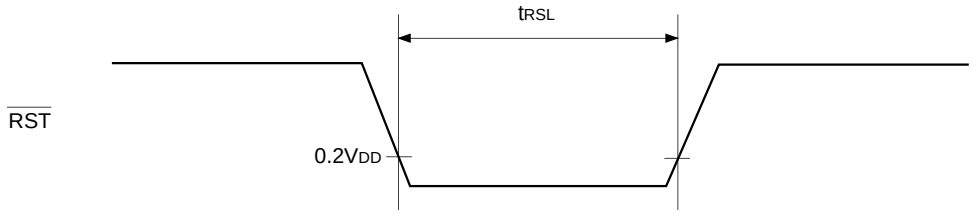


Fig. 8. Reset input timing



(5) Others (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

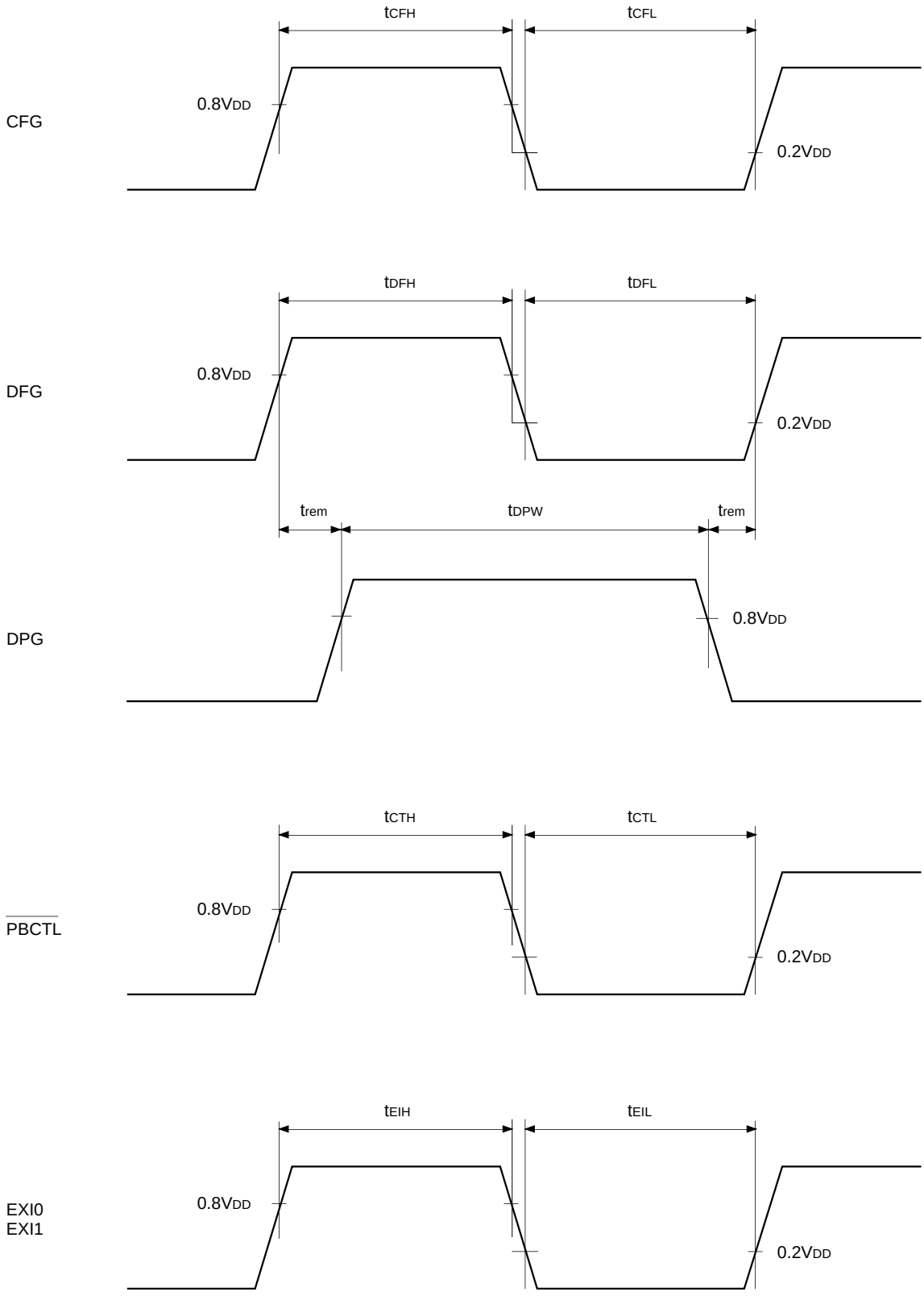
Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input High and Low level widths	t_{CFH} t_{CFL}	CFG		$t_{FRC} \times 24 + 200$		ns
DFG input High and Low level widths	t_{DFH} t_{DFL}	DFG		$t_{FRC} \times 8 + 200$		ns
DPG minimum pulse width	t_{DPW}	DPG		50		ns
DPG minimum removal time	t_{rem}	DPG		50		ns
$\overline{PBCTL}$ input High and Low level widths	t_{CTH} t_{CTL}	$\overline{PBCTL}$	tsys = 2000/fc	$t_{FRC} \times 8 + 200 + t_{sys}$		ns
EXI input High and Low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	tsys = 2000/fc	$t_{FRC} \times 8 + 200 + t_{sys}$		ns

Note) tsys indicates three values according to the contents of the clock control register (CLC; $00FE_H$) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

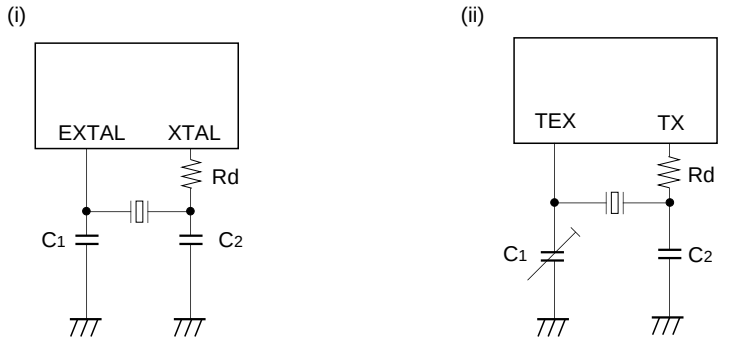
t_{FRC} [ns] = 1000/fc

Fig. 9. Other timings



Appendix

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00	5	5		
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16	12	0	(i)
		10.00	16	12		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

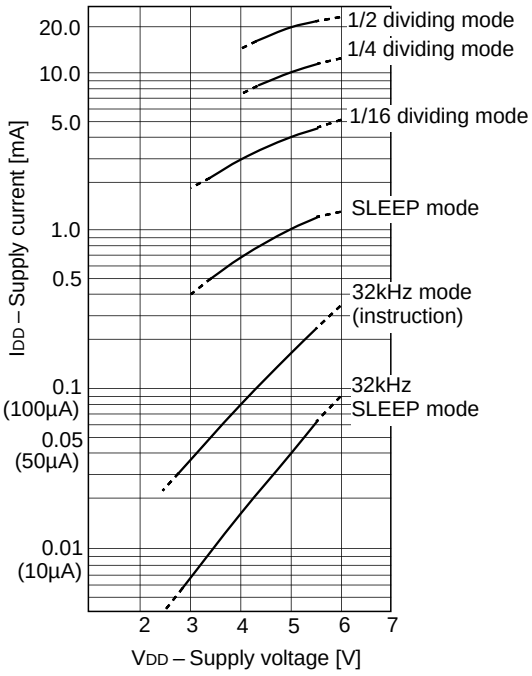
Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Input circuit format*1	C-MOS schmitt	TTL schmitt

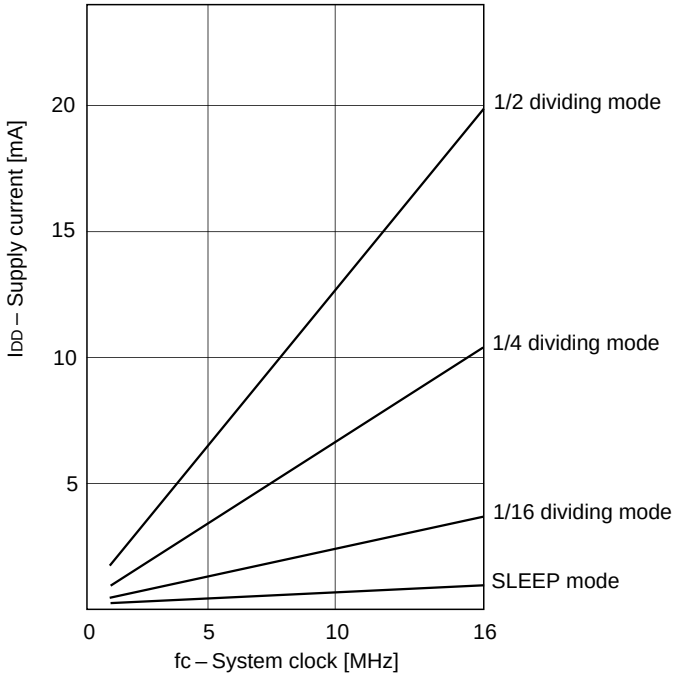
*1 The input circuit format can be selected for PG4/SYNC0 pin and PG5/SYNC1, respectively.

Characteristics Curve

IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)

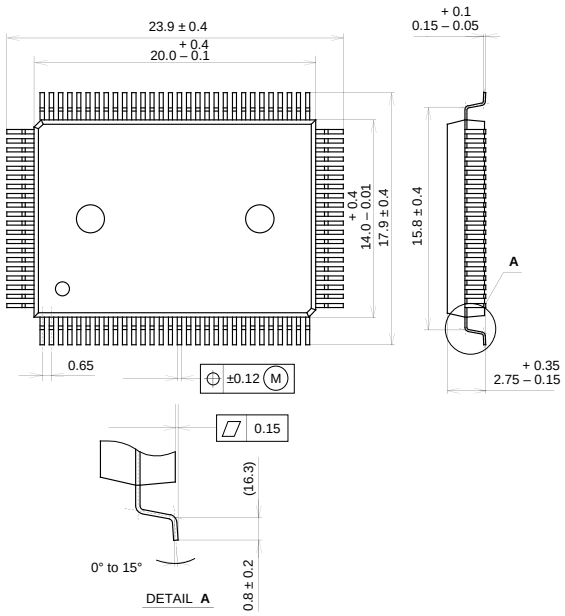


IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)

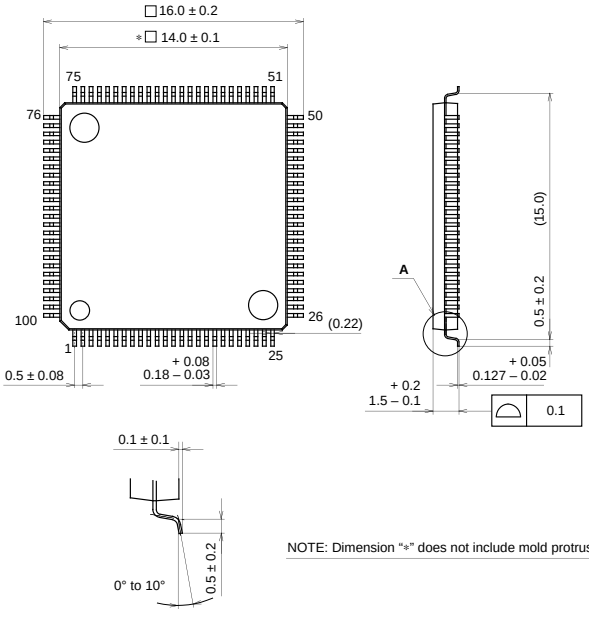


SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	*QFP100-P-1414-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————