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# HD74AC166/HD74ACT166

## 8-bit Shift Register

# HITACHI

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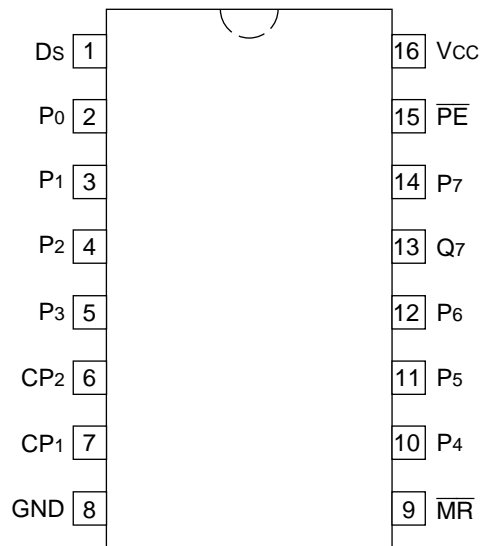
### Description

The HD74AC166/HD74ACT166 is an 8-bit, serial or parallel-in, serial-out shift register using edge triggered D-type flip-flops. Serial and parallel entry are synchronous, with state changes initiated by the rising edge of the clock. An asynchronous Master Reset overrides other inputs and clears all flip-flops. The circuit can be clocked from two sources or one CP input can be used to trigger the other.

### Features

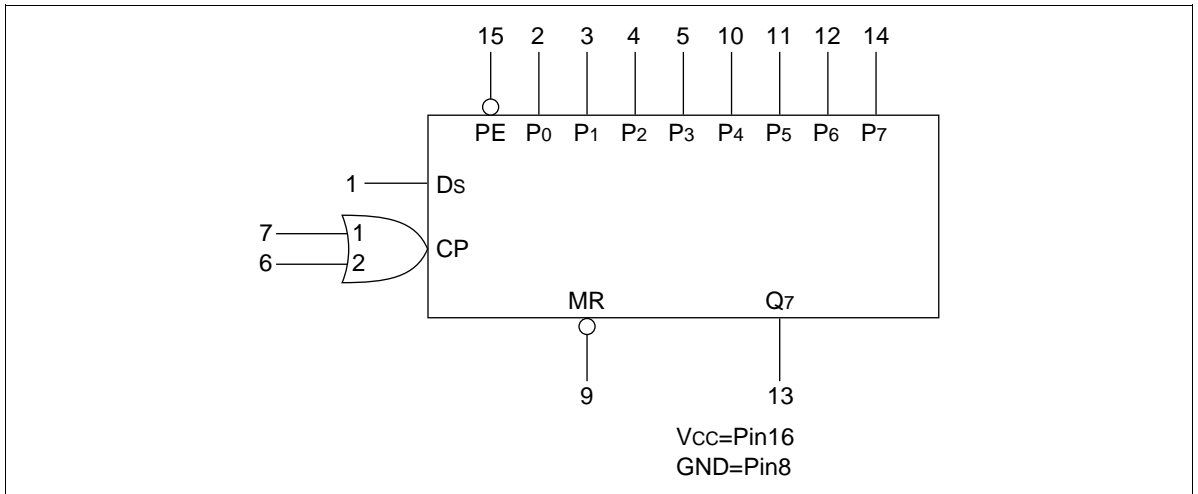
- Outputs Source/Sink 24 mA
- HD74ACT166 has TTL-Compatible Inputs

### Pin Arrangement



(Top view)

## Logic Symbol



## Pin Names

- CP<sub>1</sub>, CP<sub>2</sub> Clock Pulse Inputs (Active Rising Edge)
- D<sub>S</sub> Serial Data Input
- $\overline{PE}$  Parallel Enable Input (Active Low)
- P<sub>0</sub> to P<sub>7</sub> Parallel Data Inputs
- $\overline{MR}$  Asynchronous Master Reset Input (Active Low)
- Q<sub>7</sub> Last Stage Output

## Functional Description

Operation is synchronous (except for Master Reset) and state changes are initiated by the rising edge of either clock input if the other clock input is Low. When one of the clock inputs is used as an active High clock inhibit, it should attain the High state while the other clock is still in the High state following the previous operation. When the Parallel Enable ( $\overline{PE}$ ) input is Low, data is loaded into the register from the Parallel Data (P<sub>0</sub> to P<sub>7</sub>) inputs on the next rising edge of the clock. When  $\overline{PE}$  is High, information is shifted from the Serial Data (D<sub>S</sub>) input to Q<sub>0</sub> and all data in the register is shifted one bit position (i.e., Q<sub>0</sub> → Q<sub>1</sub>, Q<sub>1</sub> → Q<sub>2</sub>, etc.) on the rising edge of the clock.

**Truth Table**

**Inputs**

$\overline{MR}$	$\overline{PE}$	$CP_2$	$CP_1$	$D_s$	Parallel	Internal Outputs		Output
					$P_0$ to $P_7$	$Q_0$	$Q_6$	$Q_7$
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	L	L	$\lrcorner$	X	$a \dots h$	a	b	h
H	H	L	$\lrcorner$	H	X	H	$Q_{An}$	$Q_{Gn}$
H	H	L	$\lrcorner$	L	X	L	$Q_{An}$	$Q_{Gn}$
H	X	H	$\lrcorner$	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$

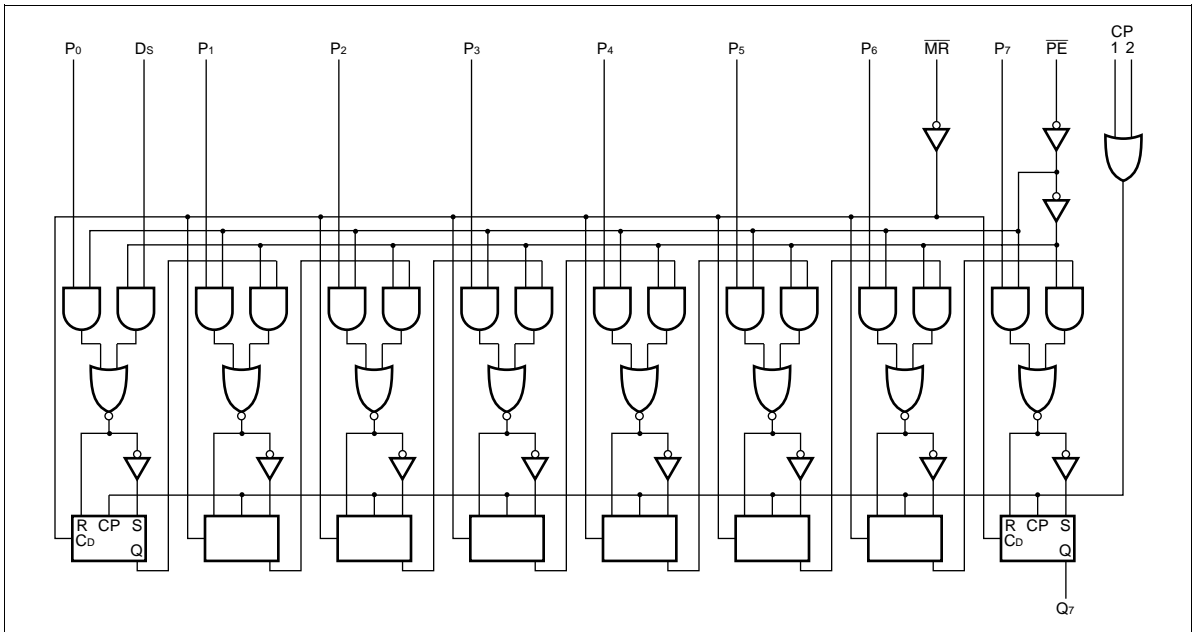
H : High Voltage Level

L : Low Voltage Level

X : Immaterial

$\lrcorner$  : Low-to-High Clock Transition

**Logic Diagram**



# HD74AC166/HD74ACT166

## DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	$I_{CC}$	80	$\mu\text{A}$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$ , $T_a = \text{Worst case}$
Maximum quiescent supply current	$I_{CC}$	8.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$ , $T_a = 25^\circ\text{C}$
Maximum additional $I_{CC}$ /input (HD74ACT166)	$I_{CCT}$	1.5	mA	$V_{IN} = V_{CC} - 2.1\text{ V}$ , $V_{CC} = 5.5\text{ V}$ , $T_a = \text{Worst case}$

## AC Characteristics: HD74AC166

Item	Symbol	$V_{CC} (\text{V})^{*1}$	$T_a = +25^\circ\text{C}$ $C_L = 50\text{ pF}$			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	$f_{max}$	3.3	75	—	—	65	—	MHz
		5.0	100	—	—	80	—	
Propagation delay $CP_1$ or $CP_2$ to $Q_7$	$t_{PLH}$	3.3	1.0	11.0	14.5	1.0	15.5	ns
		5.0	1.0	9.5	11.5	1.0	12.5	
Propagation delay $CP_1$ or $CP_2$ to $Q_7$	$t_{PHL}$	3.3	1.0	10.5	14.0	1.0	15.0	
		5.0	1.0	9.0	11.0	1.0	12.0	
Propagation delay $\overline{MR}$ to $Q_7$	$t_{PHL}$	3.3	1.0	9.5	12.0	1.0	13.0	
		5.0	1.0	6.5	9.0	1.0	10.0	

Note: 1. Voltage Range 3.3 is  $3.3\text{ V} \pm 0.3\text{ V}$   
Voltage Range 5.0 is  $5.0\text{ V} \pm 0.5\text{ V}$

AC Operating Requirements: HD74AC166

Item	Symbol	V <sub>CC</sub> (V)* <sup>1</sup>	Ta = +25°C C <sub>L</sub> = 50 pF		Ta = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Typ	Guaranteed Minimum			
Setup time	t <sub>su</sub>	3.3	3.0	5.5	6.0	ns	
$\overline{PE}$ or P <sub>n</sub> or D <sub>s</sub> to CP <sub>n</sub>		5.0	2.0	4.0	4.5		
Hold time	t <sub>h</sub>	3.3	-1.5	3.0	3.0		
CP <sub>n</sub> to $\overline{PE}$ or P <sub>n</sub> or D <sub>s</sub>		5.0	-0.5	3.0	3.0		
Pulse width	t <sub>w</sub>	3.3	2.0	5.5	7.0		
CP <sub>n</sub> or $\overline{MR}$		5.0	2.0	4.5	5.0		
Recovery time	t <sub>rec</sub>	3.3	-2.5	0.0	0.0		
$\overline{MR}$ to CP <sub>n</sub>		5.0	-1.5	0.0	0.0		

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT166

Item	Symbol	V <sub>CC</sub> (V)* <sup>1</sup>	Ta = +25°C C <sub>L</sub> = 50 pF			Ta = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f <sub>max</sub>	5.0	100	—	—	80	—	MHz
Propagation delay CP <sub>n</sub> to Q <sub>7</sub>	t <sub>PLH</sub>	5.0	1.0	10.0	12.5	1.0	13.5	ns
Propagation delay CP <sub>n</sub> to Q <sub>7</sub>	t <sub>PHL</sub>	5.0	1.0	9.5	12.0	1.0	13.0	
Propagation delay $\overline{MR}$ to Q <sub>7</sub>	t <sub>PHL</sub>	5.0	1.0	8.5	11.0	1.0	12.0	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

# HD74AC166/HD74ACT166

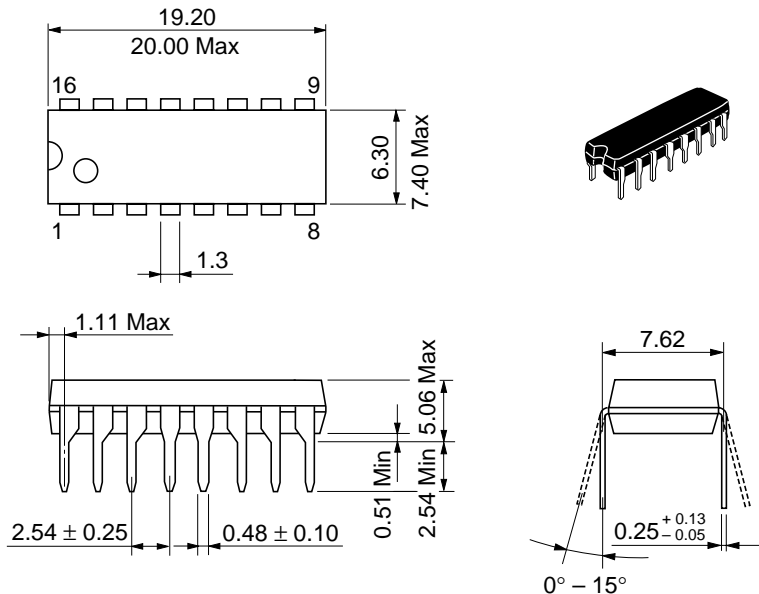
## AC Operating Requirements: HD74ACT166

Item	Symbol	$V_{CC}$ (V)*1	Ta = +25°C	Ta = -40°C		Unit
			$C_L = 50$ pF	to +85°C	$C_L = 50$ pF	
			Typ	Guaranteed Minimum		
Setup time $\overline{PE}$ or $P_n$ or $D_S$ to $CP_n$	$t_{su}$	5.0	2.5	7.0	8.0	ns
Hold time $CP_n$ to $\overline{PE}$ or $P_n$ or $D_S$	$t_h$	5.0	0.0	1.5	1.5	
Pulse width $CP_n$ or $\overline{MR}$	$t_w$	5.0	4.5	7.0	8.0	
Recovery time $\overline{MR}$ to $CP_n$	$t_{rec}$	5.0	-2.5	0.5	0.5	

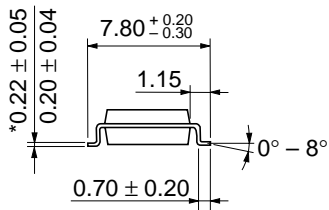
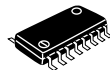
Note: 1. Voltage Range 5.0 is  $5.0\text{ V} \pm 0.5\text{ V}$

## Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	$C_{IN}$	4.5	pF	$V_{CC} = 5.5\text{ V}$
Power dissipation capacitance	$C_{PD}$	35.0	pF	$V_{CC} = 5.0\text{ V}$



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

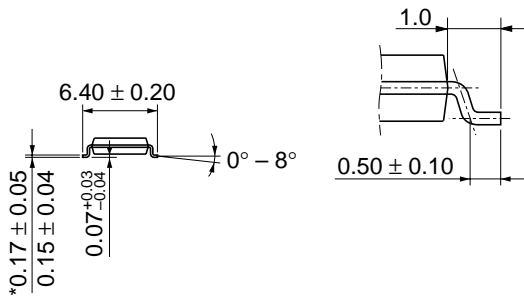
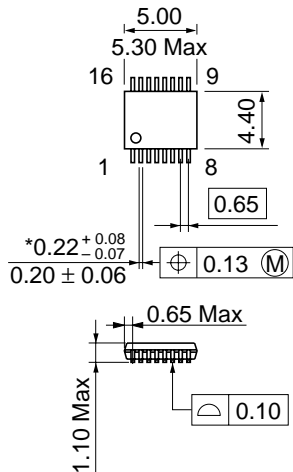
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g





\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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