
HD74HC646/HD74HC648

Octal Bus Transceivers/Registers with Multiplexed 3-state outputs

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Description

Six control inputs enable this device to be used as a latched transceiver, unlatched transceiver or a combination of both. As a latched transceiver, data from one bus is stored for later retrieval by the other bus. Alternately real time bus data (unlatched) may be directly transferred from one bus to another.

Circuit operation is determined by the Control \bar{G} , Direction, Clock AB, Clock BA, Select AB, Select BA control inputs. The enable input, Control \bar{G} , controls whether any bus outputs are enabled. The direction control Direction (DIR), determines which bus is enabled, and hence the direction data flows: The Select AB, Select BA inputs control whether the latched data (stored in D type flip-flops), or the bus data (from other bus input pins) is transferred. Each set of flip-flops has its own clock Clock AB and Clock BA, for storing data. Data is latched on the rising edge of the clock.

Features

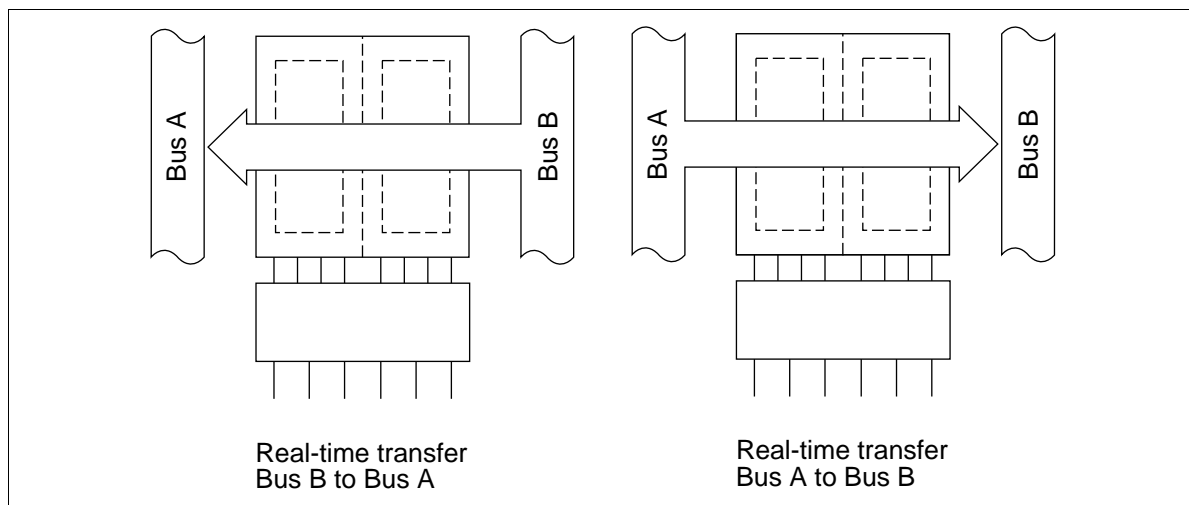
- High Speed Operation: t_{pd} (Bus to Bus) = 14 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

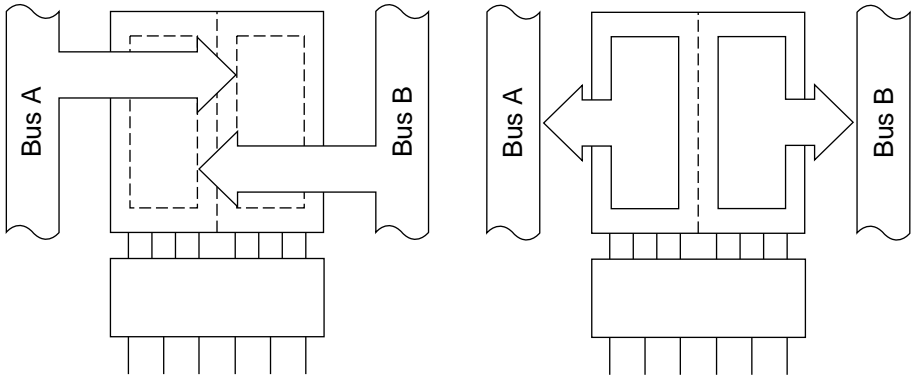
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Function Table

Inputs

Control	Clock	Select				Data I/O	Data I/O	Operation or Function	
		BA	AB	AB	BA	A1 thru A8	B1 thru B8	HD74HC646	HD74HC648
\bar{G}	Direction	BA	AB	AB	BA	A1 thru A8	B1 thru B8	HD74HC646	HD74HC648
H	X	X	X	X	X	Z (Input)	Z (Input)	Isolation	Isolation
H	X			H	H	Z (Input)	Z (Input)	Store A & B data	Store \bar{A} & \bar{B} data
L	L	X	X	X	L	Output	Z (Input)	B real-time data to A bus	\bar{B} real-time data to A bus
L	L	H	H	X	H	Output	Z (Input)	B stored data to A bus	\bar{B} stored data to A bus
L	L	L	L	X	H	Output	Z (Input)	B stored data to A bus	\bar{B} stored data to A bus
L	H	X	X	L	X	Z (Input)	Output	A real-time data to B bus	\bar{A} real-time data to B bus
L	H	H	H	H	X	Z (Input)	Output	A stored data to B bus	\bar{A} stored data to B bus
L	H	L	L	H	X	Z (Input)	Output	A stored data to B bus	\bar{A} stored data to B bus

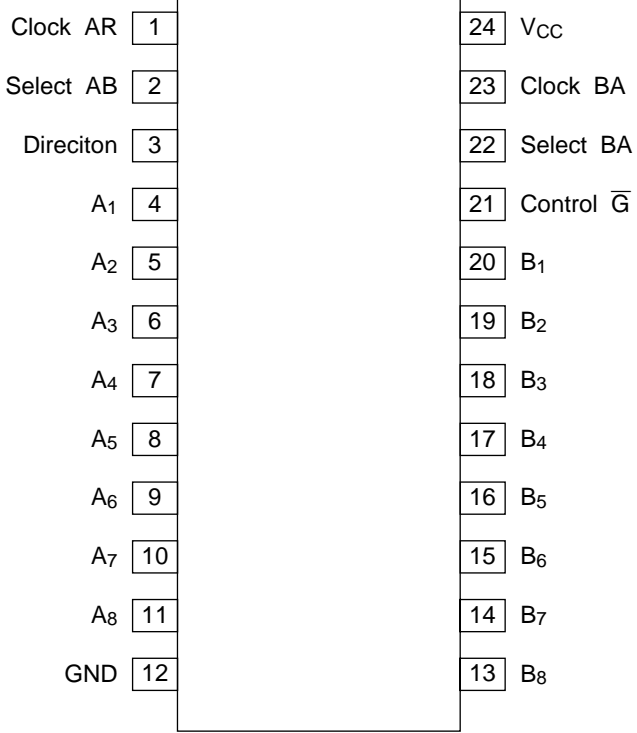




Storage from A, B, or A and B

Transfer stored data to A or B

Pin Arrangement



(Top view)

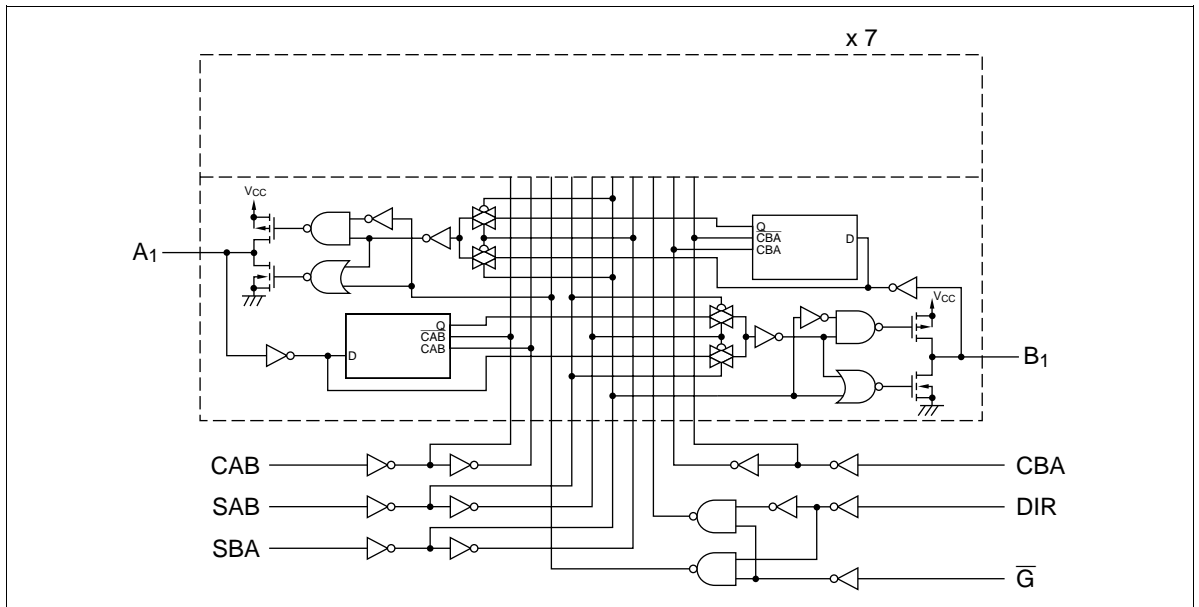
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Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Output current	I_{OUT}	± 35	mA
DC current drain per V_{CC} , GND	I_{CC} , I_{GND}	± 75	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power Dissipation per package	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$

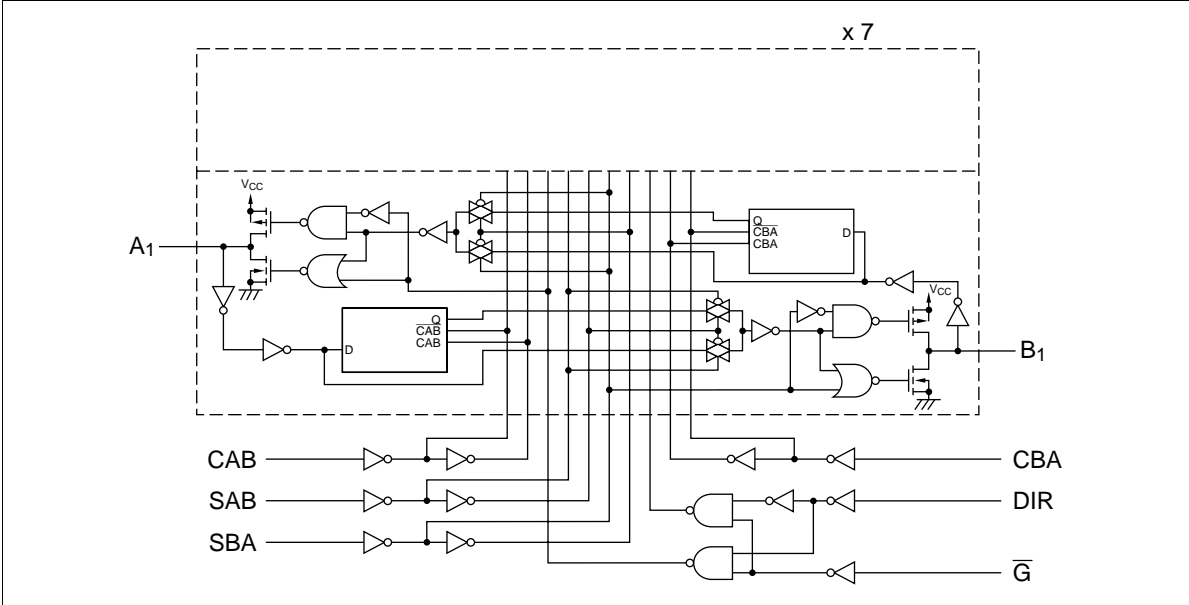
Logic Diagram

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DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V _{IL}	2.0	—	—	0.5	—	0.5		V
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I _{OH} = -6 mA
		6.0	5.68	—	—	5.63	—		I _{OH} = -7.8 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I _{OL} = 6 mA
		6.0	—	—	0.26	—	0.33		I _{OL} = 7.8 mA
Off-state output current	I _{OZ}	6.0	—	—	±0.5	—	±5.0	μA	Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, Iout = 0 μA

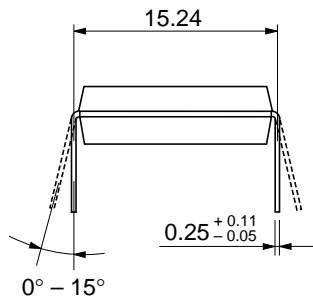
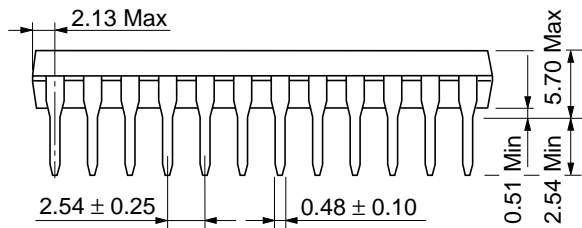
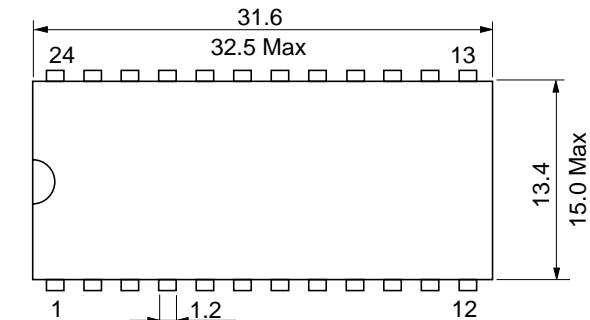
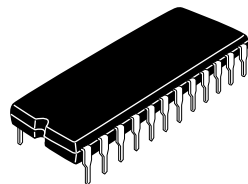
AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$		$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	ns	Clock AB to B or
		4.5	—	—	27	—	21		Clock BA to A
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH}	2.0	—	—	170	—	215	ns	A or B input to B or A output (HD74HC646 only)
		4.5	—	14	34	—	43		
		6.0	—	—	29	—	37		
	t_{PHL}	2.0	—	—	150	—	190	ns	A or B input to B or A output (HD74HC648 only)
		4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
	t_{PLH}	2.0	—	—	220	—	275	ns	Clock BA or Clock AB input to A or B output
		4.5	—	18	44	—	55		
		6.0	—	—	37	—	47		
	t_{PHL}	2.0	—	—	170	—	215	ns	Select BA or Select AB input to A or B output, with A or B high
		4.5	—	15	34	—	43		
		6.0	—	—	29	—	37		
t_{PLH}	2.0	—	—	170	—	215	ns	Select BA or Select AB input to A or B output, with A or B low	
	4.5	—	16	34	—	43			
	6.0	—	—	29	—	37			
Output enable time	t_{ZH}	2.0	—	—	150	—	190	ns	Control \overline{G} input or Direction to A or B output
		4.5	—	17	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{LZ}	2.0	—	—	150	—	190	ns	Control \overline{G} input to A or B output
		4.5	—	20	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	
		4.5	20	3	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		

HD74HC646/HD74HC648

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns) (cont)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	5	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	60	—	75	ns	
		4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	



Hitachi Code	DP-24
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	3.1 g

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