

SANYO	No. 5232	LB1951V
	3-phase Brushless Motor Driver for Portable VCR Capstan Use	

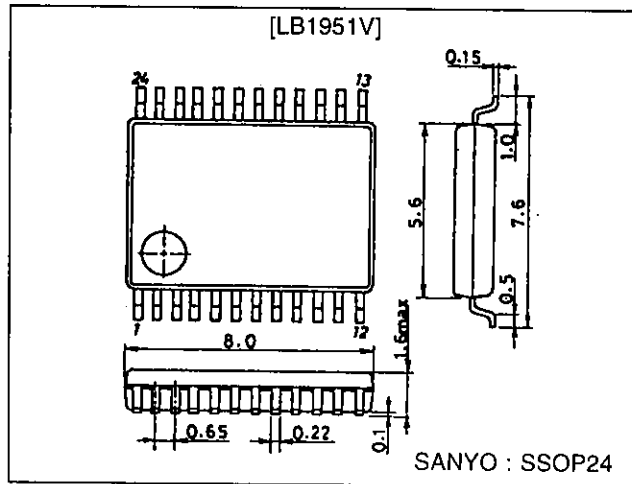
Functions

- 3-phase full-wave current linear drive system (120° voltage linear drive system).
- Torque ripple correction circuit built in (overlap correction).
- Speed control system using motor supply voltage control.
- FG comparator built in.
- Thermal shutdown circuit built in.

Package Dimensions

unit : mm

3175A-SSOP24



Specifications

Absolute Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC1} max		10	V
	V _{CC2} max		11	V
	V _S max	≅ V _{CC2}	11	V
Applied output voltage	V _O max		V _S + 2	V
Maximum output current	I _O max		1.0	A
Allowable power dissipation	P _d max	Independent IC	440	mW
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-55 to +150	°C

Allowable Operating Ranges at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC1}		2.7 to 6.0	V
	V _{CC2}		3.5 to 9.0	V
	V _S		to V _{CC2}	V
Hall input amplitude	V _{HALL}	Between Hall inputs	±20 to ±80	mV _{O-P}

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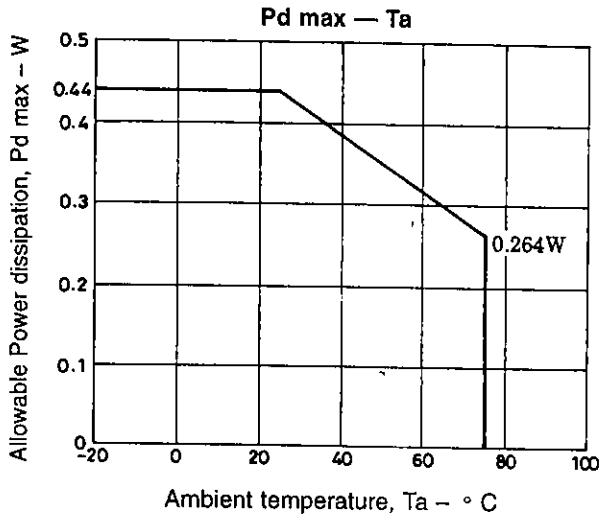
Electrical Characteristics at $T_a = 25\text{ }^\circ\text{C}$, $V_{CC1} = 3\text{ V}$, $V_{CC2} = 4.75\text{ V}$, $V_S = 1.5\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
[Supply Current]						
Supply current 1	I_{CC1}	$I_{out} = 100\text{ mA}$		3.0	5.0	mA
Supply current 2	I_{CC2}	$I_{out} = 100\text{ mA}$		7.0	10.0	mA
Static current 1	I_{CCQ1}	$V_{STBY} = 0\text{ V}$		1.5	3.0	mA
Static current 2	I_{CCQ2}	$V_{STBY} = 0\text{ V}$			100	μA
V_S static current	I_{SQ}	$V_{STBY} = 0\text{ V}$		40	100	μA
[VX1]						
Upper residual voltage	V_{XH1}	$I_{out} = 0.2\text{ A}$	0.15	0.22	0.29	V
Lower residual voltage	V_{XL1}	$I_{out} = 0.2\text{ A}$	0.16	0.21	0.26	V
[VX2]						
Upper residual voltage	V_{XH2}	$I_{out} = 0.5\text{ A}$		0.25	0.40	V
Lower residual voltage	V_{XL2}	$I_{out} = 0.5\text{ A}$		0.25	0.40	V
Output saturation voltage	V_{osat}	$I_{out} = 0.8\text{ A}$, Sink + Source			1.40	V
Overlap	O.L	$R_L = 39\ \Omega \times 3$, R angle = $20\text{ k}\Omega$ Note 1	70	77	84	%
[Hall Amplifier]						
Hall amplifier input offset voltage	V_{HOFF}	Note 2	-5		+5	mV
Hall amplifier common-mode input range	V_{HCM}	R angle = $20\text{ k}\Omega$	0.95		2.4	V
Hall amplifier I/O voltage gain	V_{GVH}	R angle = $20\text{ k}\Omega$	24.5	27.5	30.5	dB
[Standby Pin]						
Stand-by pin high-level voltage	V_{STH}		2.5			V
Standby pin low-level voltage	V_{STL}				0.4	V
Standby pin input current	I_{STIN}	$V_{STBY} = 3\text{ V}$		25	40	μA
Standby leakage current	I_{STLK}	$V_{STBY} = 0\text{ V}$			-30	μA
[FRC Pin]						
FRC pin high-level voltage	V_{FRCH}		2.5			V
FRC pin low-level voltage	V_{FRCL}				0.4	V
FRC pin input current	I_{FRCIN}	$V_{FRC} = 3\text{ V}$		20	30	μA
FRC pin leakage current	I_{FRCLK}	$V_{FRC} = 0\text{ V}$			-30	μA
[VH]						
Hall supply voltage	V_{HALL}	$I_H = 5\text{ mA}$, $V_{H(+)} - V_{H(-)}$	0.85	0.95	1.05	V
$V_{H(-)}$ pin voltage	$V_{H(-)}$	$I_H = 5\text{ mA}$	0.81	0.88	0.95	V
[FG Comparator]						
Input offset voltage	V_{FGOFF}		-3		+3	mV
Input bias current	I_{bFG}	$V_{FGIN^+} = V_{FGIN^-} = 1.5\text{ V}$			500	nA
Input bias current offset	ΔI_{bFG}	$V_{FGIN^+} = V_{FGIN^-} = 1.5\text{ V}$	-100		+100	nA
Common-mode input range	V_{FGCM}		1.2		2.5	V
Output high-level voltage	V_{FGOH}	At internal pull-up	2.8			V
Output low-level voltage	V_{FGOL}	At internal pull-up			0.2	V
Voltage gain	V_{GFG}	(Design target) Note 2		100		dB
Output current (Sink)	I_{FGOs}	With output pin "L"			5	mA
[TSD]						
TSD operating temperature	T-TSD	(Design target value) Note 2		180		$^\circ\text{C}$
TSD temperature hysteresis width	ΔTSD	(Design target value) Note 2		20		$^\circ\text{C}$

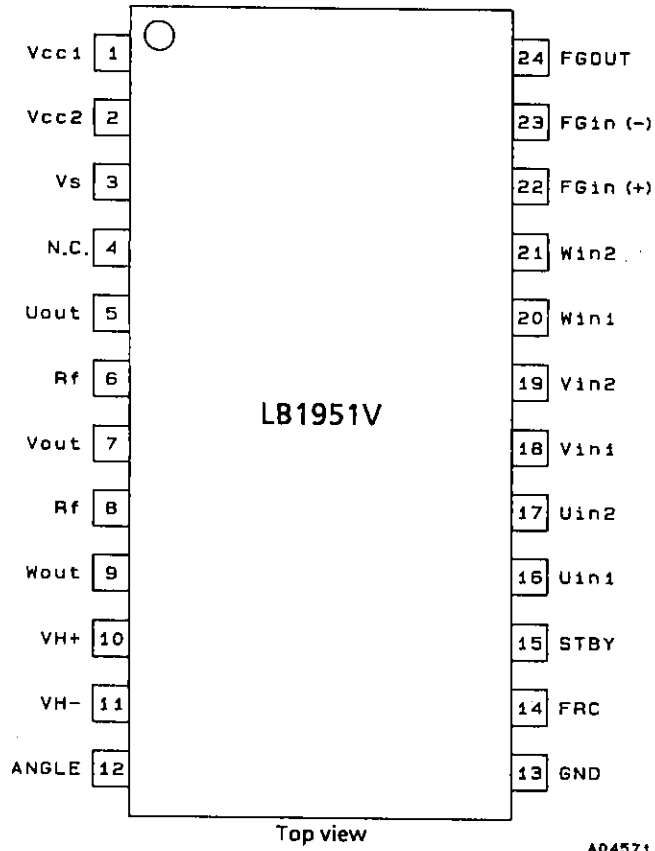
Note 1: Overlapping specifications are assumed to be test specifications.

Note 2: For parameters which have an entry of (Design target value) in the "Conditions" column, no measurements are made.

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Pin Assignment



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Pin Functions

Pin No.	Pin name	I/O equivalent circuit	Function
1	V _{CC1}		Power supply pin for supplying power to all circuits except amplitude control section in output section in IC.
2	V _{CC2}		Power supply pin for supplying power to all circuits of the amplitude control section and the output control section in IC.
3	V _S		Power supply pin for motor drive. Apply a voltage of V _{CC2} or lower to this pin.
5 7 9	U-OUT V-OUT W-OUT	<p style="text-align: center;">A04573</p>	U-phase output pin V-phase output pin W-phase output pin (Spark killer diode built in)
6, 8	R _f		
10 11	V _H ⁺ V _H ⁻	<p style="text-align: center;">A04574</p>	Pins for supplying the Hall element bias voltage. Voltage of 0.95 V (typ.) is generated between V _H ⁺ and V _H ⁻ . (when I _H = 5 mA)
12	ANGLE	<p style="text-align: center;">A04572</p>	Pins for controlling the Hall input-output gain. The gain is controlled by a resistor between this pin and GND.
16 17 18 19 20 21	U _{in} 1 U _{in} 2 V _{in} 1 V _{in} 2 W _{in} 1 W _{in} 2		U-phase Hall element input pin; Logic "H" represents I _N ⁺ > I _N ⁻ . V-phase Hall element input pin; Logic "H" represents I _N ⁺ > I _N ⁻ . W-phase Hall element input pin; Logic "H" represents I _N ⁺ > I _N ⁻ .
13	GND		Pin for grounding other than output transistors. Minimum potential of output transistors is equal to the level at R _f pin.
14	FRC	<p style="text-align: center;">A04575</p>	Forward/reverse select pin. The voltage on this pin is used for forward/reverse select. (with Hysteresis)
15	STBY		Pin for selecting the bias supply for all circuits except the FG comparator. "L" level on this pin cuts the bias supply.

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Pin No.	Pin name	I/O equivalent circuit	Function
22	FGin+		Noninverting input pin for the FG comparator. No bias is applied internally.
23	FGin-		Inverting input pin for the FG comparator. No bias is applied internally.
24	FGout		FG comparator output pin. A resistive load of 20 kΩ is provided internally.

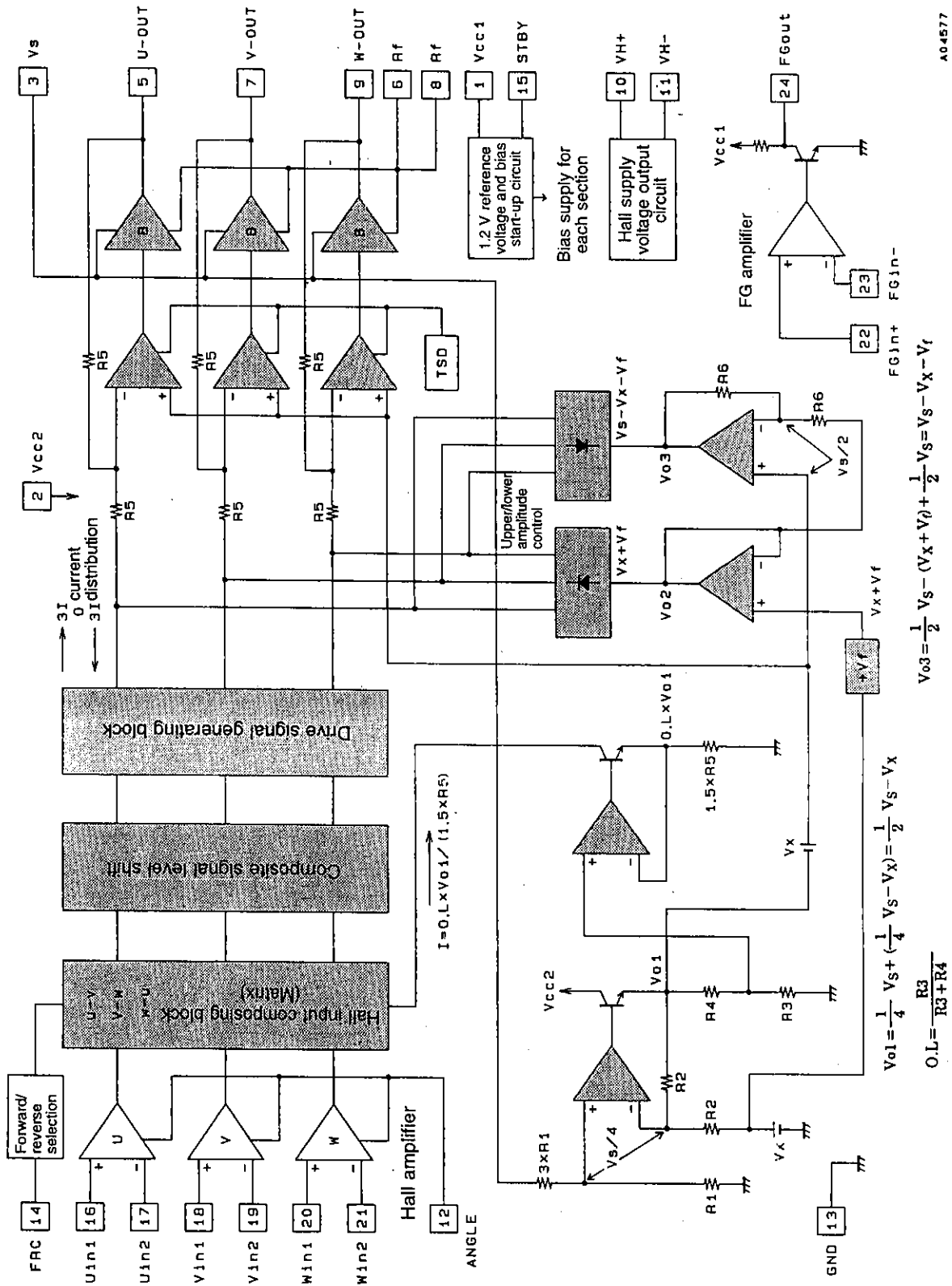
Truth Table

	Source → Sink	Hall input			FRC
		U	V	W	
1	V → W	H	H	L	H
	W → V	H	H	L	L
2	U → W	H	L	L	H
	W → U	H	L	L	L
3	U → V	H	L	H	H
	V → U	H	L	H	L
4	W → V	L	L	H	H
	V → W	L	L	H	L
5	W → U	L	H	H	H
	U → W	L	H	H	L
6	V → U	L	H	L	H
	U → V	L	H	L	L

Note: "H" in the FRC column represents a voltage of 2.5 V or more; "L" represents a voltage of 0.4 V or less.
(At $V_{CC1} = 3\text{ V}$)

Note: "H" in the Hall input columns represents a state in which "+" has a potential which is higher by 0.02 V or more than that of the "-" phase inputs.
Conversely, "L" represents a state in which "+" has a potential which is lower by 0.02 V or more than that of the "-" phase input.

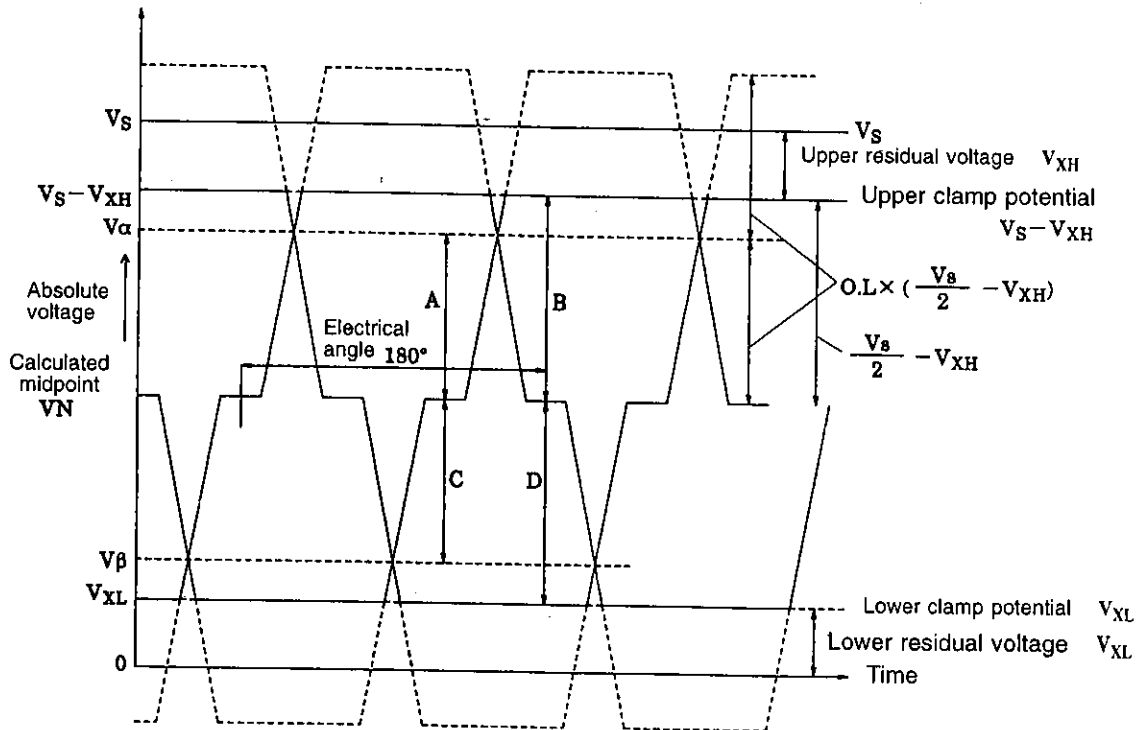
Block Diagram



AO4577

* For the shaded portions, power supply is from Vcc2.

Overlap Creation and Calculation



A0457B

i) Overlap creation

Because the voltage generated in the amplitude controller is: $2 \times O.L. \times (1/2 V_S - V_X)$ for each side, (using the midpoint as the reference point), the point at which the two waveforms cross each other is $O.L. \times (1/2 V_S - V_X)$ from the midpoint.

Because that waveform is clamped at $(1/2 V_S - V_X)$ with the midpoint as the reference point, the overlap equals $A/B \times 100$, which equals $O.L. \times 100$ (%).

ii) Overlap calculation

(1) Upper overlap amount

$$\text{Calculated midpoint } VN = \frac{(V_S - V_{XH} - V_{XL})}{2} + V_{XL} = \frac{(V_S - V_{XH} + V_{XL})}{2}$$

Because $A = V_\alpha - VN$ and $B = V_S - V_{XH} - VN$, the upper overlap amount is calculated as follows:

$$\begin{aligned} \text{Overlap amount} &= \frac{A}{B} = \frac{V_\alpha - \{(V_S - V_{XH} + V_{XL})/2\}}{V_S - V_{XH} - \{(V_S - V_{XH} + V_{XL})/2\}} \times 100 \\ &= \frac{2V_\alpha - (V_S - V_{XH}) - V_{XL}}{(V_S - V_{XH}) - V_{XL}} \times 100 (\%) \end{aligned}$$

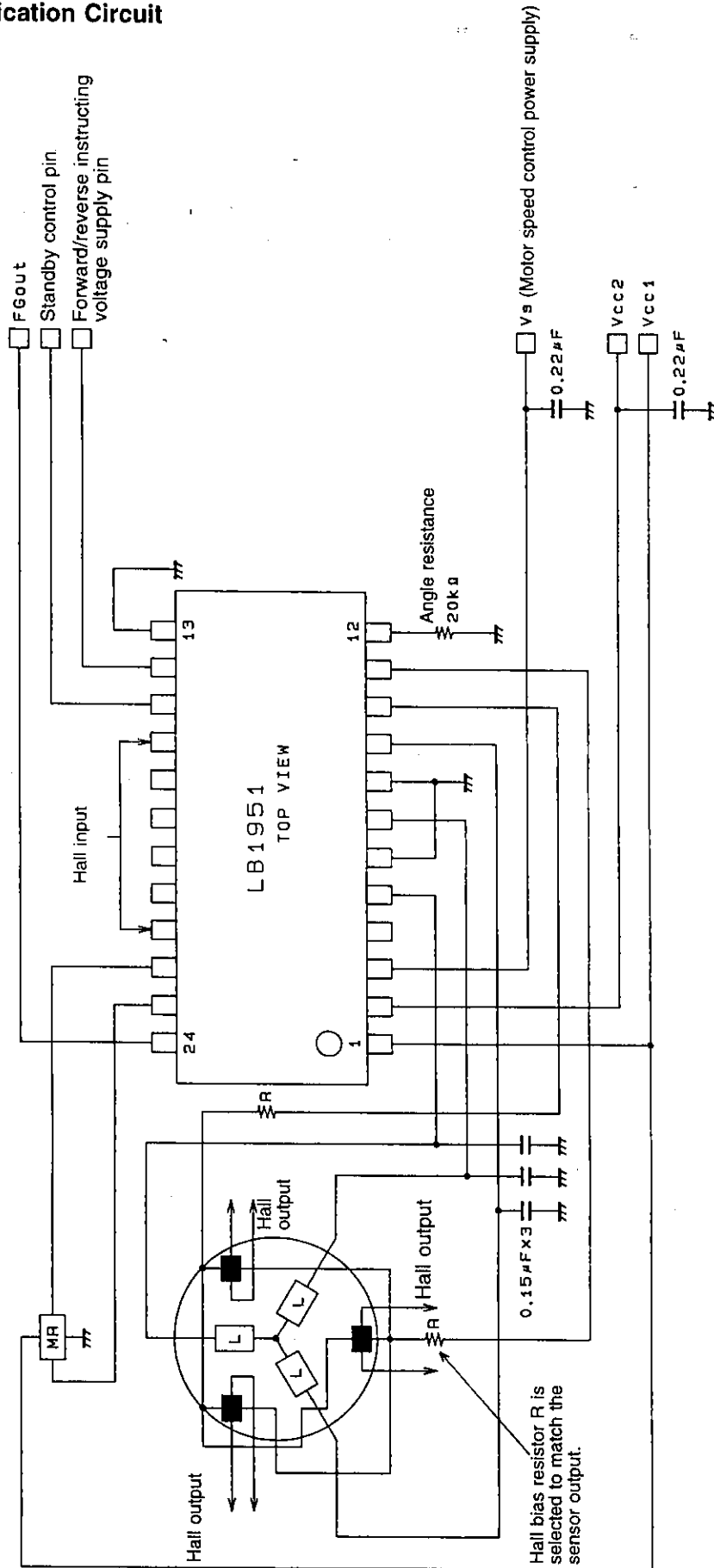
(2) Lower overlap amount

Because $C = VN - V_\beta$ and $D = VN - V_{XL}$, the lower overlap amount is calculated as follows:

$$\begin{aligned} \text{Overlap amount} &= \frac{C}{D} = \frac{\{(V_S - V_{XH} + V_{XL})/2\} - V_\beta}{\{(V_S - V_{XH} + V_{XL})/2\} - V_{XL}} \times 100 \\ &= \frac{(V_S - V_{XH}) + V_{XL} - 2V_\beta}{(V_S - V_{XH}) - V_{XL}} \times 100 (\%) \end{aligned}$$

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Sample Application Circuit



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