FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27203-6E

*ASSP*

# Switching Regulator Controller

# MB3778

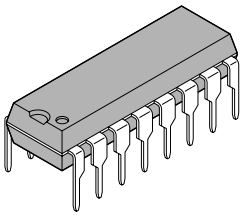
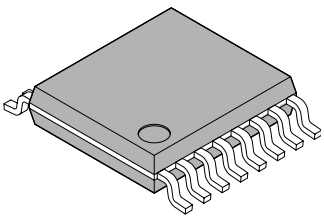
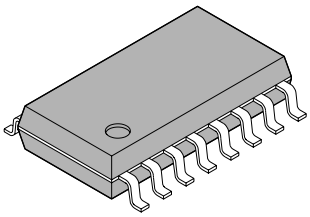
## ■ DESCRIPTION

The MB3778 is a dual switching regulator control IC. It has a two-channel basic circuit that controls PWM system switching regulator power. Complete synchronization is achieved by using the same oscillator output wave.
This IC can accept any two of the following types of output voltage: step-down, step-up, or voltage inversion (inverting voltage can be output to only one circuit). The MB3778's low power consumption makes it ideal for use in portable equipment.

## ■ FEATURES

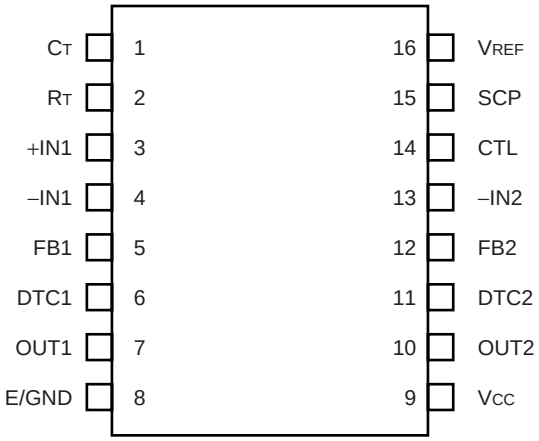
- Wide input voltage range : 3.6 V to 18 V
- Low current consumption : 1.7 mA typ. operation, 10 μA max. stand-by
- Wide oscillation frequency range:1 kHz to 500 kHz
- Built-in timer latch short-circuit protection circuit
- Built-in under-voltage lockout circuit
- Built-in 2.46 V reference voltage circuit : 1.23 V output can be obtained from $R_T$ terminal
- Variable dead-time provides control over total range
- Built-in stand-by function: power on/off function

## ■ PACKAGES

| 16-pin, Plastic DIP | 16-pin, Plastic SSOP | 16-pin, Plastic SOP |
|---|---|---|
|  |  |  |
| (DIP-16P-M04) | (FPT-16P-M05) | (FPT-16P-M06) |

## ■ PIN ASSIGNMENT

(TOP VIEW)

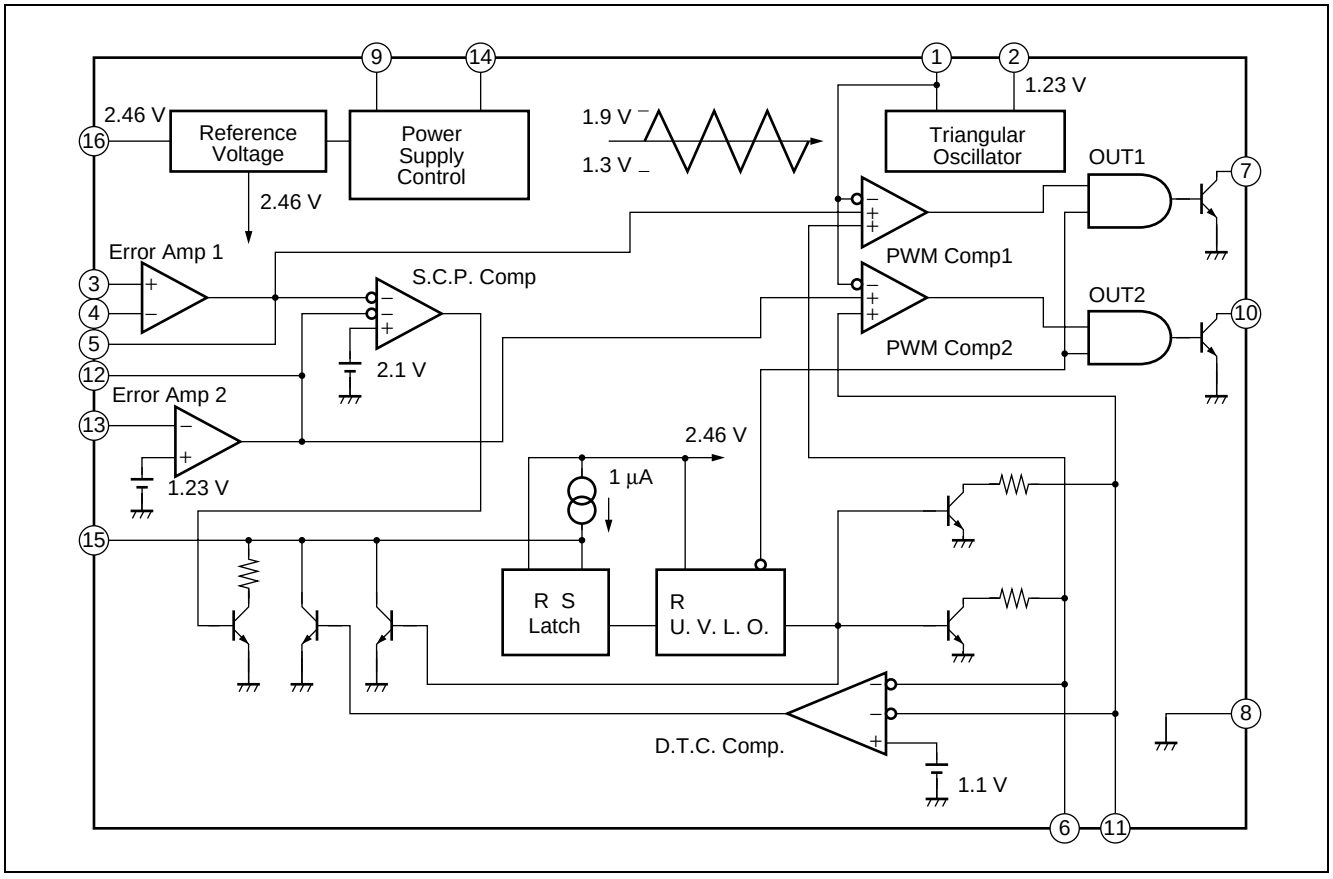



(DIP-16P-M04)
(FPT-16P-M05)
(FPT-16P-M06)

## ■ PIN DESCRIPTION

| No. | Pin | Function |
|---|---|---|
| 1 | $C_T$ | Oscillator timing capacitor terminal (150 pF to 15,000 pF) . |
| 2 | $R_T$ | Oscillator timing resistor terminal (5.1 kΩ to 100 kΩ) .<br>$V_{REF} \times 1/2$ voltage is also available at this pin for error amplifier reference input. |
| 3 | +IN1 | Error amplifier 1 non-inverted input terminal. |
| 4 | –IN1 | Error amplifier 1 inverted input terminal. |
| 5 | FB1 | Error amplifier 1 output terminal.<br>A resistor and a capacitor are connected between this terminal and the –IN1 terminal to adjust gain and frequency. |
| 6 | DTC1 | OUT1 dead-time control terminal.<br>Dead-time control is adjusted by an external resistive divider connected to the $V_{REF}$ pin.<br>A capacitor connected between this terminal and GND enables soft-start operation. |
| 7 | OUT1 | Open collector output terminal.<br>Output transistor has common ground independent of signal ground.<br>This output can source or sink up to 50 mA. |
| 8 | E/GND | Ground terminal. |
| 9 | $V_{CC}$ | Power supply terminal (3.6 to 18 V) |
| 10 | OUT2 | Open collector output terminal.<br>Output transistor has common ground independent of signal ground.<br>This output can source or sink up to 50 mA. |
| 11 | DTC2 | Sets the dead-time of OUT2.<br>The use of this terminal is the same as that of DTC1. |
| 12 | FB2 | Error amplifier 2 output terminal.<br>Sets the gain and adjusts the frequency when a resistor and a capacitor are connected between this terminal and the –IN2 terminal.<br>Voltage of $V_{REF} \times 1/2$ voltage is internally connected to the non-inverted input of error amplifier 2. Uses error amplifier 2 for positive voltage output. |
| 13 | –IN2 | Error amplifier 2 inverted input terminal. |
| 14 | CTL | Power control terminal.<br>The IC is set in the stand-by state when this terminal is set “Low.”<br>Current consumption is 10 μA or lower in the stand-by state.<br>The input can be driven by TTL or CMOS. |
| 15 | SCP | The time constant setting capacitor connection terminal of the timer latch short-circuit protection circuit.<br>Connects a capacitor between this pin and GND.<br>For details, see “How to set time constant for timer latch short-circuit protection circuit”. |
| 16 | $V_{REF}$ | 2.46 V reference voltage output terminal which can be obtained up to 1 mA.<br>This pin is used to set the reference input and idle period of the error amplifiers. |

## ■ BLOCK DIAGRAM



## ■ OPERATION DESCRIPTION

### 1. Reference voltage circuit

The reference voltage circuit generates a temperature-compensated reference voltage (≒ 2.46 V) from $V_{CC}$ (pin 9) . The reference voltage is used as an operation power supply for internal circuit.
The reference is obtained from the $V_{REF}$ terminal (pin 16).

### 2. Triangular wave oscillator

Triangular waveforms can be generated at any frequency by connecting a timing capacitor and resistor to the $C_T$ terminal (pin 1) and to the $R_T$ terminal (pin 2) .
The amplitude of this waveform is from 1.3 V to 1.9 V. These waveforms are connected to the non-inverting inputs of the PWM comparator and can be output through the $C_T$ terminal.

### 3. Error amplifiers (Error Amp.)

The error amplifier detects the output voltage of the switching regulator and outputs PWM control signals.The in-phase input voltage range is from 1.05 V to 1.45 V.The reference voltage obtained by dividing the reference voltage output (recommended value : $V_{REF}/2$) or the $R_T$ terminal voltage (1.23 V) is supplied to the non-inverting input. The $V_{REF}/2$ voltage is internally connected to non-inverting input of the other error amplifier.
Any loop gain can be chosen by connecting the feedback resistor and capacitor to the inverting input terminal from the output terminal of the error amplifier.Stable phase compensation is possible.

### 4. Timer latch short circuit protection circuit

This circuit detects the output levels of each error amplifier. If the output level of one or both of the error amplifiers is 2.1 V or higher, the timer circuit begins charging the externally connected protection enable-capacitor.
If the output level of the error amplifier does not drop below the normal voltage range before the capacitor voltage reaches the transistor base-emitter voltage, $V_{BE}$(≒ 0.65 V), the latch circuit turns the output drive transistor off and sets the idle period to 100%.

### 5. Under voltage lock-out circuit

The transition state at power-on or a momentary drops in supply voltage may cause the control IC to malfunction, which may adversely affect or even destroy the system. The under voltage lockout circuit monitors $V_{CC}$ with reference to the internal reference voltage and resets the latch circuit to turn the output drive transistor off. The idle period is set to 100%. It also pulls the SCP terminal (pin 15) “Low”.

### 6. PWM comparator unit

Each PWM comparator has one inverting input and two non-inverting inputs. This voltage-to-pulse-width converter controls the turning on time of the output pulse according to the input voltage.
The PWM comparator turns the output drive transistor on while triangular waveforms from the oscillator are lower than the error amplifier output and the DTC terminal voltage.

### 7. Output drive transistor

The output drive transistors have open collector outputs with common source supply and common grounds independent of $V_{CC}$ and signal ground. The output drive transistors for switching can sink or source up to 50 mA.

### 8. Power control unit

The power control terminal (pin 14) controls power on/off modes(the power supply current in stand-by mode is 10 μA or lower).

## ■ ABSOLUTE MAXIMUM RATINGS (See NOTE)

(Ta = 25 °C)

| Parameter | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Power Supply Voltage | $V_{CC}$ | — | — | 20 | V |
| Error Amp. Input Voltage | $V_{IN}$ | — | –0.3 | +10 | V |
| Control Input Voltage | $V_{CTL}$ | — | –0.3 | +20 | V |
| Collector Output Voltage | $V_{OUT}$ | — | — | 20 | V |
| Collector Output Current | $I_{OUT}$ | — | — | 75 | mA |
| Power Dissipation | $P_D$ | Ta ≤ +25 °C (SOP) | — | 620*1 | mW |
| | | Ta ≤ +25 °C (SSOP) | — | 444*2 | mW |
| | | Ta ≤ +25 °C (DIP) | — | 1000 | mW |
| Operating Temperature | $T_{op}$ | — | –30 | +85 | °C |
| Storage Temperature | Tstg | — | –55 | +125 | °C |

*1: The packages are mounted on the epoxy board (4 cm × 4 cm)

*2: The packages are mounted on the epoxy board (10 cm × 10 cm)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Power Supply Voltage | $V_{CC}$ | 3.6 | 6.0 | 18 | V |
| Error Amp. Input Voltage | $V_{IN}$ | 1.05 | — | 1.45 | V |
| Control Input Voltage | $V_{CTL}$ | 0 | — | 18 | V |
| Collector Output Voltage | $V_{OUT}$ | — | — | 18 | V |
| Collector Output Current | $I_{OUT}$ | 0.3 | — | 50 | mA |
| Timing Capacitor | $C_T$ | 150 | — | 15000 | pF |
| Timing Resistor | $R_T$ | 5.1 | — | 100 | kΩ |
| Oscillator Frequency | $f_{OSC}$ | 1 | — | 500 | kHz |
| Operating Temperature | $T_{op}$ | –30 | 25 | 85 | °C |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

(Ta = 25 °C, $V_{CC}$ = 6 V)

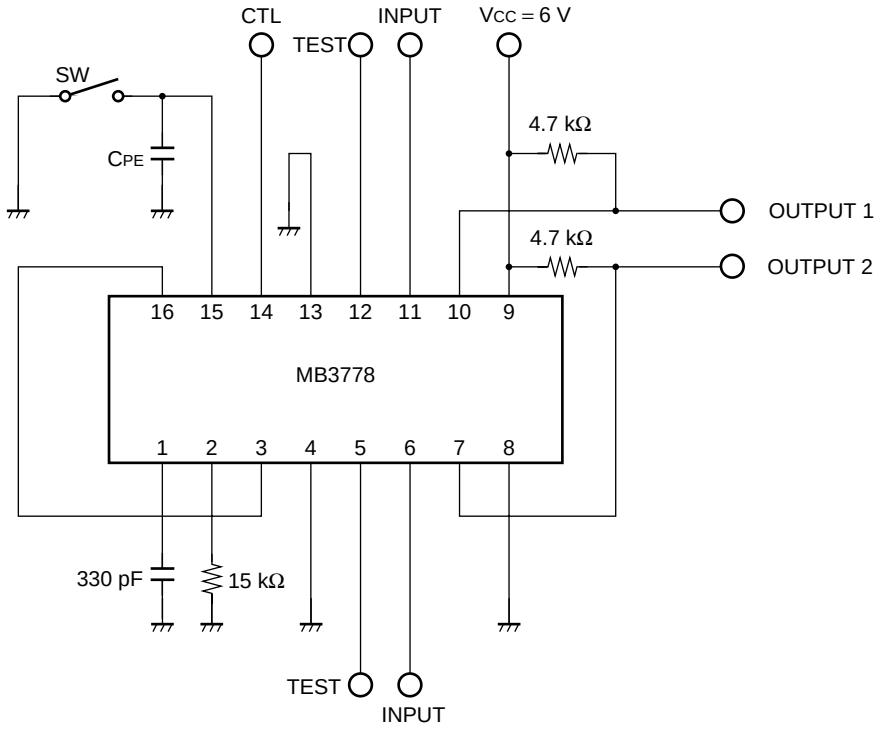
| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| **Reference Block** | | | | | | |
| Output Voltage | $V_{REF}$ | $I_{OR}$ = –1 mA | 2.41 | 2.46 | 2.51 | V |
| Output Temp. Stability | $V_{RTC}$ | Ta = –30 °C to +85 °C | –2 | ±0.2 | 2 | % |
| Input Stability | Line | $V_{CC}$ = 3.6 V to 18 V | — | 2 | 10 | mV |
| Load Stability | Load | $I_{OR}$ = –0.1 mA to –1 mA | — | 1 | 7.5 | mV |
| Short Circuit Output Current | $I_{OS}$ | $V_{REF}$ = 2 V | –30 | –10 | –3 | mA |
| **Under Voltage Lockout Protection Block** | | | | | | |
| Threshold Voltage | $V_{tH}$ | $I_{OR}$ = –0.1 mA | — | 2.72 | — | V |
| | $V_{tL}$ | $I_{OR}$ = –0.1 mA | — | 2.60 | — | V |
| Hysteresis Width | $V_{HYS}$ | $I_{OR}$ = –0.1 mA | 80 | 120 | — | mV |
| Reset Voltage ($V_{CC}$) | $V_R$ | — | 1.5 | 1.9 | — | V |
| **Protection Circuit Block (S.C.P.)** | | | | | | |
| Input Thresold Voltage | $V_{tPC}$ | — | 0.60 | 0.65 | 0.70 | V |
| Input Stand by Voltage | $V_{STB}$ | No pull up | — | 50 | 100 | mV |
| Input Latch Voltage | $V_{IN}$ | No pull up | — | 50 | 100 | mV |
| Input Source Current | $I_{bpc}$ | — | –1.4 | –1.0 | –0.6 | µA |
| Comparator Threshold Voltage | $V_{tC}$ | Pin 5, Pin 12 | — | 2.1 | — | V |
| **Triangular Waveform Oscillator Block** | | | | | | |
| Oscillator Frequency | $f_{OSC}$ | $C_T$ = 330 pF, $R_T$ = 15 kΩ | 160 | 200 | 240 | kHz |
| Frequency Deviation | $f_{dev}$ | $C_T$ = 330 pF, $R_T$ = 15 kΩ | — | ±5 | — | % |
| Frequency Stability ($V_{CC}$) | $f_{dV}$ | $V_{CC}$ = 3.6 V to 18 V | — | ±1 | — | % |
| Frequency Stability (Ta) | $f_{dT}$ | Ta = –30 °C to +85 °C | –4 | — | +4 | % |
| **Dead-Time Control Block (D.T.C.)** | | | | | | |
| Input Bias Current | $I_{bdt}$ | — | — | 0.2 | 1 | µA |
| Latch Mode Sink Current | $I_{dt}$ | $V_{dt}$ = 2.5 V | 150 | 500 | — | µA |
| Latch Input Voltage | $V_{dt}$ | $I_{dt}$ = 100 µA | — | — | 0.3 | V |

## ■ ELECTRICAL CHARACTERISTICS (Continued)

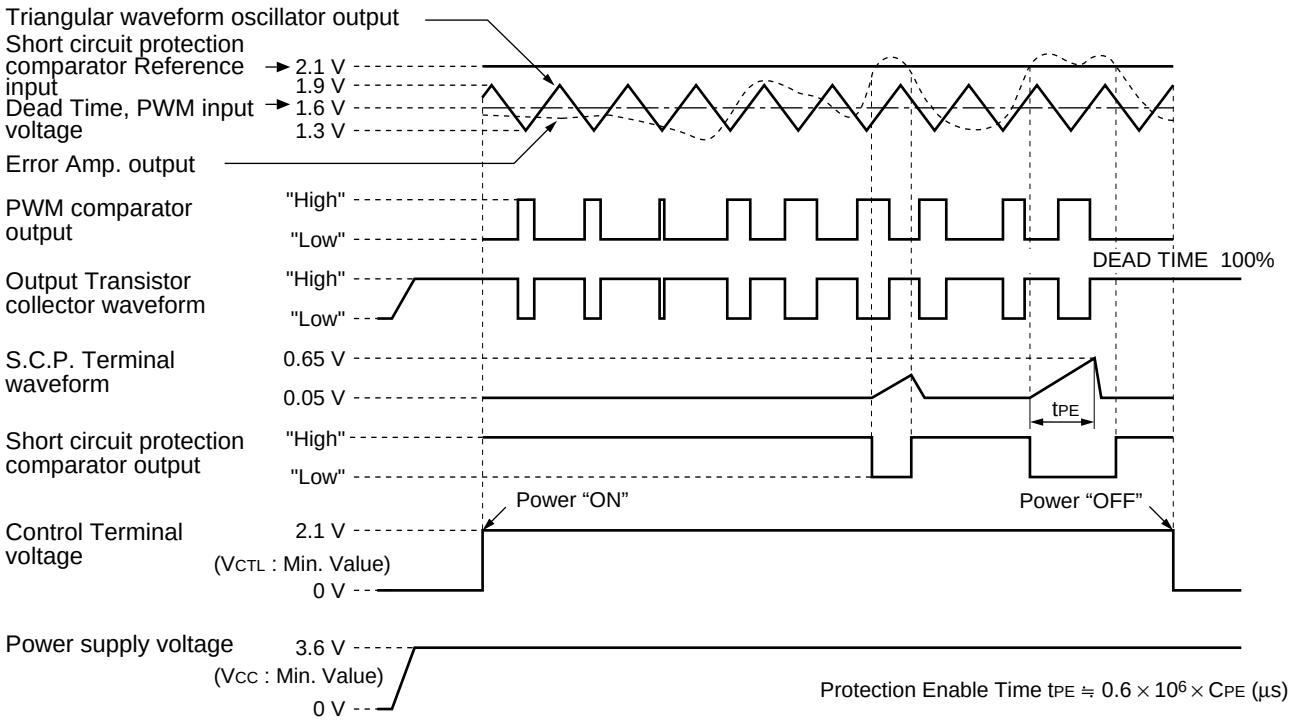
(Ta = 25 °C, $V_{CC}$ = 6 V)

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| **Error Amp. Block** | | | | | | |
| Input Offset Voltage | $V_{IO}$ | $V_O$ = 1.6 V | –6 | — | 6 | mV |
| Input Offset Current | $I_{IO}$ | $V_O$ = 1.6 V | –100 | — | 100 | nA |
| Input Bias Current | $I_B$ | $V_O$ = 1.6 V | –500 | –100 | — | nA |
| Common Mode Input Voltage Range | $V_{ICR}$ | $V_{CC}$ = 3.6 V to 18 V | 1.05 | — | 1.45 | V |
| Voltage Gain | $A_V$ | $R_{NF}$ = 200 kΩ | 70 | 80 | — | dB |
| Frequency Band Width | BW | $A_V$ = 0 dB | — | 1.0 | — | MHz |
| Common Mode Rejection Ratio | CMRR | — | 60 | 80 | — | dB |
| Max. Output Voltage Width | $V_{OM+}$ | — | $V_{REF}$ – 0.3 | — | — | V |
| | $V_{OM-}$ | — | — | 0.7 | 0.9 | V |
| Output Sink Current | $I_{OM+}$ | $V_O$ = 1.6 | — | 1.0 | — | mA |
| Output Source Current | $I_{OM-}$ | $V_O$ = 1.6 | — | –60 | — | µA |
| **PWM Comparator Block** | | | | | | |
| Input Threshold Voltage ($f_{OSC}$ = 10 kHz) | $V_{t100}$ | Duty Cycle = 100% | — | 1.9 | 2.25 | V |
| | $V_{t0}$ | Duty Cycle = 0% | 1.05 | 1.3 | — | V |
| On duty Cycle | $D_{tr}$ | $V_{dt} = V_{REF}/1.45$ | 55 | 65 | 75 | % |
| Input Sink Current | $I_{IN+}$ | Pin 5, Pin 12 = 1.6 V | — | 1.0 | — | mA |
| Input Source Current | $I_{IN-}$ | Pin 5, Pin 12 = 1.6 V | — | –60 | — | µA |
| **Control Block** | | | | | | |
| Input Off Condition | $V_{OFF}$ | — | — | — | 0.7 | V |
| Input On Condition | $V_{ON}$ | — | 2.1 | — | — | V |
| Control Terminal Current | $I_{CTL}$ | $V_{CTL}$ = 10 V | — | 200 | 400 | µA |
| **Output Block** | | | | | | |
| Output Leak Current | Leak | $V_O$ = 18 V | — | — | 10 | µA |
| Output Saturation Voltage | $V_{SAT}$ | $I_O$ = 50 mA | — | 1.1 | 1.4 | V |
| **All Device Block** | | | | | | |
| Stand-by Current | $I_{CCS}$ | $V_{CTL}$ = 0 V | — | — | 10 | µA |
| Average Supply Current | $I_{CCa}$ | $V_{CTL} = V_{CC}$, No Output Load | — | 1.7 | 2.4 | mA |

## ■ TEST CIRCUIT

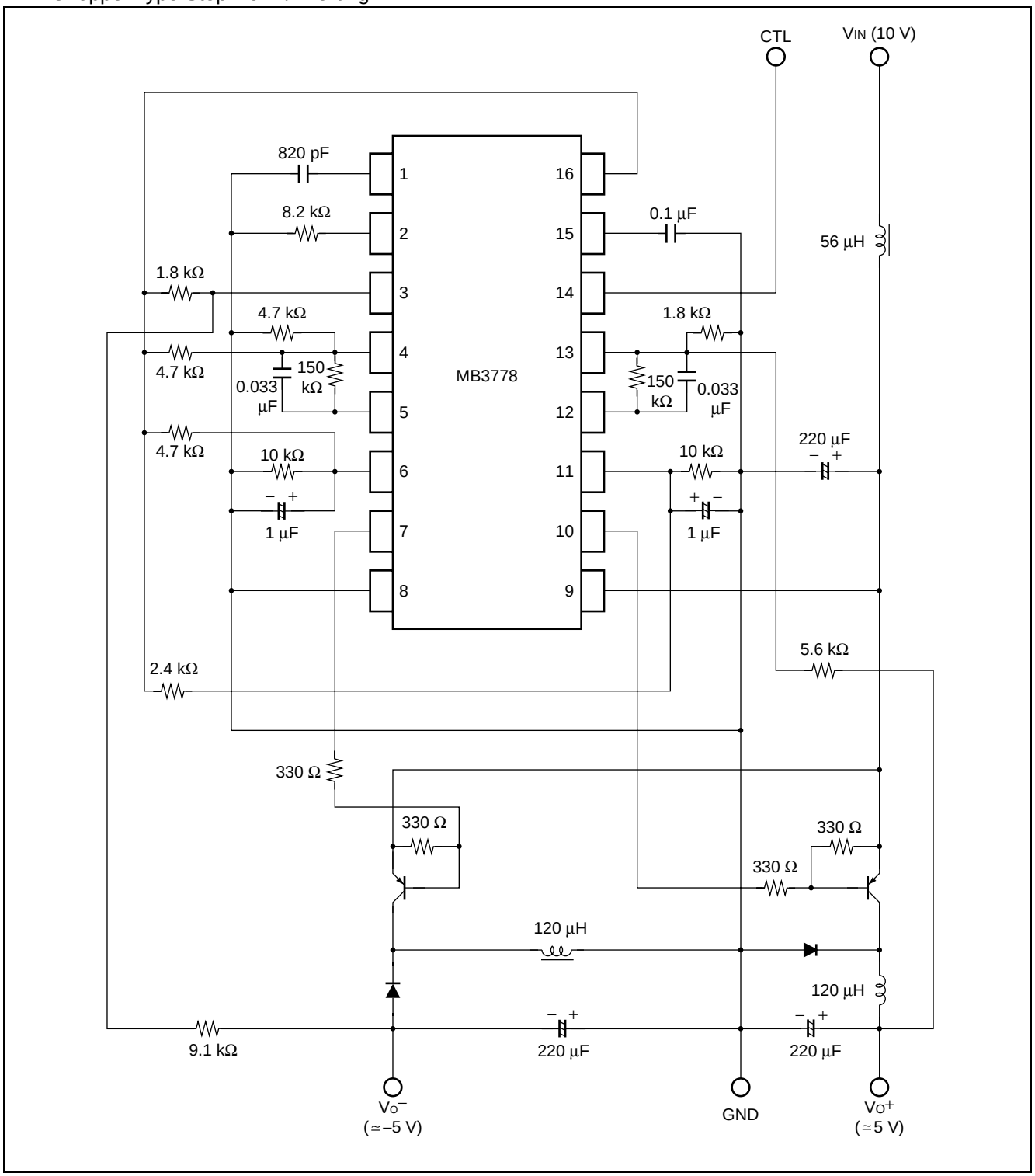



## ■ TIMING CHART (Internal Waveform)

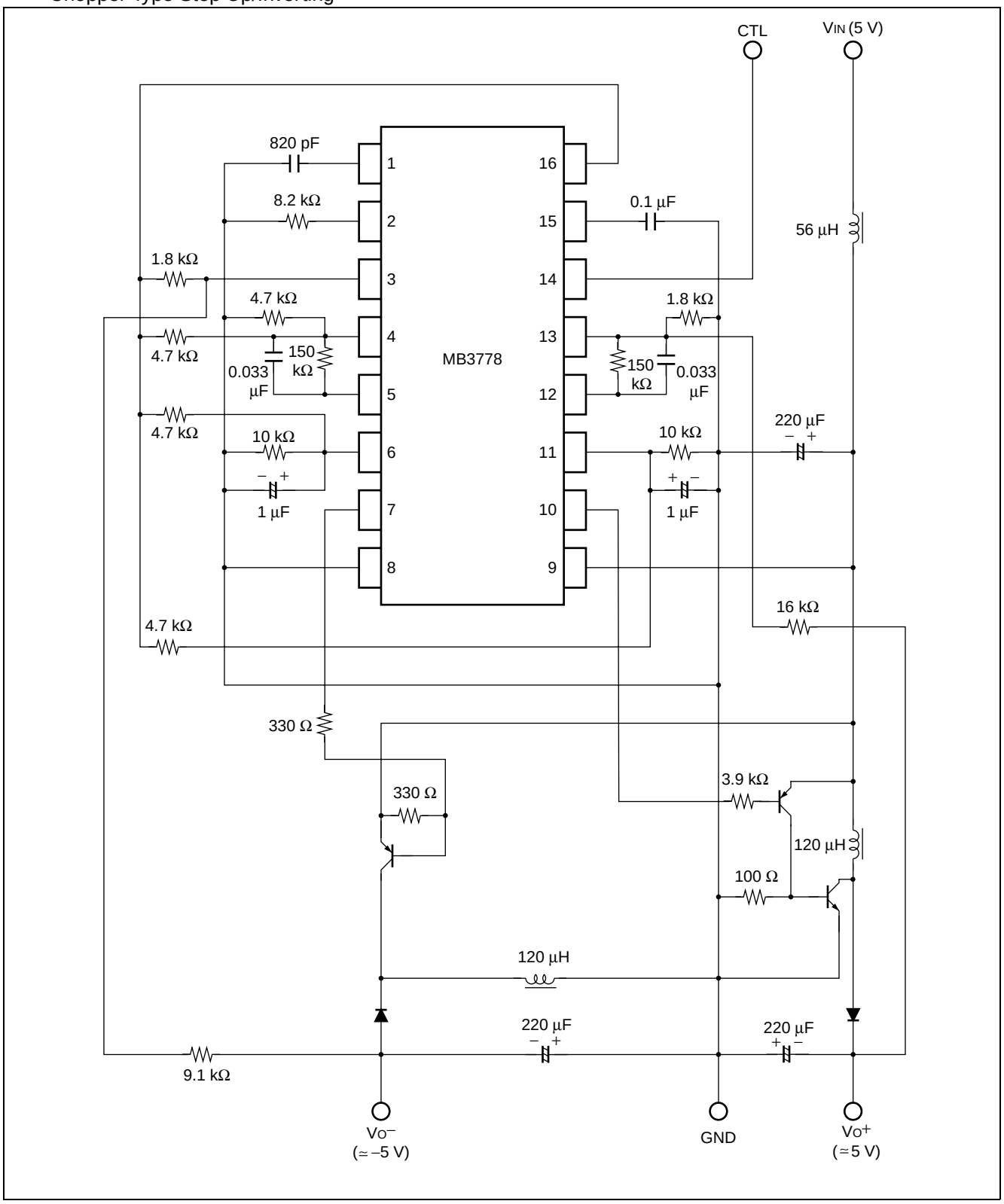


## ■ APPLICATION CIRCUIT

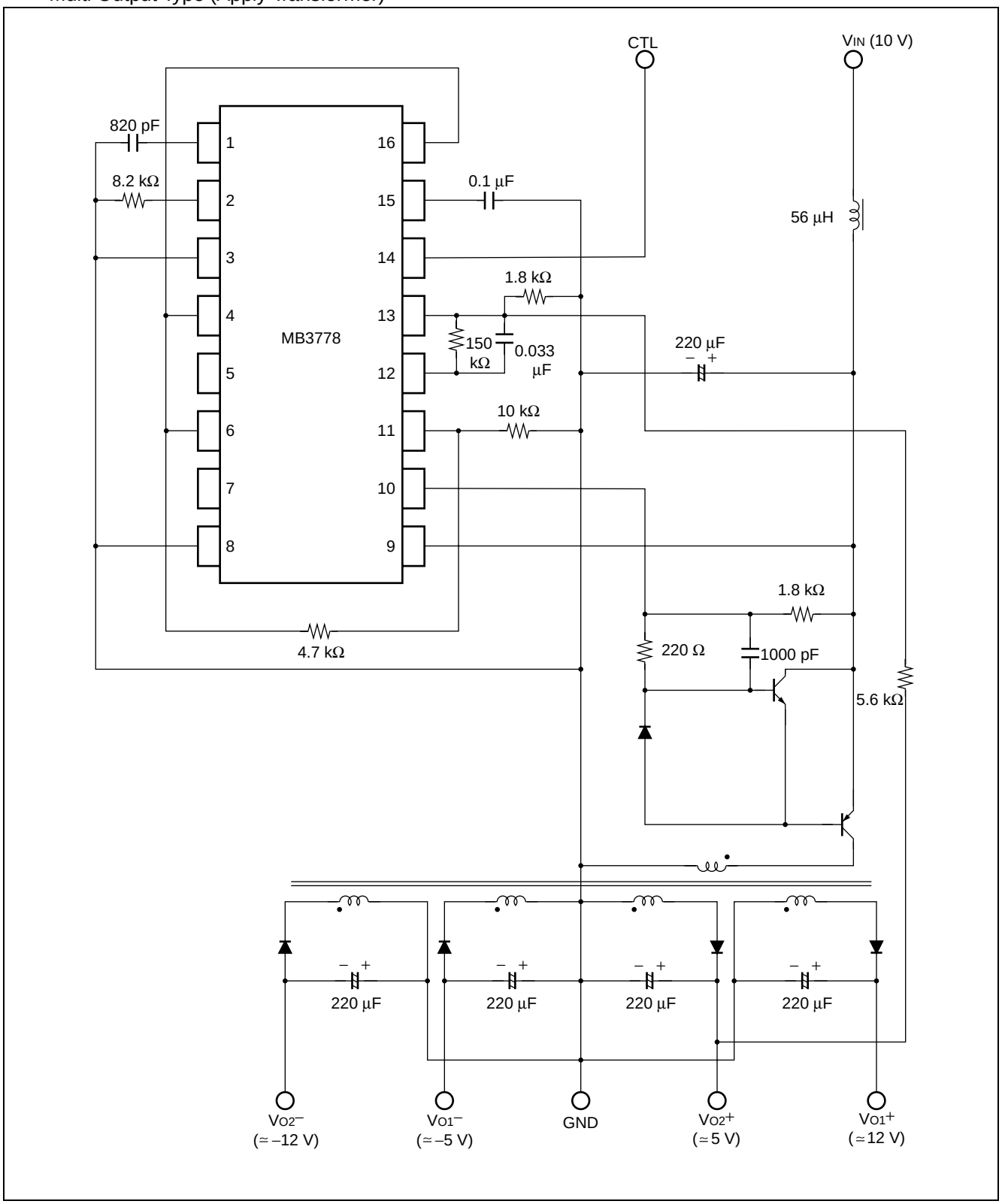
- Chopper Type Step Down/inverting



- Chopper Type Step Up/Inverting



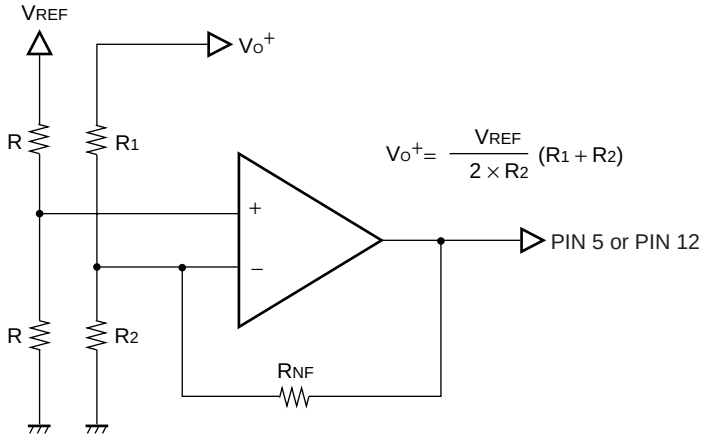
- Multi Output Type (Apply Transformer)



## ■ HOW TO SET THE OUTPUT VOLTAGE

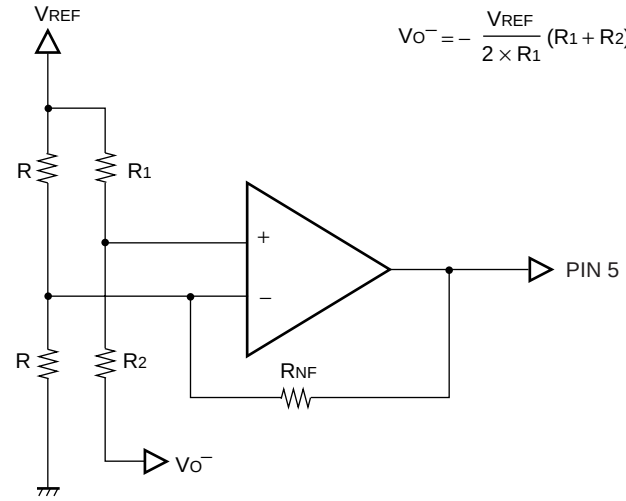
The output voltage is set using the connections shown in “Connection of error Amp. Output Voltage $V_O \geq 0$” and “Connection of Error Amp. Output Voltage $V_O < 0$”.
The error amplifier power is supplied by the reference voltage circuit as is that of the other internal circuits. The common mode input voltage range is from 1.05 V to 1.45 V.
Set 1.23 V ($V_{REF}/2$) as the reference input voltage that is connected to either inverting or non-inverting input terminals.

- Connection of Error Amp. Output Voltage $V_O \geq 0$




$$V_O^+ = \frac{V_{REF}}{2 \times R_2}(R_1 + R_2)$$

- Connection of Error Amp. Output Voltage $V_O < 0$




$$V_O^- = -\frac{V_{REF}}{2 \times R_1}(R_1 + R_2) + V_{REF}$$

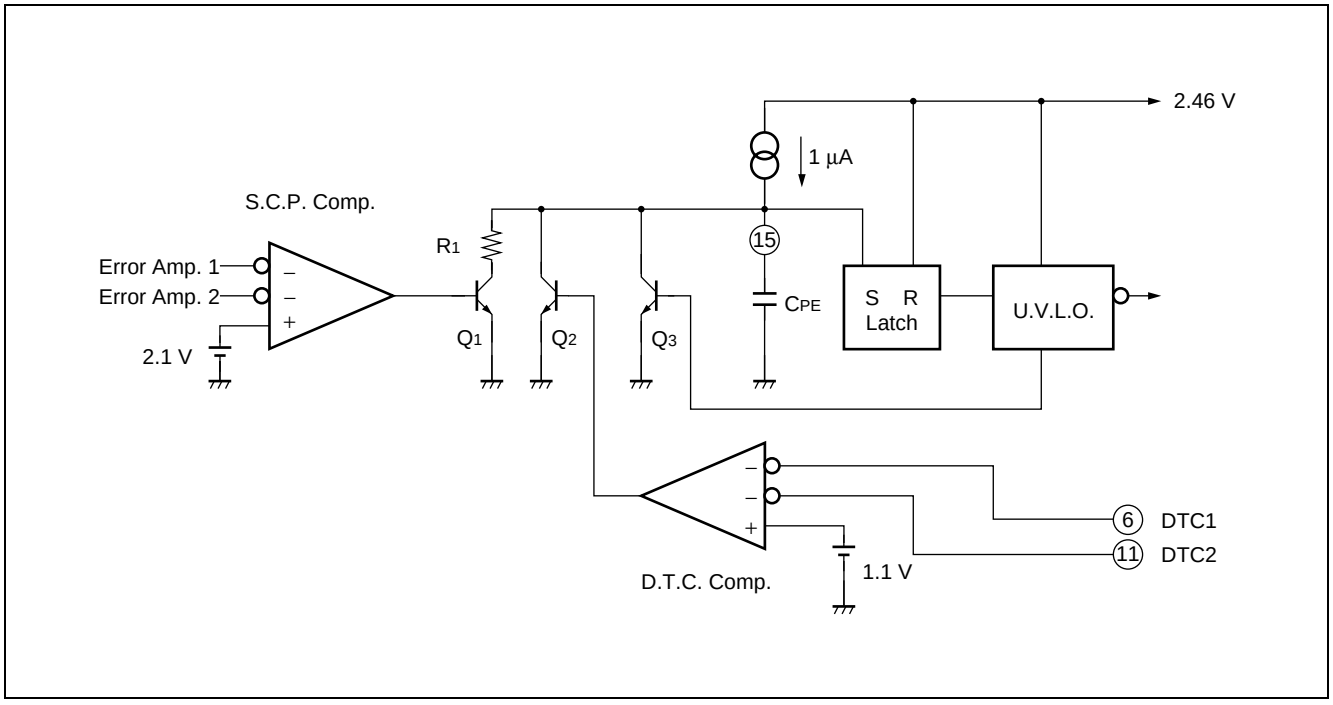
## ■ HOW TO SET TIME CONSTANT FOR TIMER LATCH SHORT-CIRCUIT PROTECTION CIRCUIT

Below Figure shows the configuration of the protection latch circuit.
Each error amplifier output is connected to the inverting inputs of the short-circuit protection comparator and is always compared with the reference voltage (2.1 V) connected to the non-inverting input.
When the load condition of the switching regulator is stable, the error amplifier has no output fluctuation. Thus, short-circuit protection control is also kept in balance, and the SCP terminal (pin 15) voltage is held at about 50 mV.
If the load changes drastically due to a load short-circuit and if the inverting inputs of the short-circuit protection comparator go above 2.1 V, the short-circuit protection comparator output goes “Low” to turn off transistor $Q_1$. The SCP terminal voltage is discharged, and then the short-circuit protection comparator charges the protection enable capacitor $C_{PE}$ according to the following formula :

$$V_{PE} = 50\ mV + t_{PE} \times 10^{-6} / C_{PE}$$
$$0.65 = 50\ mV + t_{PE} \times 10^{-6} / C_{PE}$$
$$C_{PE} = t_{PE} / 0.6\ (\mu F)$$

When the protection enable capacitor is charged to about 0.65 V, the protection latch is set to enable the under voltage lockout circuit and the output drive transistor is turned off. The idle period is also set to 100% at the same time.
Once the under voltage lockout circuit is enabled, the protection enable is released; however, the protection latch is not reset if the power is not turned off.
The inverting inputs (pin 6 or 11) of the D.T.C. comparator are compared to the reference voltage (about 1.1 V) connected to the non-inverting input.
To prevent malfunction of the short-circuit protection-circuit when the soft-start operation is done by using the DTC terminal, the D.T.C. comparator outputs a “High” level while the DTC terminal goes up to about 1.1 V, and then closes the SCP terminal by turning transistor $Q_2$ on.

• Protection Latch Circuit



## ■ SETTING THE IDLE PERIOD

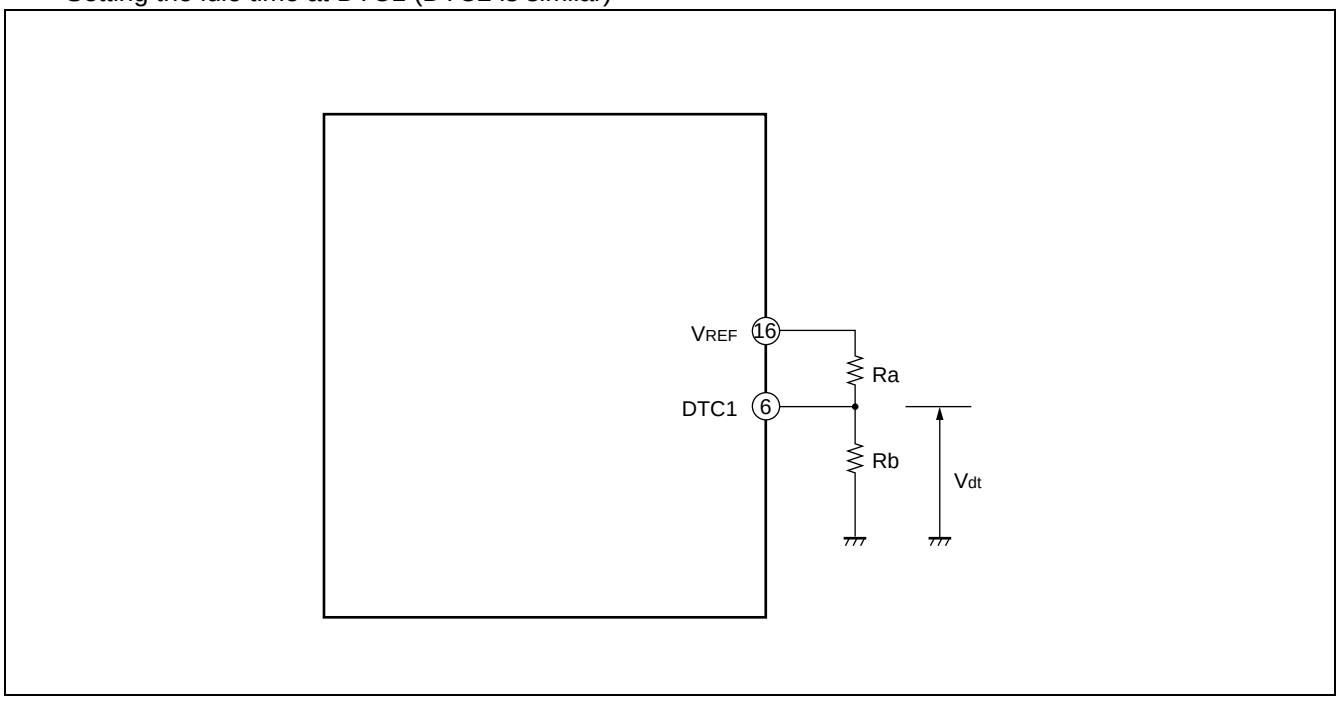
When voltage step-up, fly-back step-up or inverted output are set, the voltage at the FB terminal may go higher than the triangular wave voltage due to load fluctuation, etc. In this case the output transistor will be in full-on state(ON duty 100%). This can be prevented by setting the maximum duty for the output transistor. This is done by setting the DTC1 terminal (pin 6) voltage using resistance division of the $V_{REF}$ voltage as illustrated below.

When the DTC1 terminal voltage is higher than the triangular waveform voltage, the output transistor is turned on. If the triangular waveform amplitude specified by the maximum duty calculation formula is 0.6 V, and the lower voltage limit of the triangular waveform is 1.3 V, the formula would be as follows (other channels are similar) :

Duty (ON) max (%) $\fallingdotseq (V_{dt} - 1.3\ V) / 0.6\ V \times 100$, $V_{dt}\ (V) = Rb / (Ra + Rb) \times V_{REF}$

Also, if no output duty setting is required, the voltage should be set greater than the upper limit voltage of the triangular waveform, which is 1.9 V.

- Setting the idle time at DTC1 (DTC2 is similar)



## ■ SETTING THE SOFT START TIME

When power is switched on, the current begins charging the capacitor ($C_{DTC1}$) connected the DTC1 terminal (pin 6). The soft start process operates by comparing the soft start setting voltage, which is proportional to the DTC1 terminal voltage, with the triangular waveform, and varying the ON-duty of the OUT terminal (pin 7).

The soft start time until the ON duty reaches 50% is determined by the following equation:

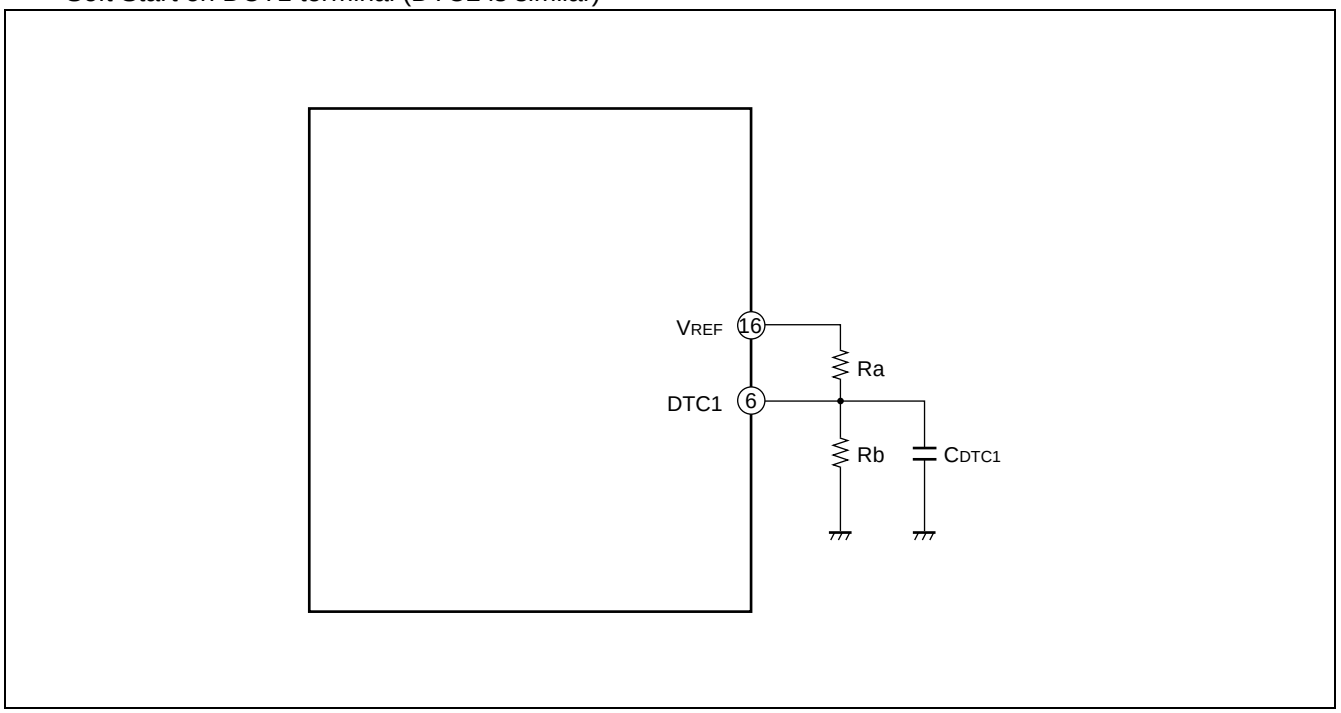
Soft start time (time until output ON duty = 50%) .

$$ts\ (s) \fallingdotseq -C_{DTC1} \times Ra \times Rb\ /\ (Ra + Rb) \times \ln (1 - 1.6\ (Ra + Rb)\ /\ (2.46\ Rb))$$

For example, if Ra = 4.7 kΩ and Rb = 10 kΩ, the result is:

$$ts\ (s) \fallingdotseq 0.1 \times C_{DTC1}\ (\mu F)$$

- Soft Start on DCT1 terminal (DTC2 is similar)

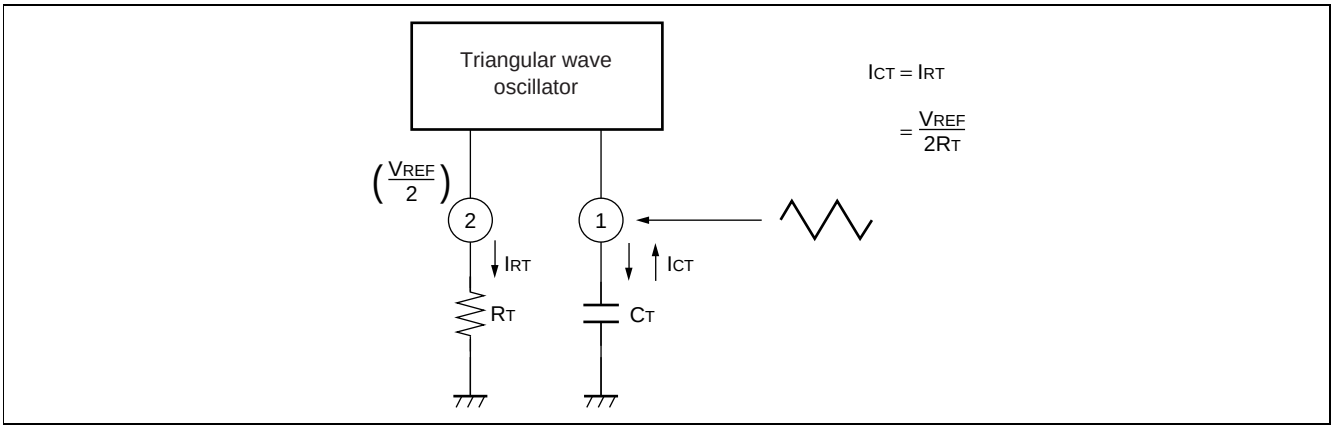


## ■ USING THE $R_T$ TERMINAL

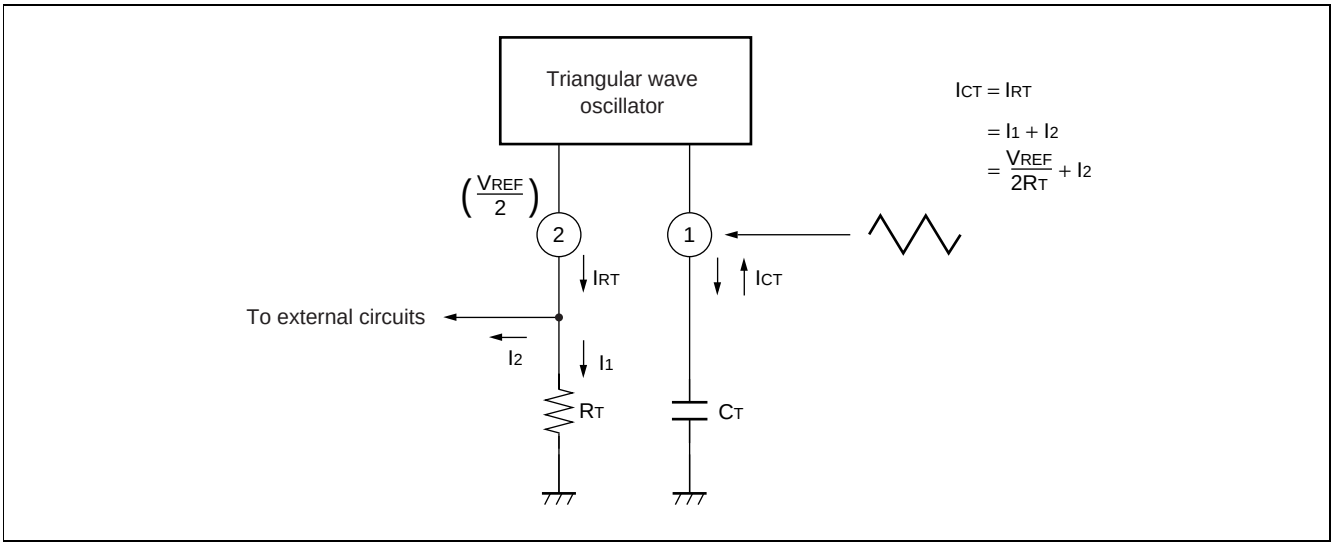
The triangular waves, as shown in Figure “No $V_{REF}/2$ connection to external circuits from $R_T$ terminal”, act to set the oscillator frequency by charging and discharging the capacitor connected to the $C_T$ terminal using the current value of the resistor connected to the $R_T$ terminal.

In addition, when voltage level $V_{REF}/2$ is output to external circuits from the RT terminal, care must be taken in making the external circuit connections to adjust for the fact that $I_1$ is increased by the value of the current $I_2$ to the external circuits in determining the oscillator frequency (see Figure “$V_{REF}/2$ connection to external circuits from $R_T$ terminal”).

**• No $V_{REF}/2$ connection to external circuits from $R_T$ terminal**



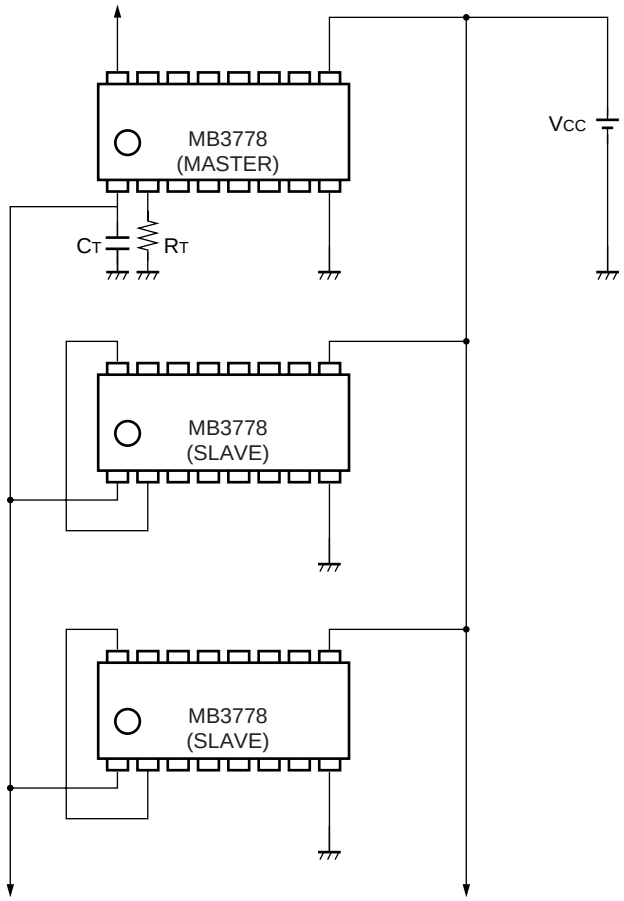

**• $V_{REF}/2$ connection to external circuits from $R_T$ terminal**



## ■ SYNCHRONIZATION OF ICs

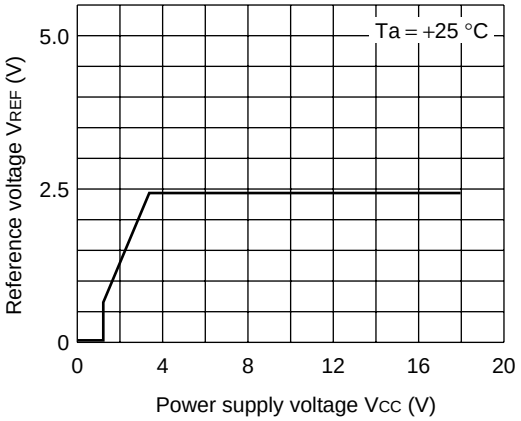
A fixed condenser and resistor are inserted in the $C_T$ and $R_T$ terminals of IC which becomes a master when synchronizing by using plurality of MB3778. As a result, the slave ICs oscillate automatically. The $R_T$ terminals (pin 2) of the slave ICs are connected to the $V_{REF}$ terminal (pin 16) to disable the charge/discharge circuit for triangular wave oscillation. The $C_T$ terminals of the master and slave ICs are connected together.

• Connection of Master, Slave

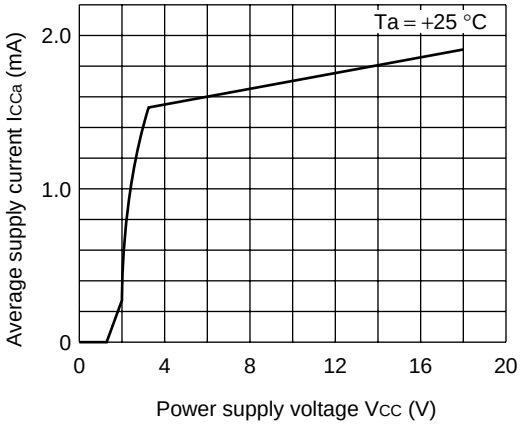


## ■ TYPICAL CHARACTERISTICS

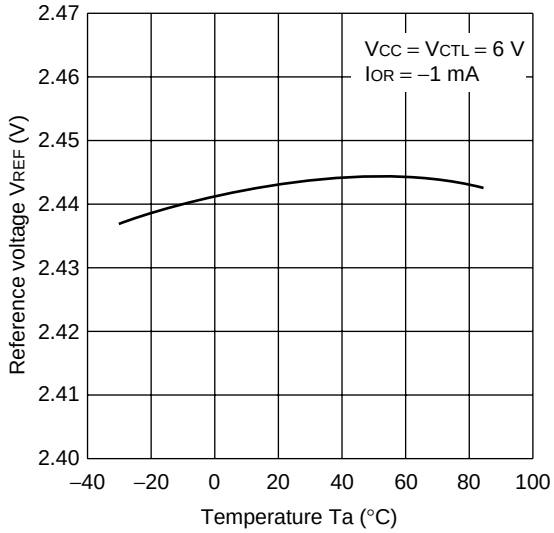
**Power supply voltage vs. Reference voltage**



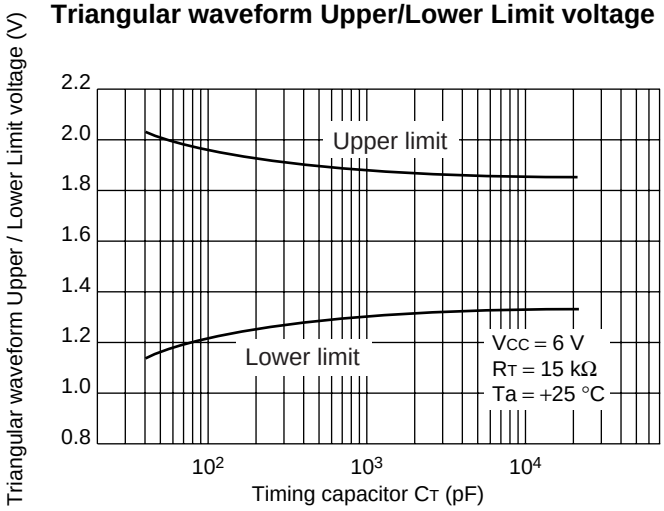

**Power supply voltage vs. Average supply current**



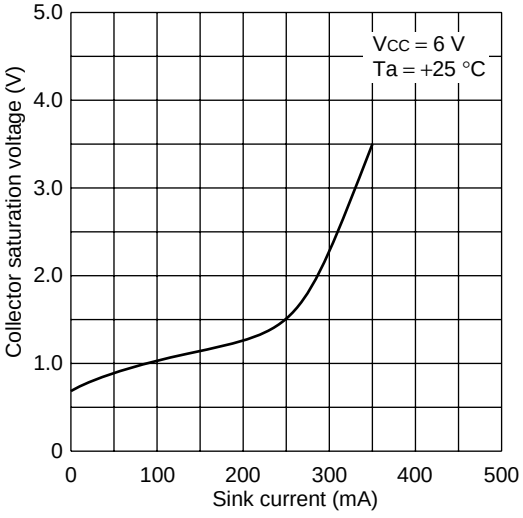

**Reference voltage vs. Temperature**



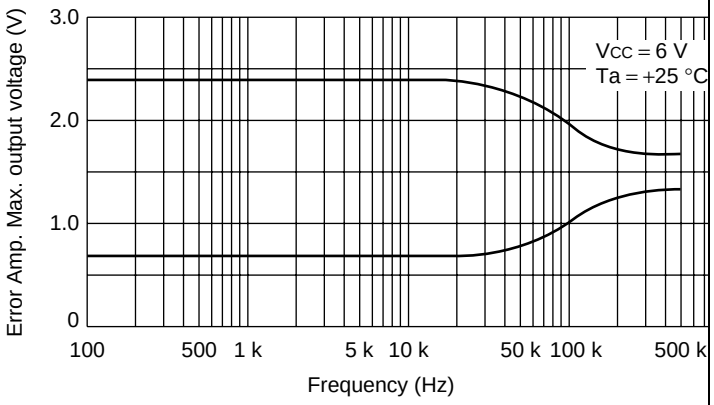

**Timing capacitor vs. Triangular waveform Upper/Lower Limit voltage**




**Collector saturation voltage vs. Sink Current**

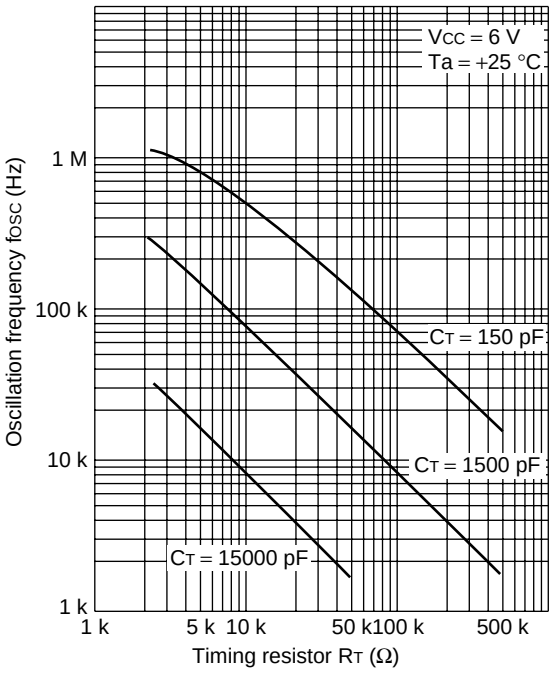



**Error Amp. Max. output voltage vs. Frequency**

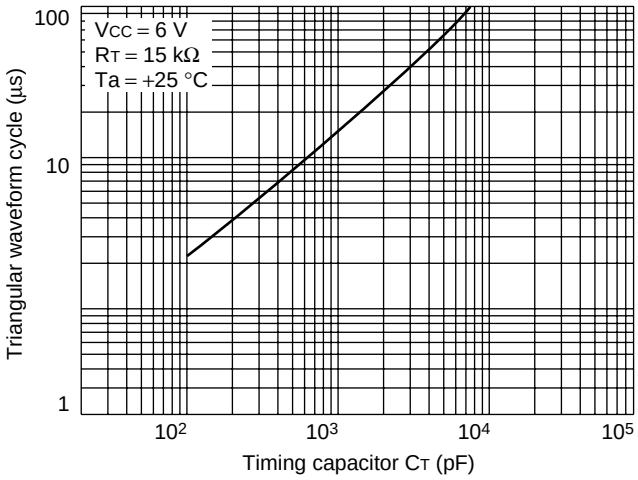


*(Continued)*

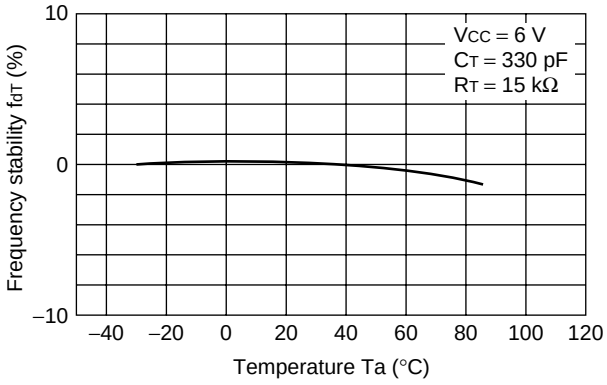
**Timing resistor vs. Oscillation frequency**



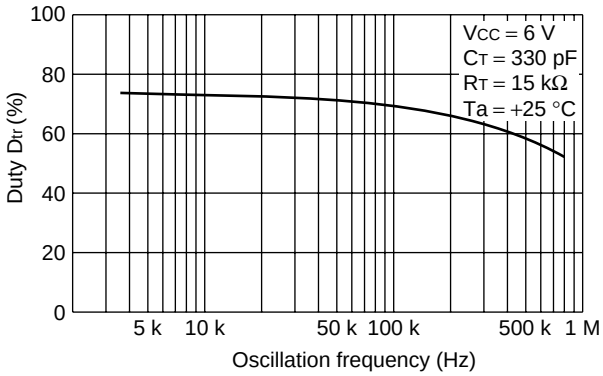

**Triangular waveform cycle vs. Timing capacitor**



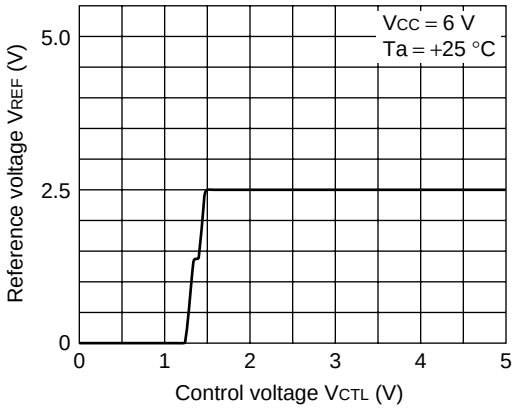

**Temperature vs. Frequency stability**



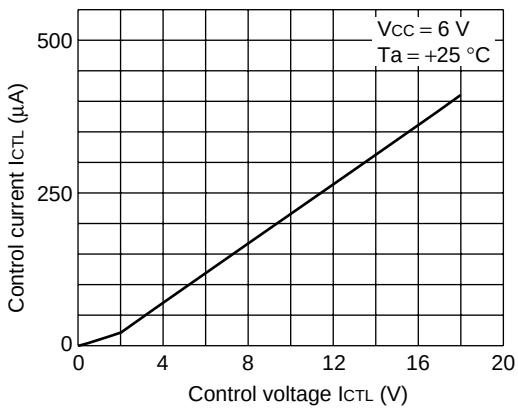

**Oscillation frequency vs. Duty**




**Control voltage vs. Reference voltage**

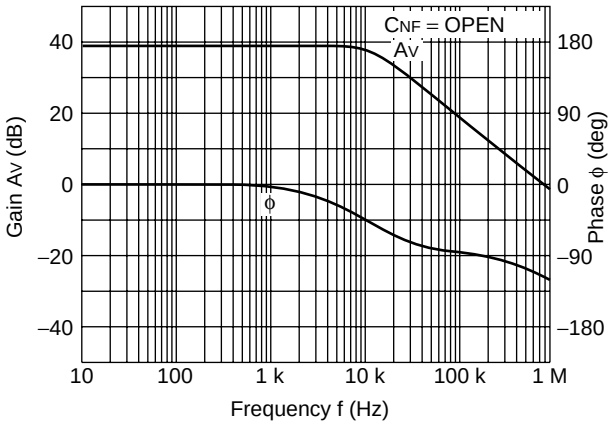



**Control input current**

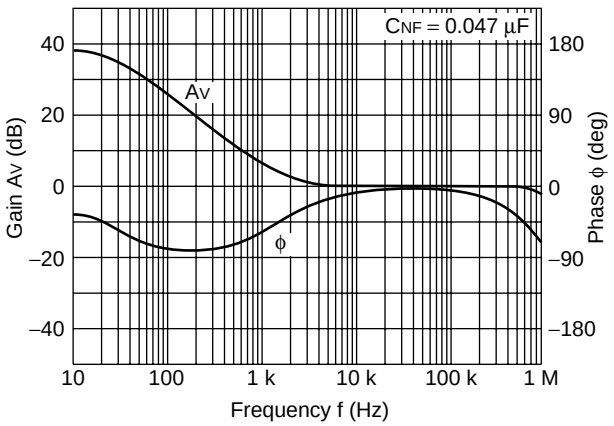


*(Continued)*

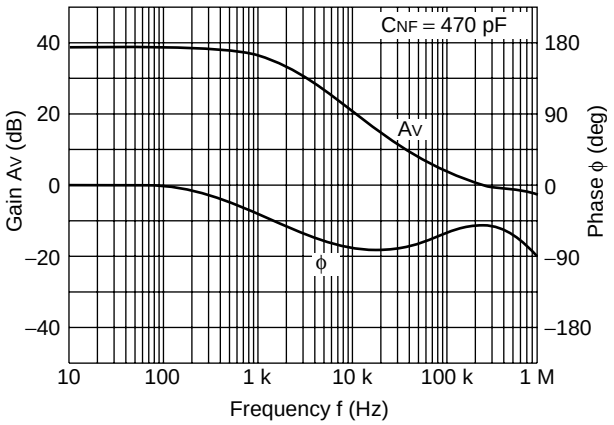
**Frequency vs. Gain/Phase**



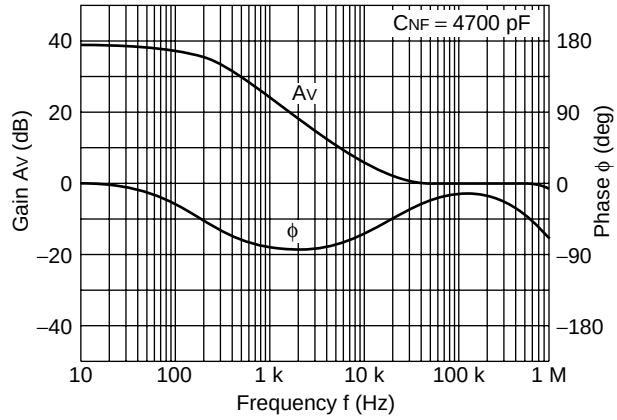

**Frequency vs. Gain/Phase (Actual Data)**



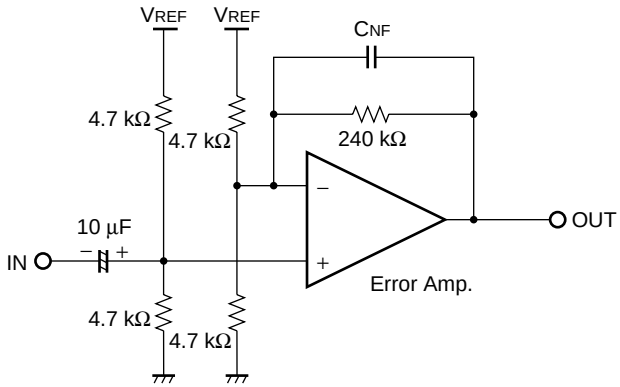

**Frequency vs. Gain/Phase (Actual Data)**




**Frequency vs. Gain/Phase (Actual Data)**

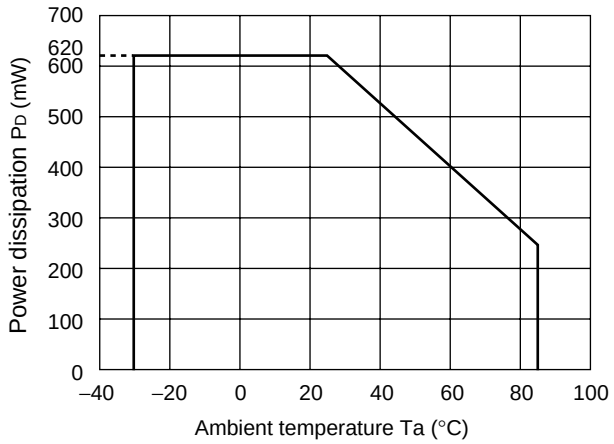



**Actual Circuit**

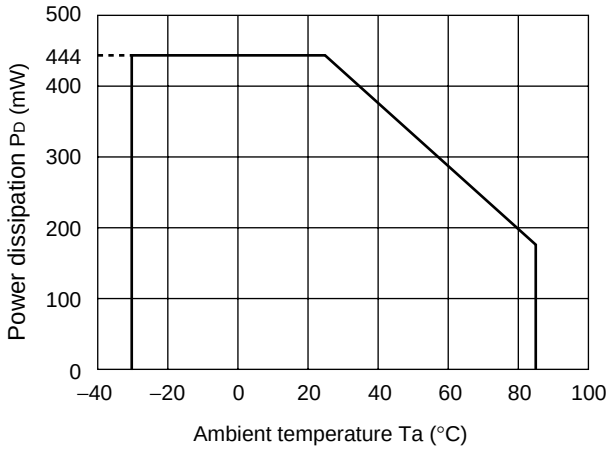


*(Continued)*

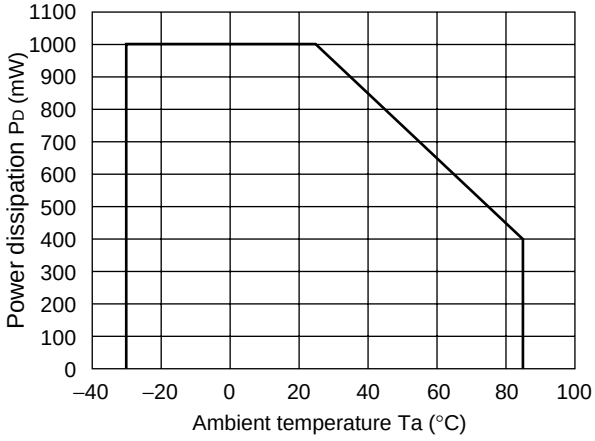
**Power Dissipation vs. Ambient Temperature (SOP)**




**Power Dissipation vs. Ambient Temperature (SSOP)**




**Power Dissipation vs. Ambient Temperature (DIP)**



## ■ APPLICATION

### 1. Equivalent series resistor and stability of smoothing capacitor

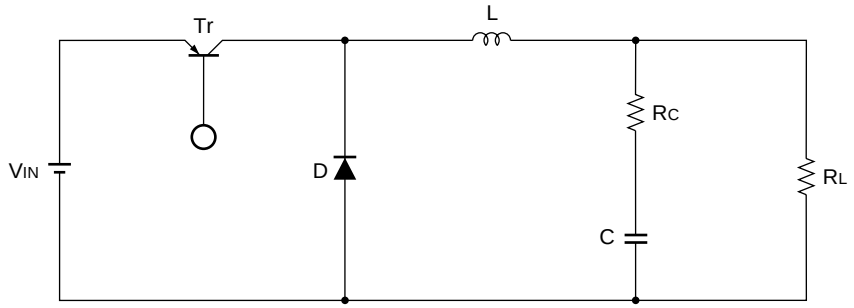
The equivalent series resistor (ESR) of the smoothing capacitor in the DC/DC converter greatly affects the loop phase characteristic.

The stability of the system is improved so that the phase characteristic may advance the phase to the ideal capacitor by ESR in the high frequency region (see “Gain vs. Frequency” and “Phase vs. Frequency”).

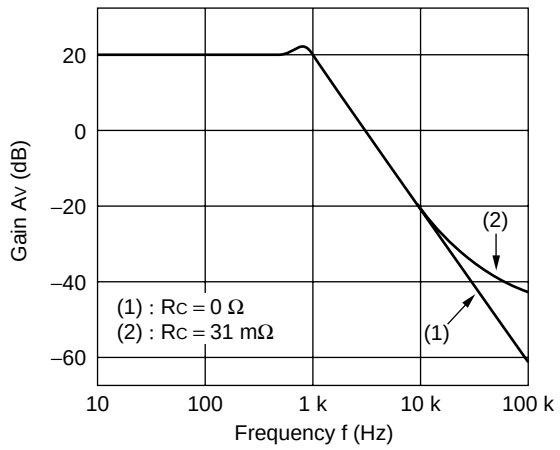
A smoothing capacitor with a low ESR reduces system stability. Use care when using low ESR electrolytic capacitors (OS CON™) and tantalum capacitors.

Note: OS CON is the trademark of Sanyo Electnic Co., Ltd.

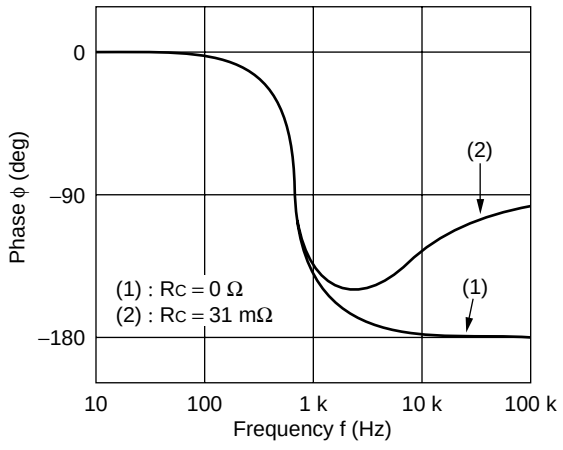
**DC/DC Converter Basic Circuit**




**Gain vs. Frequency**



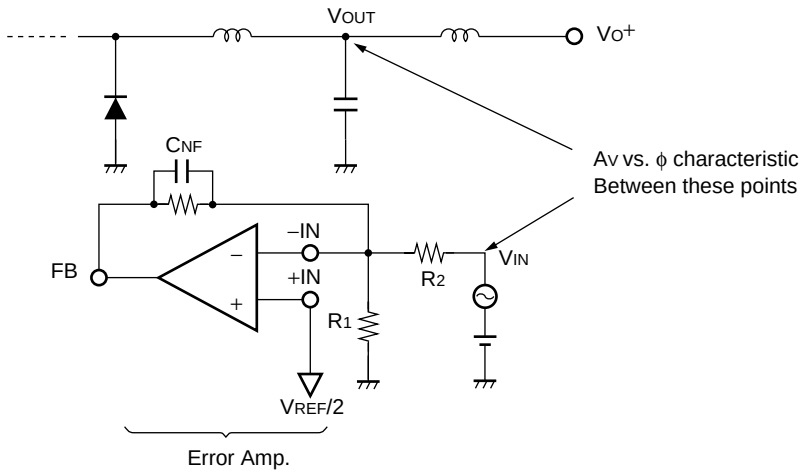

**Phase vs. Frequency**



**Reference data**

If an aluminum electrolytic smoothing capacitor (RC ≅ 1.0 Ω) is replaced with a low ESR electrolytic capacitor(OS CON™ : RC ≅ 0.2 Ω), the phase margin is reduced by half(see Fig. 37 and 38).

**DC/DC Converter $A_V$ vs. ϕ characteristic Test Circuit**




**DC/DC Converter +5 V output Gain vs. Phase**

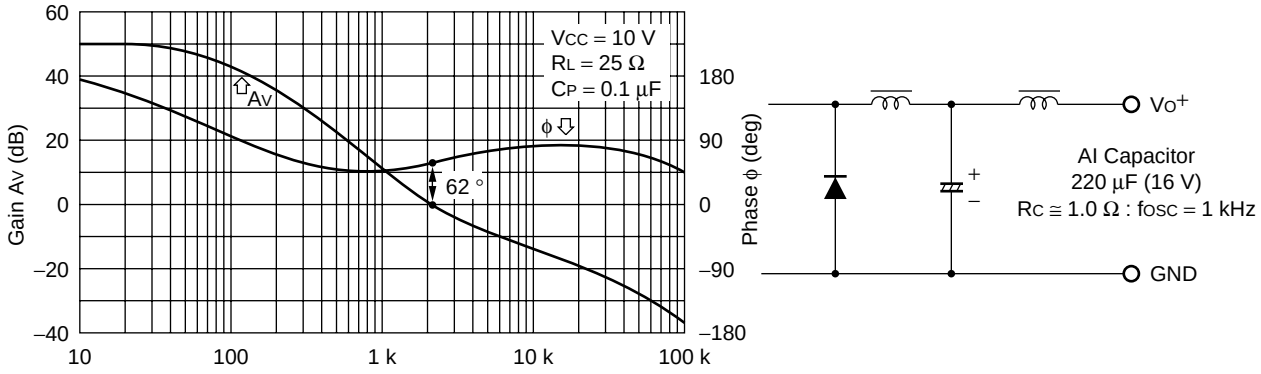
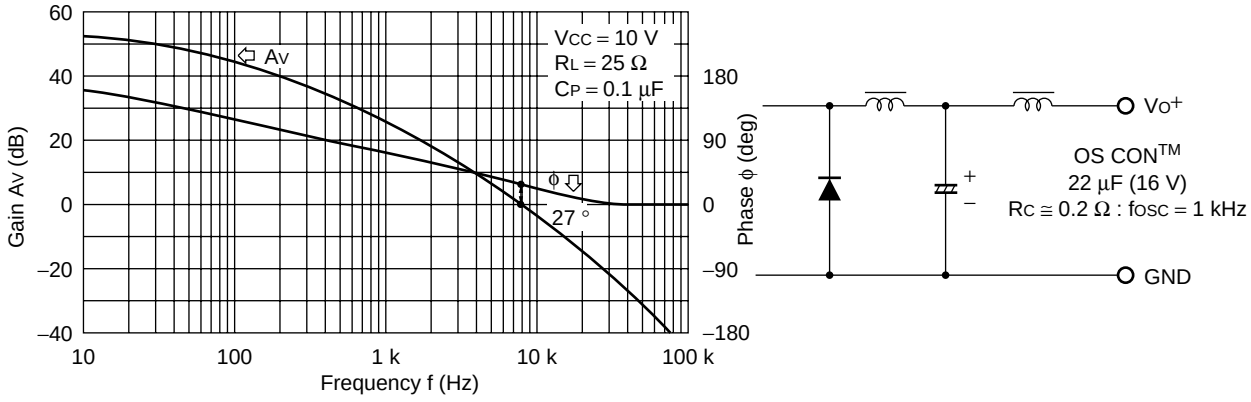



**Figure 38 DC/DC Converter +5 V output Gain vs. Phase**

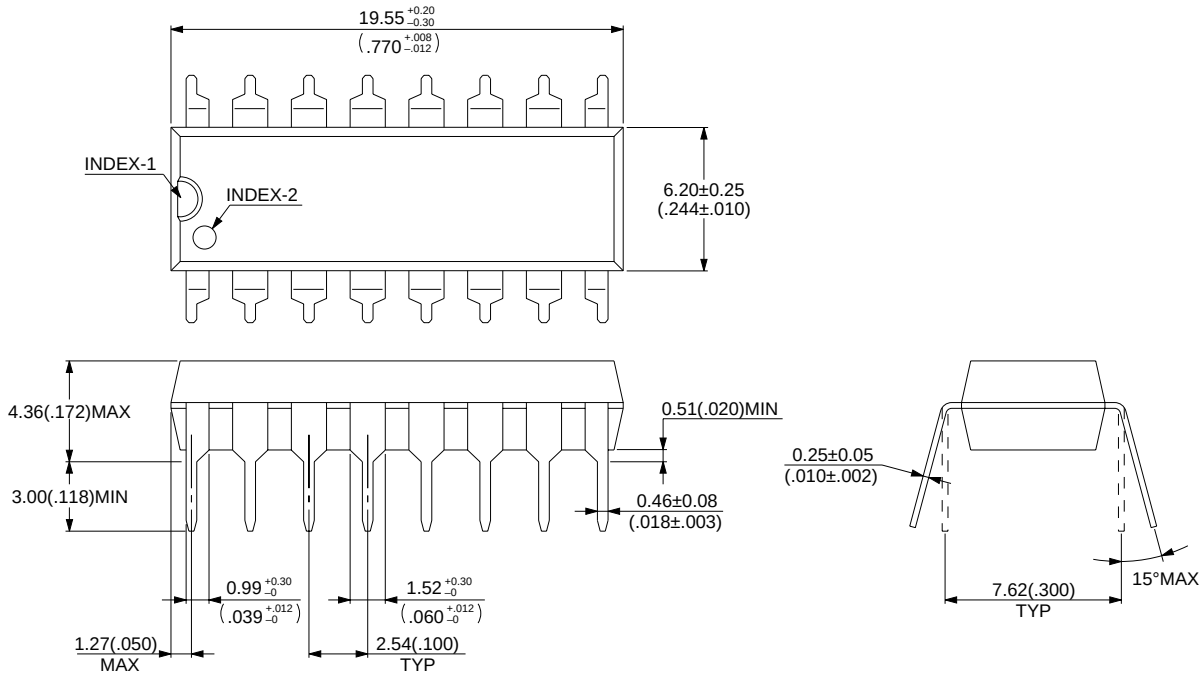


## ■ ORDERING INFORMATION

| Part number | **Package** | **Remarks** |
|---|---|---|
| MB3778P | 16-pin Plastic DIP<br>(DIP-16P-M04) | |
| MB3778PFV | 16-pin Plastic SSOP<br>(FPT-16P-M05) | |
| MB3778PF | 16-pin Plastic SOP<br>(FPT-16P-M06) | |

## ■ PACKAGES DIMENSION

16-pin, Plastic DIP
(DIP-16P-M04)



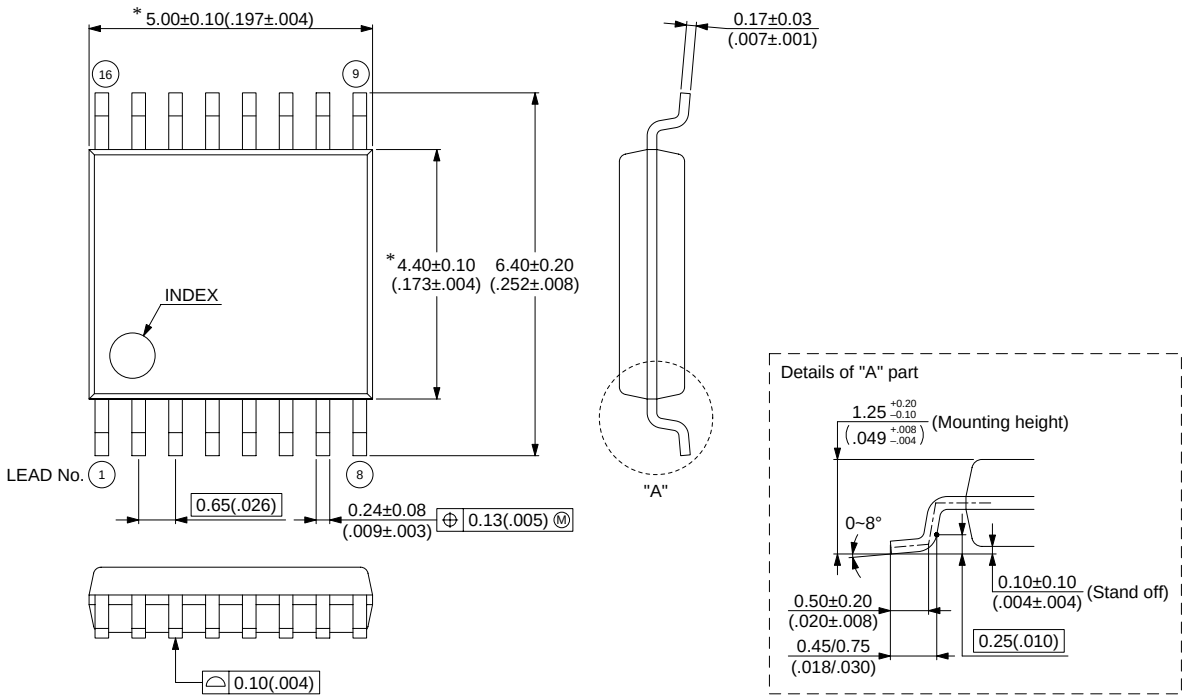



Dimensions in mm (inches) .

*(Continued)*

*(Continued)*

16-pin, Plastic SSOP
(FPT-16P-M05)



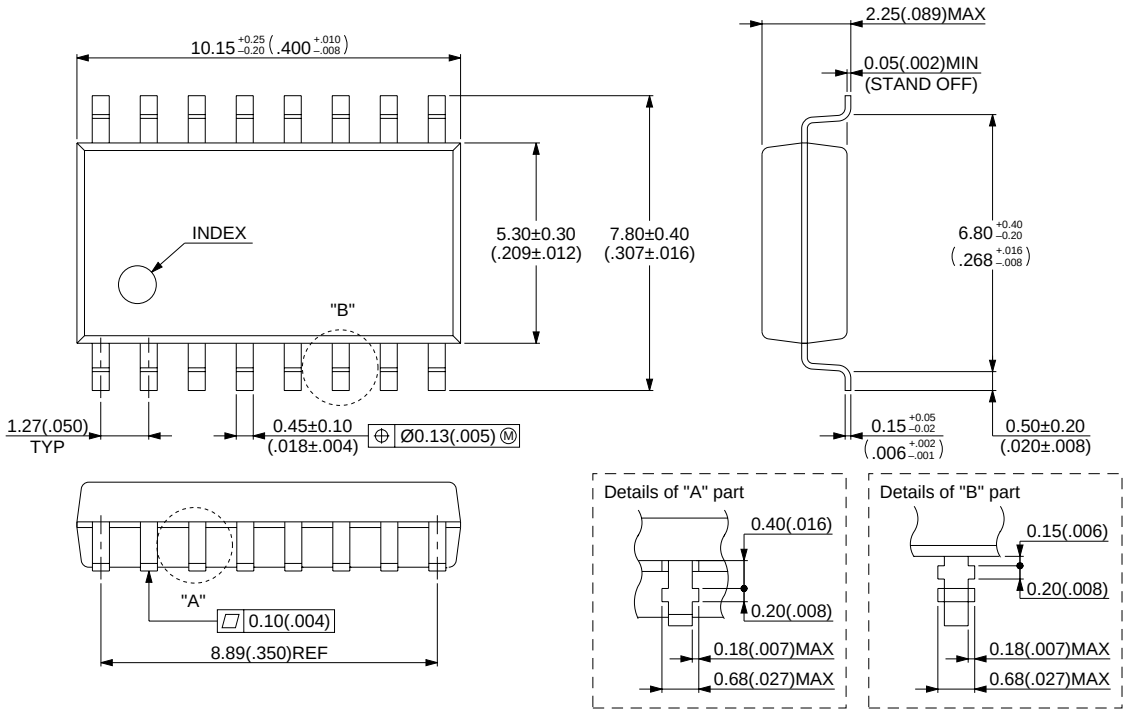



Dimensions in mm (inches) .

*(Continued)*

*(Continued)*

16-pin, Plastic SOP
(FPT-16P-M06)






Dimensions in mm (inches) .

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