Micro Linear

PRELIMINARY

ML2751 Power Amplifier and LNA

GENERAL DESCRIPTION

The 2751 is a 900 MHz ISM band radio front-end intended for use in half duplex radio applications such as cordless phones and FCC Part 15 compliant devices. It integrates a power amplifier (PA), a Low Noise Amplifier (LNA), Pin Diode drivers for an external transmit/receive switch, and control circuits. The 100mW power amplifier has output power control with a >20dB range. The ML2751 can be used to increase battery life and offers output power ramp control in TDMA applications. An internal LNA eliminates the need for a discrete design. PIN diode drivers control the transmit/receive switch directly. Internal logic individually enables the LNA, PA, and PIN diode drivers. A power down mode to minimize current consumption is included.

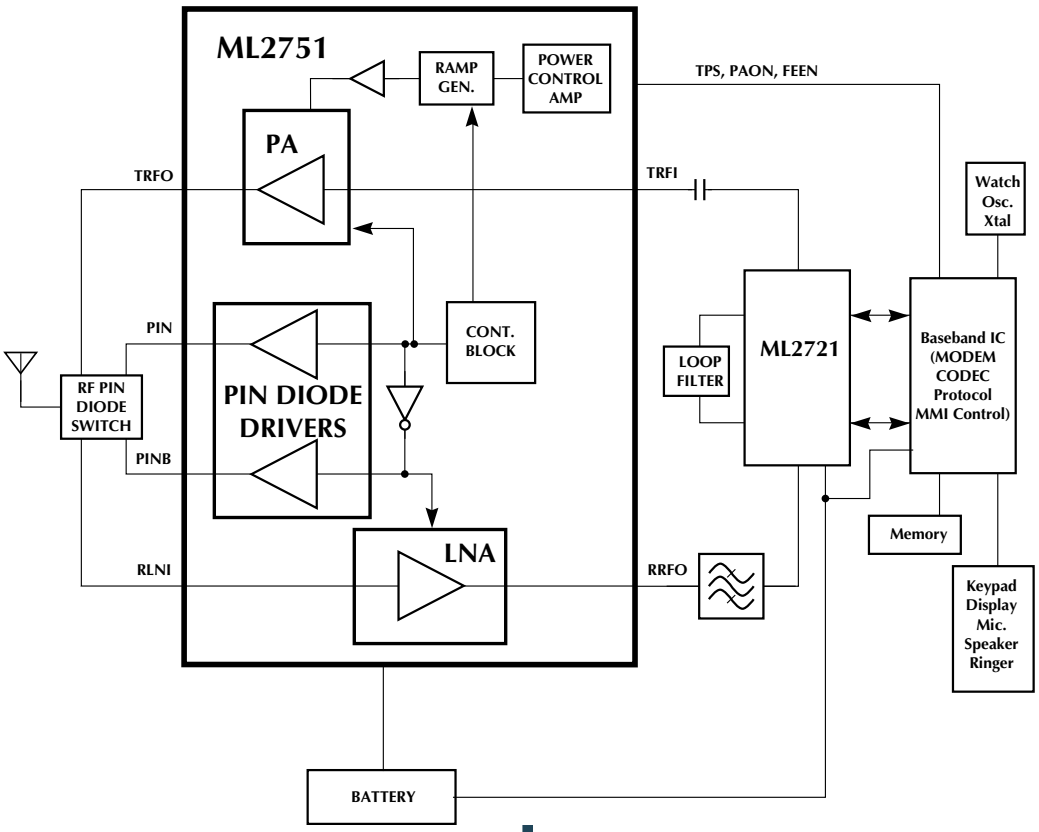
FEATURES

- Fully integrated Power Amplifier, Low Noise Amplifier, and PIN diode drivers
- 100mW Power Amplifier
- Single supply, 2.7V to 4.5V operating range
- PA output: +21 dBm at 3.0V, 35dB gain, 35% efficiency at 3.3V after harmonic filter; integrated PA ramp control
- LNA: noise figure of 2.5dB, –15dBm 3rd-order intercept point, and –25dBm

APPLICATIONS

- 900 MHz FCC Part 15 Radios
- 900 MHz Cordless Telephones
- TDD / TDMA Radios

SIMPLIFIED BLOCK DIAGRAM



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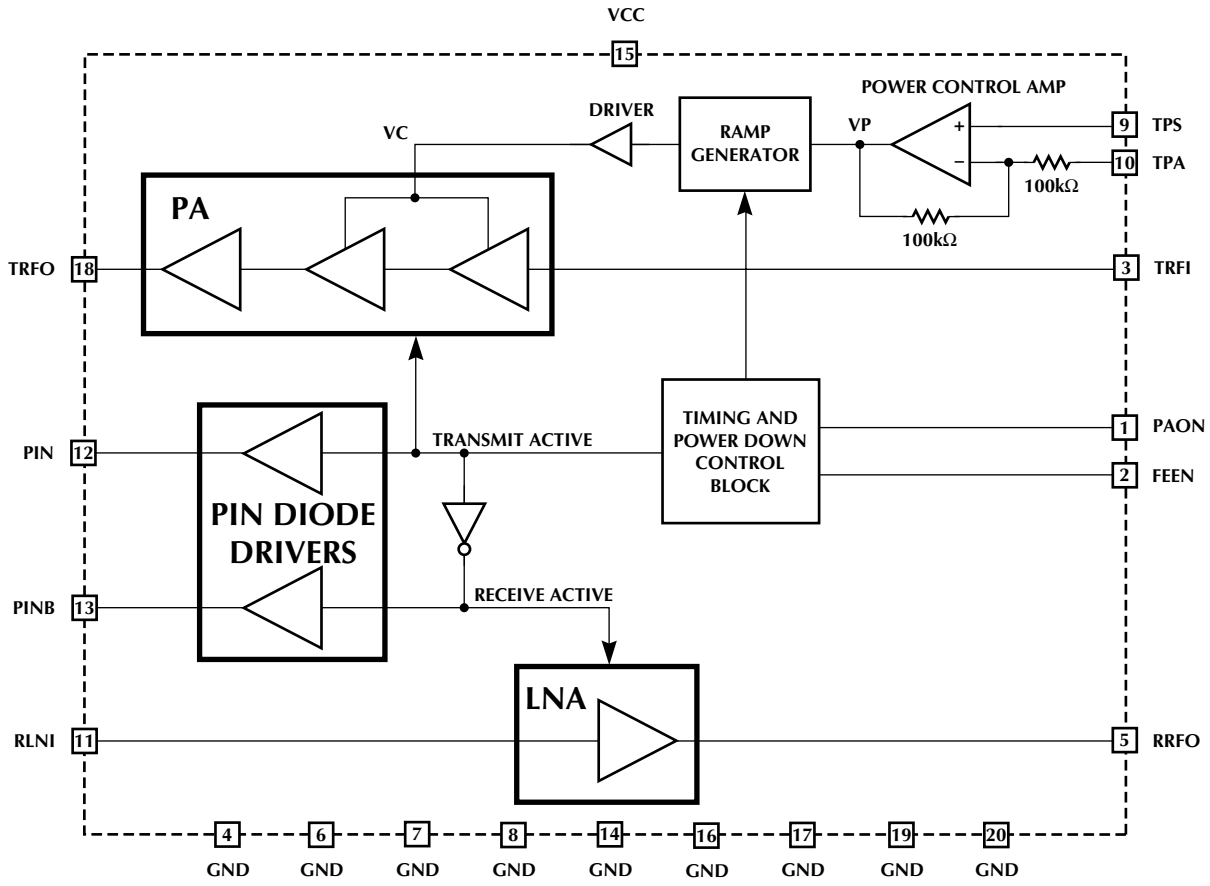
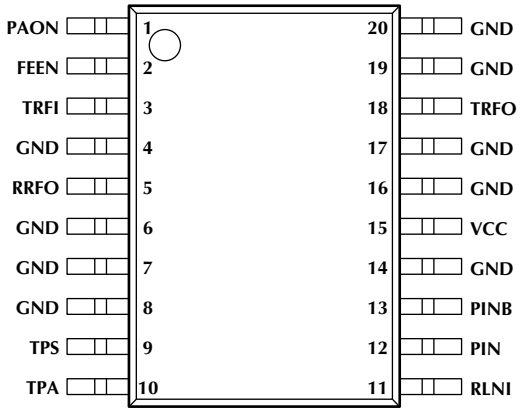
BLOCK DIAGRAM



PIN CONFIGURATION

ML2751
20-Pin TSSOP (T20)



TOP VIEW

PIN DESCRIPTIONS

Pin #	Signal Name	I/O Type	Description
LNA Section			
5	RRFO	O (analog)	Receive RF Output. LNA RF Output. This is an open collector output that requires an external load to VCC. This pin requires matching for optimum gain
11	RLNI	I (analog)	Receive LNA RF input. This pin is directly connected to the base of an NPN transistor. The input to this pin should be AC coupled using an external capacitor. This input will require matching for optimum performance
PA Section			
3	TRFI	I (analog)	Transmit RF Power Amplifier (PA) input. Requires RF choke to VCC that can handle up to 150mA. The VCC end of the choke requires both RF and low frequency decoupling to ground to minimize supply modulation
9	TPS	I (analog)	This pin is the non-inverting input of an op amp. The voltage on this pin sets the RF power produced by the PA, permitting variable power operation under control of the baseband circuits (see Figure 2)
10	TPA	I (analog)	This pin is the inverting input of an operational amplifier. A resistor from this pin to GND scales the TPS input voltage control range to match that of the external baseband control circuits. If scaling of the TPS input range is not required the TPA pin can either be grounded or left floating (see Figure 2)
18	TRFO	O (analog)	Transmit RF Power Amplifier output. Open collector output. Requires RF choke to VCC that can handle up to 150mA. The VCC end of the choke requires both RF and low frequency decoupling to ground to minimize supply modulation

PIN DESCRIPTIONS (continued)

Pin #	Signal Name	I/O	Description
PIN Diode Driver Section			
12	PIN	O (analog)	This output is a low impedance voltage source that switches between VCC and GND to drive an external PIN diode switch. This totem pole output is tri-stated when FEEN = 0. When active it pulls either to VCC (if PAON = 1) or to GND (if PAON = 0), and has a nominal output impedance of 50Ω when sourcing and 120Ω when sinking
13	PINB	O (analog)	This output is a low impedance voltage source that switches between VCC and GND to drive an external PIN diode switch. This totem pole output is tri-stated when FEEN = 0. When active it pulls either to VCC (if PAON = 0) or to GND (if PAON = 1) , and has a nominal output impedance of 50Ω when sourcing and 120Ω when sinking. PINB is the complement of PIN, providing a bipolar drive for PIN diodes from a single power rail
Control and Interface			
1	PAON	I (CMOS)	Power Amplifier on pin. The PA is active when PAON = 1, and the LNA is active when PAON = 0. Rising and falling edges of this signal initiate a controlled ramp of the PA bias circuits to eliminate AM generated sidebands on the transmitter output. The PIN diode drivers are synchronized with PAON (see Figure 3). When the ML2751 is in standby mode this pin has no effect
2	FEEN	I (CMOS)	Front-end enable. FEEN is the master power down pin. When FEEN = 0 the ML2751 is in standby mode. When FEEN = 1 either the PA or the LNA is enabled (determined by the state of PAON). See Figure 3
Power & Ground			
15	VCC	Power	Positive power supply for the LNA, the first stages of the PA, the PIN diode drivers, and the control logic. Care should be exercised in PCB layout to minimize the trace length, and the inductance and resistance both in the connection to the capacitor and from the capacitor to ground
4	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
14	GND	Ground	
16	GND	Ground	
17	GND	Ground	
19	GND	Ground	
20	GND	Ground	

FUNCTIONAL DESCRIPTION

TRANSMIT FUNCTIONALITY

Power Amplifier

The power amplifier (PA) consists of three cascaded gain stages. The last stage (output stage) is powered directly from the unregulated supply to increase end-product battery life. The TPS and TPA pins are used to control its output power. The TPS and TPA pins are connected to an internal power control op amp as shown in Figure 1. The op amp's output voltage (VP) determines the PA's gain. The voltage at VP drives a buffer that serves as a collector supply for the first two stages of the power amplifier.

A ramp generator circuit between the power control op amp and the buffer facilitates a gradual transition from the on-state to the off-state of the PA on the rising/falling edge of the PAON signal.

The DC voltage on the TPS pin determines VP, and may be varied between 0V and 1V, with a nominal 100mW/V sensitivity to this pin as shown in Figure 2. To compensate for the IC manufacturing process variations of the power amplifier the TPS voltage can be scaled by varying the resistance between the TPA pin and ground. The value of resistor RTPA effectively determines the gain of the op amp. RTPA can range in value from 0Ω to open circuit. For +20dBm output power the typical full-scale signal on the TPS will lie between 0.5V and 1V with TPA grounded.

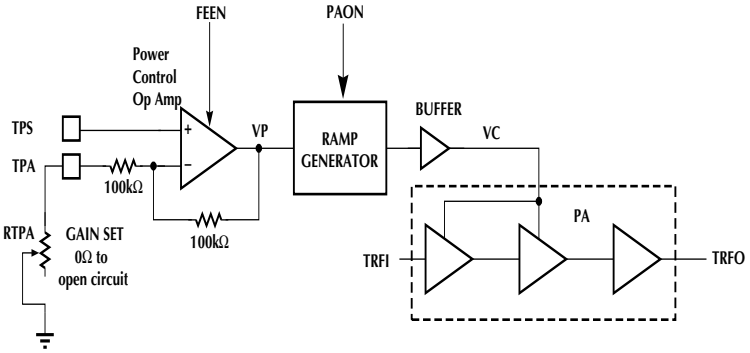


Figure 1. PA Power Setting and Ramp Generator

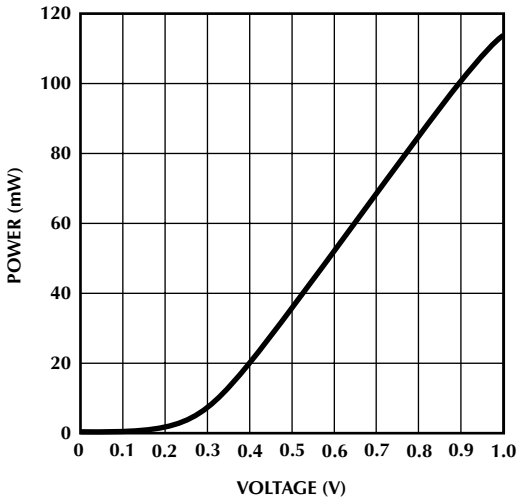


Figure 2. Output vs. TPS Curve

RECEIVE FUNCTIONALITY

Low Noise Amplifier (LNA)

The LNA is a two-stage transistor amplifier designed with internal inter-stage impedance matching. The output is an open collector that requires a load to a DC supply and external matching. All associated bias circuits are integrated internally. The LNA is controlled by the PAON signal, as shown in Figure 3.

A nominal gain of 20dB and a noise figure of 2.5dB complement the ML2721, optimizing the balance between sensitivity and high signal performance. The open-collector LNA output provides flexibility in matching the impedance that an RF filter presents to the LNA. The input can be matched for low noise using a small value series capacitor, and the two-stage design minimizes the interaction between the input and output match. The RF filter is placed between the ML2751 and the ML2721.

PIN Diode Driver

A pair of driver circuits is used to drive an external PIN diode Transmit/Receive switch. The PIN diode drivers are controlled from the timer's internal enable signals. The PIN and PINB output pins act as low impedance voltage sources that switch between VCC and GND, with the ability to both source and sink current.

The PIN and PINB outputs are under control of the FEEN and PAON control input pins (see Figure 3). The switching between the transmit and receive paths is synchronized with the PA ramp function, so that the transmit path is selected at the rising edge of the transmit ramp (when PAON = 1) and held until the PA has ramped down (about 3µs after PAON = 0).

Simple PIN diode switches can be driven directly, without the need for current limiting resistors, as each output has a nominal 100Ω series impedance. This reduces the total component count. For more complex (or lower power) switches individual current limiting resistors may be used, forcing the PIN and PINB pins to act as voltage sources. The total current drawn from each output must not exceed the current source/sink specification limits.

FUNCTIONAL DESCRIPTION

OPERATION MODES AND CONTROL INTERFACE DESCRIPTION

The signals FEEN and PAON determine the mode of operation. The three standard modes of operation are STANDBY, TRANSMIT, and RECEIVE. The control logic is shown in Table 1.

STANDBY: All circuits are off (LNA bias off), PIN driver outputs are Tri-stated.

TRANSMIT: PA and the PIN diode drivers are enabled. The LNA is off (zero current).

RECEIVE: The LNA bias circuits and the PIN diode drivers are enabled, PA is disabled.

In addition to the two mode control inputs, FEEN and PAON, there is an analog voltage input that can be used to set the power output of the amplifier. The voltage range required to set the output power level can be controlled by an external resistor.

Note that the ML2751 has an internal power amplifier ramp-on and ramp-off circuit. The power amplifier turn on/off relative to the ramp is shown in Figure 3. The ramp-on starts when the PA is enabled, the ramp-off starts when it is disabled.

Two outputs, PIN and PINB, are provided from the ML2751 to drive the external PIN diodes in the Transmit/Receive switch. The timing for these voltage outputs is shown in Figure 3 relative to the control pins FEEN and PAON.

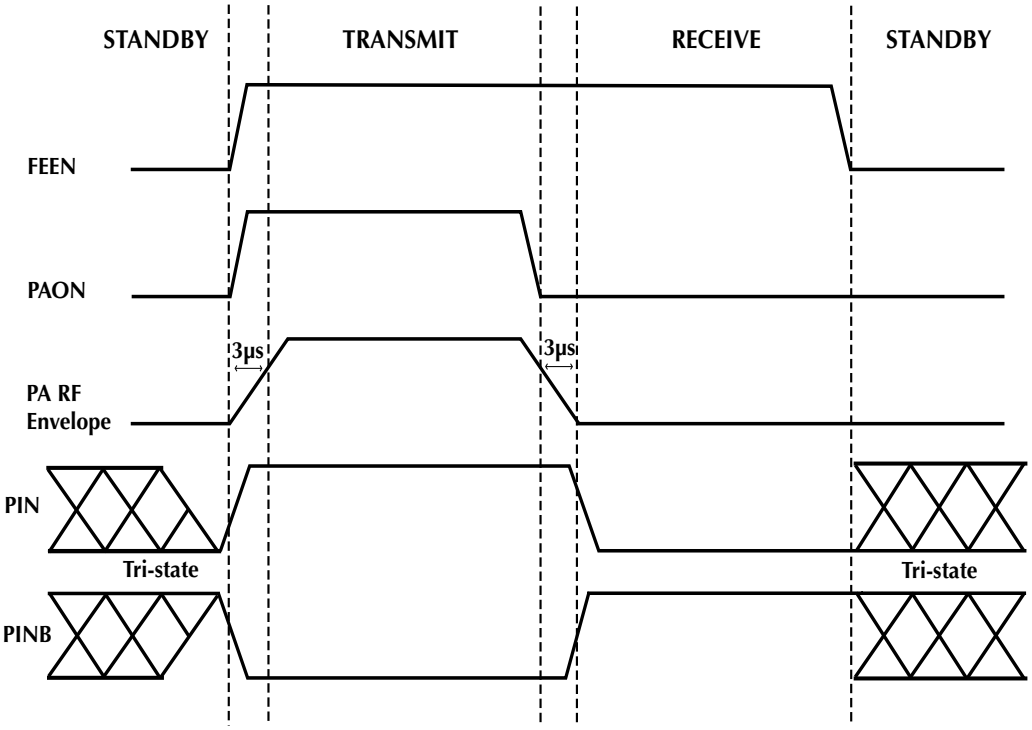


Figure 3. Signals vs. Mode Relationships

FEEN	PAON	Mode	PIN	PINB	LNA	PA
0	X	STANDBY	Tri-state	Tri-state	Off	Off
1	0	RECEIVE	VCC/-10mA	VCC/+10mA	On	Off
1	1	TRANSMIT	VCC/+10mA	VCC/-10mA	Off	On

Table 1. Control Logic

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Junction Temperature 150ºC
Storage Temperature Range ..... –65ºC to 150ºC
Lead Temperature (Soldering, 10s) 260ºC
Thermal Resistance) 150ºC/W
Input Voltage, VCC Pin 6.0V
Input Voltage, GND Pin ..... –0.3V to 0.3V
Input Voltage, Other Pins ..... –0.3V to V_{CC} + 0.3V

OPERATING CONDITIONS

Normal Temperature Range ..... –10ºC to 60ºC
VCC Range ..... 2.7V to 3.0V
Thermal Resistance 150ºC/W

ELECTRICAL TABLES

Unless otherwise specified, VCC = 3.3V, T_A = Operating Temperature Range. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL SPECIFICATIONS						
VCC	Supply Voltage		3.0	3.3	4.5	V
ICC	Supply Current			20		µA
tON	Turn on time	Standby to Transmit or Receive (Note 2)		3		µs
tSW	Turn around time	Transmit to Receive/ Receive to Transmit		3		µs
Tx ICC	Transmit active current	3v, FEEN & PAON high, P_{OUT} = +20dBm		110		mA
		3v, FEEN & PAON high, P_{OUT} = 0dBm		15		mA
Rx ICC	Receive active current	3v, FEEN & PAON low		4		mA
TRANSMIT POWER AMPLIFIER						
PMAX	Maximum output power	TPS = 1.0V (Note 3), Input power 0dBm		20.5		dBm
PMID	Mid range output power	TPS = 0.3V (Note 3)		10		dBm
PMIN	Low output power	TPS = 0.15V (Note 3)		0		dBm
PGAIN	Power gain	Maximum power setting		37		dB
RECEIVE LOW NOISE AMPLIFIER						
GAIN	Power gain	Input power <–30dBm		18		dB
NF	Noise figure			2.5		dB
IP3	3rd-order intercept point			–15		dBm
P1dB	1dB compression point			–25		dBm

ELECTRICAL TABLES (Continued)

SYMBOL		PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PIN DIODE DRIVERS							
VOUT	High				VCC –0.3		V
	Low				0.3		
IOUT	High				10		mA
	Low				–10		

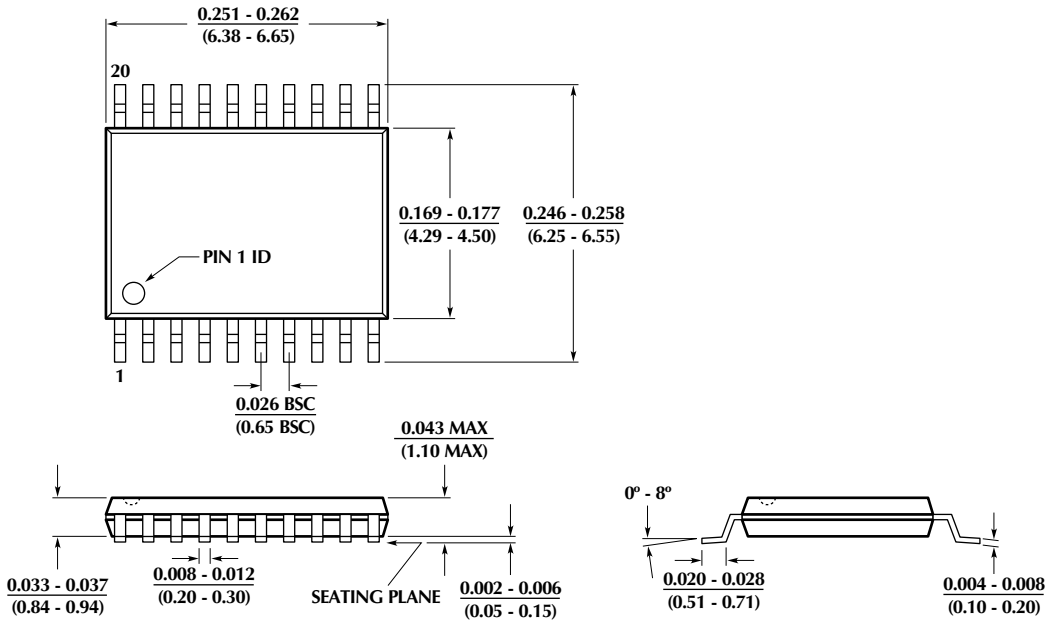
Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2: PA turn on is measured from the rising edge of either PAON or FEEN to 90% of the programmed power output.

Note 3: PA power measurements are made at the output of the external harmonic filter under the following conditions: 0dBm input drive at 915MHz; the resistor on TPA is set for +20dBm ±0.5dB output power; the TPS signal is 1V.

PHYSICAL DIMENSIONS

Package: T20
20-Pin TSSOP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2751DT	–10ºC to 60ºC	20P Pin TSSOP

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