## DATA SHEET

74F647
Octal transceiver/register, non-inverting (open-collector)
74F649
Octal transceiver/register, inverting (open-collector)

IC15 Data Handbook

PHILIPS

## 74F647 Octal Transceiver/Register, Non-inverting (Open Collector)

74F649 Octal Transceiver/Register, Inverting (Open Collector)

## FEATURES

- High impedance NPN base inputs for reduced loading ( $20 \mu \mathrm{~A}$ in High and Low states)
- Independent registers for $A$ and $B$ buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- Open Collector outputs
- 300 mil wide 24 -pin Slim Dip package


## DESCRIPTION

The 74F647 and 74F649 Transceivers/Registers consist of bus transceiver circuits with open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Output Enable (OE) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.
The select (SAB, SBA) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive

PIN CONFIGURATION - 74F647

data when the Output Enable, $\overline{\mathrm{OE}}$ is active Low. In the isolation mode (Output Enable, $\mathrm{OE}=\mathrm{High}$ ), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74F647 and 74F649.

| TYPE | TYPICAL <br> $\boldsymbol{f}_{\max }$ | TYPICAL SUPPLY CURRENT <br> (TOTAL) |
| :--- | :---: | :---: |
| 74 F 647 | 65 MHz | 125 mA |
| 74 F 649 | 65 MHz | 125 mA |

ORDERING INFORMATION

| DESCRIPTION | $\begin{gathered} \text { COMMERCIAL RANGE } \\ \mathrm{V}_{\mathrm{cc}}=5 \mathrm{~V} \pm 10 \%, \\ \mathrm{~T}_{\mathrm{amb}}=0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \end{gathered}$ | PKG DWG \# |
| :---: | :---: | :---: |
| 24-pin plastic Slim DIP (300mil) | N74F647N, N74F649N | SOT222-1 |
| 24 -pin plastic SOL | N74F647D, N74F649D | SOT137-1 |

PIN CONFIGURATION - 74F649


LOGIC SYMBOL - 74F647


LOGIC SYMBOL - 74 F647


SF01199

LOGIC SYMBOL - 74F649


LOGIC SYMBOL - 74F648


OE DIR CPAB CPBA SAB SBA $\mathrm{x} \quad \mathrm{x}$
$L \quad L \quad X \quad H$ or $L \quad X \quad H$
L H HorL
SF01201

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | $\begin{aligned} & \text { 74F(U.L.) } \\ & \text { HIGH/LOW } \end{aligned}$ | LOAD VALUE HIGH/LOW |
| :---: | :---: | :---: | :---: |
| A0-A7 | A inputs | 1.0/0.033 | $20 \mu \mathrm{~A} / 20 \mu \mathrm{~A}$ |
| B0-B7 | $B$ inputs | 1.0/0.033 | $20 \mu \mathrm{~A} / 20 \mu \mathrm{~A}$ |
| CPAB | A-to-B clock input | 1.0/0.033 | $20 \mu \mathrm{~A} / 20 \mu \mathrm{~A}$ |
| CPBA | B-to-A clock input | 1.0/0.033 | $20 \mu \mathrm{~A} / 20 \mu \mathrm{~A}$ |
| SAB | A-to-B select input | 1.0/0.033 | $20 \mu \mathrm{~A} / 20 \mu \mathrm{~A}$ |
| SBA | B-to-A select input | 1.0/0.033 | $20 \mu \mathrm{~A} / 20 \mu \mathrm{~A}$ |
| DIR | Data flow Directional control enable input | 1.0/0.066 | $20 \mu \mathrm{~A} / 20 \mu \mathrm{~A}$ |
| OE | Output Enable input | 1.0/0.066 | $20 \mu \mathrm{~A} / 20 \mu \mathrm{~A}$ |
| A0-A7 | A outputs | OC/106.7 | OC/64mA |
| B0-B7 | B outputs | OC/106.7 | OC/64mA |

NOTE: One (1.0) FAST Unit Load is defined as: $20 \mu \mathrm{~A}$ in the High state and 0.6 mA in the Low state. OC = Open Collector
FUNCTION TABLE

| INPUTS |  |  |  |  |  | DATA I/O |  | OPERATING MODE |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OE | DIR | CPAB | CPBA | SAB | SBA | A0-A7 | B0-B7 |  |  |
| X | X | $\uparrow$ | X | X | X | Input | Unspecified* | Store A, B unspecified* | Store A, B unspecified* |
| X | X | X | $\uparrow$ | X | X | Unspecified* | Input | Store B, A unspecified* | Store B, A unspecified* |
| $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \hline x \\ & x \end{aligned}$ | $\begin{gathered} \uparrow \\ \mathrm{H} \text { or } \mathrm{L} \end{gathered}$ | $\begin{gathered} \uparrow \\ \mathrm{H} \text { or } \mathrm{L} \end{gathered}$ | $\begin{aligned} & \hline X \\ & x \end{aligned}$ | $\begin{aligned} & \hline X \\ & x \end{aligned}$ | Input | Input | Store A and B data Isolation, hold storage | Store A and B data Isolation, hold storage |
| $\stackrel{L}{L}$ | $\stackrel{L}{L}$ | $\begin{aligned} & \mathrm{x} \\ & \mathrm{x} \end{aligned}$ | $\begin{gathered} \text { X } \\ \mathrm{H} \text { or L } \end{gathered}$ | $\begin{aligned} & \mathrm{X} \\ & \mathrm{x} \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | Output | Input | Real time B data to A bus Stored B data to A bus | Real time B data to $A$ bus Stored B data to A bus |
| $\begin{aligned} & \bar{L} \\ & L \end{aligned}$ | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $\begin{gathered} \mathrm{H} \text { or } \mathrm{X} \\ \mathrm{X} \end{gathered}$ | $\begin{aligned} & \hline x \\ & x \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \mathrm{X} \\ & \mathrm{X} \end{aligned}$ | Input | Output | Real time $A$ data to $B$ bus Stored A data to B bus | Real time $A$ data to $B$ bus Stored A data to B bus |

$H=$ High voltage level
$L=$ Low voltage level
X = Don't care
$\uparrow=$ Low-to-High clock transition

* The data output function may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM - 74F647


LOGIC DIAGRAM - 74F649


## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
| :--- | :--- | :---: | :---: |
| $\mathrm{V}_{\text {CC }}$ | Supply voltage | -0.5 to +7.0 | V |
| $\mathrm{~V}_{\text {IN }}$ | Input voltage | -0.5 to +7.0 | V |
| $\mathrm{I}_{\mathrm{N}}$ | Input current | -30 to +5 | mA |
| $\mathrm{~V}_{\text {OUT }}$ | Voltage applied to output in High output state | -0.5 to $+\mathrm{V}_{\mathrm{CC}}$ | V |
| $\mathrm{I}_{\text {OUT }}$ | Current applied to output in Low output state | 128 | mA |
| $\mathrm{~T}_{\text {amb }}$ | Operating free-air temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {stg }}$ | Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX |  |
| $\mathrm{V}_{\text {cc }}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $\mathrm{V}_{1 \mathrm{H}}$ | High-level input voltage | 2.0 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  | 0.8 | V |
| IIK | Input clamp current |  |  | -18 | mA |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  |  | 4.5 | V |
| loL | Low-level output current |  |  | 64 | mA |
| $\mathrm{T}_{\text {amb }}$ | Operating free-air temperature range | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER |  | TEST CONDITIONS ${ }^{1}$ |  |  | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP ${ }^{2}$ | MAX |  |
| IOH | High-level output current |  |  |  |  | $\begin{aligned} & V_{C C}=\mathrm{MIN}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{MAX}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{MIN}, \mathrm{~V}_{\mathrm{OH}}=\mathrm{MAX} \end{aligned}$ |  |  |  |  | 250 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {OL }}$ | Low-level output voltage |  | $\begin{aligned} & V_{C C}=\mathrm{MIN}, \\ & V_{I L}=M A X \\ & V_{I H}=M I N, \end{aligned}$ | $\mathrm{l}_{\mathrm{OL}}=48 \mathrm{~mA}$ | $\pm 10 \% \mathrm{~V}_{\mathrm{CC}}$ |  | 0.38 | 0.55 | V |
|  |  |  | $\mathrm{IOL}=64 \mathrm{~mA}$ | $\pm 5 \% \mathrm{~V}_{\text {CC }}$ |  | 0.42 | 0.55 | V |  |
| V | Input clamp voltage |  |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}, \mathrm{I}_{1}=\mathrm{I}_{\mathrm{IK}}$ |  |  |  | -0.73 | -1.2 | V |
| 1 | Input current at maximum input voltage | Others | $\mathrm{V}_{\mathrm{CC}}=0.0, \mathrm{~V}_{\mathrm{I}}=7.0 \mathrm{~V}$ |  |  |  |  | 100 | $\mu \mathrm{A}$ |
|  |  | An, Bn | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{1}=5.5 \mathrm{~V}$ |  |  |  |  | 1 | mA |
| IIH | High-level input current |  | $\mathrm{V}_{C C}=\mathrm{MAX}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low-level input current |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}, \mathrm{V}_{1}=0.5 \mathrm{~V}$ |  |  |  |  | -20 | $\mu \mathrm{A}$ |
| ICC | Supply current (total) | $\mathrm{I}_{\text {CCH }}$ | $V_{C C}=\mathrm{MAX}$ |  |  |  | 105 | 145 | mA |
|  |  | $\mathrm{I}_{\text {CCL }}$ |  |  |  |  | 145 | 200 | mA |

1. For conditions shown as MIN or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}$.

## AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS |  |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{amb}}=+25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}}=+5.0 \mathrm{~V} \\ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=500 \Omega \end{gathered}$ |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{amb}}=0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}}=+5.0 \mathrm{~V} \pm 10 \% \\ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=500 \Omega \end{gathered}$ |  |  |
|  |  |  | MIN | TYP | MAX | MIN | MAX |  |
| $\mathrm{f}_{\text {MAX }}$ | Maximum clock frequency | Waveform 1 | 50 | 65 |  | 40 |  | MHz |
| $\begin{aligned} & \mathrm{t}_{\mathrm{pLH}} \\ & \mathrm{t}_{\mathrm{pHL}} \\ & \hline \end{aligned}$ | Propagation delay CPAB to Bn or CPBA or An | Waveform 1 | $\begin{aligned} & 7.0 \\ & 5.5 \\ & \hline \end{aligned}$ | $\begin{gathered} 12.0 \\ 8.5 \end{gathered}$ | $\begin{aligned} & \hline 15.0 \\ & 11.0 \end{aligned}$ | $\begin{aligned} & 7.0 \\ & 5.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 16.5 \\ & 12.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \end{aligned}$ |
| $\begin{aligned} & \text { tpLH } \\ & \mathrm{t}_{\mathrm{pHHL}} \end{aligned}$ | Propagation delay <br> An to Bn or Bn to An | Waveform 2 <br> Waveform 3 | $\begin{aligned} & \hline 7.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & \hline 10.5 \\ & 7.0 \end{aligned}$ | $\begin{gathered} 13.5 \\ 9.5 \\ \hline \end{gathered}$ | $\begin{aligned} & \hline 7.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & \hline 16.0 \\ & 10.5 \\ & \hline \end{aligned}$ | ns |
| $\begin{aligned} & \hline \mathrm{tpLH}^{\prime} \\ & \mathrm{t}_{\mathrm{pHL}} \end{aligned}$ | Propagation delay SBA to An or SAB to Bn | Waveform 2 <br> Waveform 3 | $\begin{aligned} & 7.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 11.5 \\ & 7.0 \\ & \hline \end{aligned}$ | $\begin{gathered} 14.5 \\ 9.5 \\ \hline \end{gathered}$ | $\begin{aligned} & \hline 7.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 17.0 \\ & 10.5 \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \end{aligned}$ |
| $\begin{aligned} & \text { tpLH } \\ & \mathrm{t}_{\mathrm{pH}} \end{aligned}$ | Propagation delay OE to An or Bn | Waveform 2 Waveform 3 | $\begin{aligned} & 9.0 \\ & 6.5 \end{aligned}$ | $\begin{aligned} & 13.0 \\ & 10.0 \end{aligned}$ | $\begin{aligned} & 16.0 \\ & 12.5 \end{aligned}$ | $\begin{aligned} & 9.0 \\ & 6.5 \end{aligned}$ | $\begin{aligned} & 18.5 \\ & 13.5 \end{aligned}$ | ns |
| $\begin{aligned} & \text { tpLH } \\ & t_{\text {pHHL }} \end{aligned}$ | Propagation delay DIR to An or Bn | Waveform 2 Waveform 3 | $\begin{aligned} & 9.0 \\ & 7.0 \end{aligned}$ | $\begin{aligned} & 13.0 \\ & 15.0 \end{aligned}$ | $\begin{aligned} & 16.0 \\ & 18.0 \end{aligned}$ | $\begin{aligned} & 9.0 \\ & 7.0 \end{aligned}$ | $\begin{aligned} & \hline 18.5 \\ & 20.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \end{aligned}$ |

## AC SETUP REQUIREMENTS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS |  |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{amb}}=+25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}}=+5.0 \mathrm{~V} \\ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=500 \Omega \end{gathered}$ |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{amb}}=0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{Cc}}=+5.0 \mathrm{~V} \pm 10 \% \\ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=500 \Omega \end{gathered}$ |  |  |
|  |  |  | MIN | TYP | MAX | MIN | MAX |  |
| $\begin{aligned} & \hline \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\ & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\ & \hline \end{aligned}$ | Setup time, High or Low An to CPBA or Bn to CPAB | Waveform 4 | $\begin{aligned} & 4.0 \\ & 4.0 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ |  | $\begin{aligned} & \mathrm{ns} \\ & \text { ns } \end{aligned}$ |
| $\begin{aligned} & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\ & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \end{aligned}$ | Hold time, High or Low <br> An to CPBA or Bn to CPAB | Waveform 4 | 0 |  |  | 0 |  | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ |
| $\begin{aligned} & \mathrm{t}_{\mathrm{w}}(\mathrm{H}) \\ & \mathrm{t}_{\mathrm{w}}(\mathrm{~L}) \end{aligned}$ | Pulse width, High or Low CPAB or CPBA | Waveform 1 | 4.5 6.0 |  |  | 4.5 6.5 |  | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ |

## AC WAVEFORMS

For all waveforms, $\mathrm{V}_{\mathrm{M}}=1.5 \mathrm{~V}$
The shaded areas indicate when the input is permitted to change for predictable output performance.
An or Bn


Waveform 2. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn

Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

## AC WAVEFORMS (Continued)

For all waveforms, $\mathrm{V}_{\mathrm{M}}=1.5 \mathrm{~V}$
The shaded areas indicate when the input is permitted to change for predictable output performance.


Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn


Waveform 4. Data Setup and Hold Times

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS


## NOTE:

When using open-collector part, the value of the pull-up resistor greatly affects the value of the tplh. For example, changing the pull-up resistor value from $500 \Omega$ to $100 \Omega$ will improve the $t_{\text {PLH }}$ up to $50 \%$ with only slight increase in the $t_{\text {PHL }}$. However, if the pull-up resistor is changed, the user must take certain that the total lol current through the resistor and the total I IL's of the receivers do not exceed the lol maximum specification.

## TEST CIRCUIT AND WAVEFORMS




DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

| UNIT | $\mathbf{A}$ <br> max. | $\mathbf{A}_{\mathbf{1}}$ <br> $\mathbf{m i n}$. | $\mathbf{A}_{\mathbf{2}}$ <br> max. | $\mathbf{b}$ | $\mathbf{b}_{\mathbf{1}}$ | $\mathbf{c}$ | $\mathbf{D}^{(1)}$ | $\mathbf{E}^{(1)}$ | $\mathbf{e}$ | $\mathbf{e}_{\mathbf{1}}$ | $\mathbf{L}$ | $\mathbf{M}_{\mathbf{E}}$ | $\mathbf{M}_{\mathbf{H}}$ | $\mathbf{w}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| mm | 4.70 | 0.38 | 3.94 | 1.63 <br> 1.14 | 0.56 <br> $\mathbf{m a x}$ |  |  |  |  |  |  |  |  |  |
| inches | 0.43 | 0.36 <br> 0.25 | 31.9 <br> 31.5 | 6.73 <br> 6.48 | 2.54 | 7.62 | 3.51 <br> 3.05 | 8.13 <br> 7.62 | 10.03 <br> 7.62 | 0.25 | 2.05 |  |  |  |

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

| OUTLINE <br> VERSION | REFERENCES |  |  | EUROPEAN PROJECTION | ISSUE DATE |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | IEC | JEDEC | EIAJ |  |  |
| SOT222-1 |  | MS-001AF |  | $\square$ ( | 95-03-11 |



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | $\underset{\max .}{A}$ | $\mathrm{A}_{1}$ | $\mathrm{A}_{2}$ | $\mathrm{A}_{3}$ | $\mathrm{b}_{\mathrm{p}}$ | c | $\mathrm{D}^{(1)}$ | $E^{(1)}$ | e | $\mathrm{H}_{\mathrm{E}}$ | L | $L_{p}$ | Q | v | w | y | $z^{(1)}$ | $\theta$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| mm | 2.65 | $\begin{aligned} & 0.30 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 2.45 \\ & 2.25 \end{aligned}$ | 0.25 | $\begin{aligned} & 0.49 \\ & 0.36 \end{aligned}$ | $\begin{aligned} & 0.32 \\ & 0.23 \end{aligned}$ | $\begin{aligned} & 15.6 \\ & 15.2 \end{aligned}$ | $\begin{aligned} & 7.6 \\ & 7.4 \end{aligned}$ | 1.27 | $\begin{aligned} & 10.65 \\ & 10.00 \end{aligned}$ | 1.4 | $\begin{aligned} & 1.1 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 1.1 \\ & 1.0 \end{aligned}$ | 0.25 | 0.25 | 0.1 | 0.9 0.4 | $\begin{aligned} & 8^{0} \\ & 0^{\circ} \end{aligned}$ |
| inches | 0.10 | $\begin{aligned} & 0.012 \\ & 0.004 \end{aligned}$ | $\begin{aligned} & 0.096 \\ & 0.089 \end{aligned}$ | 0.01 | $\begin{aligned} & 0.019 \\ & 0.014 \end{aligned}$ | $\begin{aligned} & 0.013 \\ & 0.009 \end{aligned}$ | $\begin{aligned} & 0.61 \\ & 0.60 \end{aligned}$ | $\begin{aligned} & \hline 0.30 \\ & 0.29 \end{aligned}$ | 0.050 | $\begin{aligned} & 0.419 \\ & 0.394 \end{aligned}$ | 0.055 | $\begin{aligned} & 0.043 \\ & 0.016 \end{aligned}$ | $\begin{aligned} & 0.043 \\ & 0.039 \end{aligned}$ | 0.01 | 0.01 | 0.004 | $\begin{aligned} & 0.035 \\ & 0.016 \end{aligned}$ |  |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| outline VERSION | REFERENCES |  |  | EUROPEAN PROJECTION | ISSUE DATE |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | IEC | JEDEC | EIAJ |  |  |
| SOT137-1 | 075E05 | MS-013AD |  |  | $\begin{aligned} & -95-01-24 \\ & 97-05-22 \end{aligned}$ |

Data sheet status

| Data sheet <br> status | Product <br> status | Definition [1] |
| :--- | :--- | :--- |
| Objective <br> specification | Development | This data sheet contains the design target or goal specifications for product development. <br> Specification may change in any manner without notice. |
| Preliminary <br> specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. <br> Philips Semiconductors reserves the right to make chages at any time without notice in order to <br> improve design and supply the best possible product. |
| Product <br> specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make <br> changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

Short-form specification - The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values definition - Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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