

## 4-BIT SINGLE-CHIP MICROCONTROLLER

The  $\mu$ PD75P3116 replaces the  $\mu$ PD753108's internal mask ROM with a one-time PROM, and features expanded ROM capacity.

Because the  $\mu$ PD75P3116 supports programming by users, it is suitable for use in evaluation of systems in the development stage using the  $\mu$ PD753104, 753106, or 753108, and for use in small-scale production.

Detailed information about functions is provided in the following User's Manual. Be sure to read it before designing:

$\mu$ PD753108 User's Manual : U10890E

## FEATURES

- ☐ Compatible with  $\mu$ PD753108
- ☐ Memory capacity:
  - PROM : 16384 x 8 bits
  - RAM : 512 x 4 bits
- ☐ Can be operated in same power supply voltage range as the mask version  $\mu$ PD753108
  - $V_{DD} = 1.8$  to  $5.5$  V
- ☐ On-chip LCD controller/driver
- ☐ QTOP™ microcontroller

**Remark** QTOP microcontrollers are microcontrollers with on-chip one-time PROM that are totally supported by NEC. The support include writing application programs, marking, screening, and verification.

## ORDERING INFORMATION

| Part Number           | Package                                        |
|-----------------------|------------------------------------------------|
| $\mu$ PD75P3116GC-AB8 | 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)  |
| $\mu$ PD75P3116GK-8A8 | 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch) |

**Caution** This device does not provide an internal pull-up resistor connection function by means of mask option.

The information in this document is subject to change without notice.

## FUNCTION OUTLINE

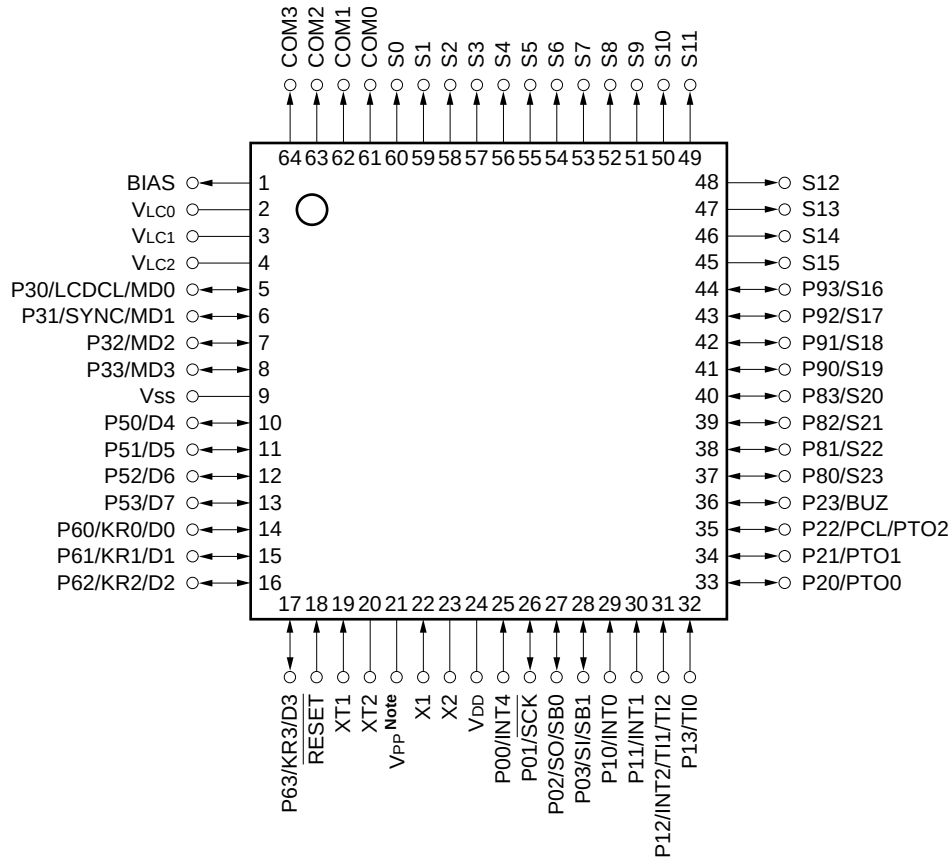
| Item                             |                     | Function                                                                                                                                                                                                                                                                                        |                                                                                                   |
|----------------------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|
| Instruction execution time       |                     | <ul style="list-style-type: none"> <li>• 0.95, 1.91, 3.81, or 15.3 <math>\mu</math>s (main system clock: @ 4.19 MHz)</li> <li>• 0.67, 1.33, 2.67, or 10.7 <math>\mu</math>s (main system clock: @ 6.0 MHz)</li> <li>• 122 <math>\mu</math>s (subsystem clock: @ 32.768 kHz)</li> </ul>          |                                                                                                   |
| Internal memory                  | PROM                | 16384 x 8 bits                                                                                                                                                                                                                                                                                  |                                                                                                   |
|                                  | RAM                 | 512 x 4 bits                                                                                                                                                                                                                                                                                    |                                                                                                   |
| General-purpose register         |                     | <ul style="list-style-type: none"> <li>• 4-bit manipulation: 8 x 4 banks</li> <li>• 8-bit manipulation: 4 x 4 banks</li> </ul>                                                                                                                                                                  |                                                                                                   |
| I/O ports                        | CMOS input          | 8                                                                                                                                                                                                                                                                                               | Internal pull-up resistor connection can be specified by software: 7                              |
|                                  | CMOS I/O            | 20                                                                                                                                                                                                                                                                                              | Internal pull-up resistor connection can be specified by software: 12<br>Shared by segment pin: 8 |
|                                  | N-ch open-drain I/O | 4                                                                                                                                                                                                                                                                                               | 13-V withstand voltage                                                                            |
|                                  | Total               | 32                                                                                                                                                                                                                                                                                              |                                                                                                   |
| LCD controller/driver            |                     | <ul style="list-style-type: none"> <li>• Segment number selection: 16/20/24 segments (Switchable to CMOS I/O ports in a batch of 4 pins, max. 8 pins)</li> <li>• Display mode selection : static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias)</li> </ul> |                                                                                                   |
| Timers                           |                     | 5 channels: <ul style="list-style-type: none"> <li>• 8-bit timer/event counter : 3 channels<br/>(Can be used as 16-bit timer/event counter, carrier generator, and timer with gate)</li> <li>• Basic interval timer/watchdog timer : 1 channel</li> <li>• Watch timer : 1 channel</li> </ul>    |                                                                                                   |
| Serial interface                 |                     | <ul style="list-style-type: none"> <li>• 3-wire serial I/O mode ... MSB/LSB first switchable</li> <li>• 2-wire serial I/O mode</li> <li>• SBI mode</li> </ul>                                                                                                                                   |                                                                                                   |
| Bit sequential buffer (BSB)      |                     | 16 bits                                                                                                                                                                                                                                                                                         |                                                                                                   |
| Clock output (PCL)               |                     | $\Phi$ , 524, 262, and 65.5 kHz (main system clock: @ 4.19 MHz)<br>$\Phi$ , 750, 375, and 93.8 kHz (main system clock: @ 6.0 MHz)                                                                                                                                                               |                                                                                                   |
| Buzzer output (BUZ)              |                     | <ul style="list-style-type: none"> <li>• 2, 4, and 32 kHz (main system clock: @ 4.19 MHz or subsystem clock: @ 32.768 kHz)</li> <li>• 2.93, 5.86, 46.9 kHz (main system clock: @ 6.0 MHz)</li> </ul>                                                                                            |                                                                                                   |
| Vectored interrupts              |                     | <ul style="list-style-type: none"> <li>• External : 3</li> <li>• Internal : 5</li> </ul>                                                                                                                                                                                                        |                                                                                                   |
| Test inputs                      |                     | <ul style="list-style-type: none"> <li>• External : 1</li> <li>• Internal : 1</li> </ul>                                                                                                                                                                                                        |                                                                                                   |
| System clock oscillation circuit |                     | <ul style="list-style-type: none"> <li>• Ceramic/crystal oscillation circuit for main system clock</li> <li>• Crystal oscillation circuit for subsystem clock</li> </ul>                                                                                                                        |                                                                                                   |
| Standby function                 |                     | STOP/HALT mode                                                                                                                                                                                                                                                                                  |                                                                                                   |
| Power supply voltage             |                     | $V_{DD}$ = 1.8 to 5.5 V                                                                                                                                                                                                                                                                         |                                                                                                   |
| Package                          |                     | <ul style="list-style-type: none"> <li>• 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)</li> <li>• 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)</li> </ul>                                                                                                                                     |                                                                                                   |

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## 1. PIN CONFIGURATION (Top View)

- 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch) :  $\mu$ PD75P3116GC-AB8
- 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch):  $\mu$ PD75P3116GK-8A8

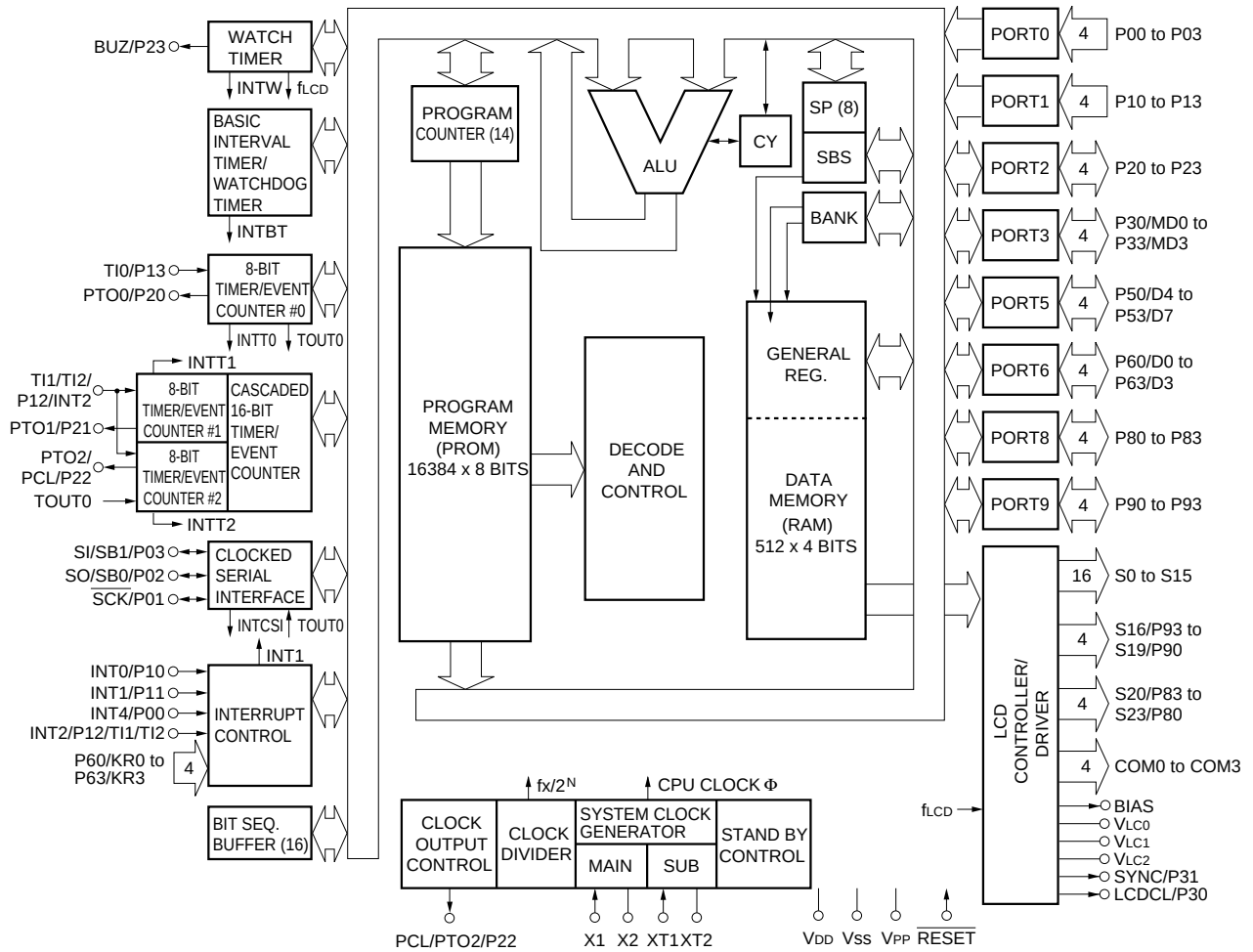


**Note** Always connect the V<sub>PP</sub> pin directly to V<sub>DD</sub> during normal operation.

## PIN IDENTIFICATIONS

|            |                          |                                      |                                       |
|------------|--------------------------|--------------------------------------|---------------------------------------|
| P00-P03    | : Port0                  | COM0 to COM3                         | : Common Output 0 to 3                |
| P10-P13    | : Port1                  | V <sub>LC0</sub> to V <sub>LC2</sub> | : LCD Power Supply 0 to 2             |
| P20-P23    | : Port2                  | BIAS                                 | : LCD Power Supply Bias Control       |
| P30-P33    | : Port3                  | LCDCL                                | : LCD Clock                           |
| P50-P53    | : Port5                  | SYNC                                 | : LCD Synchronization                 |
| P60-P63    | : Port6                  | TI0 to TI2                           | : Timer Input 0 to 2                  |
| P80-P83    | : Port8                  | PTO0 to PTO2                         | : Programmable Timer Output 0 to 2    |
| P90-P93    | : Port9                  | BUZ                                  | : Buzzer Clock                        |
| KR0-KR3    | : Key Return 0 to 3      | PCL                                  | : Programmable Clock                  |
| SCK        | : Serial Clock           | INT0, 1, 4                           | : External Vectored Interrupt 0, 1, 4 |
| SI         | : Serial Input           | INT2                                 | : External Test Input 2               |
| SO         | : Serial Output          | X1, X2                               | : Main System Clock Oscillation 1, 2  |
| SB0, SB1   | : Serial Data Bus 0, 1   | XT1, XT2                             | : Subsystem Clock Oscillation 1, 2    |
| RESET      | : Reset                  | V <sub>PP</sub>                      | : Programming Power Supply            |
| MD0 to MD3 | : Mode Selection 0 to 3  | V <sub>DD</sub>                      | : Positive Power Supply               |
| D0 to D7   | : Data Bus 0 to 7        | VSS                                  | : Ground                              |
| S0 to S23  | : Segment Output 0 to 23 |                                      |                                       |

## 2. BLOCK DIAGRAM



### 3. PIN FUNCTIONS

#### 3.1 Port Pins (1/2)

| Pin name              | I/O   | Alternate function      | Function                                                                                                                                                                                            | 8-bit I/O | Status after reset | I/O circuit type <sup>Note 1</sup> |
|-----------------------|-------|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------|------------------------------------|
| P00                   | Input | INT4                    | 4-bit input port (PORT0)<br>P01 to P03 are 3-bit pins for which connection of an internal pull-up resistor can be specified by software.                                                            | X         | Input              | <B>                                |
| P01                   | I/O   | $\overline{\text{SCK}}$ |                                                                                                                                                                                                     |           |                    | <F>-A                              |
| P02                   | I/O   | SO/SB0                  |                                                                                                                                                                                                     |           |                    | <F>-B                              |
| P03                   | I/O   | SI/SB1                  |                                                                                                                                                                                                     |           |                    | <M>-C                              |
| P10                   | Input | INT0                    | 4-bit input port (PORT1)<br>Connection of an internal pull-up resistor can be specified by software in 4-bit units.<br>P10/INT0 can select noise elimination circuit.                               | X         | Input              | <B>-C                              |
| P11                   |       | INT1                    |                                                                                                                                                                                                     |           |                    |                                    |
| P12                   |       | TI1/TI2/INT2            |                                                                                                                                                                                                     |           |                    |                                    |
| P13                   |       | TI0                     |                                                                                                                                                                                                     |           |                    |                                    |
| P20                   | I/O   | PTO0                    | 4-bit I/O port (PORT2)<br>Connection of an internal pull-up resistor can be specified by software in 4-bit units.                                                                                   | X         | Input              | E-B                                |
| P21                   |       | PTO1                    |                                                                                                                                                                                                     |           |                    |                                    |
| P22                   |       | PCL/PTO2                |                                                                                                                                                                                                     |           |                    |                                    |
| P23                   |       | BUZ                     |                                                                                                                                                                                                     |           |                    |                                    |
| P30                   | I/O   | LCDCL/MD0               | Programmable 4-bit I/O port (PORT3)<br>Input and output in single-bit units can be specified.<br>When set for 4-bit units, connection of an internal pull-up resistor can be specified by software. | X         | Input              | E-B                                |
| P31                   |       | SYNC/MD1                |                                                                                                                                                                                                     |           |                    |                                    |
| P32                   |       | MD2                     |                                                                                                                                                                                                     |           |                    |                                    |
| P33                   |       | MD3                     |                                                                                                                                                                                                     |           |                    |                                    |
| P50 <sup>Note 2</sup> | I/O   | D4                      | N-ch open-drain 4-bit I/O port (PORT5)<br>When set to open-drain, voltage is 13 V.                                                                                                                  | X         | High impedance     | M-E                                |
| P51 <sup>Note 2</sup> |       | D5                      |                                                                                                                                                                                                     |           |                    |                                    |
| P52 <sup>Note 2</sup> |       | D6                      |                                                                                                                                                                                                     |           |                    |                                    |
| P53 <sup>Note 2</sup> |       | D7                      |                                                                                                                                                                                                     |           |                    |                                    |

**Notes** 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

2. Low-level input leakage current increases when input instructions or bit manipulation instructions are executed.

## 3.1 Port Pins (2/2)

| Pin name | I/O | Alternate function | Function                                                                                                                                                                                            | 8-bit I/O | Status after reset | I/O circuit type <sup>Note 1</sup> |
|----------|-----|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------|------------------------------------|
| P60      | I/O | KR0/D0             | Programmable 4-bit I/O port (PORT6)<br>Input and output in single-bit units can be specified.<br>When set for 4-bit units, connection of an internal pull-up resistor can be specified by software. | X         | Input              | <F>-A                              |
| P61      |     | KR1/D1             |                                                                                                                                                                                                     |           |                    |                                    |
| P62      |     | KR2/D2             |                                                                                                                                                                                                     |           |                    |                                    |
| P63      |     | KR3/D3             |                                                                                                                                                                                                     |           |                    |                                    |
| P80      | I/O | S23                | 4-bit I/O port (PORT8)<br>When set for 4-bit units, connection of an internal pull-up resistor can be specified by software <sup>Note 3</sup> .                                                     | ○         | Input              | H                                  |
| P81      |     | S22                |                                                                                                                                                                                                     |           |                    |                                    |
| P82      |     | S21                |                                                                                                                                                                                                     |           |                    |                                    |
| P83      |     | S20                |                                                                                                                                                                                                     |           |                    |                                    |
| P90      | I/O | S19                | Programmable 4-bit I/O port (PORT9)<br>When set for 4-bit units, connection of an internal pull-up resistor can be specified by software <sup>Note 3</sup> .                                        | ○         | Input              | H                                  |
| P91      |     | S18                |                                                                                                                                                                                                     |           |                    |                                    |
| P92      |     | S17                |                                                                                                                                                                                                     |           |                    |                                    |
| P93      |     | S16                |                                                                                                                                                                                                     |           |                    |                                    |

**Notes** 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

2. Low-level leak current increases when an input instruction or a bit manipulation instruction is performed.

3. Do not connect an internal pull-up resistor by software when used as the segment signal output.

## 3.2 Non-port Pins (1/2)

| Pin name                          | I/O    | Alternate function | Function                                                                                                                                                                                      |                                                        | Status after reset | I/O circuit type <sup>Note 1</sup> |
|-----------------------------------|--------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|--------------------|------------------------------------|
| TI0                               | Input  | P13                | External event pulse input to timer/event counter                                                                                                                                             |                                                        | Input              | <B>-C                              |
| TI1                               |        | P12/INT2/TI2       |                                                                                                                                                                                               |                                                        |                    |                                    |
| TI2                               |        | P12/INT2/TI1       |                                                                                                                                                                                               |                                                        |                    |                                    |
| PTO0                              | Output | P20                | Timer/event counter output                                                                                                                                                                    |                                                        | Input              | E-B                                |
| PTO1                              |        | P21                |                                                                                                                                                                                               |                                                        |                    |                                    |
| PTO2                              |        | P22/PCL            |                                                                                                                                                                                               |                                                        |                    |                                    |
| PCL                               |        | P22/PTO2           | Clock output                                                                                                                                                                                  |                                                        |                    |                                    |
| BUZ                               |        | P23                | Frequency output (for buzzer or system clock trimming)                                                                                                                                        |                                                        |                    |                                    |
| $\overline{\text{SCK}}$           | I/O    | P01                | Serial clock I/O                                                                                                                                                                              |                                                        | Input              | <F>-A                              |
| SO/SB0                            |        | P02                | Serial data output<br>Serial data bus I/O                                                                                                                                                     |                                                        |                    | <F>-B                              |
| SI/SB1                            |        | P03                | Serial data input<br>Serial data bus I/O                                                                                                                                                      |                                                        |                    | <M>-C                              |
| INT4                              | Input  | P00                | Edge detection vectored interrupt input<br>(valid for detecting both rising and falling edges)                                                                                                |                                                        |                    | <B>                                |
| INT0                              | Input  | P10                | Edge detection vectored interrupt input<br>(detection edge is selectable)                                                                                                                     | With noise elimination<br>circuit/asynch is selectable | Input              | <B>-C                              |
| INT1                              |        | P11                | INT0/P10 can select noise elimination circuit.                                                                                                                                                | Asynch                                                 |                    |                                    |
| INT2                              | Input  | P12/TI1/TI2        | Rising edge detection testable input                                                                                                                                                          | Asynch                                                 |                    |                                    |
| KR0 to KR3                        | I/O    | P60 to P63         | Parallel falling edge detection testable input                                                                                                                                                |                                                        | Input              | <F>-A                              |
| X1                                | Input  | —                  | Ceramic/crystal resonator connection for main system<br>clock oscillation. If using an external clock, input signal to X1<br>and input inverted phase to X2.                                  |                                                        | —                  | —                                  |
| X2                                | —      |                    |                                                                                                                                                                                               |                                                        |                    |                                    |
| XT1                               | Input  | —                  | Crystal resonator connection for subsystem clock oscillation.<br>If using an external clock, input signal to XT1 and input inverted<br>phase to XT2. XT1 can be used as a 1-bit (test) input. |                                                        | —                  | —                                  |
| XT2                               | —      |                    |                                                                                                                                                                                               |                                                        |                    |                                    |
| $\overline{\text{RESET}}$         | Input  | —                  | System reset input (low-level active)                                                                                                                                                         |                                                        | —                  | <B>                                |
| MD0 to MD3                        | Input  | P30 to P33         | Mode selection for program memory (PROM) write/verify                                                                                                                                         |                                                        | Input              | E-B                                |
| D0 to D3                          | I/O    | P60/KR0 to P63/KR3 | Data bus for program memory (PROM) write/verify                                                                                                                                               |                                                        | Input              | <F>-A                              |
| D4 to D7                          |        | P50 to P53         |                                                                                                                                                                                               |                                                        |                    | M-E                                |
| V <sub>PP</sub> <sup>Note 2</sup> | —      | —                  | Programmable power supply voltage applied for program<br>memory (PROM) write/verify.<br>For normal operation, connect directly to V <sub>DD</sub> .<br>Apply +12.5 V for PROM write/verify.   |                                                        | —                  | —                                  |
| V <sub>DD</sub>                   | —      | —                  | Positive power supply                                                                                                                                                                         |                                                        | —                  | —                                  |
| V <sub>SS</sub>                   | —      | —                  | Ground potential                                                                                                                                                                              |                                                        | —                  | —                                  |

**Notes** 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

2. The V<sub>PP</sub> pin does not operate correctly when it is not connected to the V<sub>DD</sub> pin during normal operation.



## 3.2 Non-port Pins (2/2)

| Pin name                             | I/O    | Alternate function | Function                                                      | Status after reset | I/O circuit type |
|--------------------------------------|--------|--------------------|---------------------------------------------------------------|--------------------|------------------|
| S0 to S15                            | Output | —                  | Segment signal output                                         | <b>Note 1</b>      | G-A              |
| S16 to S19                           | Output | P93 to P90         | Segment signal output                                         | Input              | H                |
| S20 to S23                           | Output | P83 to P80         | Segment signal output                                         | Input              | H                |
| COM0 to COM3                         | Output | —                  | Common signal output                                          | <b>Note 1</b>      | G-B              |
| V <sub>LC0</sub> to V <sub>LC2</sub> | —      | —                  | Power supply for driving LCD                                  | —                  | —                |
| BIAS                                 | Output | —                  | Output for external split resistor cut                        | <b>Note 2</b>      | —                |
| LCDCL <small>Note 3</small>          | I/O    | P30/MD0            | Clock output for driving external expansion driver            | Input              | E-B              |
| SYNC <small>Note 3</small>           | I/O    | P31/MD1            | Clock output for synchronization of external expansion driver | Input              | E-B              |

**Notes 1.** The V<sub>PP</sub> pin does not operate normally if it is not connected with V<sub>DD</sub> pin when normal operation.

**2.** The V<sub>LCX</sub> (X = 0, 1, 2) shown below are selected as the input source for the display outputs.

S0 to S23: V<sub>LC1</sub>, COM0 to COM2: V<sub>LC2</sub>, COM3: V<sub>LC0</sub>

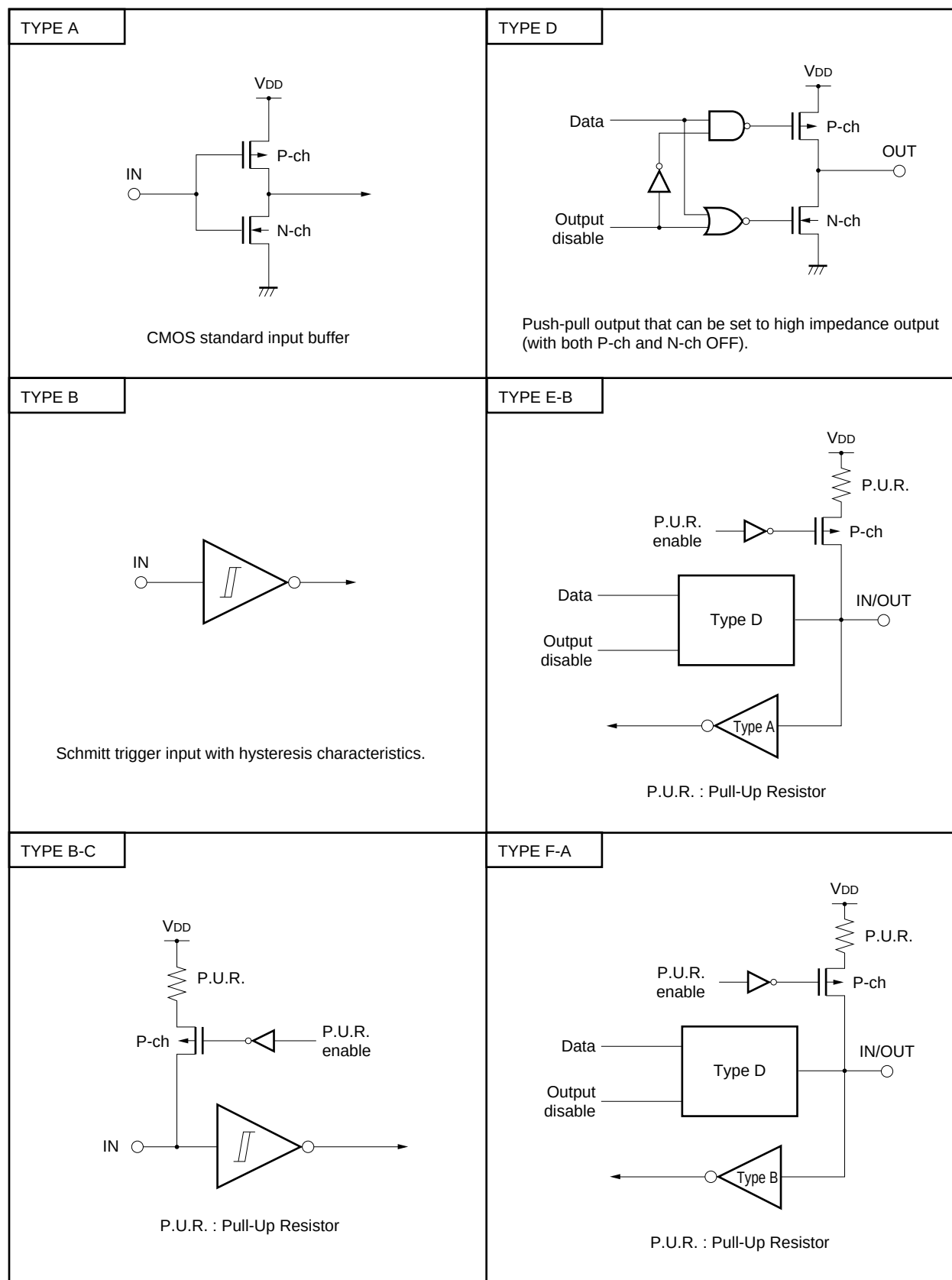
**3.** When the split resistor is incorporated : Low level

When the split resistor is not incorporated : High impedance

**4.** These pins are provided for future system expansion. Currently, only P30 and P31 are used.

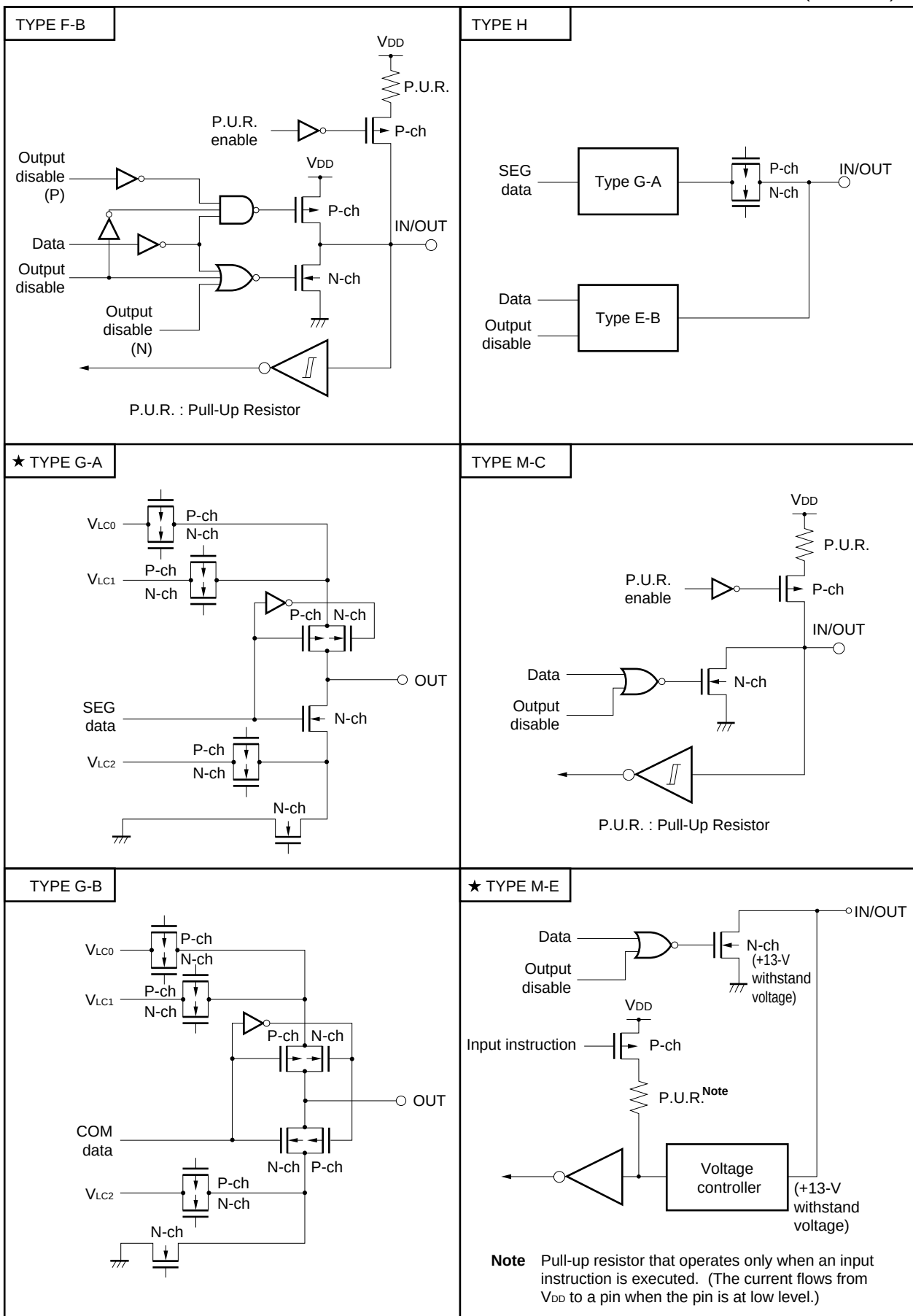
### 3.3 Equivalent Circuits for Pins

The equivalent circuits for the μPD75P3116's pins are shown in abbreviated form below.



(Continued)

(Continued)



## 3.4 Recommended Connection of Unused Pins

★

Table 3-1. List of Unused Pin Connection

| Pin                      | Recommended connection                                                                             |
|--------------------------|----------------------------------------------------------------------------------------------------|
| P00/INT4                 | Connect to Vss or VDD                                                                              |
| P01/SCK                  | Individually connect to Vss or VDD through a resistor.                                             |
| P02/SO/SB0               |                                                                                                    |
| P03/SI/SB1               | Connect to Vss                                                                                     |
| P10/INT0 and P11/INT1    | Connect to Vss or VDD                                                                              |
| P12/TI1/TI2/INT2         |                                                                                                    |
| P13/TI0                  |                                                                                                    |
| P20/PTO0                 | Input status : Individually connect to Vss or VDD through a resistor                               |
| P21/PTO1                 |                                                                                                    |
| P22/PTO2/PCL             | Output status : Leave open                                                                         |
| P23/BUZ                  |                                                                                                    |
| P30/LCDCL/MD0            |                                                                                                    |
| P31/SYNC/MD1             |                                                                                                    |
| P32/MD2                  |                                                                                                    |
| P33/MD3                  |                                                                                                    |
| P50/D4 to P53/D7         | Connect to Vss                                                                                     |
| P60/KR0/D0 to P63/KR3/D3 | Input status : Individually connect to Vss or VDD through a resistor<br>Output status : Leave open |
| S0 to S15                | Leave open                                                                                         |
| COM0 to COM3             |                                                                                                    |
| S16/P93 to S19/P90       | Input status : Individually connect to Vss or VDD through a resistor                               |
| S20/P83 to S23/P80       | Output status : Leave open                                                                         |
| VLC0 to VLC2             | Connect to Vss                                                                                     |
| BIAS                     | Connect to Vss only when neither of VLC0, VLC1 and VLC2 is used. In other cases, leave open.       |
| XT1 <sup>Note</sup>      | Connect to Vss or VDD                                                                              |
| XT2 <sup>Note</sup>      | Leave open                                                                                         |
| VPP                      | Always connect to VDD directly                                                                     |

**Note** In case the subsystem clock is not used, set SOS.0 = 1 (on-chip feedback resistor not used).

#### 4. Mk I AND Mk II MODE SELECTION FUNCTION

Setting a stack bank selection (SBS) register for the μPD75P3116 enables the program memory to be switched between the Mk I mode and Mk II mode. This function is applicable when using the μPD75P3116 to evaluate the μPD753104, 753106, or 753108.

When the SBS bit 3 is set to 1 : sets the Mk I mode (supports the Mk I mode for the μPD753104, 753106, and 753108)

When the SBS bit 3 is set to 0 : sets the Mk II mode (supports the Mk II mode for the μPD753104, 753106, and 753108)

##### 4.1 Differences between Mk I Mode and Mk II Mode

**Table 4-1** lists differences between the Mk I mode and the Mk II mode for the μPD75P3116.

**Table 4-1. Differences between Mk I Mode and Mk II Mode**

| Item                       |                          | Mk I mode                                               | Mk II mode                                               |
|----------------------------|--------------------------|---------------------------------------------------------|----------------------------------------------------------|
| Program counter            |                          | PC <sub>13-0</sub>                                      |                                                          |
| Program memory (bytes)     |                          | 16384                                                   |                                                          |
| Data memory (bits)         |                          | 512 x 4                                                 |                                                          |
| Stack                      | Stack bank               | Selectable via memory banks 0, 1                        |                                                          |
|                            | No. of stack bytes       | 2 bytes                                                 | 3 bytes                                                  |
| Instruction                | BRA !addr1 instruction   | Not available                                           | Available                                                |
|                            | CALLA !addr1 instruction |                                                         |                                                          |
| Instruction execution time | CALL !addr instruction   | 3 machine cycles                                        | 4 machine cycles                                         |
|                            | CALLF !faddr instruction | 2 machine cycles                                        | 3 machine cycles                                         |
| Supported mask ROMs        |                          | When set to Mk I mode:<br>μPD753104, 753106, and 753108 | When set to Mk II mode:<br>μPD753104, 753106, and 753108 |

★ **Caution** The Mk II mode supports a program area exceeding 16 Kbytes for the 75X and 75XL Series. Therefore, this mode is effective for enhancing software compatibility with products that have a program area of more than 16 Kbytes.

With regard to the number of stack bytes during execution of subroutine call instructions, the usable area increases by 1 byte per stack compared to the Mk I mode when the Mk II mode is selected.

However, when the CALL !addr and CALLF !faddr instructions are used, the machine cycle becomes longer by 1 machine cycle. Therefore, if more emphasis is placed on RAM use efficiency and processing performance than on software compatibility, the Mk I mode should be used.

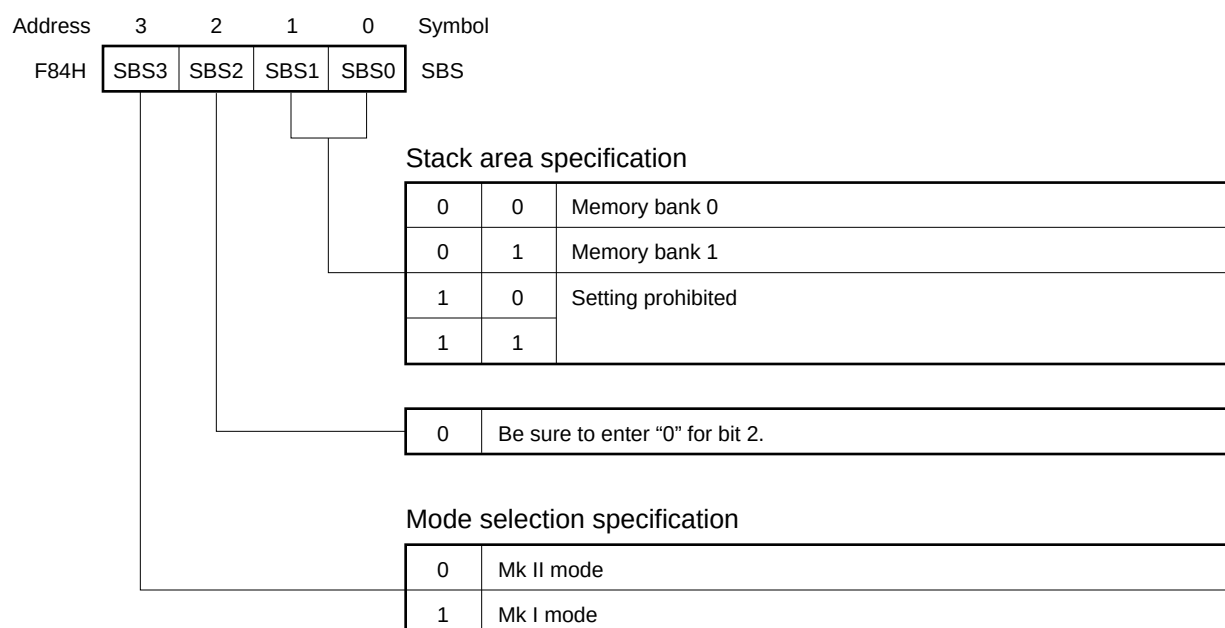
## 4.2 Setting of Stack Bank Selection (SBS) Register

Use the stack bank selection register to switch between the Mk I mode and Mk II mode. **Figure 4-1** shows the format of the stack bank selection register.

The stack bank selection register is set using a 4-bit memory manipulation instruction. When using the Mk I mode, be sure to initialize the stack bank selection register to 100XB <sup>Note</sup> at the beginning of the program. When using the Mk II mode, be sure to initialize it to 000XB <sup>Note</sup>.

**Note** Set the desired value for X.

**Figure 4-1. Format of Stack Bank Selection Register**



**Caution** SBS3 is set to "1" after RESET input, and consequently the CPU operates in the Mk I mode. When using instructions for the Mk II mode, set SBS3 to "0" and set the Mk II mode before using the instructions.

## 5. DIFFERENCES BETWEEN $\mu$ PD75P3116 AND $\mu$ PD753104, 753106, 753108

The  $\mu$ PD75P3116 replaces the internal mask ROM in the  $\mu$ PD753104, 753106, and 753108 with a one-time PROM and features expanded ROM capacity. The  $\mu$ PD75P3116's Mk I mode supports the Mk I mode in the  $\mu$ PD753104, 753106, and 753108 and the  $\mu$ PD75P3116's Mk II mode supports the Mk II mode in the  $\mu$ PD753104, 753106, and 753108.

**Table 5-1** lists differences among the  $\mu$ PD75P3116 and the  $\mu$ PD753104, 753106, and 753108. Be sure to check the differences among these products before using them with PROMs for debugging or prototype testing of application systems or, later, when using them with a mask ROM for full-scale production.

For details on the CPU functions and internal hardware, refer to the **User's Manual**.

**Table 5-1. Differences between  $\mu$ PD75P3116 and  $\mu$ PD753104, 753106, and 753108**

| Item                   |                                             | $\mu$ PD753104                                                                                       | $\mu$ PD753106   | $\mu$ PD753108   | $\mu$ PD75P3116                                           |
|------------------------|---------------------------------------------|------------------------------------------------------------------------------------------------------|------------------|------------------|-----------------------------------------------------------|
| Program counter        |                                             | 12 bits                                                                                              | 13 bits          |                  | 14 bits                                                   |
| Program memory (bytes) |                                             | Mask ROM<br>4096                                                                                     | Mask ROM<br>6144 | Mask ROM<br>8192 | One-time PROM<br>16384                                    |
| Data memory (x 4 bits) |                                             | 512                                                                                                  |                  |                  |                                                           |
| Mask options           | Pull-up resistor for PORT5                  | Available<br>(On chip/not on chip can be specified.)                                                 |                  |                  | Not available<br>(Not on chip)                            |
|                        | Split resistor for LCD driving power supply |                                                                                                      |                  |                  |                                                           |
|                        | Wait time after RESET                       | Available<br>(Selectable between $2^{17}/f_x$ and $2^{15}/f_x$ )                                     |                  |                  | Not available<br>(fixed to $2^{15}/f_x$ ) <sup>Note</sup> |
|                        | Feedback resistor of subsystem clock        | Available<br>(Use/not use can be selected.)                                                          |                  |                  | Not available<br>(Enable)                                 |
| Pin configuration      | Pin Nos. 5 to 8                             | P30 to P33                                                                                           |                  |                  | P30/MD0 to P33/MD3                                        |
|                        | Pin Nos. 10 to 13                           | P50 to P53                                                                                           |                  |                  | P50/D4 to P53/D7                                          |
|                        | Pin Nos. 14 to 17                           | P60/KR0 to P63/KR3                                                                                   |                  |                  | P60/KR0/D0 to P63/KR3/D3                                  |
|                        | Pin No. 21                                  | IC                                                                                                   |                  |                  | VPP                                                       |
| Other                  |                                             | Noise resistance and noise radiation may differ due to the different circuit sizes and mask layouts. |                  |                  |                                                           |

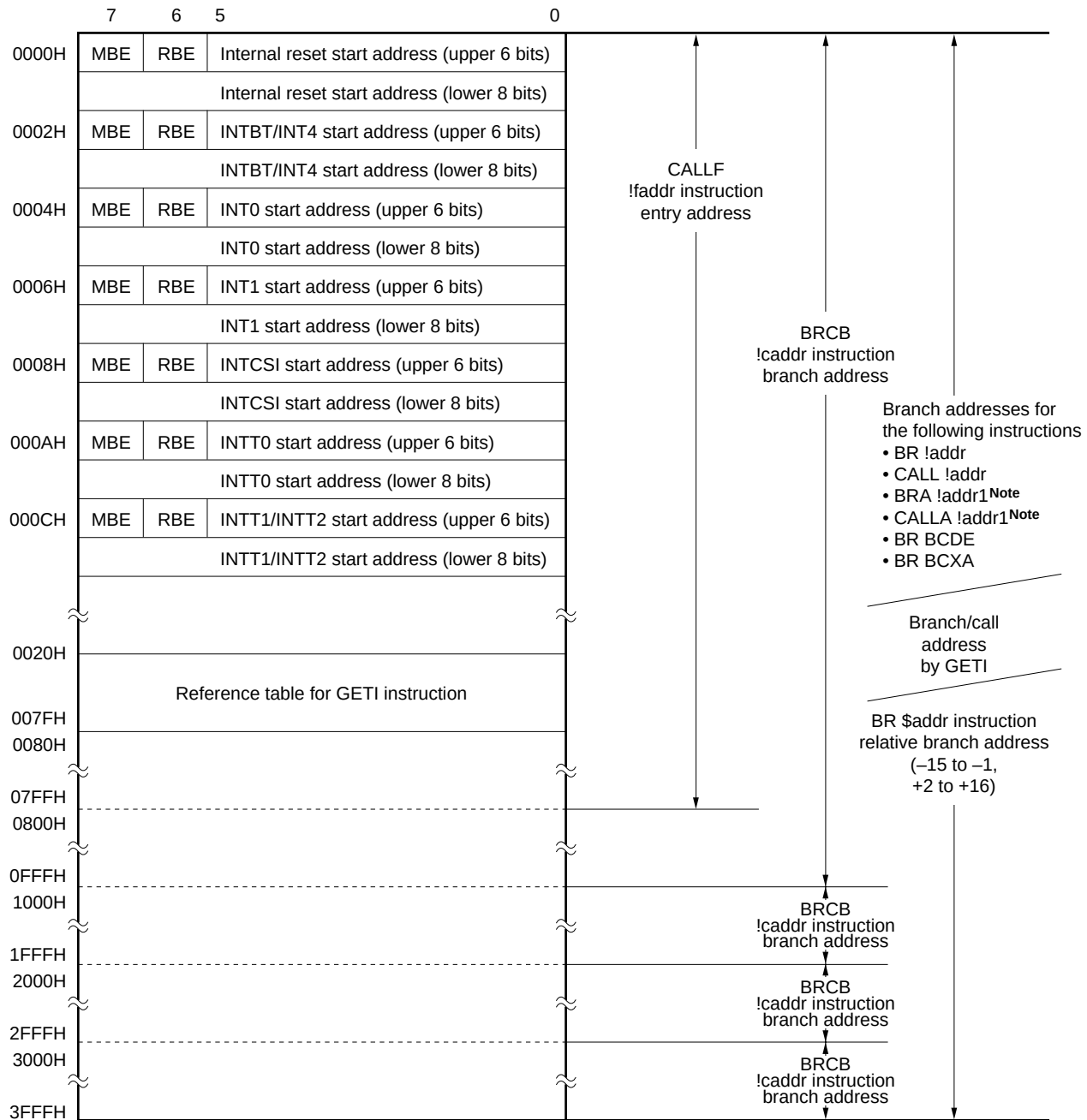
**Note**  $2^{17}/f_x$  : 21.8 ms at 6.0-MHz operation, 31.3 ms at 4.19-MHz operation

$2^{15}/f_x$  : 5.46 ms at 6.0-MHz operation, 7.81 ms at 4.19-MHz operation

**Caution** Noise resistance and noise radiation are different in PROM and mask ROMs. When changing from PROM versions to mask ROM versions when switching from prototype development to full production, be sure to fully evaluate the mask ROM version's CS (not ES).

## 6. MEMORY CONFIGURATION

Figure 6-1. Program Memory Map

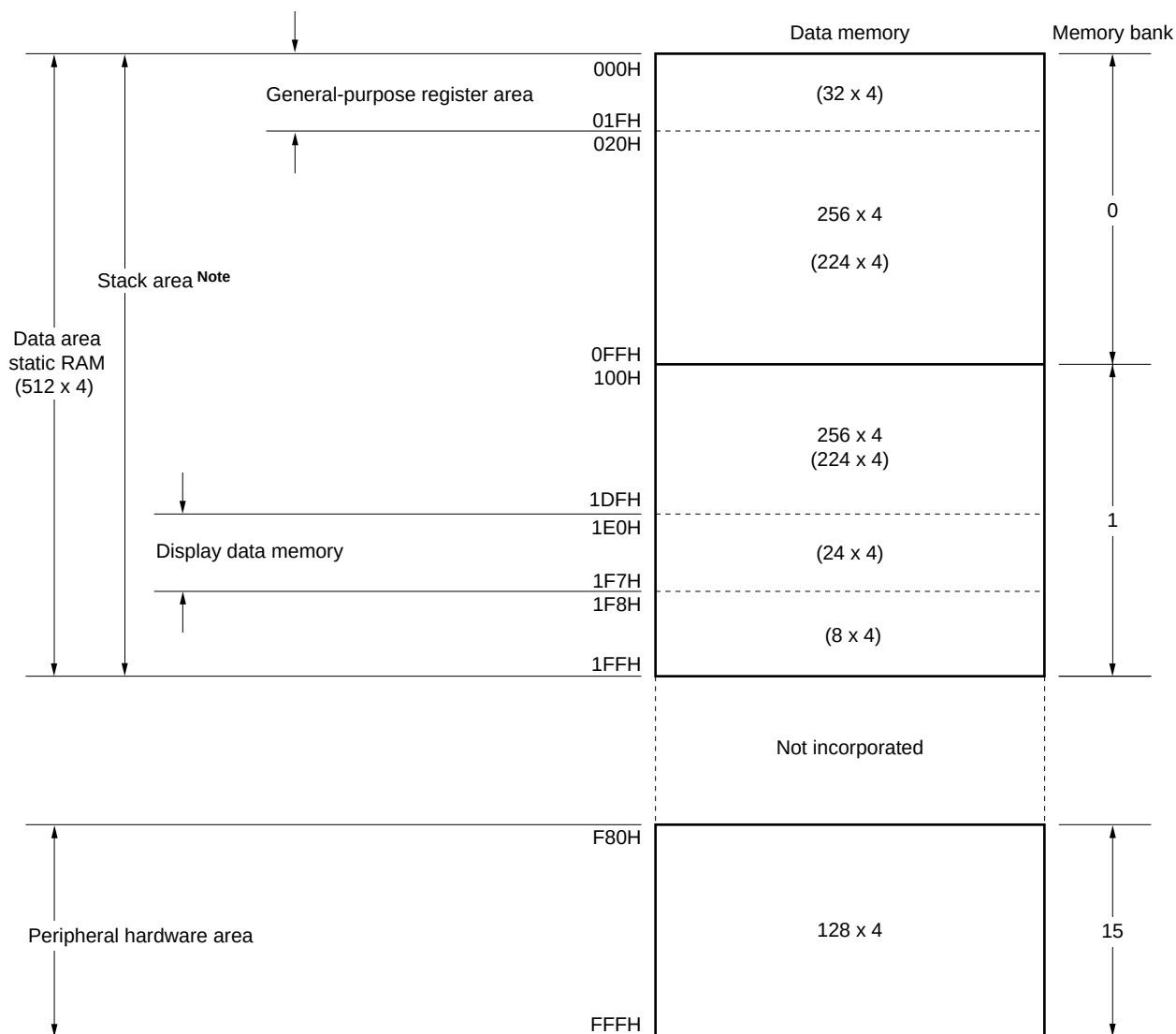


**Note** Can be used only in the Mk II mode

**Remark** For instructions other than those noted above, the BR PCDE and BR PCXA instructions can be used to branch to addresses with changes in the PC's lower 8 bits only.



Figure 6-2. Data Memory Map



**Note** Memory bank 0 or 1 can be selected as the stack area.

## 7. INSTRUCTION SET

### (1) Representation and coding formats for operands

In the instruction's operand area, use the following coding format to describe operands corresponding to the instruction's operand representations (for further description, refer to the **RA75X Assembler Package User's Manual Language (EEU-1363)**). When there are several codes, select and use just one. Codes that consist of upper-case letters and + or – symbols are key words that should be entered as they are.

For immediate data, enter an appropriate numerical value or label.

Enter register flag symbols as label descriptors instead of mem, fmem, pmem, bit, etc. (for further description, refer to the **User's Manual**). The number of labels that can be entered for fmem and pmem are restricted.

| Representation | Coding format                                            |
|----------------|----------------------------------------------------------|
| reg            | X, A, B, C, D, E, H, L                                   |
| reg1           | X, B, C, D, E, H, L                                      |
| rp             | XA, BC, DE, HL                                           |
| rp1            | BC, DE, HL                                               |
| rp2            | BC, DE                                                   |
| rp'            | XA, BC, DE, HL, XA', BC', DE', HL'                       |
| rp'1           | BC, DE, HL, XA', BC', DE', HL'                           |
| rpa            | HL, HL+, HL–, DE, DL                                     |
| rpa1           | DE, DL                                                   |
| n4             | 4-bit immediate data or label                            |
| n8             | 8-bit immediate data or label                            |
| mem            | 8-bit immediate data or label <sup>Note</sup>            |
| bit            | 2-bit immediate data or label                            |
| fmem           | FB0H to FBFH, FF0H to FFFH immediate data or label       |
| pmem           | FC0H to FFFH immediate data or label                     |
| addr           | 0000H to 3FFFH immediate data or label                   |
| addr1          | 0000H to 3FFFH immediate data or label (Mk II mode only) |
| caddr          | 12-bit immediate data or label                           |
| faddr          | 11-bit immediate data or label                           |
| taddr          | 20H to 7FH immediate data (however, bit0 = 0) or label   |
| PORTn          | PORT0 to PORT3, PORT5, PORT6, PORT8, PORT9               |
| IEXXX          | IEBT, IECSI, IET0 to IET2, IE0 to IE2, IE4, IEW          |
| RBn            | RB0 to RB3                                               |
| MBn            | MB0, MB1, MB15                                           |

**Note** When processing 8-bit data, only even-numbered addresses can be specified.

**(2) Operation legend**

|       |                                         |
|-------|-----------------------------------------|
| A     | : A register; 4-bit accumulator         |
| B     | : B register                            |
| C     | : C register                            |
| D     | : D register                            |
| E     | : E register                            |
| H     | : H register                            |
| L     | : L register                            |
| X     | : X register                            |
| XA    | : Register pair (XA); 8-bit accumulator |
| BC    | : Register pair (BC)                    |
| DE    | : Register pair (DE)                    |
| HL    | : Register pair (HL)                    |
| XA'   | : Expansion register pair (XA')         |
| BC'   | : Expansion register pair (BC')         |
| DE'   | : Expansion register pair (DE')         |
| HL'   | : Expansion register pair (HL')         |
| PC    | : Program counter                       |
| SP    | : Stack pointer                         |
| CY    | : Carry flag; bit accumulator           |
| PSW   | : Program status word                   |
| MBE   | : Memory bank enable flag               |
| RBE   | : Register bank enable flag             |
| PORTn | : Port n (n = 0 to 3, 5, 6, 8, 9)       |
| IME   | : Interrupt master enable flag          |
| IPS   | : Interrupt priority selection register |
| IEXXX | : Interrupt enable flag                 |
| RBS   | : Register bank selection register      |
| MBS   | : Memory bank selection register        |
| PCC   | : Processor clock control register      |
| .     | : Delimiter for address and bit         |
| (XX)  | : Addressed data with xx                |
| XXH   | : Hexadecimal data                      |

**(3) Description of symbols used in addressing area**

|     |                                                                                                                                                           |                              |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| *1  | MB = MBE • MBS<br>MBS = 0, 1, 15                                                                                                                          | Data memory<br>addressing    |
| *2  | MB = 0                                                                                                                                                    |                              |
| *3  | MBE = 0 : MB = 0 (000H to 07FH)<br>MB = 15 (F80H to FFFH)<br>MBE = 1 : MB = MBS<br>MBS = 0, 1, 15                                                         |                              |
| *4  | MB = 15, fmem = FB0H to FBFH, FF0H to FFFH                                                                                                                |                              |
| *5  | MB = 15, pmem = FC0H to FFFH                                                                                                                              |                              |
| *6  | addr = 0000H to 3FFFH                                                                                                                                     | Program memory<br>addressing |
| *7  | addr, addr1 = (Current PC) –15 to (Current PC) –1<br>(Current PC) +2 to (Current PC) +16                                                                  |                              |
| *8  | caddr = 0000H to 0FFFH (PC13, 12 = 00B) or<br>1000H to 1FFFH (PC13, 12 = 01B) or<br>2000H to 2FFFH (PC13, 12 = 10B) or<br>3000H to 3FFFH (PC13, 12 = 11B) |                              |
| *9  | faddr = 0000H to 07FFH                                                                                                                                    |                              |
| *10 | taddr = 0020H to 007FH                                                                                                                                    |                              |
| *11 | addr1 = 0000H to 3FFFH (Mk II mode only)                                                                                                                  |                              |

**Remarks 1.** MB indicates access-enabled memory banks.

2. In area \*2, MB = 0 for both MBE and MBS.

3. In areas \*4 and \*5, MB = 15 for both MBE and MBS.

4. Areas \*6 to \*11 indicate corresponding address-enabled areas.

**(4) Description of machine cycles**

S indicates the number of machine cycles required for skipping of skip-specified instructions. The value of S varies as shown below.

- No skip ..... S = 0
- Skipped instruction is 1-byte or 2-byte instruction .... S = 1
- Skipped instruction is 3-byte instruction<sup>Note</sup> ..... S = 2

**Note** 3-byte instructions: BR !addr, BRA !addr1, CALL !addr, and CALLA !addr1

**Caution** The GETI instruction is skipped for one machine cycle.

One machine cycle equals one cycle (= t<sub>cy</sub>) of the CPU clock Φ. Use the PCC setting to select among four cycle times.

| Instruction group | Mnemonic | Operand                   | No. of bytes | Machine cycle | Operation                      | Addressing area | Skip condition  |
|-------------------|----------|---------------------------|--------------|---------------|--------------------------------|-----------------|-----------------|
| Transfer          | MOV      | A, #n4                    | 1            | 1             | A<-n4                          |                 | String-effect A |
|                   |          | reg1, #n4                 | 2            | 2             | reg1<-n4                       |                 |                 |
|                   |          | XA, #n8                   | 2            | 2             | XA<-n8                         |                 | String-effect A |
|                   |          | HL, #n8                   | 2            | 2             | HL<-n8                         |                 | String-effect B |
|                   |          | rp2, #n8                  | 2            | 2             | rp2<-n8                        |                 |                 |
|                   |          | A, @HL                    | 1            | 1             | A<-(HL)                        | *1              |                 |
|                   |          | A, @HL+                   | 1            | 2+S           | A<-(HL), then L<-L+1           | *1              | L=0             |
|                   |          | A, @HL-                   | 1            | 2+S           | A<-(HL), then L<-L-1           | *1              | L=FH            |
|                   |          | A, @rpa1                  | 1            | 1             | A<-(rpa1)                      | *2              |                 |
|                   |          | XA, @HL                   | 2            | 2             | XA<-(HL)                       | *1              |                 |
|                   |          | @HL, A                    | 1            | 1             | (HL)<-A                        | *1              |                 |
|                   |          | @HL, XA                   | 2            | 2             | (HL)<-XA                       | *1              |                 |
|                   |          | A, mem                    | 2            | 2             | A<-(mem)                       | *3              |                 |
|                   |          | XA, mem                   | 2            | 2             | XA<-(mem)                      | *3              |                 |
|                   |          | mem, A                    | 2            | 2             | (mem)<-A                       | *3              |                 |
|                   |          | mem, XA                   | 2            | 2             | (mem)<-XA                      | *3              |                 |
|                   |          | A, reg                    | 2            | 2             | A<-reg                         |                 |                 |
|                   |          | XA, rp'                   | 2            | 2             | XA<-rp'                        |                 |                 |
|                   |          | reg1, A                   | 2            | 2             | reg1<-A                        |                 |                 |
|                   |          | rp'1, XA                  | 2            | 2             | rp'1<-XA                       |                 |                 |
|                   | XCH      | A, @HL                    | 1            | 1             | A<->(HL)                       | *1              |                 |
|                   |          | A, @HL+                   | 1            | 2+S           | A<->(HL), then L<-L+1          | *1              | L=0             |
|                   |          | A, @HL-                   | 1            | 2+S           | A<->(HL), then L<-L-1          | *1              | L=FH            |
|                   |          | A, @rpa1                  | 1            | 1             | A<->(rpa1)                     | *2              |                 |
|                   |          | XA, @HL                   | 2            | 2             | XA<->(HL)                      | *1              |                 |
|                   |          | A, mem                    | 2            | 2             | A<->(mem)                      | *3              |                 |
|                   |          | XA, mem                   | 2            | 2             | XA<->(mem)                     | *3              |                 |
|                   |          | A, reg1                   | 1            | 1             | A<->reg1                       |                 |                 |
|                   |          | XA, rp'                   | 2            | 2             | XA<->rp'                       |                 |                 |
| Table reference   | MOVT     | XA, @PCDE                 | 1            | 3             | XA<-(PC13-8+DE) <sub>ROM</sub> |                 |                 |
|                   |          | XA, @PCXA                 | 1            | 3             | XA<-(PC13-8+XA) <sub>ROM</sub> |                 |                 |
|                   |          | XA, @BCDE <sup>Note</sup> | 1            | 3             | XA<-(BCDE) <sub>ROM</sub>      | *6              |                 |
|                   |          | XA, @BCXA <sup>Note</sup> | 1            | 3             | XA<-(BCXA) <sub>ROM</sub>      | *6              |                 |

**Note** Only the lower 3 bits in the B register are valid.

| Instruction group       | Mnemonic | Operand        | No. of bytes | Machine cycle | Operation                                                                   | Addressing area | Skip condition |
|-------------------------|----------|----------------|--------------|---------------|-----------------------------------------------------------------------------|-----------------|----------------|
| Bit transfer            | MOV1     | CY, fmem.bit   | 2            | 2             | CY<-(fmem.bit)                                                              | *4              |                |
|                         |          | CY, pmem.@L    | 2            | 2             | CY<-(pmem7-2+L3-2.bit(L1-0))                                                | *5              |                |
|                         |          | CY, @H+mem.bit | 2            | 2             | CY<-(H+mem3-0.bit)                                                          | *1              |                |
|                         |          | fmem.bit, CY   | 2            | 2             | (fmem.bit)<-CY                                                              | *4              |                |
|                         |          | pmem.@L, CY    | 2            | 2             | (pmem7-2+L3-2.bit(L1-0))<-CY                                                | *5              |                |
|                         |          | @H+mem.bit, CY | 2            | 2             | (H+mem3-0.bit)<-CY                                                          | *1              |                |
| Arithmetic              | ADDS     | A, #n4         | 1            | 1+S           | A<-A+n4                                                                     |                 | carry          |
|                         |          | XA, #n8        | 2            | 2+S           | XA<-XA+n8                                                                   |                 | carry          |
|                         |          | A, @HL         | 1            | 1+S           | A<-A+(HL)                                                                   | *1              | carry          |
|                         |          | XA, rp'        | 2            | 2+S           | XA<-XA+rp'                                                                  |                 | carry          |
|                         |          | rp'1, XA       | 2            | 2+S           | rp'1<-rp'1+XA                                                               |                 | carry          |
|                         | ADDC     | A, @HL         | 1            | 1             | A, CY<-A+(HL)+CY                                                            | *1              |                |
|                         |          | XA, rp'        | 2            | 2             | XA, CY<-XA+rp'+CY                                                           |                 |                |
|                         |          | rp'1, XA       | 2            | 2             | rp'1, CY<-rp'1+XA+CY                                                        |                 |                |
|                         | SUBS     | A, @HL         | 1            | 1+S           | A<-A-(HL)                                                                   | *1              | borrow         |
|                         |          | XA, rp'        | 2            | 2+S           | XA<-XA-rp'                                                                  |                 | borrow         |
|                         |          | rp'1, XA       | 2            | 2+S           | rp'1<-rp'1-XA                                                               |                 | borrow         |
|                         | SUBC     | A, @HL         | 1            | 1             | A, CY<-A-(HL)-CY                                                            | *1              |                |
|                         |          | XA, rp'        | 2            | 2             | XA, CY<-XA-rp'-CY                                                           |                 |                |
|                         |          | rp'1, XA       | 2            | 2             | rp'1, CY<-rp'1-XA-CY                                                        |                 |                |
|                         | AND      | A, #n4         | 2            | 2             | A<-A $\wedge$ n4                                                            |                 |                |
|                         |          | A, @HL         | 1            | 1             | A<-A $\wedge$ (HL)                                                          | *1              |                |
|                         |          | XA, rp'        | 2            | 2             | XA<-XA $\wedge$ rp'                                                         |                 |                |
|                         |          | rp'1, XA       | 2            | 2             | rp'1<-rp'1 $\wedge$ XA                                                      |                 |                |
|                         | OR       | A, #n4         | 2            | 2             | A<-A $\vee$ n4                                                              |                 |                |
|                         |          | A, @HL         | 1            | 1             | A<-A $\vee$ (HL)                                                            | *1              |                |
|                         |          | XA, rp'        | 2            | 2             | XA<-XA $\vee$ rp'                                                           |                 |                |
|                         |          | rp'1, XA       | 2            | 2             | rp'1<-rp'1 $\vee$ XA                                                        |                 |                |
|                         | XOR      | A, #n4         | 2            | 2             | A<-A $\vee$ n4                                                              |                 |                |
|                         |          | A, @HL         | 1            | 1             | A<-A $\vee$ (HL)                                                            | *1              |                |
|                         |          | XA, rp'        | 2            | 2             | XA<-XA $\vee$ rp'                                                           |                 |                |
|                         |          | rp'1, XA       | 2            | 2             | rp'1<-rp'1 $\vee$ XA                                                        |                 |                |
| Accumulator             | RORC     | A              | 1            | 1             | CY<-A <sub>0</sub> , A <sub>3</sub> <-CY, A <sub>n-1</sub> <-A <sub>n</sub> |                 |                |
| manipulation            | NOT      | A              | 2            | 2             | A<- $\overline{A}$                                                          |                 |                |
| Increment/<br>decrement | INCS     | reg            | 1            | 1+S           | reg<-reg+1                                                                  |                 | reg=0          |
|                         |          | rp1            | 1            | 1+S           | rp1<-rp1+1                                                                  |                 | rp1=00H        |
|                         |          | @HL            | 2            | 2+S           | (HL)<-(HL)+1                                                                | *1              | (HL)=0         |
|                         |          | mem            | 2            | 2+S           | (mem)<-(mem)+1                                                              | *3              | (mem)=0        |
|                         | DECS     | reg            | 1            | 1+S           | reg<-reg-1                                                                  |                 | reg=FFH        |
|                         |          | rp'            | 2            | 2+S           | rp'<-rp'-1                                                                  |                 | rp'=FFH        |

| Instruction group       | Mnemonic | Operand        | No. of bytes | Machine cycle | Operation                                   | Addressing area | Skip condition |
|-------------------------|----------|----------------|--------------|---------------|---------------------------------------------|-----------------|----------------|
| Comparison              | SKE      | reg, #n4       | 2            | 2+S           | Skip if reg=n4                              |                 | reg=n4         |
|                         |          | @HL, #n4       | 2            | 2+S           | Skip if (HL)=n4                             | *1              | (HL)=n4        |
|                         |          | A, @HL         | 1            | 1+S           | Skip if A=(HL)                              | *1              | A=(HL)         |
|                         |          | XA, @HL        | 2            | 2+S           | Skip if XA=(HL)                             | *1              | XA=(HL)        |
|                         |          | A, reg         | 2            | 2+S           | Skip if A=reg                               |                 | A=reg          |
|                         |          | XA, rp'        | 2            | 2+S           | Skip if XA=rp'                              |                 | XA=rp'         |
| Carry flag manipulation | SET1     | CY             | 1            | 1             | CY<-1                                       |                 |                |
|                         | CLR1     | CY             | 1            | 1             | CY<-0                                       |                 |                |
|                         | SKT      | CY             | 1            | 1+S           | Skip if CY=1                                |                 | CY=1           |
|                         | NOT1     | CY             | 1            | 1             | CY<- $\overline{\text{CY}}$                 |                 |                |
| Memory bit manipulation | SET1     | mem.bit        | 2            | 2             | (mem.bit)<-1                                | *3              |                |
|                         |          | fmem.bit       | 2            | 2             | (fmem.bit)<-1                               | *4              |                |
|                         |          | pmem.@L        | 2            | 2             | (pmem7-2+L3-2.bit(L1-0))<-1                 | *5              |                |
|                         |          | @H+mem.bit     | 2            | 2             | (H+mem3-0.bit)<-1                           | *1              |                |
|                         | CLR1     | mem.bit        | 2            | 2             | (mem.bit)<-0                                | *3              |                |
|                         |          | fmem.bit       | 2            | 2             | (fmem.bit)<-0                               | *4              |                |
|                         |          | pmem.@L        | 2            | 2             | (pmem7-2+L3-2.bit(L1-0))<-0                 | *5              |                |
|                         |          | @H+mem.bit     | 2            | 2             | (H+mem3-0.bit)<-0                           | *1              |                |
|                         | SKT      | mem.bit        | 2            | 2+S           | Skip if(mem.bit)=1                          | *3              | (mem.bit)=1    |
|                         |          | fmem.bit       | 2            | 2+S           | Skip if(fmem.bit)=1                         | *4              | (fmem.bit)=1   |
|                         |          | pmem.@L        | 2            | 2+S           | Skip if(pmem7-2+L3-2.bit(L1-0))=1           | *5              | (pmem.@L)=1    |
|                         |          | @H+mem.bit     | 2            | 2+S           | Skip if(H+mem3-0.bit)=1                     | *1              | (@H+mem.bit)=1 |
|                         | SKF      | mem.bit        | 2            | 2+S           | Skip if(mem.bit)=0                          | *3              | (mem.bit)=0    |
|                         |          | fmem.bit       | 2            | 2+S           | Skip if(fmem.bit)=0                         | *4              | (fmem.bit)=0   |
|                         |          | pmem.@L        | 2            | 2+S           | Skip if(pmem7-2+L3-2.bit(L1-0))=0           | *5              | (pmem.@L)=0    |
|                         |          | @H+mem.bit     | 2            | 2+S           | Skip if(H+mem3-0.bit)=0                     | *1              | (@H+mem.bit)=0 |
|                         | SKTCLR   | fmem.bit       | 2            | 2+S           | Skip if(fmem.bit)=1 and clear               | *4              | (fmem.bit)=1   |
|                         |          | pmem.@L        | 2            | 2+S           | Skip if(pmem7-2+L3-2.bit(L1-0))=1 and clear | *5              | (pmem.@L)=1    |
|                         |          | @H+mem.bit     | 2            | 2+S           | Skip if(H+mem3-0.bit)=1 and clear           | *1              | (@H+mem.bit)=1 |
|                         | AND1     | CY, fmem.bit   | 2            | 2             | CY<-CY ∧ (fmem.bit)                         | *4              |                |
|                         |          | CY, pmem.@L    | 2            | 2             | CY<-CY ∧ (pmem7-2+L3-2.bit(L1-0))           | *5              |                |
|                         |          | CY, @H+mem.bit | 2            | 2             | CY<-CY ∧ (H+mem3-0.bit)                     | *1              |                |
|                         | OR1      | CY, fmem.bit   | 2            | 2             | CY<-CY ∨ (fmem.bit)                         | *4              |                |
|                         |          | CY, pmem.@L    | 2            | 2             | CY<-CY ∨ (pmem7-2+L3-2.bit(L1-0))           | *5              |                |
|                         |          | CY, @H+mem.bit | 2            | 2             | CY<-CY ∨ (H+mem3-0.bit)                     | *1              |                |
|                         | XOR1     | CY, fmem.bit   | 2            | 2             | CY<-CY ⊕ (fmem.bit)                         | *4              |                |
|                         |          | CY, pmem.@L    | 2            | 2             | CY<-CY ⊕ (pmem7-2+L3-2.bit(L1-0))           | *5              |                |
|                         |          | CY, @H+mem.bit | 2            | 2             | CY<-CY ⊕ (H+mem3-0.bit)                     | *1              |                |

| Instruction group | Mnemonic             | Operand               | No. of bytes | Machine cycle | Operation                                                                                                                                                                        | Addressing area | Skip condition |
|-------------------|----------------------|-----------------------|--------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------|
| Branch            | BR <sup>Note 1</sup> | addr                  | —            | —             | PC <sub>13-0</sub> ←-addr<br>(Use the assembler to select the most appropriate instruction among the following.)<br>• BR !addr<br>• BRCB !caddr<br>• BR \$addr                   | *6              |                |
|                   |                      | addr1                 | —            | —             | PC <sub>13-0</sub> ←-addr1<br>(Use the assembler to select the most appropriate instruction among the following.)<br>• BRA !addr1<br>• BR !addr<br>• BRCB !caddr<br>• BR \$addr1 | *11             |                |
|                   |                      | !addr                 | 3            | 3             | PC <sub>13-0</sub> ←-addr                                                                                                                                                        | *6              |                |
|                   |                      | \$addr                | 1            | 2             | PC <sub>13-0</sub> ←-addr                                                                                                                                                        | *7              |                |
|                   |                      | \$addr1               | 1            | 2             | PC <sub>13-0</sub> ←-addr1                                                                                                                                                       |                 |                |
|                   |                      | PCDE                  | 2            | 3             | PC <sub>13-0</sub> ←-PC <sub>13-8</sub> +DE                                                                                                                                      |                 |                |
|                   |                      | PCXA                  | 2            | 3             | PC <sub>13-0</sub> ←-PC <sub>13-8</sub> +XA                                                                                                                                      |                 |                |
|                   |                      | BCDE                  | 2            | 3             | PC <sub>13-0</sub> ←-BCDE <sup>Note 2</sup>                                                                                                                                      | *6              |                |
|                   |                      | BCXA                  | 2            | 3             | PC <sub>13-0</sub> ←-BCXA <sup>Note 2</sup>                                                                                                                                      | *6              |                |
|                   |                      | BRA <sup>Note 1</sup> | 3            | 3             | PC <sub>13-0</sub> ←-addr1                                                                                                                                                       | *11             |                |
|                   | BRCB                 | !caddr                | 2            | 2             | PC <sub>13-0</sub> ←-PC <sub>13, 12</sub> +caddr <sub>11-0</sub>                                                                                                                 | *8              |                |

**Notes** 1. The portion in a double box can be supported only in the Mk II mode. The others can be supported only in the Mk I mode.

2. The B register is valid only for the lower two bits.



| Instruction group        | Mnemonic              | Operand | No. of bytes | Machine cycle | Operation                                                                                                                                                                                                                                                                    | Addressing area | Skip condition |
|--------------------------|-----------------------|---------|--------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------|
| Subroutine stack control | CALLA <sup>Note</sup> | !addr1  | 3            | 3             | (SP-6)(SP-3)(SP-4)<-PC <sub>11-0</sub><br>(SP-5)<-0, 0, PC <sub>13, 12</sub><br>(SP-2)<-X, X, MBE, RBE<br>PC <sub>13-0</sub> <-addr1, SP<-SP-6                                                                                                                               | *11             |                |
|                          | CALL <sup>Note</sup>  | !addr   | 3            | 3             | (SP-4)(SP-1)(SP-2)<-PC <sub>11-0</sub><br>(SP-3)<-MBE, RBE, PC <sub>13, 12</sub><br>PC <sub>13-0</sub> <-addr, SP<-SP-4                                                                                                                                                      | *6              |                |
|                          |                       |         |              | 4             | (SP-6)(SP-3)(SP-4)<-PC <sub>11-0</sub><br>(SP-5)<-0, 0, PC <sub>13, 12</sub><br>(SP-2)<-X, X, MBE, RBE<br>PC <sub>13-0</sub> <-addr, SP<-SP-6                                                                                                                                |                 |                |
|                          | CALLF <sup>Note</sup> | !faddr  | 2            | 2             | (SP-4)(SP-1)(SP-2)<-PC <sub>11-0</sub><br>(SP-3)<-MBE, RBE, PC <sub>13, 12</sub><br>PC <sub>13-0</sub> <-000+faddr, SP<-SP-4                                                                                                                                                 | *9              |                |
|                          |                       |         |              | 3             | (SP-6)(SP-3)(SP-4)<-PC <sub>11-0</sub><br>(SP-5)<-0, 0, PC <sub>13, 12</sub><br>(SP-2)<-X, X, MBE, RBE<br>PC <sub>13-0</sub> <-000+faddr, SP<-SP-6                                                                                                                           |                 |                |
|                          | RET <sup>Note</sup>   |         | 1            | 3             | MBE, RBE, PC <sub>13, 12</sub> <-(SP+1)<br>PC <sub>11-0</sub> <-(SP)(SP+3)(SP+2)<br>SP<-SP+4<br>X, X, MBE, RBE<-(SP+4)<br>PC <sub>11-0</sub> <-(SP)(SP+3)(SP+2)<br>0, 0, PC <sub>13, 12</sub> <-(SP+1)<br>SP<-SP+6                                                           |                 |                |
|                          | RETS <sup>Note</sup>  |         | 1            | 3+S           | MBE, RBE, PC <sub>13, 12</sub> <-(SP+1)<br>PC <sub>11-0</sub> <-(SP)(SP+3)(SP+2)<br>SP<-SP+4<br>then skip unconditionally<br>X, X, MBE, RBE<-(SP+4)<br>PC <sub>11-0</sub> <-(SP)(SP+3)(SP+2)<br>0, 0, PC <sub>13, 12</sub> <-(SP+1)<br>SP<-SP+6<br>then skip unconditionally |                 | Unconditional  |
|                          | RETI <sup>Note</sup>  |         | 1            | 3             | MBE, RBE, PC <sub>13, 12</sub> <-(SP+1)<br>PC <sub>11-0</sub> <-(SP)(SP+3)(SP+2)<br>PSW<-(SP+4)(SP+5)<br>SP<-SP+6<br>0, 0, PC <sub>13, 12</sub> <-(SP+1)<br>PC <sub>11-0</sub> <-(SP)(SP+3)(SP+2)<br>PSW<-(SP+4)(SP+5), SP<-SP+6                                             |                 |                |

**Note** The portion in a double box can be supported only in the Mk II mode. Other portions can be supported only in the Mk I mode.

| Instruction group        | Mnemonic                  | Operand   | No. of bytes | Machine cycle | Operation                                                                                                                                                                                                                                                                    | Addressing area | Skip condition                       |
|--------------------------|---------------------------|-----------|--------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--------------------------------------|
| Subroutine stack control | PUSH                      | rp        | 1            | 1             | (SP-1)(SP-2)<-rp, SP<-SP-2                                                                                                                                                                                                                                                   |                 |                                      |
|                          |                           | BS        | 2            | 2             | (SP-1)<-MBS, (SP-2)<-RBS, SP<-SP-2                                                                                                                                                                                                                                           |                 |                                      |
|                          | POP                       | rp        | 1            | 1             | rp<-(SP+1)(SP), SP<-SP+2                                                                                                                                                                                                                                                     |                 |                                      |
|                          |                           | BS        | 2            | 2             | MBS<-(SP+1), RBS<-(SP), SP<-SP+2                                                                                                                                                                                                                                             |                 |                                      |
| Interrupt control        | EI                        |           | 2            | 2             | IME(IPS.3)<-1                                                                                                                                                                                                                                                                |                 |                                      |
|                          |                           | IEXXX     | 2            | 2             | IEXXX<-1                                                                                                                                                                                                                                                                     |                 |                                      |
|                          | DI                        |           | 2            | 2             | IME(IPS.3)<-0                                                                                                                                                                                                                                                                |                 |                                      |
|                          |                           | IEXXX     | 2            | 2             | IEXXX<-0                                                                                                                                                                                                                                                                     |                 |                                      |
| I/O                      | IN <sup>Note 1</sup>      | A, PORTn  | 2            | 2             | A<-PORTn (n=0 to 3, 5, 6, 8, 9)                                                                                                                                                                                                                                              |                 |                                      |
|                          |                           | XA, PORTn | 2            | 2             | XA<-PORTn+1, PORTn (n=8)                                                                                                                                                                                                                                                     |                 |                                      |
|                          |                           | PORTn, A  | 2            | 2             | PORTn<-A (n=2 to 3, 5, 6, 8, 9)                                                                                                                                                                                                                                              |                 |                                      |
|                          | OUT <sup>Note 1</sup>     | PORTn, A  | 2            | 2             | PORTn<-A (n=2 to 3, 5, 6, 8, 9)                                                                                                                                                                                                                                              |                 |                                      |
|                          |                           | PORTn, XA | 2            | 2             | PORTn+1, PORTn<-XA (n=8)                                                                                                                                                                                                                                                     |                 |                                      |
| CPU control              | HALT                      |           | 2            | 2             | Set HALT Mode(PCC.2<-1)                                                                                                                                                                                                                                                      |                 |                                      |
|                          | STOP                      |           | 2            | 2             | Set STOP Mode(PCC.3<-1)                                                                                                                                                                                                                                                      |                 |                                      |
|                          | NOP                       |           | 1            | 1             | No Operation                                                                                                                                                                                                                                                                 |                 |                                      |
| Special                  | SEL                       | RBn       | 2            | 2             | RBS<-n (n=0 to 3)                                                                                                                                                                                                                                                            |                 |                                      |
|                          |                           | MBn       | 2            | 2             | MBS<-n (n=0, 1, 15)                                                                                                                                                                                                                                                          |                 |                                      |
|                          | GETI <sup>Note 2, 3</sup> | taddr     | 1            | 3             | <ul style="list-style-type: none"> <li>When using TBR instruction<br/>PC<sub>13-0</sub>&lt;-(taddr)<sub>5-0</sub>+(taddr+1)</li> </ul>                                                                                                                                       | *10             |                                      |
|                          |                           |           |              | 4             | <ul style="list-style-type: none"> <li>When using TCALL instruction<br/>(SP-4)(SP-1)(SP-2)&lt;-PC<sub>11-0</sub><br/>(SP-3)&lt;-MBE, RBE, PC<sub>13, 12</sub><br/>PC<sub>13-0</sub>&lt;-(taddr)<sub>5-0</sub>+(taddr+1)<br/>SP&lt;-SP-4</li> </ul>                           |                 |                                      |
|                          |                           |           |              | 3             | <ul style="list-style-type: none"> <li>When using instruction other than TBR or TCALL<br/>Execute (taddr)(taddr+1) instructions</li> </ul>                                                                                                                                   |                 |                                      |
|                          |                           |           | 1            | 3             | <ul style="list-style-type: none"> <li>When using TBR instruction<br/>PC<sub>13-0</sub>&lt;-(taddr)<sub>5-0</sub>+(taddr+1)</li> </ul>                                                                                                                                       | *10             |                                      |
|                          |                           |           |              | 4             | <ul style="list-style-type: none"> <li>When using TCALL instruction<br/>(SP-6)(SP-3)(SP-4)&lt;-PC<sub>11-0</sub><br/>(SP-5)&lt;-0, 0, PC<sub>13, 12</sub><br/>(SP-2)&lt;-X, X, MBE, RBE<br/>PC<sub>13-0</sub>&lt;-(taddr)<sub>5-0</sub>+(taddr+1)<br/>SP&lt;-SP-6</li> </ul> |                 |                                      |
|                          |                           |           | 3            | 3             | <ul style="list-style-type: none"> <li>When using instruction other than TBR or TCALL<br/>Execute (taddr)(taddr+1) instructions</li> </ul>                                                                                                                                   |                 | Determined by referenced instruction |

- Notes**
- Setting MBE=0 or MBE=1, MBS=15 is required during the execution of IN or OUT instruction.
  - TBR and TCALL instructions are assembler pseudo-instructions for the GETI instruction table definitions.
  - The portion in a double box can be supported only in the Mk II mode. Other portions can be supported only in the Mk I mode.

## 8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The program memory contained in the  $\mu$ PD75P3116 is a 16384 x 8-bit one-time PROM that can be electrically written one time only. The pins listed in the table below are used for this PROM's write/verify operations. Clock input from the X1 pin is used instead of address input as a method for updating addresses.

| Pin                                                                      | Function                                                                                                                           |
|--------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>PP</sub>                                                          | Pin where program voltage is applied during program memory write/verify (usually V <sub>DD</sub> potential)                        |
| X1, X2                                                                   | Clock input pins for address updating during program memory write/verify. Input the X1 pin's inverted signal to the X2 pin.        |
| MD0 to MD3                                                               | Operation mode selection pin for program memory write/verify                                                                       |
| D0/P60 to D3/P63<br>(lower 4 bits)<br>D4/P50 to D7/P53<br>(upper 4 bits) | 8-bit data I/O pins for program memory write/verify                                                                                |
| V <sub>DD</sub>                                                          | Pin where power supply voltage is applied. Applies 1.8 to 5.5 V in normal operation mode and +6 V for program memory write/verify. |

**Caution** Pins not used for program memory write/verify should be connected to V<sub>ss</sub>.

### 8.1 Operation Modes for Program Memory Write/Verify

When +6 V is applied to the V<sub>DD</sub> pin and +12.5 V to the V<sub>PP</sub> pin, the  $\mu$ PD75P3116 enters the program memory write/verify mode. The following operation modes can be specified by setting pins MD0 to MD3 as shown below.

| Operation mode specification |                 |     |     |     |     | Operation mode                    |
|------------------------------|-----------------|-----|-----|-----|-----|-----------------------------------|
| V <sub>PP</sub>              | V <sub>DD</sub> | MD0 | MD1 | MD2 | MD3 |                                   |
| +12.5 V                      | +6 V            | H   | L   | H   | L   | Zero-clear program memory address |
|                              |                 | L   | H   | H   | H   | Write mode                        |
|                              |                 | L   | L   | H   | H   | Verify mode                       |
|                              |                 | H   | X   | H   | H   | Program inhibit mode              |

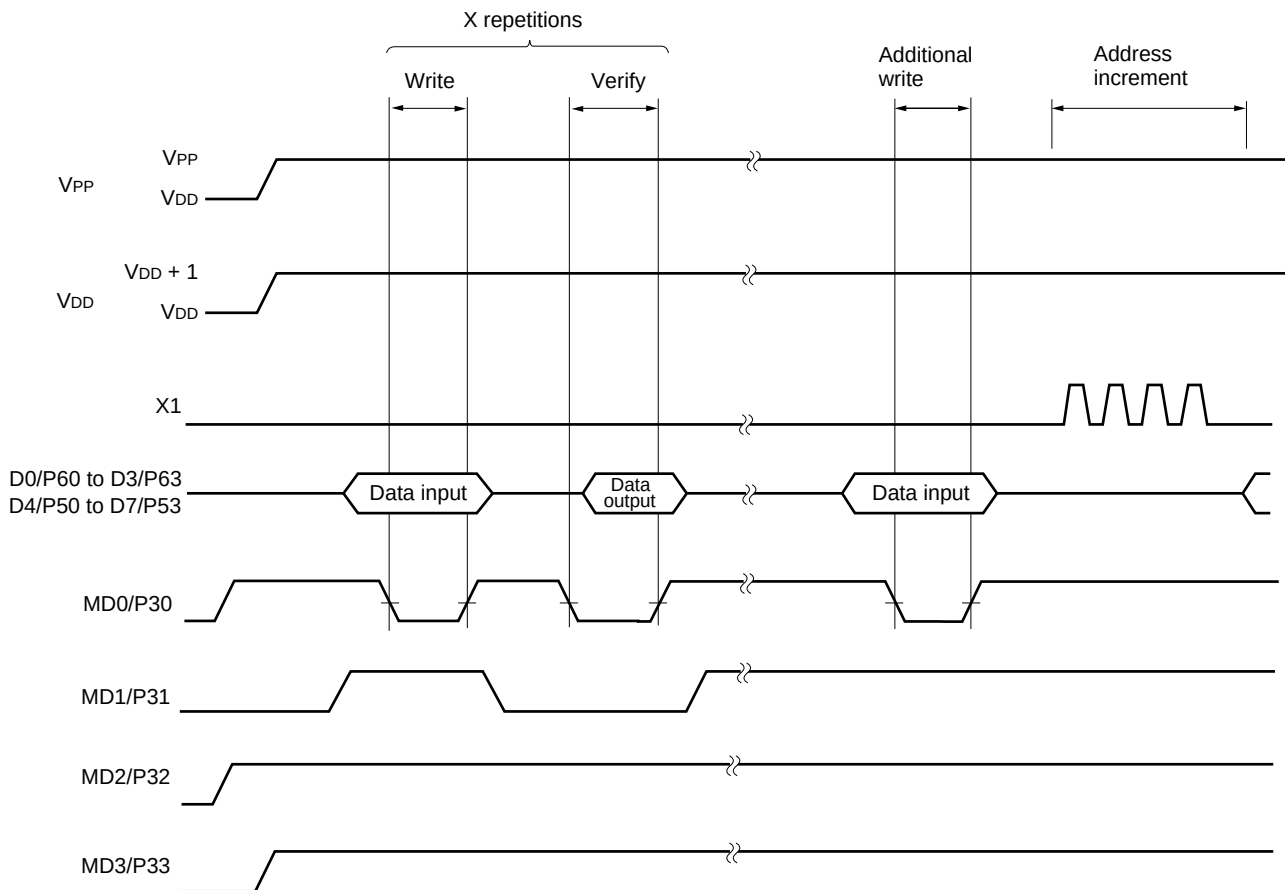
X: L or H

## ★ 8.2 Program Memory Write Procedure

Program memory can be written at high speed using the following procedure.

- (1) Pull down unused pins to  $V_{SS}$  through resistors. Set the X1 pin low.
- (2) Supply 5 V to the  $V_{DD}$  and  $V_{PP}$  pins.
- (3) Wait 10  $\mu s$ .
- (4) Select the program memory address zero-clear mode.
- (5) Supply 6 V to  $V_{DD}$  and 12.5 V to  $V_{PP}$  pins.
- (6) Write data in the 1-ms write mode.
- (7) Select the verify mode. If the data is written, go to (8) and if not, repeat (6) and (7).
- (8) Additional write. (X: number of write operations from (6) and (7))  $\times$  1 ms
- (9) Apply four pulses to the X1 pin to increment the program memory address by one.
- (10) Repeat (6) to (9) until the end address is reached.
- (11) Select the program memory address zero-clear mode.
- (12) Return the  $V_{DD}$ - and  $V_{PP}$ -pin voltages to 5 V.
- (13) Turn off the power.

The following figure shows steps (2) to (9).

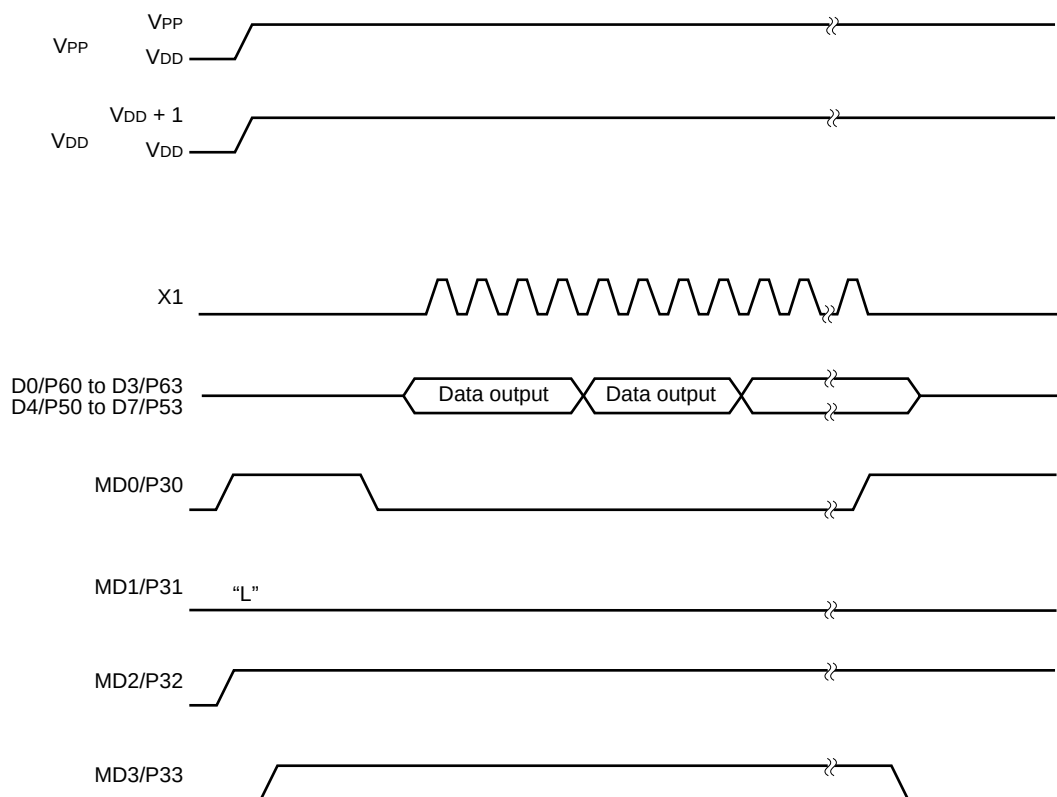


## ★ 8.3 Program Memory Read Procedure

The  $\mu$ PD75P3116 can read program memory contents using the following procedure.

- (1) Pull down unused pins to  $V_{SS}$  through resistors. Set the X1 pin low.
- (2) Supply 5 V to the  $V_{DD}$  and  $V_{PP}$  pins.
- (3) Wait 10  $\mu$ s.
- (4) Select the program memory address zero-clear mode.
- (5) Supply 6 V to the  $V_{DD}$  and 12.5 to the  $V_{PP}$  pins.
- (6) Select the verify mode. Apply four pulses to the X1 pin. Every four clock pulses will output the data stored in one address.
- (7) Select the program memory address zero-clear mode.
- (8) Return the  $V_{DD}$ - and  $V_{PP}$ -pin voltages to 5V.
- (9) Turn off the power.

The following figure shows steps (2) to (7).



#### 8.4 One-time PROM Screening

Due to its structure, the one-time PROM cannot be fully tested before shipment by NEC. Therefore, NEC recommends that after the required data is written and the PROM is stored under the temperature and time conditions shown below, the PROM should be verified via a screening.

| Storage temperature | Storage time |
|---------------------|--------------|
| 125°C               | 24 hours     |

- ★ NEC offers QTOP microcontrollers for which one-time PROM writing, marking, screening, and verification are provided at additional cost. For more detailed information, contact an NEC sales representative.

## 9. ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

| Parameter                     | Symbol           | Test Conditions          | Rating                       | Unit |
|-------------------------------|------------------|--------------------------|------------------------------|------|
| Power supply voltage          | V <sub>DD</sub>  |                          | −0.3 to +7.0                 | V    |
| PROM power supply voltage     | V <sub>PP</sub>  |                          | −0.3 to +13.5                | V    |
| Input voltage                 | V <sub>I1</sub>  | Except port 5            | −0.3 to V <sub>DD</sub> +0.3 | V    |
|                               | V <sub>I2</sub>  | Port 5 (N-ch open drain) | −0.3 to +14                  | V    |
| Output voltage                | V <sub>O</sub>   |                          | −0.3 to V <sub>DD</sub> +0.3 | V    |
| Output current high           | I <sub>OH</sub>  | Per pin                  | −10                          | mA   |
|                               |                  | Total of all pins        | −30                          | mA   |
| Output current low            | I <sub>OL</sub>  | Per pin                  | 30                           | mA   |
|                               |                  | Total of all pins        | 220                          | mA   |
| Operating ambient temperature | T <sub>A</sub>   |                          | −40 to +85 <sup>Note</sup>   | °C   |
| Storage temperature           | T <sub>stg</sub> |                          | −65 to +150                  | °C   |

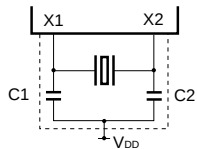
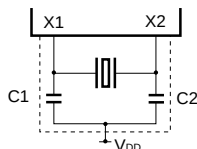
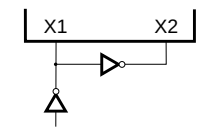
**Note** When LCD is driven in normal mode: T<sub>A</sub> = −10 to +85°C

**Caution** If any of the parameters exceeds the absolute maximum ratings, even momentarily, the reliability of the product may be impaired. The absolute maximum ratings are values that may physically damage the products. Be sure to use the products within the ratings.

### CAPACITANCE (T<sub>A</sub> = 25°C, V<sub>DD</sub> = 0 V)

| Parameter          | Symbol           | Test Conditions                               | MIN. | TYP. | MAX. | Unit |
|--------------------|------------------|-----------------------------------------------|------|------|------|------|
| Input capacitance  | C <sub>IN</sub>  | f = 1 MHz<br>Unmeasured pins returned to 0 V. |      |      | 15   | pF   |
| Output capacitance | C <sub>OUT</sub> |                                               |      |      | 15   | pF   |
| I/O capacitance    | C <sub>IO</sub>  |                                               |      |      | 15   | pF   |

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 1.8$  to  $5.5$  V)

| Resonator         | Recommended constant                                                              | Parameter                                              | Test conditions                                       | MIN. | TYP. | MAX.                  | Unit |
|-------------------|-----------------------------------------------------------------------------------|--------------------------------------------------------|-------------------------------------------------------|------|------|-----------------------|------|
| Ceramic resonator |  | Oscillation frequency ( $f_x$ ) <sup>Note 1</sup>      |                                                       | 1.0  |      | 6.0 <sup>Note 2</sup> | MHz  |
|                   |                                                                                   | Oscillation stabilization time <sup>Note 3</sup>       | After $V_{DD}$ reaches oscillation voltage range MIN. |      |      | 4                     | ms   |
| Crystal resonator |  | Oscillation frequency ( $f_x$ ) <sup>Note 1</sup>      |                                                       | 1.0  |      | 6.0 <sup>Note 2</sup> | MHz  |
|                   |                                                                                   | Oscillation stabilization time <sup>Note 3</sup>       | $V_{DD} = 4.5$ to $5.5$ V                             |      |      | 10<br>30              | ms   |
| ★ External clock  |  | X1 input frequency ( $f_x$ ) <sup>Note 1</sup>         |                                                       | 1.0  |      | 6.0 <sup>Note 2</sup> | MHz  |
|                   |                                                                                   | X1 input high-/low-level width ( $t_{XH}$ , $t_{XL}$ ) |                                                       | 83.3 |      | 500                   | ns   |

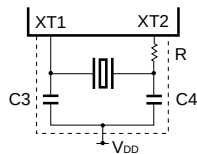
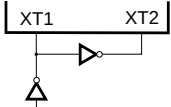
- Notes**
1. The oscillation frequency and X1 input frequency indicate characteristics of the oscillator only. For the instruction execution time, refer to AC Characteristics.
  2. When the power supply voltage is  $1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$  and the oscillation frequency is  $4.19\text{ MHz} < f_x \leq 6.0\text{ MHz}$ , setting the processor clock control register (PCC) to 0011 results in 1 machine cycle being less than the required  $0.95\text{ }\mu\text{s}$ . Therefore, set PCC to a value other than 0011.
  3. The oscillation stabilization time is necessary for oscillation to stabilize after applying  $V_{DD}$  or releasing the STOP mode.

**Caution** When using the main system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as  $V_{DD}$ .
- Do not ground to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.



**SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 1.8$  to  $5.5$  V)**

| Resonator         | Recommended constant                                                              | Parameter                                                 | Test conditions           | MIN. | TYP.   | MAX. | Unit |
|-------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------|---------------------------|------|--------|------|------|
| Crystal resonator |  | Oscillation frequency ( $f_{XT}$ ) <sup>Note 1</sup>      |                           | 32   | 32.768 | 35   | kHz  |
|                   |                                                                                   | Oscillation stabilization time <sup>Note 2</sup>          | $V_{DD} = 4.5$ to $5.5$ V |      | 1.0    | 2    | s    |
|                   |                                                                                   |                                                           |                           |      |        | 10   |      |
| External clock    |  | XT1 input frequency ( $f_{XT}$ ) <sup>Note 1</sup>        |                           | 32   |        | 100  | kHz  |
|                   |                                                                                   | XT1 input high-/low-level width ( $t_{XTH}$ , $t_{XTL}$ ) |                           | 5    |        | 15   | μs   |

- Notes**
1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.
  2. The oscillation stabilization time is necessary for oscillation to stabilize after applying  $V_{DD}$ .

**Caution** When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as  $V_{DD}$ .
- Do not ground to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

The subsystem clock oscillator is designed as a low amplification circuit to provide low consumption current, and is more liable to misoperation by noise than the main system clock oscillation circuit. Special care should therefore be taken regarding the wiring method when the subsystem clock is used.

DC CHARACTERISTICS (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

| Parameter                   | Symbol            | Test conditions                                                                 |                                                                                         | MIN.                    | TYP. | MAX.               | Unit               |    |
|-----------------------------|-------------------|---------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|-------------------------|------|--------------------|--------------------|----|
| Output current low          | I <sub>OL</sub>   | Per pin                                                                         |                                                                                         |                         |      | 15                 | mA                 |    |
|                             |                   | Total of all pins                                                               |                                                                                         |                         |      | 150                | mA                 |    |
| Input voltage high          | V <sub>IH1</sub>  | Ports 2, 3, 8, and 9                                                            | 2.7 ≤ V <sub>DD</sub> ≤ 5.5 V                                                           | 0.7V <sub>DD</sub>      |      | V <sub>DD</sub>    | V                  |    |
|                             |                   |                                                                                 | 1.8 ≤ V <sub>DD</sub> < 2.7 V                                                           | 0.9V <sub>DD</sub>      |      | V <sub>DD</sub>    | V                  |    |
|                             | V <sub>IH2</sub>  | Ports 0, 1, 6, $\overline{\text{RESET}}$                                        | 2.7 ≤ V <sub>DD</sub> ≤ 5.5 V                                                           | 0.8V <sub>DD</sub>      |      | V <sub>DD</sub>    | V                  |    |
|                             |                   |                                                                                 | 1.8 ≤ V <sub>DD</sub> < 2.7 V                                                           | 0.9V <sub>DD</sub>      |      | V <sub>DD</sub>    | V                  |    |
|                             | V <sub>IH3</sub>  | Port 5<br>(N-ch open-drain)                                                     | 2.7 ≤ V <sub>DD</sub> ≤ 5.5 V                                                           | 0.7V <sub>DD</sub>      |      | 13                 | V                  |    |
|                             |                   |                                                                                 | 1.8 ≤ V <sub>DD</sub> < 2.7 V                                                           | 0.9V <sub>DD</sub>      |      | 13                 | V                  |    |
| V <sub>IH4</sub>            | X1, XT1           |                                                                                 |                                                                                         | V <sub>DD</sub> - 0.1   |      | V <sub>DD</sub>    | V                  |    |
| Input voltage low           | V <sub>IL1</sub>  | Ports 2, 3, 5, 8, and 9                                                         | 2.7 ≤ V <sub>DD</sub> ≤ 5.5 V                                                           | 0                       |      | 0.3V <sub>DD</sub> | V                  |    |
|                             |                   |                                                                                 | 1.8 ≤ V <sub>DD</sub> < 2.7 V                                                           | 0                       |      | 0.1V <sub>DD</sub> | V                  |    |
|                             | V <sub>IL2</sub>  | Ports 0, 1, 6, $\overline{\text{RESET}}$                                        | 2.7 ≤ V <sub>DD</sub> ≤ 5.5 V                                                           | 0                       |      | 0.2V <sub>DD</sub> | V                  |    |
|                             |                   |                                                                                 | 1.8 ≤ V <sub>DD</sub> < 2.7 V                                                           | 0                       |      | 0.1V <sub>DD</sub> | V                  |    |
|                             | V <sub>IL3</sub>  | X1, XT1                                                                         |                                                                                         |                         | 0    |                    | 0.1                | V  |
| Output voltage high         | V <sub>OH</sub>   | $\overline{\text{SCK}}$ , SO, Ports 2, 3, 6, 8, and 9 I <sub>OH</sub> = -1.0 mA |                                                                                         | V <sub>DD</sub> - 0.5   |      |                    | V                  |    |
| Output voltage low          | V <sub>OL1</sub>  | $\overline{\text{SCK}}$ , SO, Ports 2, 3, 5, 6, 8, and 9                        | I <sub>OL</sub> = 15 mA,<br>V <sub>DD</sub> = 4.5 to 5.5 V                              |                         | 0.2  | 2.0                | V                  |    |
|                             |                   |                                                                                 | I <sub>OL</sub> = 1.6 mA                                                                |                         |      | 0.4                | V                  |    |
|                             | V <sub>OL2</sub>  | SB0, SB1                                                                        | When N-ch open-drain pull-up resistor ≥ 1 kΩ                                            |                         |      |                    | 0.2V <sub>DD</sub> | V  |
| Input leakage current high  | I <sub>LIH1</sub> | V <sub>IN</sub> = V <sub>DD</sub>                                               | Pins other than X1, XT1                                                                 |                         |      |                    | 3                  | μA |
|                             | I <sub>LIH2</sub> |                                                                                 | X1, XT1                                                                                 |                         |      |                    | 20                 | μA |
|                             | I <sub>LIH3</sub> | V <sub>IN</sub> = 13 V                                                          | Port 5 (N-ch open-drain)                                                                |                         |      |                    | 20                 | μA |
| Input leakage current low   | I <sub>LIL1</sub> | V <sub>IN</sub> = 0 V                                                           | Pins other than X1, XT1, and Port 5                                                     |                         |      |                    | -3                 | μA |
|                             | I <sub>LIL2</sub> |                                                                                 | X1, XT1                                                                                 |                         |      |                    | -20                | μA |
|                             | I <sub>LIL3</sub> |                                                                                 | Port 5 (N-ch open-drain)<br>When another instruction than input instruction is executed |                         |      |                    | -3                 | μA |
|                             |                   |                                                                                 | Port 5 (N-ch open-drain)                                                                |                         |      |                    | -30                | μA |
|                             |                   |                                                                                 | When input instruction is executed                                                      | V <sub>DD</sub> = 5.0 V |      | -10                | -27                | μA |
|                             |                   |                                                                                 |                                                                                         | V <sub>DD</sub> = 3.0 V |      | -3                 | -8                 | μA |
| Output leakage current high | I <sub>LOH1</sub> | V <sub>OUT</sub> = V <sub>DD</sub>                                              | $\overline{\text{SCK}}$ , SO/SB0, SB1, Ports 2, 3, 6, 8, and 9                          |                         |      |                    | 3                  | μA |
|                             | I <sub>LOH2</sub> | V <sub>OUT</sub> = 13 V                                                         | Port 5 (N-ch open-drain)                                                                |                         |      |                    | 20                 | μA |
| Output leakage current low  | I <sub>LOL</sub>  | V <sub>OUT</sub> = 0 V                                                          |                                                                                         |                         |      |                    | -3                 | μA |
| On-chip pull-up resistor    | R <sub>L</sub>    | V <sub>IN</sub> = 0 V                                                           | Ports 0, 1, 2, 3, 6, 8, and 9<br>(Excluding P00 pin)                                    |                         | 50   | 100                | 200                | kΩ |

★

DC CHARACTERISTICS (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

| Parameter                                                | Symbol                                       | Test conditions                                     |                                                                                          |                                                |           | MIN.                               | TYP.                          | MAX. | Unit |
|----------------------------------------------------------|----------------------------------------------|-----------------------------------------------------|------------------------------------------------------------------------------------------|------------------------------------------------|-----------|------------------------------------|-------------------------------|------|------|
| LCD drive voltage                                        | V <sub>LCD</sub>                             | VAC0 = 0                                            | T <sub>A</sub> = −40 to +85°C                                                            |                                                | 2.7       |                                    | V <sub>DD</sub>               | V    |      |
|                                                          |                                              |                                                     | T <sub>A</sub> = −10 to +85°C                                                            |                                                | 2.2       |                                    | V <sub>DD</sub>               | V    |      |
|                                                          |                                              | VAC0 = 1                                            |                                                                                          |                                                | 1.8       |                                    | V <sub>DD</sub>               | V    |      |
| VAC current <sup>Note 1</sup>                            | I <sub>VAC</sub>                             | VAC0 = 1, V <sub>DD</sub> = 2.0 V ± 10%             |                                                                                          |                                                |           |                                    | 1                             | 4    | μA   |
| LCD output voltage deviation <sup>Note 2</sup> (common)  | V <sub>ODC</sub>                             | I <sub>o</sub> = ±1.0 μA                            | V <sub>LCD0</sub> = V <sub>LCD</sub><br>V <sub>LCD1</sub> = V <sub>LCD</sub> × 2/3       |                                                |           | 0                                  |                               | ±0.2 | V    |
| LCD output voltage deviation <sup>Note 2</sup> (segment) | V <sub>ODS</sub>                             | I <sub>o</sub> = ±0.5 μA                            | V <sub>LCD2</sub> = V <sub>LCD</sub> × 1/3<br>1.8 V ≤ V <sub>LCD</sub> ≤ V <sub>DD</sub> |                                                |           | 0                                  |                               | ±0.2 | V    |
| Supply current <sup>Note 3</sup>                         | I <sub>DD1</sub>                             | 6.00 MHz <sup>Note 4</sup>                          | V <sub>DD</sub> = 5.0 V ± 10% <sup>Note 5</sup>                                          |                                                |           |                                    | 3.2                           | 9.5  | mA   |
|                                                          |                                              | Crystal oscillation                                 | V <sub>DD</sub> = 3.0 V ± 10% <sup>Note 6</sup>                                          |                                                |           |                                    | 0.55                          | 1.6  | mA   |
|                                                          | I <sub>DD2</sub>                             | C1 = C2 = 22 pF                                     | HALT mode                                                                                | V <sub>DD</sub> = 5.0 V ± 10%                  |           |                                    | 0.7                           | 2.0  | mA   |
|                                                          |                                              |                                                     |                                                                                          | V <sub>DD</sub> = 3.0 V ± 10%                  |           |                                    | 0.25                          | 0.8  | mA   |
|                                                          | I <sub>DD1</sub>                             | 4.19 MHz <sup>Note 4</sup>                          | V <sub>DD</sub> = 5.0 V ± 10% <sup>Note 5</sup>                                          |                                                |           |                                    | 2.5                           | 7.5  | mA   |
|                                                          |                                              | Crystal oscillation                                 | V <sub>DD</sub> = 3.0 V ± 10% <sup>Note 6</sup>                                          |                                                |           |                                    | 0.45                          | 1.35 | mA   |
|                                                          | I <sub>DD2</sub>                             | C1 = C2 = 22 pF                                     | HALT mode                                                                                | V <sub>DD</sub> = 5.0 V ± 10%                  |           |                                    | 0.65                          | 1.8  | mA   |
|                                                          |                                              |                                                     |                                                                                          | V <sub>DD</sub> = 3.0 V ± 10%                  |           |                                    | 0.22                          | 0.7  | mA   |
|                                                          | I <sub>DD3</sub>                             | 32.768 kHz <sup>Note 7</sup><br>Crystal oscillation | Low-voltage mode <sup>Note 8</sup>                                                       | V <sub>DD</sub> = 3.0 V ± 10%                  |           |                                    | 45                            | 130  | μA   |
|                                                          |                                              |                                                     |                                                                                          | V <sub>DD</sub> = 2.0 V ± 10%                  |           |                                    | 20                            | 55   | μA   |
|                                                          |                                              |                                                     |                                                                                          | V <sub>DD</sub> = 3.0 V, T <sub>A</sub> = 25°C |           |                                    | 45                            | 90   | μA   |
|                                                          |                                              |                                                     | Low power consumption mode <sup>Note 9</sup>                                             | V <sub>DD</sub> = 3.0 V ± 10%                  |           |                                    | 42                            | 120  | μA   |
|                                                          |                                              |                                                     |                                                                                          | V <sub>DD</sub> = 3.0 V, T <sub>A</sub> = 25°C |           |                                    | 42                            | 85   | μA   |
|                                                          |                                              |                                                     |                                                                                          | I <sub>DD4</sub>                               | HALT mode | Low-voltage mode <sup>Note 8</sup> | V <sub>DD</sub> = 3.0 V ± 10% |      | 5.5  |
|                                                          | V <sub>DD</sub> = 2.0 V ± 10%                |                                                     | 2.2                                                                                      |                                                |           |                                    | 7                             | μA   |      |
|                                                          | Low power consumption mode <sup>Note 9</sup> | V <sub>DD</sub> = 3.0 V, T <sub>A</sub> = 25°C      |                                                                                          |                                                |           | 5.5                                | 12                            | μA   |      |
|                                                          |                                              | V <sub>DD</sub> = 3.0 V ± 10%                       |                                                                                          |                                                |           | 4.0                                | 12                            | μA   |      |
|                                                          | I <sub>DD4</sub>                             |                                                     | Low power consumption mode <sup>Note 9</sup>                                             | V <sub>DD</sub> = 3.0 V, T <sub>A</sub> = 25°C |           |                                    | 4.0                           | 8    | μA   |
|                                                          |                                              |                                                     |                                                                                          |                                                |           |                                    |                               |      |      |
|                                                          |                                              |                                                     |                                                                                          |                                                |           |                                    |                               |      |      |
|                                                          | I <sub>DD5</sub>                             | XT1 = 0 V <sup>Note 10</sup><br>STOP mode           | V <sub>DD</sub> = 5.0 V ± 10%                                                            |                                                |           |                                    | 0.05                          | 10   | μA   |
| V <sub>DD</sub> = 3.0 V<br>± 10%                         |                                              |                                                     |                                                                                          |                                                |           | 0.02                               | 5                             | μA   |      |
|                                                          |                                              |                                                     | T <sub>A</sub> = 25°C                                                                    |                                                |           | 0.02                               | 3                             | μA   |      |

★ **Notes 1.** Set to VAC0 = 0 when the low power consumption mode and the stop mode are used. If VAC0 = 1 is set, the current increases for approx. 1 μA.

2. The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V<sub>LCDn</sub>; n = 0, 1, 2).

3. Not including currents flowing in on-chip pull-up resistors.

4. Including oscillation of the subsystem clock.

5. When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

6. When PCC is set to 0000 and the device is operated in the low-speed mode.

7. When the system clock control register (SCC) is set to 1001 and the device is operated on the subsystem clock, with main system clock oscillation stopped.

★ 8. When the sub-oscillation circuit control register (SOS) is set to 0000.

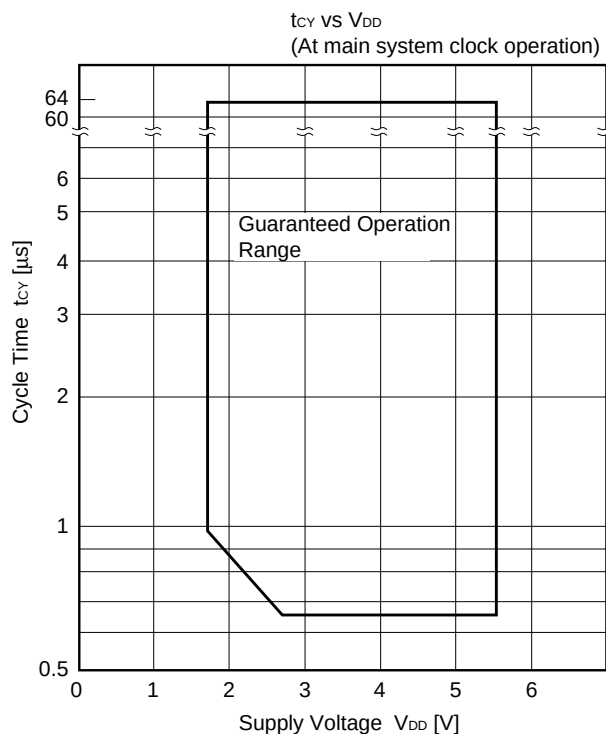
★ 9. When SOS is set to 0010.

★ 10. When SOS is set to 00×1 and the feedback resistor of the sub-oscillation circuit is not used.

**AC CHARACTERISTICS ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 1.8$  to  $5.5$  V)**

| Parameter                                                                                     | Symbol               | Test conditions                |                           | MIN.          | TYP. | MAX. | Unit          |
|-----------------------------------------------------------------------------------------------|----------------------|--------------------------------|---------------------------|---------------|------|------|---------------|
| CPU clock cycle time <sup>Note 1</sup><br>(Min. instruction execution time = 1 machine cycle) | $t_{CY}$             | Operating on main system clock | $V_{DD} = 2.7$ to $5.5$ V | 0.67          |      | 64   | $\mu\text{s}$ |
|                                                                                               |                      |                                |                           | 0.95          |      | 64   | $\mu\text{s}$ |
|                                                                                               |                      | Operating on subsystem clock   |                           | 114           | 122  | 125  | $\mu\text{s}$ |
| TI0, TI1, TI2 input frequency                                                                 | $f_{TI}$             | $V_{DD} = 2.7$ to $5.5$ V      |                           | 0             |      | 1.0  | MHz           |
|                                                                                               |                      |                                |                           | 0             |      | 275  | kHz           |
| TI0, TI1, TI2 input high-/low-level width                                                     | $t_{TIH}, t_{TIL}$   | $V_{DD} = 2.7$ to $5.5$ V      |                           | 0.48          |      |      | $\mu\text{s}$ |
|                                                                                               |                      |                                |                           | 1.8           |      |      | $\mu\text{s}$ |
| Interrupt input high-/low-level width                                                         | $t_{INTH}, t_{INTL}$ | INT0                           | IM02 = 0                  | <b>Note 2</b> |      |      | $\mu\text{s}$ |
|                                                                                               |                      |                                | IM02 = 1                  | 10            |      |      | $\mu\text{s}$ |
|                                                                                               |                      | INT1, 2, 4                     |                           | 10            |      |      | $\mu\text{s}$ |
|                                                                                               |                      | KR0 to KR7                     |                           | 10            |      |      | $\mu\text{s}$ |
| $\overline{\text{RESET}}$ low-level width                                                     | $t_{RSL}$            |                                |                           | 10            |      |      | $\mu\text{s}$ |

- Notes 1.** The cycle time (minimum instruction execution time) of the CPU clock ( $\Phi$ ) is determined by the oscillation frequency of the connected resonator (and external clock), the system clock control register (SCC) and the processor clock control register (PCC). The figure at the right indicates the cycle time  $t_{CY}$  versus supply voltage  $V_{DD}$  characteristic with the main system clock operating.
- 2.**  $2t_{CY}$  or  $128/f_x$  is set by setting the interrupt mode register (IM0).



## SERIAL TRANSFER OPERATION

2-Wire and 3-Wire Serial I/O Mode ( $\overline{\text{SCK}}$ ...Internal clock output): ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 1.8$  to  $5.5$  V)

| Parameter                                                                               | Symbol                           | Test conditions                         |                           | MIN.                    | TYP. | MAX. | Unit |
|-----------------------------------------------------------------------------------------|----------------------------------|-----------------------------------------|---------------------------|-------------------------|------|------|------|
| $\overline{\text{SCK}}$ cycle time                                                      | $t_{\text{KCY1}}$                | $V_{DD} = 2.7$ to $5.5$ V               |                           | 1300                    |      |      | ns   |
|                                                                                         |                                  |                                         |                           | 3800                    |      |      | ns   |
| $\overline{\text{SCK}}$ high-/low-level width                                           | $t_{\text{KL1}}, t_{\text{KH1}}$ | $V_{DD} = 2.7$ to $5.5$ V               |                           | $t_{\text{KCY1}}/2-50$  |      |      | ns   |
|                                                                                         |                                  |                                         |                           | $t_{\text{KCY1}}/2-150$ |      |      | ns   |
| SI <sup>Note 1</sup> setup time<br>(to $\overline{\text{SCK}}\uparrow$ )                | $t_{\text{SIK1}}$                | $V_{DD} = 2.7$ to $5.5$ V               |                           | 150                     |      |      | ns   |
|                                                                                         |                                  |                                         |                           | 500                     |      |      | ns   |
| SI <sup>Note 1</sup> hold time<br>(from $\overline{\text{SCK}}\uparrow$ )               | $t_{\text{KSI1}}$                | $V_{DD} = 2.7$ to $5.5$ V               |                           | 400                     |      |      | ns   |
|                                                                                         |                                  |                                         |                           | 600                     |      |      | ns   |
| $\overline{\text{SCK}}\downarrow\rightarrow\text{SO}^{\text{Note 1}}$ output delay time | $t_{\text{KSO1}}$                | $R_L = 1\text{ k}\Omega$ ,              | $V_{DD} = 2.7$ to $5.5$ V | 0                       |      | 250  | ns   |
|                                                                                         |                                  | $C_L = 100\text{ pF}$ <sup>Note 2</sup> |                           | 0                       |      | 1000 | ns   |

**Notes 1.** In 2-wire serial I/O mode, read this parameter as SB0 or SB1 instead.

**2.**  $R_L$  and  $C_L$  are the load resistance and load capacitance of the SO output lines, respectively.

2-Wire and 3-Wire Serial I/O Mode ( $\overline{\text{SCK}}$ ...External clock input): ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 1.8$  to  $5.5$  V)

| Parameter                                                                               | Symbol                           | Test conditions                         |                           | MIN. | TYP. | MAX. | Unit |
|-----------------------------------------------------------------------------------------|----------------------------------|-----------------------------------------|---------------------------|------|------|------|------|
| $\overline{\text{SCK}}$ cycle time                                                      | $t_{\text{KCY2}}$                | $V_{DD} = 2.7$ to $5.5$ V               |                           | 800  |      |      | ns   |
|                                                                                         |                                  |                                         |                           | 3200 |      |      | ns   |
| $\overline{\text{SCK}}$ high-/low-level width                                           | $t_{\text{KL2}}, t_{\text{KH2}}$ | $V_{DD} = 2.7$ to $5.5$ V               |                           | 400  |      |      | ns   |
|                                                                                         |                                  |                                         |                           | 1600 |      |      | ns   |
| SI <sup>Note 1</sup> setup time<br>(to $\overline{\text{SCK}}\uparrow$ )                | $t_{\text{SIK2}}$                | $V_{DD} = 2.7$ to $5.5$ V               |                           | 100  |      |      | ns   |
|                                                                                         |                                  |                                         |                           | 150  |      |      | ns   |
| SI <sup>Note 1</sup> hold time<br>(from $\overline{\text{SCK}}\uparrow$ )               | $t_{\text{KSI2}}$                | $V_{DD} = 2.7$ to $5.5$ V               |                           | 400  |      |      | ns   |
|                                                                                         |                                  |                                         |                           | 600  |      |      | ns   |
| $\overline{\text{SCK}}\downarrow\rightarrow\text{SO}^{\text{Note 1}}$ output delay time | $t_{\text{KSO2}}$                | $R_L = 1\text{ k}\Omega$ ,              | $V_{DD} = 2.7$ to $5.5$ V | 0    |      | 300  | ns   |
|                                                                                         |                                  | $C_L = 100\text{ pF}$ <sup>Note 2</sup> |                           | 0    |      | 1000 | ns   |

**Notes 1.** In 2-wire serial I/O mode, read this parameter as SB0 or SB1 instead.

**2.**  $R_L$  and  $C_L$  are the load resistance and load capacitance of the SO output lines, respectively.

**SBI Mode ( $\overline{\text{SCK}}$ ...Internal clock output (master)): ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 1.8$  to  $5.5$  V)**

| Parameter                                                              | Symbol                           | Test conditions                                              |                           | MIN.                    | TYP. | MAX. | Unit |
|------------------------------------------------------------------------|----------------------------------|--------------------------------------------------------------|---------------------------|-------------------------|------|------|------|
| $\overline{\text{SCK}}$ cycle time                                     | $t_{\text{KCY3}}$                | $V_{DD} = 2.7$ to $5.5$ V                                    |                           | 1300                    |      |      | ns   |
|                                                                        |                                  |                                                              |                           | 3800                    |      |      | ns   |
| $\overline{\text{SCK}}$ high-/low-level width                          | $t_{\text{KL3}}, t_{\text{KH3}}$ | $V_{DD} = 2.7$ to $5.5$ V                                    |                           | $t_{\text{KCY3}}/2-50$  |      |      | ns   |
|                                                                        |                                  |                                                              |                           | $t_{\text{KCY3}}/2-150$ |      |      | ns   |
| SB0, 1 setup time (to $\overline{\text{SCK}}\uparrow$ )                | $t_{\text{SIK3}}$                | $V_{DD} = 2.7$ to $5.5$ V                                    |                           | 150                     |      |      | ns   |
|                                                                        |                                  |                                                              |                           | 500                     |      |      | ns   |
| SB0, 1 hold time (from $\overline{\text{SCK}}\uparrow$ )               | $t_{\text{KSI3}}$                |                                                              |                           | $t_{\text{KCY3}}/2$     |      |      | ns   |
| $\overline{\text{SCK}}\downarrow \rightarrow$ SB0, 1 output delay time | $t_{\text{KSO3}}$                | $R_L = 1$ k $\Omega$ ,<br>$C_L = 100$ pF <small>Note</small> | $V_{DD} = 2.7$ to $5.5$ V | 0                       |      | 250  | ns   |
|                                                                        |                                  |                                                              |                           | 0                       |      | 1000 | ns   |
| $\overline{\text{SCK}}\uparrow \rightarrow$ SB0, 1 $\downarrow$        | $t_{\text{KSB}}$                 |                                                              |                           | $t_{\text{KCY3}}$       |      |      | ns   |
| SB0, 1 $\downarrow \rightarrow \overline{\text{SCK}}\downarrow$        | $t_{\text{SBK}}$                 |                                                              |                           | $t_{\text{KCY3}}$       |      |      | ns   |
| SB0, 1 low-level width                                                 | $t_{\text{SBL}}$                 |                                                              |                           | $t_{\text{KCY3}}$       |      |      | ns   |
| SB0, 1 high-level width                                                | $t_{\text{SBH}}$                 |                                                              |                           | $t_{\text{KCY3}}$       |      |      | ns   |

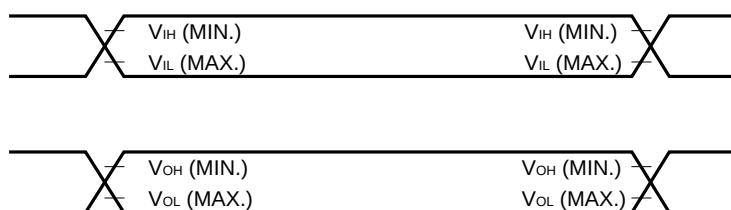
**Note**  $R_L$  and  $C_L$  are the load resistance and load capacitance of the SB0 and SB1 output lines, respectively.

**SBI Mode ( $\overline{\text{SCK}}$ ...External clock input (slave)): ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 1.8$  to  $5.5$  V)**

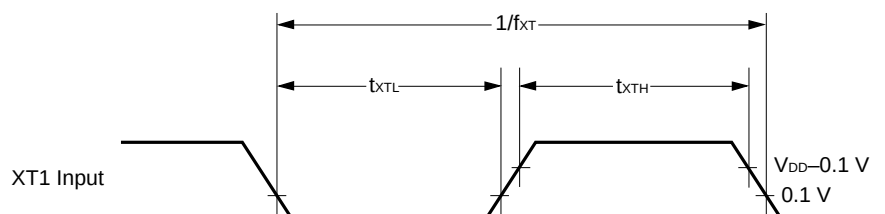
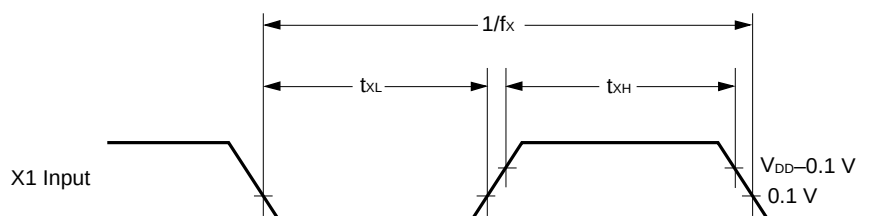
| Parameter                                                              | Symbol                           | Test conditions                                              |                           | MIN.                | TYP. | MAX. | Unit |
|------------------------------------------------------------------------|----------------------------------|--------------------------------------------------------------|---------------------------|---------------------|------|------|------|
| $\overline{\text{SCK}}$ cycle time                                     | $t_{\text{KCY4}}$                | $V_{DD} = 2.7$ to $5.5$ V                                    |                           | 800                 |      |      | ns   |
|                                                                        |                                  |                                                              |                           | 3200                |      |      | ns   |
| $\overline{\text{SCK}}$ high-/low-level width                          | $t_{\text{KL4}}, t_{\text{KH4}}$ | $V_{DD} = 2.7$ to $5.5$ V                                    |                           | 400                 |      |      | ns   |
|                                                                        |                                  |                                                              |                           | 1600                |      |      | ns   |
| SB0, 1 setup time (to $\overline{\text{SCK}}\uparrow$ )                | $t_{\text{SIK4}}$                | $V_{DD} = 2.7$ to $5.5$ V                                    |                           | 100                 |      |      | ns   |
|                                                                        |                                  |                                                              |                           | 150                 |      |      | ns   |
| SB0, 1 hold time (from $\overline{\text{SCK}}\uparrow$ )               | $t_{\text{KSI4}}$                |                                                              |                           | $t_{\text{KCY4}}/2$ |      |      | ns   |
| $\overline{\text{SCK}}\downarrow \rightarrow$ SB0, 1 output delay time | $t_{\text{KSO4}}$                | $R_L = 1$ k $\Omega$ ,<br>$C_L = 100$ pF <small>Note</small> | $V_{DD} = 2.7$ to $5.5$ V | 0                   |      | 300  | ns   |
|                                                                        |                                  |                                                              |                           | 0                   |      | 1000 | ns   |
| $\overline{\text{SCK}}\uparrow \rightarrow$ SB0, 1 $\downarrow$        | $t_{\text{KSB}}$                 |                                                              |                           | $t_{\text{KCY4}}$   |      |      | ns   |
| SB0, 1 $\downarrow \rightarrow \overline{\text{SCK}}\downarrow$        | $t_{\text{SBK}}$                 |                                                              |                           | $t_{\text{KCY4}}$   |      |      | ns   |
| SB0, 1 low-level width                                                 | $t_{\text{SBL}}$                 |                                                              |                           | $t_{\text{KCY4}}$   |      |      | ns   |
| SB0, 1 high-level width                                                | $t_{\text{SBH}}$                 |                                                              |                           | $t_{\text{KCY4}}$   |      |      | ns   |

**Note**  $R_L$  and  $C_L$  are the load resistance and load capacitance of the SB0 and SB1 output lines, respectively.

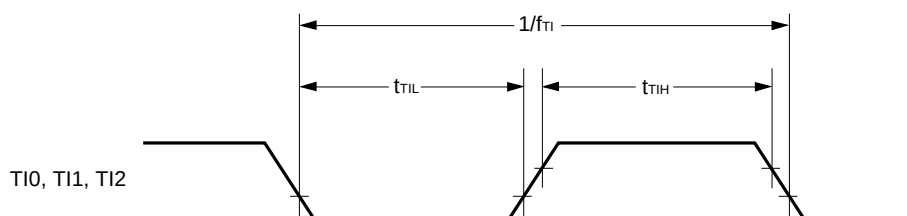
★ AC Timing Test Point (Excluding X1, XT1 Input)



★ Clock Timing

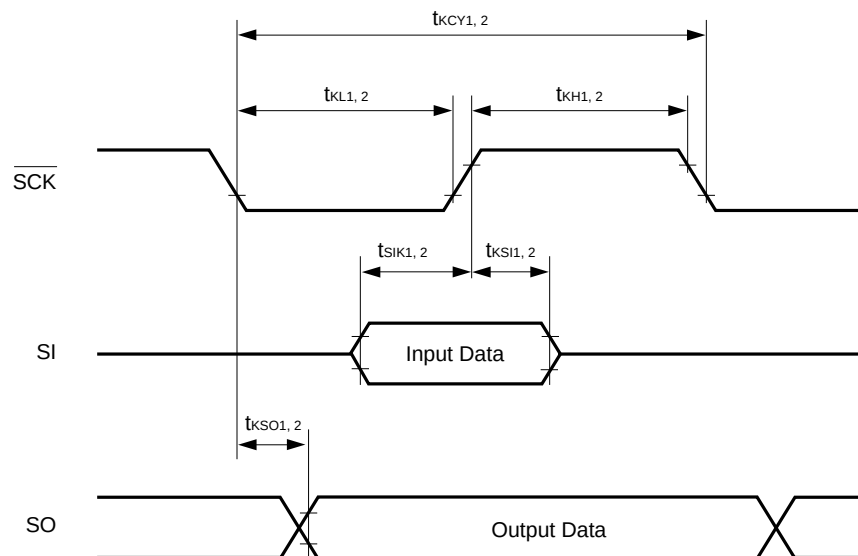


TI0, TI1, TI2 Timing

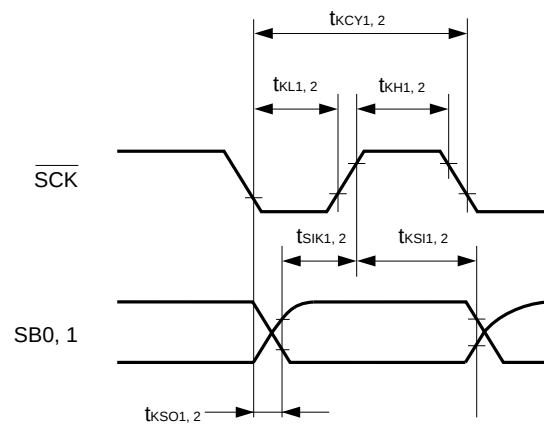


## Serial Transfer Timing

### 3-wire serial I/O mode



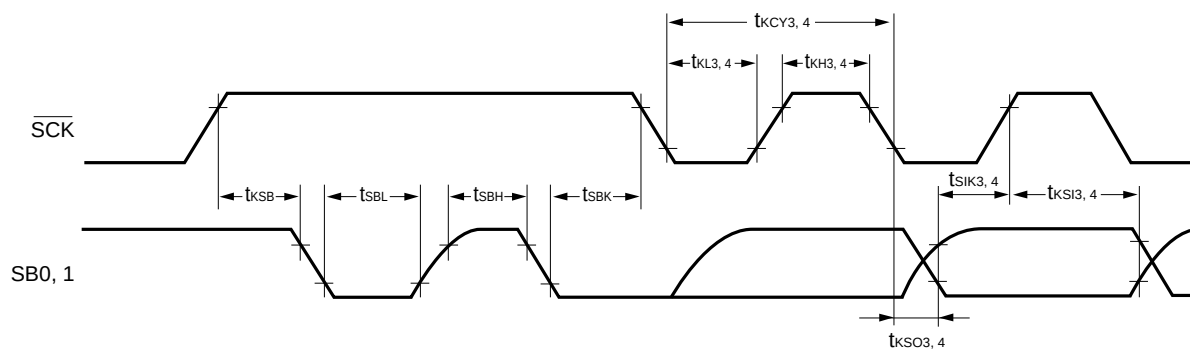
### 2-wire serial I/O mode



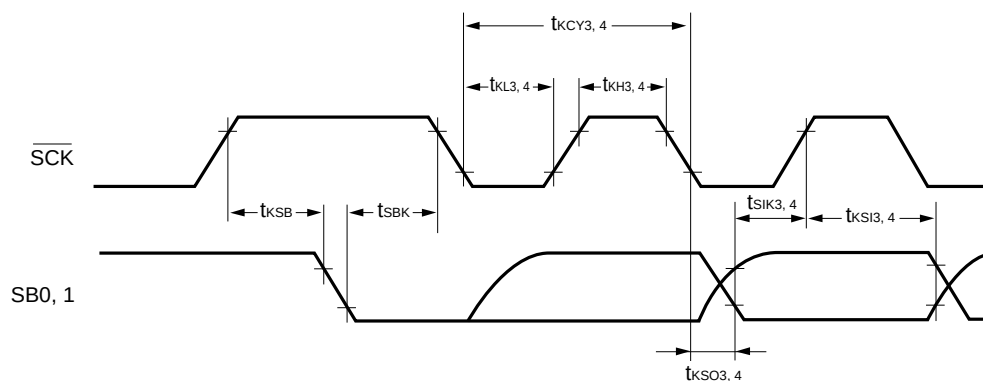


## Serial Transfer Timing

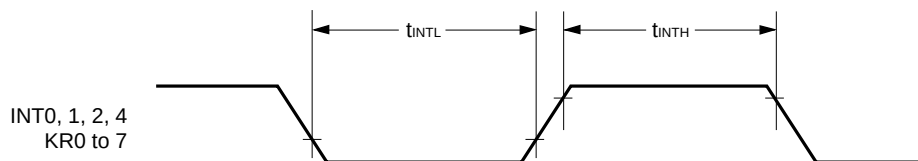
### Bus release signal transfer



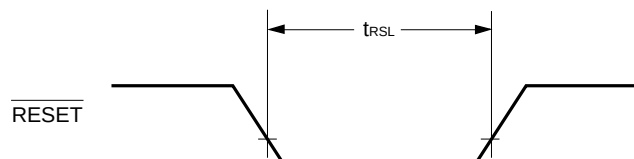
### Command signal transfer



### Interrupt input timing



### RESET input timing



## DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

(T<sub>A</sub> = -40 to +85°C)

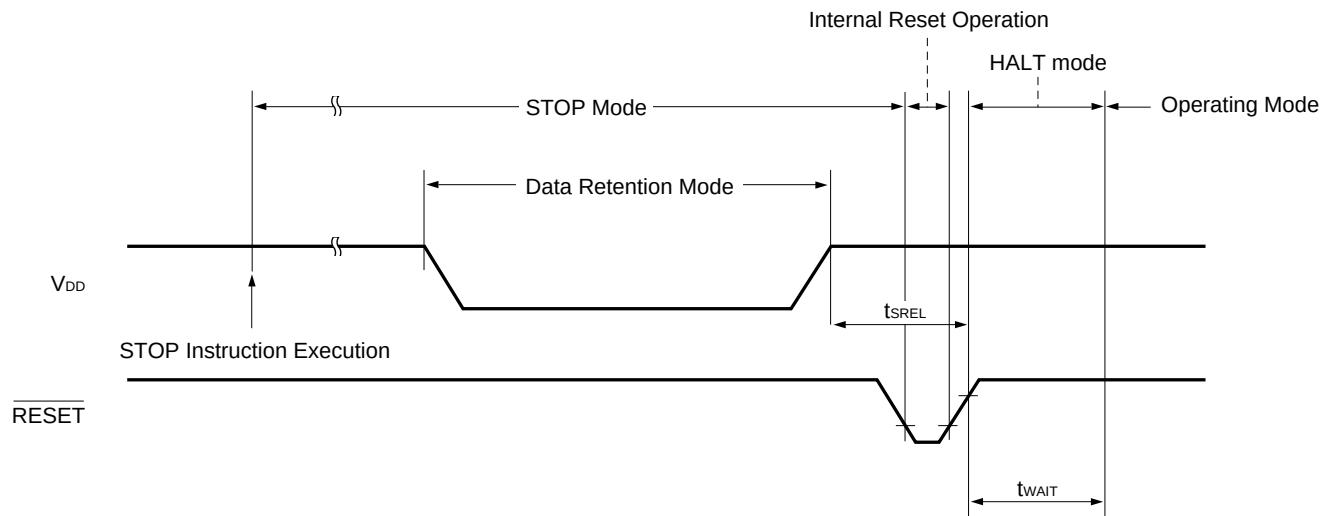
| Parameter                                                 | Symbol            | Test conditions                      | MIN. | TYP.                            | MAX. | Unit |
|-----------------------------------------------------------|-------------------|--------------------------------------|------|---------------------------------|------|------|
| Release signal set time                                   | t <sub>SREL</sub> |                                      | 0    |                                 |      | μs   |
| Oscillation stabilization wait time <small>Note 1</small> | t <sub>WAIT</sub> | Release by $\overline{\text{RESET}}$ |      | 2 <sup>15</sup> /f <sub>x</sub> |      | ms   |
|                                                           |                   | Release by interrupt request         |      | <b>Note 2</b>                   |      | ms   |

**Notes 1.** The oscillation stabilization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the oscillation start.

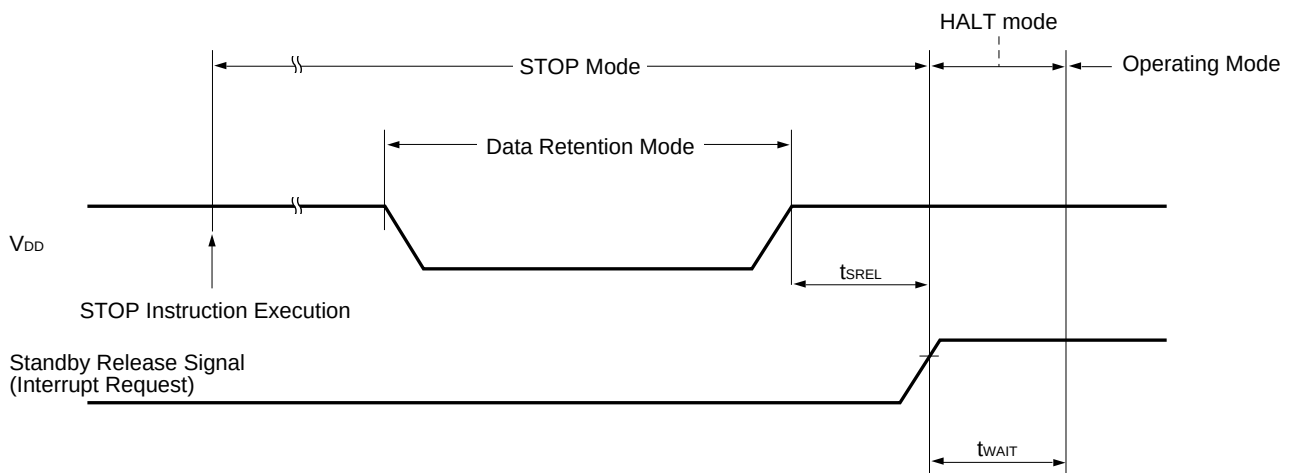
**2.** Depends on the basic interval timer mode register (BTM) settings (See the table below).

| BTM3 | BTM2 | BTM1 | BTM0 | Wait time                                         |                                                   |
|------|------|------|------|---------------------------------------------------|---------------------------------------------------|
|      |      |      |      | f <sub>x</sub> = at 4.19 MHz                      | f <sub>x</sub> = at 6.0 MHz                       |
| —    | 0    | 0    | 0    | 2 <sup>20</sup> /f <sub>x</sub> (approx. 250 ms)  | 2 <sup>20</sup> /f <sub>x</sub> (approx. 175 ms)  |
| —    | 0    | 1    | 1    | 2 <sup>17</sup> /f <sub>x</sub> (approx. 31.3 ms) | 2 <sup>17</sup> /f <sub>x</sub> (approx. 21.8 ms) |
| —    | 1    | 0    | 1    | 2 <sup>15</sup> /f <sub>x</sub> (approx. 7.81 ms) | 2 <sup>15</sup> /f <sub>x</sub> (approx. 5.46 ms) |
| —    | 1    | 1    | 1    | 2 <sup>13</sup> /f <sub>x</sub> (approx. 1.95 ms) | 2 <sup>13</sup> /f <sub>x</sub> (approx. 1.37 ms) |

### Data Retention Timing (STOP Mode Release by RESET)



### Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



**DC PROGRAMMING CHARACTERISTICS** ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 6.0 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5 \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                     | Symbol    | Test conditions                 | MIN.         | TYP. | MAX.        | Unit          |
|-------------------------------|-----------|---------------------------------|--------------|------|-------------|---------------|
| Input voltage high            | $V_{IH1}$ | Except X1 and X2 pins           | $0.7V_{DD}$  |      | $V_{DD}$    | V             |
|                               | $V_{IH2}$ | X1, X2                          | $V_{DD}-0.5$ |      | $V_{DD}$    | V             |
| Input voltage low             | $V_{IL1}$ | Except X1 and X2 pins           | 0            |      | $0.3V_{DD}$ | V             |
|                               | $V_{IL2}$ | X1, X2                          | 0            |      | 0.4         | V             |
| Input leakage current         | $I_{LI}$  | $V_{IN} = V_{IL}$ or $V_{IH}$   |              |      | 10          | $\mu\text{A}$ |
| Output voltage high           | $V_{OH}$  | $I_{OH} = -1\text{ mA}$         | $V_{DD}-1.0$ |      |             | V             |
| Output voltage low            | $V_{OL}$  | $I_{OL} = 1.6\text{ mA}$        |              |      | 0.4         | V             |
| $V_{DD}$ power supply current | $I_{DD}$  |                                 |              |      | 30          | mA            |
| $V_{PP}$ power supply current | $I_{PP}$  | MD0 = $V_{IL}$ , MD1 = $V_{IH}$ |              |      | 30          | mA            |

**Cautions 1. Avoid exceeding +13.5 V for  $V_{PP}$  including the overshoot.**

**2.  $V_{DD}$  must be applied before  $V_{PP}$ , and cut after  $V_{PP}$ .**

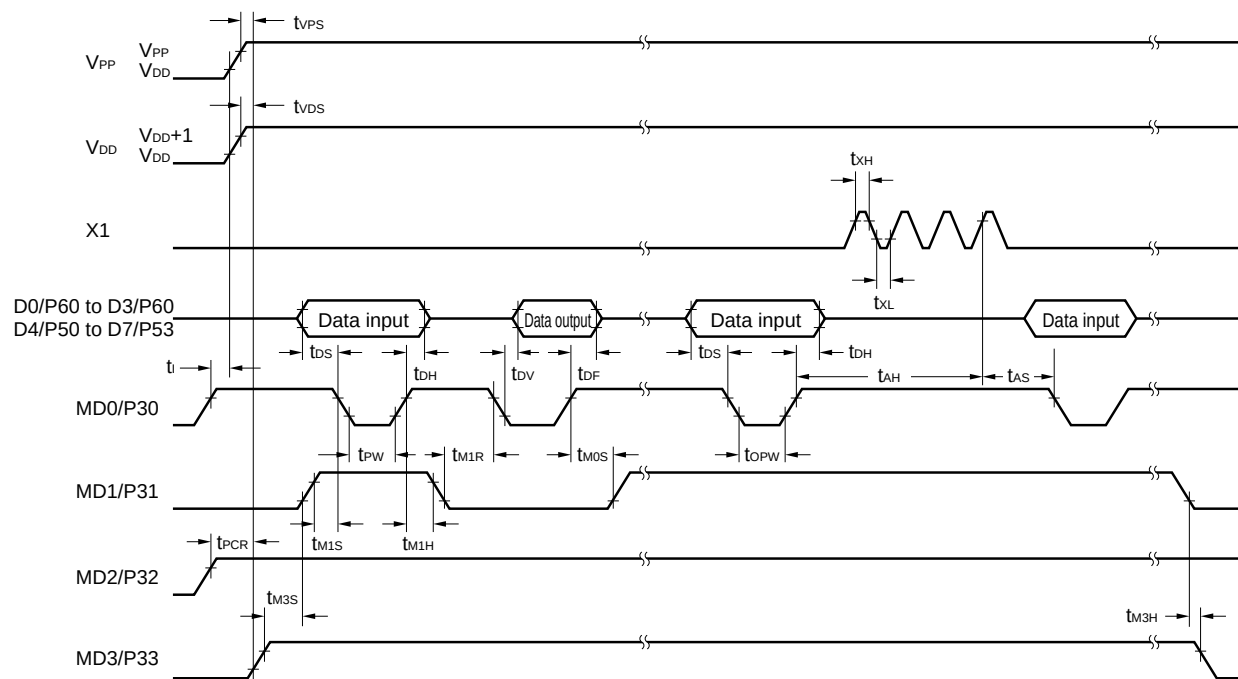
**AC PROGRAMMING CHARACTERISTICS** ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 6.0 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5 \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                                          | Symbol              | Note 1     | Test conditions                                | MIN.  | TYP. | MAX. | Unit          |
|----------------------------------------------------|---------------------|------------|------------------------------------------------|-------|------|------|---------------|
| Address setup time <sup>Note 2</sup> (to MD0↓)     | $t_{AS}$            | $t_{AS}$   |                                                | 2     |      |      | $\mu\text{s}$ |
| MD1 setup time (to MD0↓)                           | $t_{M1S}$           | $t_{OES}$  |                                                | 2     |      |      | $\mu\text{s}$ |
| Data setup time (to MD0↓)                          | $t_{DS}$            | $t_{DS}$   |                                                | 2     |      |      | $\mu\text{s}$ |
| Address hold time <sup>Note 2</sup> (from MD0↑)    | $t_{AH}$            | $t_{AH}$   |                                                | 2     |      |      | $\mu\text{s}$ |
| Data hold time (from MD0↑)                         | $t_{DH}$            | $t_{DH}$   |                                                | 2     |      |      | $\mu\text{s}$ |
| MD0↑→data output float delay time                  | $t_{DF}$            | $t_{DF}$   |                                                | 0     |      | 130  | ns            |
| $V_{PP}$ setup time (to MD3↑)                      | $t_{VPS}$           | $t_{VPS}$  |                                                | 2     |      |      | $\mu\text{s}$ |
| $V_{DD}$ setup time (to MD3↑)                      | $t_{VDS}$           | $t_{VCS}$  |                                                | 2     |      |      | $\mu\text{s}$ |
| Initial program pulse width                        | $t_{PW}$            | $t_{PW}$   |                                                | 0.95  | 1.0  | 1.05 | ms            |
| Additional program pulse width                     | $t_{OPW}$           | $t_{OPW}$  |                                                | 0.95  |      | 21.0 | ms            |
| MD0 setup time (to MD1↑)                           | $t_{M0S}$           | $t_{CES}$  |                                                | 2     |      |      | $\mu\text{s}$ |
| MD0↓→data output delay time                        | $t_{DV}$            | $t_{DV}$   | MD0 = MD1 = $V_{IL}$                           |       |      | 1    | $\mu\text{s}$ |
| MD1 hold time (from MD0↑)                          | $t_{M1H}$           | $t_{OE H}$ | $t_{M1H} + t_{M1R} \geq 50\text{ }\mu\text{s}$ | 2     |      |      | $\mu\text{s}$ |
| MD1 recovery time (from MD0↓)                      | $t_{M1R}$           | $t_{OR}$   |                                                | 2     |      |      | $\mu\text{s}$ |
| Program counter reset time                         | $t_{PCR}$           | —          |                                                | 10    |      |      | $\mu\text{s}$ |
| X1 input high-/low-level width                     | $t_{XH}$ , $t_{XL}$ | —          |                                                | 0.125 |      |      | $\mu\text{s}$ |
| X1 input frequency                                 | $f_X$               | —          |                                                |       |      | 4.19 | MHz           |
| Initial mode set time                              | $t_i$               | —          |                                                | 2     |      |      | $\mu\text{s}$ |
| MD3 setup time (to MD1↑)                           | $t_{M3S}$           | —          |                                                | 2     |      |      | $\mu\text{s}$ |
| MD3 hold time (from MD1↓)                          | $t_{M3H}$           | —          |                                                | 2     |      |      | $\mu\text{s}$ |
| MD3 setup time (to MD0↓)                           | $t_{M3SR}$          | —          | During program memory read                     | 2     |      |      | $\mu\text{s}$ |
| Address <sup>Note 2</sup> →data output delay time  | $t_{DAD}$           | $t_{ACC}$  | During program memory read                     |       |      | 2    | $\mu\text{s}$ |
| ★ Address <sup>Note 2</sup> →data output hold time | $t_{HAD}$           | $t_{OH}$   | During program memory read                     | 0     |      | 130  | ns            |
| MD3 hold time (from MD0↑)                          | $t_{M3HR}$          | —          | During program memory read                     | 2     |      |      | $\mu\text{s}$ |
| MD3↓→data output float delay time                  | $t_{DFR}$           | —          | During program memory read                     |       |      | 2    | $\mu\text{s}$ |

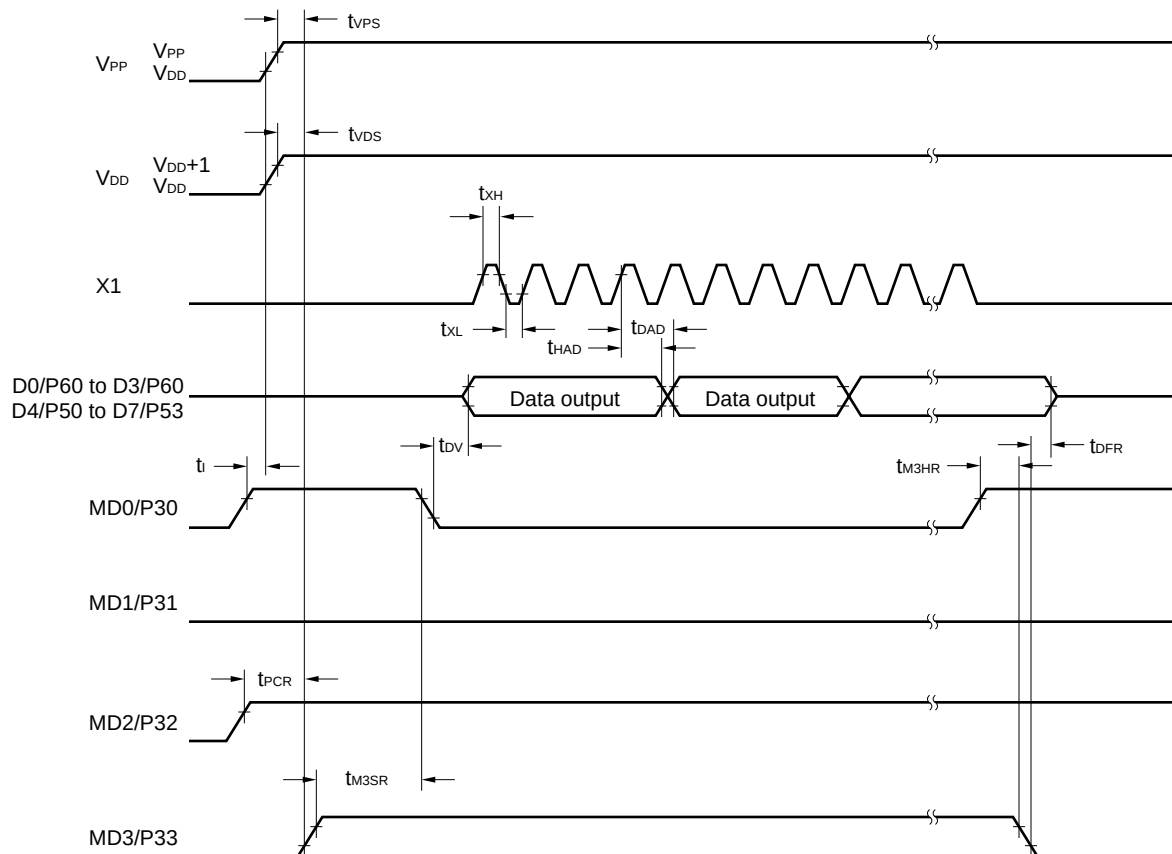
**Notes** 1. Corresponding symbol of  $\mu$ PD27C256A

2. The internal address signal is incremented by 1 at the rising edge of the fourth X1 input and is not connected to a pin.

## Program Memory Write Timing

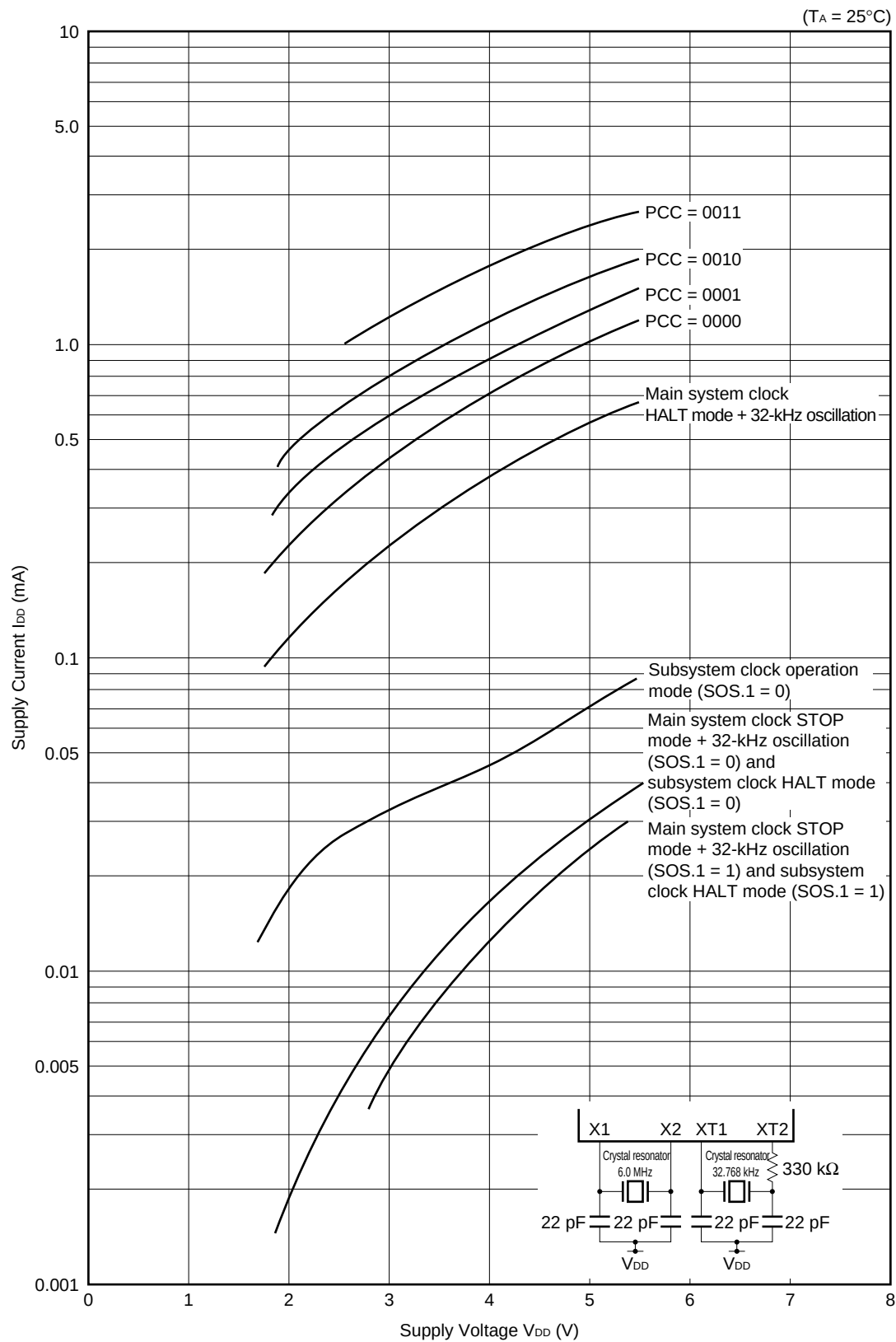


## Program Memory Read Timing



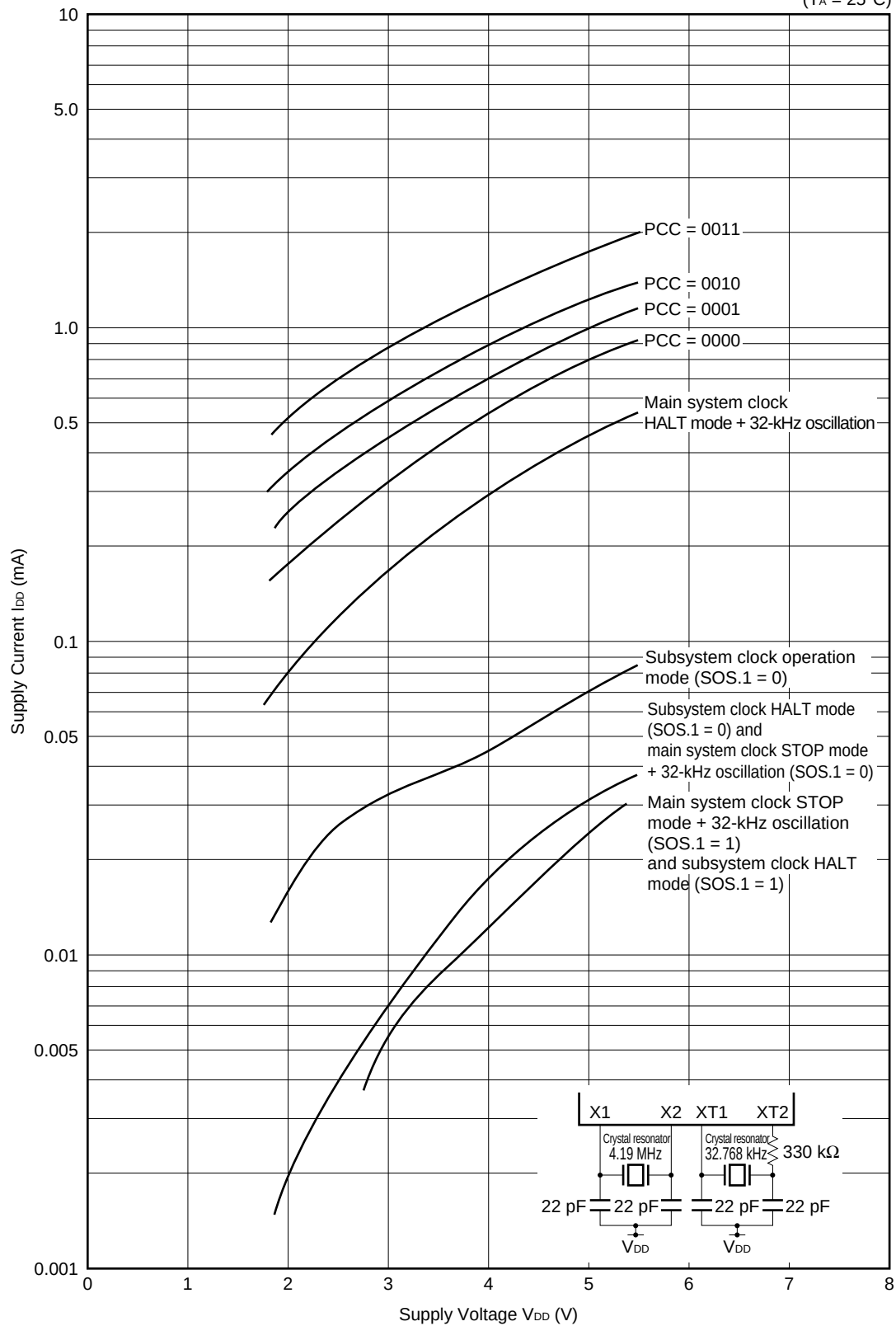
# 10. CHARACTERISTIC CURVES (REFERENCE VALUES)

$I_{DD}$  vs  $V_{DD}$  (Main System Clock: 6.0-MHz Crystal Resonator)



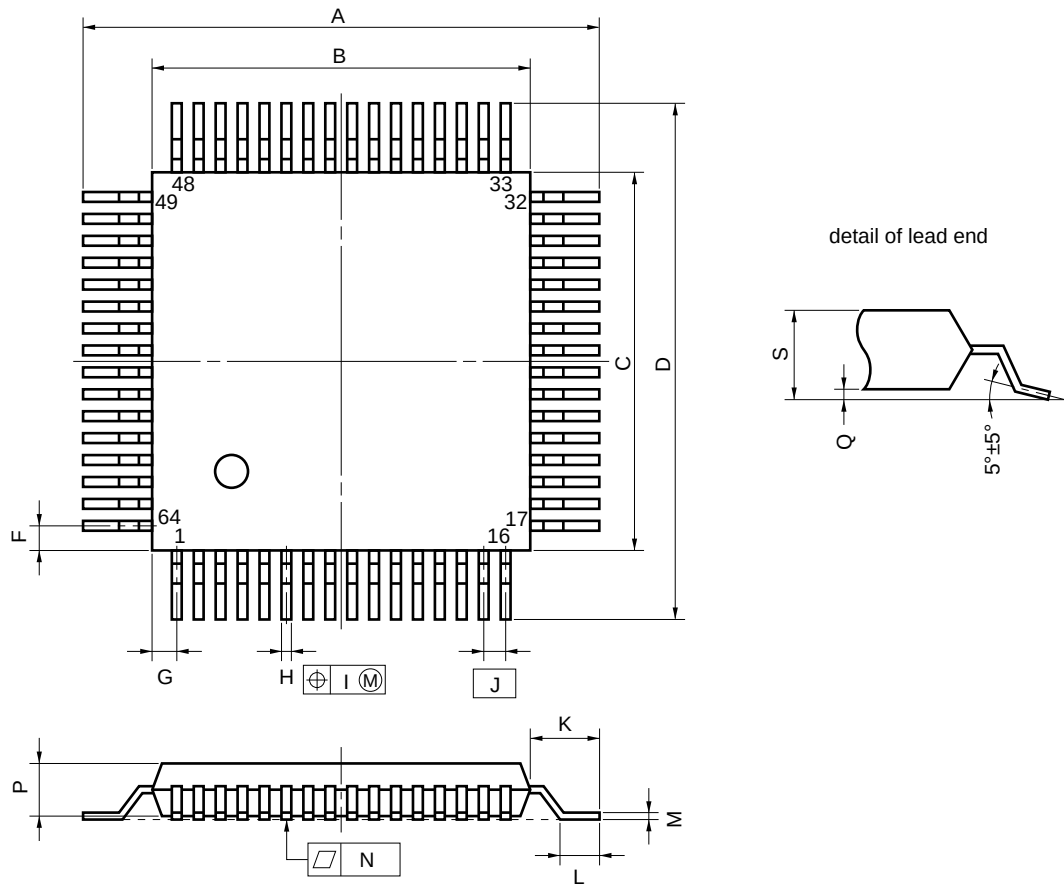
$I_{DD}$  vs  $V_{DD}$  (Main System Clock: 4.19-MHz Crystal Resonator)

( $T_A = 25^\circ\text{C}$ )



## 11. PACKAGE DRAWINGS

## 64 PIN PLASTIC QFP (□14)

**NOTE**

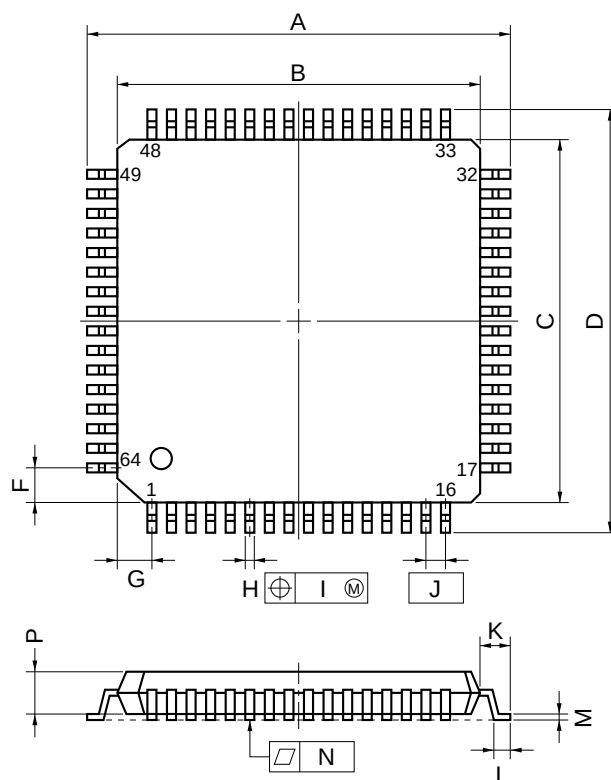
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P64GC-80-AB8-3

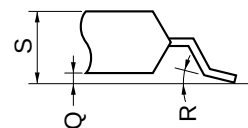
| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 17.6±0.4                               | 0.693±0.016                               |
| B    | 14.0±0.2                               | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| C    | 14.0±0.2                               | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| D    | 17.6±0.4                               | 0.693±0.016                               |
| F    | 1.0                                    | 0.039                                     |
| G    | 1.0                                    | 0.039                                     |
| H    | 0.35±0.10                              | 0.014 <sup>+0.004</sup> <sub>-0.005</sub> |
| I    | 0.15                                   | 0.006                                     |
| J    | 0.8 (T.P.)                             | 0.031 (T.P.)                              |
| K    | 1.8±0.2                                | 0.071±0.008                               |
| L    | 0.8±0.2                                | 0.031 <sup>+0.009</sup> <sub>-0.008</sub> |
| M    | 0.15 <sup>+0.10</sup> <sub>-0.05</sub> | 0.006 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.10                                   | 0.004                                     |
| P    | 2.55                                   | 0.100                                     |
| Q    | 0.1±0.1                                | 0.004±0.004                               |
| S    | 2.85 MAX.                              | 0.112 MAX.                                |



# 64 PIN PLASTIC LQFP (□12)



detail of lead end



## NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 14.8±0.4                               | 0.583±0.016                               |
| B    | 12.0±0.2                               | 0.472 <sup>+0.009</sup> <sub>-0.008</sub> |
| C    | 12.0±0.2                               | 0.472 <sup>+0.009</sup> <sub>-0.008</sub> |
| D    | 14.8±0.4                               | 0.583±0.016                               |
| F    | 1.125                                  | 0.044                                     |
| G    | 1.125                                  | 0.044                                     |
| H    | 0.30±0.10                              | 0.012 <sup>+0.004</sup> <sub>-0.005</sub> |
| I    | 0.13                                   | 0.005                                     |
| J    | 0.65 (T.P.)                            | 0.026 (T.P.)                              |
| K    | 1.4±0.2                                | 0.055±0.008                               |
| L    | 0.6±0.2                                | 0.024 <sup>+0.008</sup> <sub>-0.009</sub> |
| M    | 0.15 <sup>+0.10</sup> <sub>-0.05</sub> | 0.006 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.10                                   | 0.004                                     |
| P    | 1.4                                    | 0.055                                     |
| Q    | 0.125±0.075                            | 0.005±0.003                               |
| R    | 5°±5°                                  | 5°±5°                                     |
| S    | 1.7 MAX.                               | 0.067 MAX.                                |

P64GK-65-8A8-1

## 12. RECOMMENDED SOLDERING CONDITIONS

The μPD75P3116 should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC Sales representative.

★

**Table 12-1. Surface Mounting Type Soldering Conditions**

(1) μPD75P3116GC-AB8: 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)

| Soldering Method | Soldering Conditions                                                                                                                                | Symbol    |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| Infrared reflow  | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C min.),<br>Number of times: Three times max.                                        | IR35-00-3 |
| VPS              | Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C min.),<br>Number of times: Three times max.                                        | VP15-00-3 |
| Wave soldering   | Solder temperature: 260°C max., Flow time: 10 seconds max., Number of times: Once, Preheating temperature: 120°C max. (Package surface temperature) | WS60-00-1 |
| Partial heating  | Pin temperature: 300°C max., Time : 3 seconds max. (per device)                                                                                     | —         |

**Caution** Use of more than one soldering method should be avoided (except for partial heating).

(2) μPD75P3116GK-8A8: 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)

| Soldering Method | Soldering Conditions                                                                                                                                                                                                                                                                                                                                                       | Recommended Conditions Reference Code |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------|
| Infrared reflow  | Package peak temperature: 235°C,<br>Time: 30 seconds max. (at 210°C min.),<br>Number of times: Twice max., Number of days: 7 <sup>Note</sup> (after that, prebaking is necessary at 125°C for 10 hours)<br><Precaution><br>Products other than those supplied in thermal-resistant tray (magazine, taping, and non-thermal-resistant tray) cannot be baked in their packs. | IR35-107-2                            |
| VPS              | Package peak temperature: 215°C,<br>Time: 40 seconds max. (at 200°C min.),<br>Number of times: Twice max., Number of days: 7 <sup>Note</sup> (after that, prebaking is necessary at 125°C for 10 hours)<br><Precaution><br>Products other than those supplied in thermal-resistant tray (magazine, taping, and non-thermal-resistant tray) cannot be baked in their packs. | VP15-107-2                            |
| Wave soldering   | Soldering bath temperature: 260°C max., Time: 10 seconds max.,<br>Number of times: Once<br>Preheating temperature: 120°C max. (package surface temperature)<br>Number of days: 7 <sup>Note</sup> (after that, prebaking is necessary at 125°C for 10 hours)                                                                                                                | WS 60-107-1                           |
| Partial heating  | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)                                                                                                                                                                                                                                                                                                            | —                                     |

**Note** Number of days after unpacking the dry pack. Storage conditions are 25°C and 65%RH max.

**Caution** Do not use different soldering methods together (however, partial heating can be performed with other soldering methods.)

APPENDIX A. FUNCTION LIST OF  $\mu$ PD75308B, 753108 AND 75P3116

| Parameter                  |                                                        | $\mu$ PD75308B                                                                                                        | $\mu$ PD753108                                                                                                                                                                       | $\mu$ PD75P3116                                      |
|----------------------------|--------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|
| Program memory             |                                                        | Mask ROM<br>0000H to 1F7FH<br>(8064 x 8 bits)                                                                         | Mask ROM<br>0000H to 1FFFFH<br>(8192 x 8 bits)                                                                                                                                       | One-time PROM<br>0000H to 3FFFFH<br>(16384 x 8 bits) |
| Data memory                |                                                        | 000H to 1FFH<br>(512 x 4 bits)                                                                                        |                                                                                                                                                                                      |                                                      |
| CPU                        |                                                        | 75X Standard                                                                                                          | 75XL CPU                                                                                                                                                                             |                                                      |
| Instruction execution time | When main system clock is selected                     | 0.95, 1.91, 15.3 $\mu$ s<br>(during 4.19-MHz operation)                                                               | • 0.95, 1.91, 3.81, 15.3 $\mu$ s (during 4.19-MHz operation)<br>• 0.67, 1.33, 2.67, 10.7 $\mu$ s (during 6.0-MHz operation)                                                          |                                                      |
|                            | When subsystem clock is selected                       | 122 $\mu$ s (during 32.768-kHz operation)                                                                             |                                                                                                                                                                                      |                                                      |
| Stack                      | SBS register                                           | None                                                                                                                  | SBS.3 = 1: Mk I mode selection<br>SBS.3 = 0: Mk II mode selection                                                                                                                    |                                                      |
|                            | Stack area                                             | 000H to 0FFH                                                                                                          | 000H to 1FFH                                                                                                                                                                         |                                                      |
|                            | Subroutine call instruction stack operation            | 2-byte stack                                                                                                          | When Mk I mode : 2-byte stack<br>When Mk II mode : 3-byte stack                                                                                                                      |                                                      |
| Instruction                | BRA !addr1<br>CALLA !addr1                             | Unavailable                                                                                                           | When Mk I mode : unavailable<br>When Mk II mode : available                                                                                                                          |                                                      |
|                            | MOVT XA, @BCDE<br>MOVT XA, @BCXA<br>BR BCDE<br>BR BCXA |                                                                                                                       | Available                                                                                                                                                                            |                                                      |
|                            | CALL !addr                                             | 3 machine cycles                                                                                                      | Mk I mode : 3 machine cycles<br>Mk II mode : 4 machine cycles                                                                                                                        |                                                      |
|                            | CALLF !addr                                            | 2 machine cycles                                                                                                      | Mk I mode : 2 machine cycles<br>Mk II mode : 3 machine cycles                                                                                                                        |                                                      |
| I/O port                   | CMOS input                                             | 8                                                                                                                     | 8                                                                                                                                                                                    |                                                      |
|                            | CMOS input/output                                      | 16                                                                                                                    | 20                                                                                                                                                                                   |                                                      |
|                            | Bit port output                                        | 8                                                                                                                     | 0                                                                                                                                                                                    |                                                      |
|                            | N-ch open-drain input/output                           | 8                                                                                                                     | 4                                                                                                                                                                                    |                                                      |
|                            | Total                                                  | 40                                                                                                                    | 32                                                                                                                                                                                   |                                                      |
| LCD controller/driver      |                                                        | Segment selection: 24/28/32<br>(can be changed to CMOS input/output port in 4-unit; max. 8)                           | Segment selection: 16/20/24 segments<br>(can be changed to CMOS input/output port in 4-unit; max. 8)                                                                                 |                                                      |
|                            |                                                        | Display mode selection: static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias)    |                                                                                                                                                                                      |                                                      |
|                            |                                                        | On-chip split resistor for LCD driver can be specified by using mask option.                                          |                                                                                                                                                                                      | No on-chip split resistor for LCD driver             |
| Timer                      |                                                        | 3 channels<br>• Basic interval timer: 1 channel<br>• 8-bit timer/event counter: 1 channel<br>• Watch timer: 1 channel | 5 channels<br>• Basic interval timer/watchdog timer: 1 channel<br>• 8-bit timer/event counter: 3 channels<br>(can be used as 16-bit timer/event counter)<br>• Watch timer: 1 channel |                                                      |

| Parameter                              |                                                  | μPD75308B                                                                                                                                                                                             | μPD753108                                                                                                                                                                                                                                   | μPD75P3116 |
|----------------------------------------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| Clock output (PCL)                     |                                                  | <ul style="list-style-type: none"><li>• Φ, 524, 262, 65.5 kHz<br/>(Main system clock: during 4.19-MHz operation)</li></ul>                                                                            | <ul style="list-style-type: none"><li>• Φ, 524, 262, 65.5 kHz<br/>(Main system clock: during 4.19-MHz operation)</li><li>• Φ, 750, 375, 93.8 kHz<br/>(Main system clock: during 6.0-MHz operation)</li></ul>                                |            |
| BUZ output (BUZ)                       |                                                  | 2 kHz<br>(Main system clock: during 4.19-MHz operation)                                                                                                                                               | <ul style="list-style-type: none"><li>• 2, 4, 32 kHz<br/>(Main system clock: during 4.19-MHz operation or subsystem clock: during 32.768-kHz operation)</li><li>• 2.93, 5.86, 46.9 kHz<br/>(Main system clock: 6.0-MHz operation)</li></ul> |            |
| Serial interface                       |                                                  | 3 modes are available <ul style="list-style-type: none"><li>• 3-wire serial I/O mode ... MSB/LSB can be selected for transfer first bit</li><li>• 2-wire serial I/O mode</li><li>• SBI mode</li></ul> |                                                                                                                                                                                                                                             |            |
| SOS register                           | Feedback resistor cut flag (SOS.0)               | None                                                                                                                                                                                                  | Contained                                                                                                                                                                                                                                   |            |
|                                        | Sub-oscillation circuit current cut flag (SOS.1) | None                                                                                                                                                                                                  | Contained                                                                                                                                                                                                                                   |            |
| Register bank selection register (RBS) |                                                  | None                                                                                                                                                                                                  | Yes                                                                                                                                                                                                                                         |            |
| Standby release by INTO                |                                                  | No                                                                                                                                                                                                    | Yes                                                                                                                                                                                                                                         |            |
| Vectored interrupt                     |                                                  | External: 3, Internal: 3                                                                                                                                                                              | External: 3, Internal: 5                                                                                                                                                                                                                    |            |
| Supply voltage                         |                                                  | V <sub>DD</sub> = 2.0 to 6.0 V                                                                                                                                                                        | V <sub>DD</sub> = 1.8 to 5.5 V                                                                                                                                                                                                              |            |
| Operating ambient temperature          |                                                  | T <sub>A</sub> = −40 to +85°C                                                                                                                                                                         |                                                                                                                                                                                                                                             |            |
| Package                                |                                                  | <ul style="list-style-type: none"><li>• 80-pin plastic QFP (14 x 20 mm)</li><li>• 80-pin plastic QFP (14 x 14 mm)</li><li>• 80-pin plastic TQFP (Fine pitch) (12 x 12 mm)</li></ul>                   | <ul style="list-style-type: none"><li>• 84-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)</li><li>• 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)</li></ul>                                                                                    |            |

## APPENDIX B. DEVELOPMENT TOOLS

The following development tools have been provided for system development using the μPD75P3116.  
In the 75XL series, a common relocatable assembler is used in combination with a device file dedicated to each model.

| RA75X relocatable assembler | Host machine                 |                                                    |               | Part No. (name) |
|-----------------------------|------------------------------|----------------------------------------------------|---------------|-----------------|
|                             |                              | OS                                                 | Supply medium |                 |
|                             | PC-9800 Series               | MS-DOS™<br>( Ver.3.30 to Ver.6.2 <sup>Note</sup> ) | 3.5" 2HD      | μS5A13RA75X     |
|                             |                              |                                                    | 5" 2HD        | μS5A10RA75X     |
|                             | IBM PC/AT™<br>or compatibles | Refer to <b>OS for IBM PCs</b>                     | 3.5" 2HC      | μS7B13RA75X     |
|                             |                              |                                                    | 5" 2HC        | μS7B10RA75X     |

| Device file | Host machine                |                                                   |               | Part No. (name) |
|-------------|-----------------------------|---------------------------------------------------|---------------|-----------------|
|             |                             | OS                                                | Supply medium |                 |
|             | PC-9800 Series              | MS-DOS<br>( Ver.3.30 to Ver.6.2 <sup>Note</sup> ) | 3.5" 2HD      | μS5A13DF753108  |
|             |                             |                                                   | 5" 2HD        | μS5A10DF753108  |
|             | IBM PC/AT<br>or compatibles | Refer to <b>OS for IBM PCs</b>                    | 3.5" 2HC      | μS7B13DF753108  |
|             |                             |                                                   | 5" 2HC        | μS7B10DF753108  |

**Note** Ver. 5.00 and later include a task swapping function, but this function cannot be used in this software.

**Remark** Operation of the assembler and device file is guaranteed only when using the host machine and OS described above.

## PROM Write Tools

|          |                    |                                                                                                                                                                                                                                                                                                    |                                                                                                  |                 |                   |
|----------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-----------------|-------------------|
| Hardware | PG-1500            | This is a PROM writer that can program single-chip microcontroller with PROM in stand-alone mode or under control of host machine when connected with supplied accessory board and optional programmer adapter.<br>It can also program typical PROMs in capacities ranging from 256 K to 4 M bits. |                                                                                                  |                 |                   |
|          | PA-75P3116BGC      | This is a PROM programmer adapter for the $\mu$ PD75P3116GC.<br>It can be used when connected to a PG-1500.                                                                                                                                                                                        |                                                                                                  |                 |                   |
|          | PA-75P3116BGK      | This is a PROM programmer adapter for the $\mu$ PD75P3116GK.<br>It can be used when connected to a PG-1500.                                                                                                                                                                                        |                                                                                                  |                 |                   |
| Software | PG-1500 controller | Connects PG-1500 to host machine with serial and parallel interface and controls PG-1500 on host machine.                                                                                                                                                                                          |                                                                                                  |                 |                   |
|          |                    | Host machine                                                                                                                                                                                                                                                                                       |                                                                                                  | Part No. (name) |                   |
|          |                    |                                                                                                                                                                                                                                                                                                    | OS                                                                                               | Supply medium   |                   |
|          |                    | PC-9800 Series                                                                                                                                                                                                                                                                                     | MS-DOS                                                                                           | 3.5" 2HD        | $\mu$ S5A13PG1500 |
|          |                    |                                                                                                                                                                                                                                                                                                    | $\left( \begin{array}{c} \text{Ver.3.30 to} \\ \text{Ver.6.2} \end{array} \right)^{\text{Note}}$ | 5" 2HD          | $\mu$ S5A10PG1500 |
|          |                    | IBM PC/AT<br>or compatible                                                                                                                                                                                                                                                                         | Refer to <b>OS for<br/>IBM PCs</b>                                                               | 3.5" 2HD        | $\mu$ S7B13PG1500 |
|          |                    |                                                                                                                                                                                                                                                                                                    |                                                                                                  | 5" 2HC          | $\mu$ S7B10PG1500 |

**Note** Ver. 5.00 and later include a task swapping function, but this function cannot be used in this software.

**Remark** Operation of the PG-1500 controller is guaranteed only when using the host machine and OS described above.

## Debugging Tools

In-circuit emulators (IE-75000-R and IE-75001-R) are provided as program debugging tools for the μPD75P3116.

Various system configurations using these in-circuit emulators are listed below.

|          |                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                           |          |                 |
|----------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|----------|-----------------|
| Hardware | IE-75000-R <sup>Note 1</sup> | The IE-75000-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products.<br>For development of the μPD753108 Subseries, the IE-75000-R is used with optional emulation board (IE-75300-R-EM) and emulation probe (EP-753108GC-R or EP-753108GK-R).<br>Highly efficient debugging can be performed when connected to host machine and PROM programmer.<br>The IE-75000-R includes a connected emulation board (IE-75000-R-EM). |                                           |          |                 |
|          | IE-75001-R                   | The IE-75001-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products.<br>The IE-75001-R is used in combination with optional emulation board (IE-75300-R-EM) and emulation probe (EP-753108GC-R or EP-753108GK-R).<br>Highly efficient debugging can be performed when connected to host machine and PROM programmer.                                                                                                      |                                           |          |                 |
|          | IE-75300-R-EM                | This is an emulation board for evaluating application systems using the μPD75P3116.<br>It is used in combination with the IE-75000-R or IE-75001-R.                                                                                                                                                                                                                                                                                                                                                                           |                                           |          |                 |
|          | EP-753108GC-R                | This is an emulation probe for the μPD75P3116GC.<br>When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.                                                                                                                                                                                                                                                                                                                                                                                 |                                           |          |                 |
|          | EV-9200GC-64                 | It includes a 64-pin conversion socket (EV-9200GC-64) to facilitate connections with target system.                                                                                                                                                                                                                                                                                                                                                                                                                           |                                           |          |                 |
|          | EP-753108GK-R                | This is an emulation probe for the μPD75P3116GK.<br>When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.                                                                                                                                                                                                                                                                                                                                                                                 |                                           |          |                 |
|          | TGK-064SBW <sup>Note 2</sup> | It includes a 64-pin conversion adapter (TGK-064SBW) to facilitate connections with target system.                                                                                                                                                                                                                                                                                                                                                                                                                            |                                           |          |                 |
| Software | IE control program           | This program can control the IE-75000-R or IE-75001-R on a host machine when connected to the IE-75000-R or IE-75001-R via an RS-232C or Centronics interface.                                                                                                                                                                                                                                                                                                                                                                |                                           |          |                 |
|          |                              | Host machine                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                           |          | Part No. (name) |
|          |                              | OS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Supply medium                             |          |                 |
|          |                              | PC-9800 Series                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | MS-DOS                                    | 3.5" 2HD | μS5A13IE75X     |
|          |                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | ( Ver.3.30 to Ver.6.2 <sup>Note 3</sup> ) | 5" 2HD   | μS5A10IE75X     |
|          |                              | IBM PC/AT or compatible                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Refer to <b>OS for IBM PCs</b>            | 3.5" 2HC | μS7B13IE75X     |
|          |                              | 5" 2HC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | μS7B10IE75X                               |          |                 |

**Notes 1.** This is a maintenance product.

**2.** Made by TOKYO ELETECH Corporation (Tokyo, 03-5295-1661).

Contact to an NEC sales representative for detailed information.

**3.** Ver. 5.00 and later include a task swapping function, but this function cannot be used in this software.

**Remarks 1.** Operation of the IE control program is guaranteed only when using the host machine and OS described above.

**2.** The μPD753104, 753106, 753108, and 75P3116 are generically called the μPD753108 Subseries.

**OS for IBM PCs**

The following operating systems for the IBM PC are supported.

| OS       | Version                                                          |
|----------|------------------------------------------------------------------|
| PC DOS™  | Ver.3.1 to 6.3, J6.1/V <sup>Note</sup> to J6.3/V <sup>Note</sup> |
| MS-DOS   | Ver.5.0 to 6.2<br>5.0/V <sup>Note</sup> to 6.2/V <sup>Note</sup> |
| IBM DOS™ | J5.02/V <sup>Note</sup>                                          |

**Note** Only English mode is supported.

**Caution** Ver. 5.0 and later include a task swapping function, but this function cannot be used in this software.



## APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

### Device Related Documents

| Document Name                            | Document No.            |          |
|------------------------------------------|-------------------------|----------|
|                                          | English                 | Japanese |
| μPD753104, 753106, and 753108 Data Sheet | U10086E                 | U10086J  |
| μPD75P3116 Data Sheet                    | U11369E (This document) | U11369J  |
| μPD753108 User's Manual                  | U10890E                 | U10890J  |
| μPD753108 Instruction Table              | —                       | IEM-5600 |
| 75XL Series Selection Guide              | U10453E                 | U10453J  |

### Development Tool Related Documents

| Document Name |                                          |                                 | Document No. |          |
|---------------|------------------------------------------|---------------------------------|--------------|----------|
|               |                                          |                                 | English      | Japanese |
| Hardware      | IE-75000-R/IE-75001-R User's Manual      |                                 | EEU-1416     | EEU-846  |
|               | IE-75300-R-EM User's Manual              |                                 | U11354E      | U11354J  |
|               | EP-753108GC/GK-R User's Manual           |                                 | EEU-1495     | EEU-968  |
|               | PG-1500 User's Manual                    |                                 | EEU-1335     | U11940J  |
| Software      | RA75X Assembler Package<br>User's Manual | Operation                       | EEU-1346     | EEU-731  |
|               |                                          | Language                        | EEU-1363     | EEU-730  |
|               | PG-1500 Controller User's Manual         | PC-9800 series<br>(MS-DOS) base | EEU-1291     | EEU-704  |
|               |                                          | IBM PC series<br>(PC DOS) base  | U10540E      | EEU-5008 |

### Other Related Documents

| Document Name                                               | Document No. |          |
|-------------------------------------------------------------|--------------|----------|
|                                                             | English      | Japanese |
| IC Package Manual                                           | C10943X      |          |
| Semiconductor Device Mounting Technology Manual             | C10535E      | C10535J  |
| Quality Grades on NEC Semiconductor Devices                 | C11531E      | C11531J  |
| NEC Semiconductor Device Reliability/Quality Control System | C10983E      | C10983J  |
| Electrostatic Discharge (ESD) Test                          | —            | MEM-539  |
| Guide to Quality Assurance for Semiconductor Devices        | MEI-1202     | C11893J  |
| Microcontroller-related Product Guide Third Party's Product | —            | U11416J  |

**Caution** The above related documents are subject to change without notice. For design purposes, etc., be sure to use the latest versions.

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

## Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 800-729-9288

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Tel: 0211-65 03 02  
Fax: 0211-65 03 490

### **NEC Electronics (UK) Ltd.**

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Fax: 01908-670-290

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Fax: 08-63 80 388

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Fax: 02-528-4411

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Tel: 253-8311  
Fax: 250-3583

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Fax: 02-719-5951

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