intersil

CD4042BMS

CMOS Quad Clocked "D" Latch

Features

- **High-Voltage Type (20V Rating)**
- **Clock Polarity Control**
- **Q and $\overline{Q}$ Outputs**
- **Common Clock**
- **Low Power TTL Compatible**
- **Standardized Symmetrical Output Characteristics**
- **100% Tested for Quiescent Current at 20V**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **5V, 10V and 15V Parametric Ratings**
- **Noise Margin (Over Full Package Temperature Range):**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Buffer Storage**
- **Holding Register**
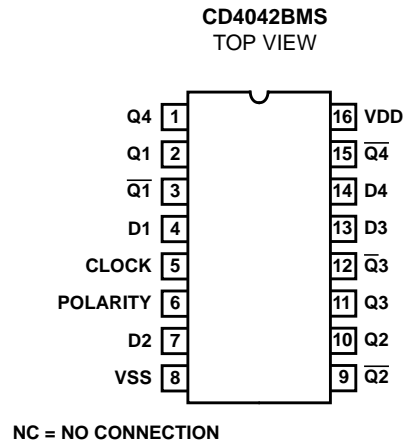- **General Digital Logic**

Description

CD4042BMS types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p- channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and Q during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.
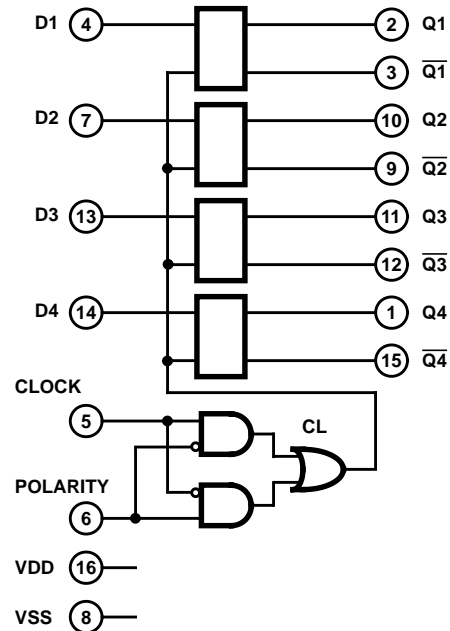
The CD4042BMS is supplied in these 16 lead outline packages:

Braze Seal DIP   H4T

Frit Seal DIP   H1E

Ceramic Flatpack   H6W

Pinout

CD4042BMS
TOP VIEW

Q4	1	16 VDD
Q1	2	15 $\overline{Q4}$
$\overline{Q1}$	3	14 D4
D1	4	13 D3
CLOCK	5	12 $\overline{Q3}$
POLARITY	6	11 Q3
D2	7	10 Q2
VSS	8	9 $\overline{Q2}$

NC = NO CONNECTION

Functional Diagram

File Number   **3310**

Specifications CD4042BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . -0.5V to +20V
  (Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . ±10mA
Operating Temperature Range. . . . . -55°C to +125°C
  Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . +265°C
  At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
  10s Maximum

Reliability Information

Thermal Resistance . . . . θ_{ja} θ_{jc}
  Ceramic DIP Package . . . . 80°C/W   20°C/W
  Flatpack Package . . . . 70°C/W   20°C/W
Maximum Package Power Dissipation (PD) at +125°C
  For TA = -55°C to +100°C (Package Type D, F, K) 500mW
  For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate
                Linearity at 12mW/^{o}C to 200mW
Device Dissipation per Output Transistor 100mW
  For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	MIN	MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND.
        2. Go/no go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay (Note 2) Data in to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	220	ns
			10, 11	+125°C, -55°C	-	297	ns
Propagation Delay (Note 2) Data in to $\overline{Q}$	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay (Note 2) Clock to Q	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	450	ns
			10, 11	+125°C, -55°C	-	608	ns
Propagation Delay (Note 2) Clock to $\overline{Q}$	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time (Note 2)	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K, input TR, TF < 20ns.

2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Data in to Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay Data in to $\overline{Q}$	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay Clock to Q	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Clock to $\overline{Q}$	TPLH4 TPHL4	VDD = 10V	1, 2, 3	+25°C	-	230	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Clock Input Rise and Fall Time (Note 4)	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	*	-
		VDD = 10V	1, 2, 3	+25°C	-	*	-
		VDD = 15V	1, 2, 3	+25°C	-	*	-
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	50	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	25	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	120	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.

2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

3. CL = 50pF, RL = 200K.

4. * Not sensitive

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.   3. See Table 2 for +25°C limit.

2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.   4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE:

1. 1.5% parametric, 3% functional; cumulative for static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1 - 3, 9 - 12, 15	4 - 8, 13, 14	16			
Static Burn-In 2 Note 1	1 - 3, 9 - 12, 15	8	4 - 7, 13, 14, 16			
Dynamic Burn-In Note 1	-	8	6, 16	1 - 3, 9 - 12, 15	5	4, 7, 13, 14
Irradiation Note 2	1 - 3, 9 - 12, 15	8	4 - 7, 13, 14, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V

2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

ONE OF FOUR LATCHES

CONTROL

LOGIC BLOCK DIAGRAM

*ALL INPUTS ARE PROTECTED
BY CMOS PROTECTION
NETWORK
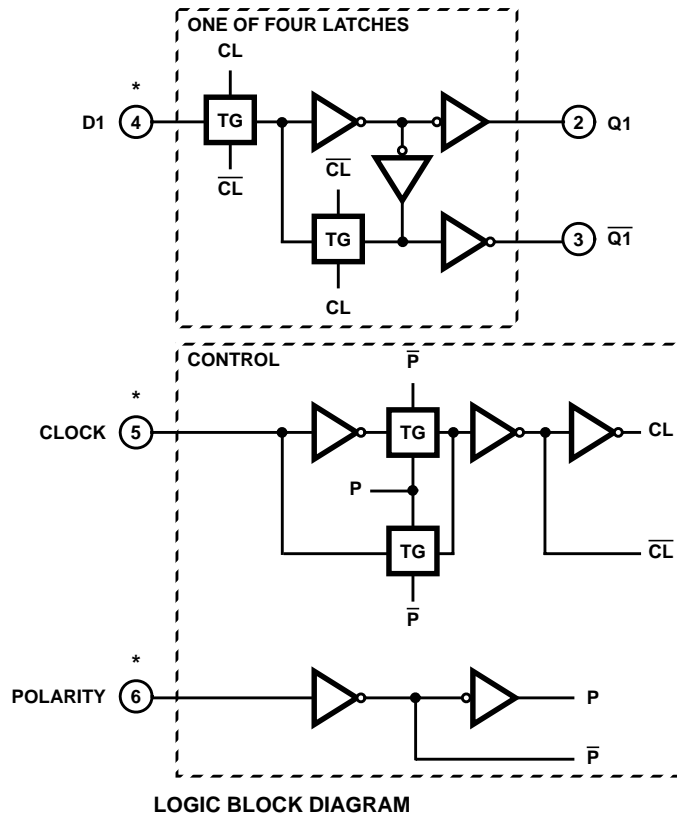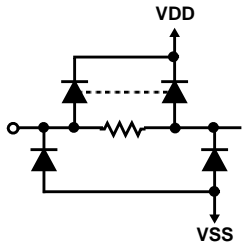
TRUTH TABLE

CLOCK	POLARITY	Q
0	0	D
⌐	0	LATCH
1	1	D
⌐	1	LATCH

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Typical Performance Characteristics
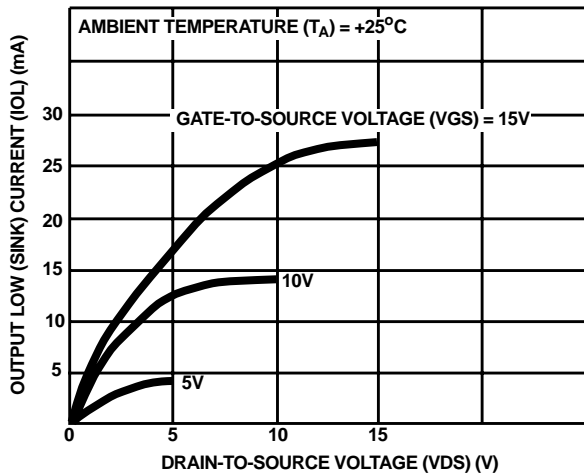
FIGURE 1. TYPICAL OUTPUT LOW (SINK) CURRENT CHAR-
ACTERISTICS
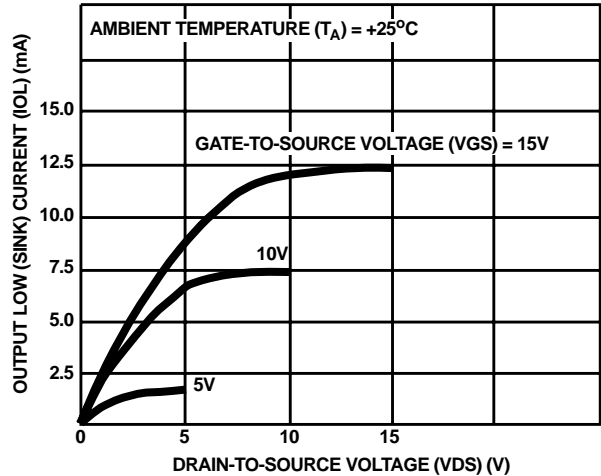
FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CHAR-
ACTERISTICS
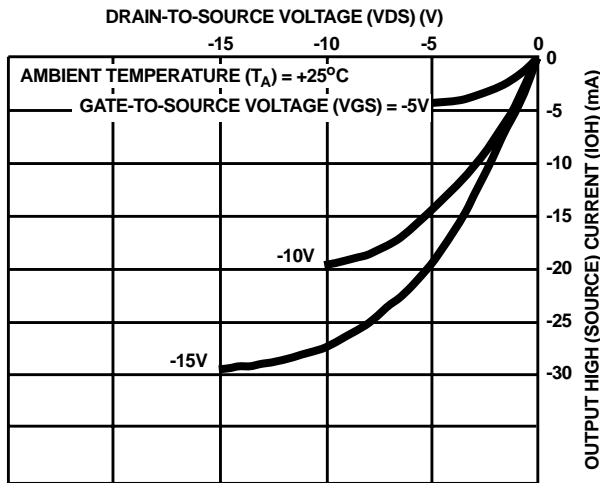
FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT
CHARACTERISTICS
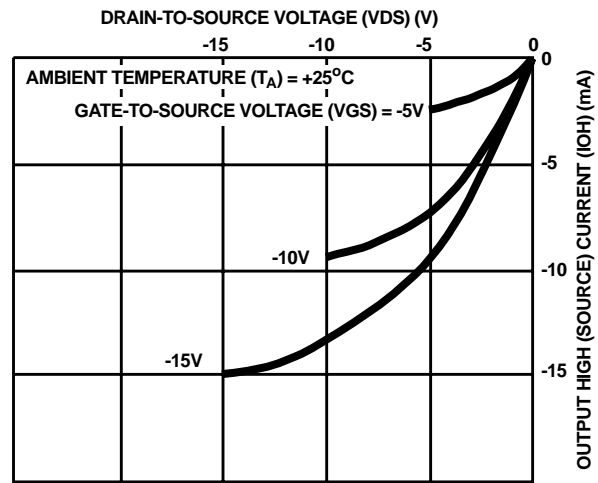
FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT
CHARACTERISTICS
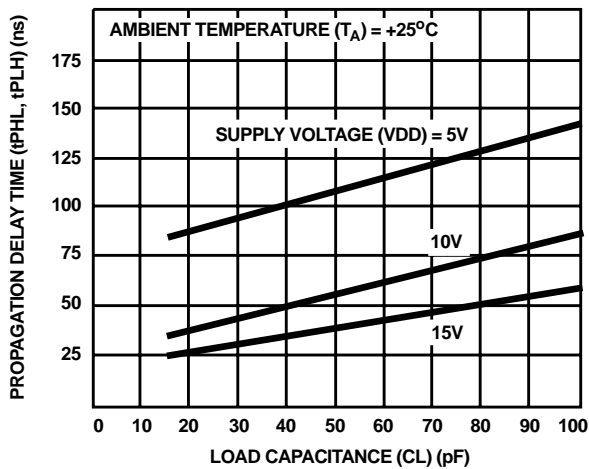
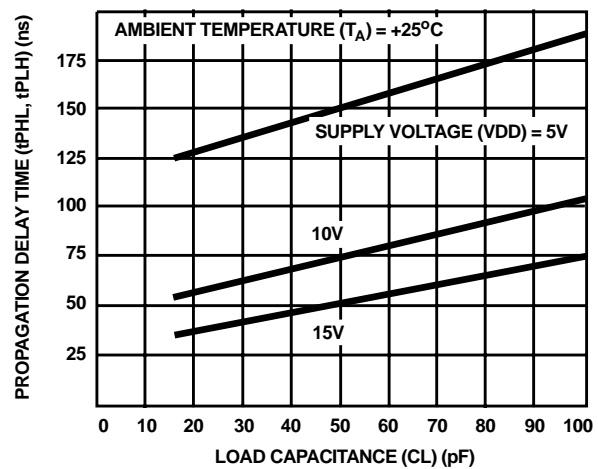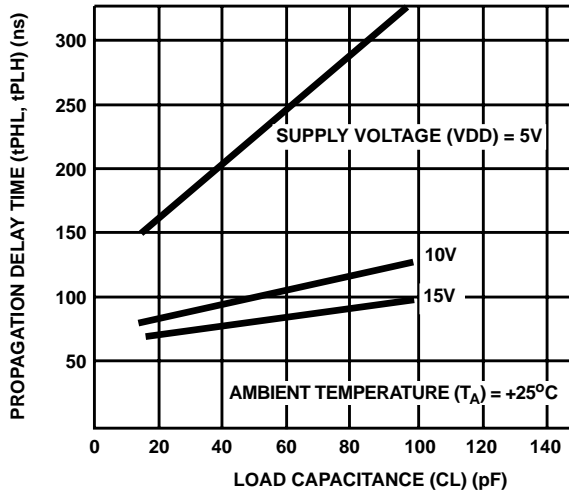FIGURE 5. TYPICAL PROPAGATION DELAY TIME vs LOAD
CAPACITANCE - DATA TO Q

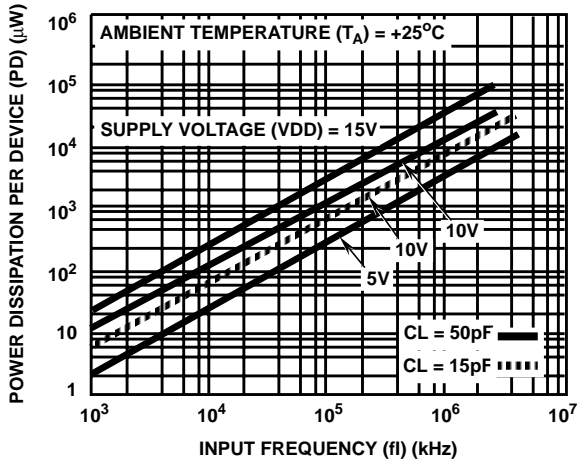FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD
CAPACITANCE - DATA TO $\overline{Q}$

Typical Performance Characteristics (Continued)

FIGURE 7. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE - CLOCK TO Q
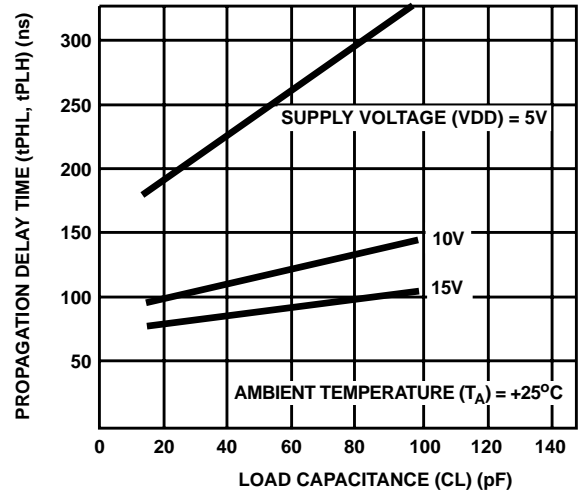
FIGURE 8. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE - CLOCK TO $\overline{Q}$

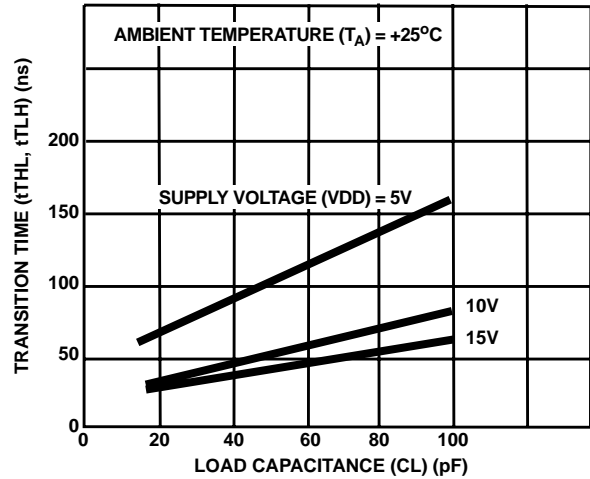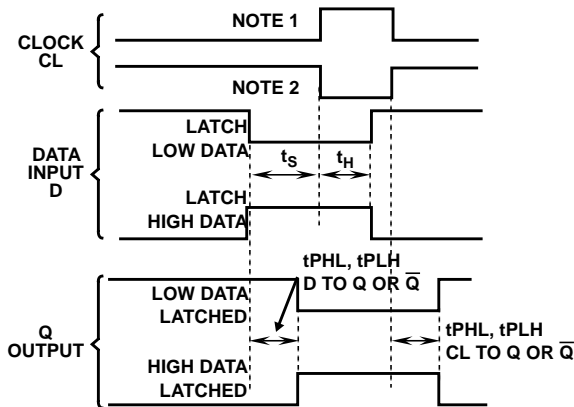**FIGURE 9. TYPICAL POWER DISSIPATION vs FREQUENCY**

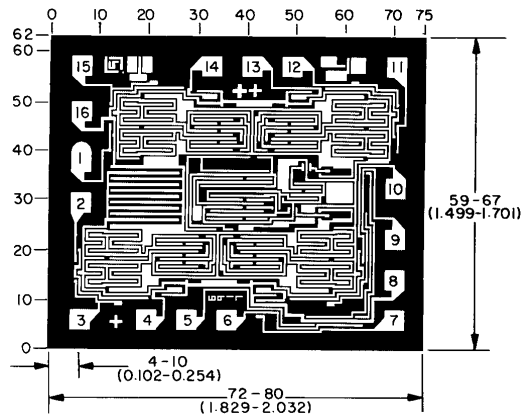**FIGURE 10. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE**

NOTES:
1. For positive clock edge, input data is latched when polarity is low.
2. For negative clock edge, input data is latched when polarity is high.

FIGURE 11. DYNAMIC TEST PARAMETERS

Chip Dimensions and Pad Layout

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated Grid graduations are in mils (10^{-3} inch).