CY28343

Zero Delay SDR/DDR Clock Buffer

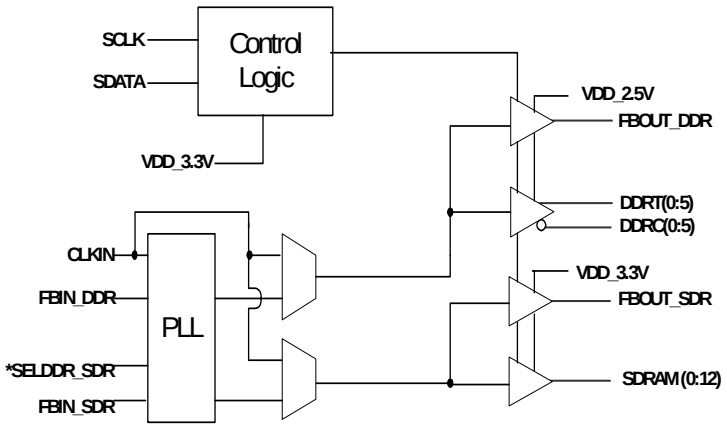
Features

- **Phase-lock loop clock distribution for DDR and SDR SDRAM applications**
- **One-single-end clock input to 6 pairs DDR outputs or 13 SDR outputs.**
- **External feedback pins FBIN_SDR/FBOUT_SDR are used to synchronize the outputs to the clock input for SDR.**
- **External feedback pins FBIN_SDR/FBOUT_SDR are used to synchronize the outputs to the clock input for DDR.**
- **SMBus interface enables/disables outputs.**
- **Conforms to JEDEC SDR/DDR specifications**
- **Low jitter, low skew**
- **48 pin SSOP package**

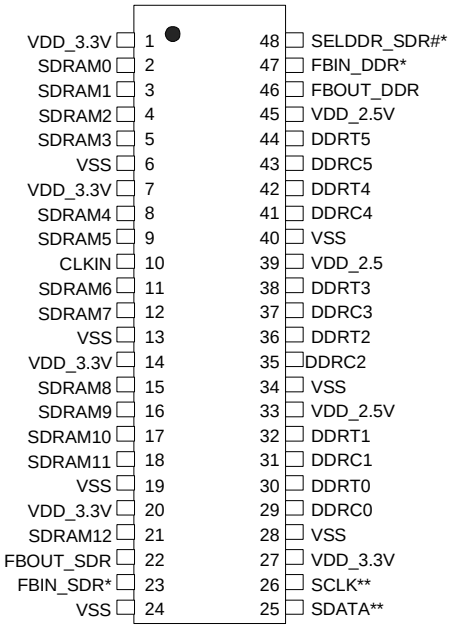
Table 1. Function Table

SELDDR_SDR#	CLKIN	SDRAM(0:12)	DDRT/C(0:5)	FBIN_DDR	FBOUT_DDR	FBIN_SDR	FBOUT_SDR
1= DDR Mode	2.5V Compatible	OFF	Active 2.5V Compatible	2.5V Compatible	Active 2.5V Compatible	OFF	OFF
0 = SDRAM Mode	3.3V Compatible	Active 3.3V Compatible	OFF	OFF	OFF	Active 3.3V Compatible	Active 3.3V Compatible

Block Diagram



Pin Configuration[1]



Note:

1. Pins marked with [*] have internal pull-down resistors. Pins marked with [**] have internal pull-up resistors.

Pin Description[2, 3]

Pin	Name	I/O	Description
10	CLKIN	I	**Clock Input**. Reference the PLL
47	FBIN_DDR	I PD	**Feedback Clock Output**. Connect to FBOUT_DDR for accessing the PLL. See *Function Table on page 1*
23	FBIN_SDR	I PD	**Feedback Clock Input**. Connect to FBOUT_SDR for accessing the PLL. See *Function Table on page 1*
30,32,36,38 42,44	DDRT(0:5)	O	**Clock Outputs**. True copies of the CLKIN input
29,31,35,37 41,43	DDRC(0:5)	O	**Clock Outputs**. Complementary copies of the CLKIN input
2-5,8,9 15-18,21	SDRAM(0:12)	O	**Clock Outputs**. True copies of the CLKIN input
46	FBOUT_DDR	O	**Feedback Clock Output**. Connect to FBIN_DDR for normal operation. A true copy of the CLKIN input. The delay of the PCB trace RC at this output will control Input Reference/DDR Output Clocks phase relationships.
22	FBOUT_SDR	O	**Feedback Clock Output**. Connect to FBIN_SDR for normal operation. A true copy of the CLKIN input. The delay of the PCB trace RC at this output will control Input Reference/ SDR Output Clocks phase relationships.
48	SELDDR_SDR#	I PD	**SDR or DDR Select Pin**. See *Function Table on page 1*
26	SCLK	I PU	**Serial Clock Input**. Clocks data at SDATA into the internal register.
25	SDATA	I/O PU	**Serial Data Input**. Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.
1,7,14,20,27	VDD_3.3V		**3.3V power supply for SDR outputs and two line serial Interface**
33,39,45	VDD_2.5V		**2.5V power supply for DDR outputs**
6,13,19,24,28 ,34,40	VSS		**Common Ground**

Notes:
2. PU = internal pull-up PD = internal pull-down.
3. A bypass capacitor (0.1 mF) should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Power Management

The individual output enable/disable control of the CY28343 allows the user to implement unique power management schemes into the design. Outputs are in LOW state when disabled through the two-line interface as individual bits are set LOW in Byte0 to Byte2 registers. The feedback output FBOUT_DDR and FBOUT_SDR cannot be disabled via two-line serial bus.

Zero Delay Buffer

When used as a ZERO delay buffer the CY28343 will likely be in a nested clock tree application. For these applications the CY28343 offers single-end input as a PLL reference. The CY28343 then can lock onto the reference and translate with near zero to low-skew outputs. For normal operation, the external feedback input, FBIN_DDR and FBIN_SDR, are connected to the feedback output, FBOUT_DDR and FBOUT_SDR. By connecting the feedback output to the feedback input the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc., can be individually enabled or disabled.

The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operation from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol.

The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be ’0000000’

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 Bit'00000000' stands for block operation	11:18	Command Code – 8 Bit'00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 – 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge	39:46	Data byte from slave –8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave – 8 bits
		....	Not Acknowledge
		....	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits'1xxxxxxx' stands for byte operationbit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits'1xxxxxxx' stands for byte operationbit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not Acknowledge
		39	stop

Byte 0: Output Register (1 = Enable, 0 = Disable)[4]

Bit	@Pup	Pin #	Description
7	1	29,30	DDRT/C0. 1 = Enable, 0 = Output disabled asynchronously in a low state
6	1	31,32	DDRT/C1. 1 = Enable, 0 = Output disabled asynchronously in a low state
5	1	35,36	DDRT/C2. 1 = Enable, 0 = Output disabled asynchronously in a low state
4	1	37,38	DDRT/C3. 1 = Enable, 0 = Output disabled asynchronously in a low state
3	1	41,42	DDRT/C4. 1 = Enable, 0 = Output disabled asynchronously in a low state
2	1	43,44	DDRT/C5. 1 = Enable, 0 = Output disabled asynchronously in a low state
1	1		Reserved
0	1	48	SELDDR_DDR hardware setting value. Read only.

Byte 1: Output Register (1 = Enable, 0 = Disable)[4]

Bit	@Pup	Pin #	Description
7	1	12	SDRAM7. 1 = Enable, 0 = Output disabled asynchronously in a low state
6	1	11	SDRAM6. 1 = Enable, 0 = Output disabled asynchronously in a low state
5	1	9	SDRAM5. 1 = Enable, 0 = Output disabled asynchronously in a low state
4	1	8	SDRAM4. 1 = Enable, 0 = Output disabled asynchronously in a low state
3	1	5	SDRAM3. 1 = Enable, 0 = Output disabled asynchronously in a low state
2	1	4	SDRAM2. 1 = Enable, 0 = Output disabled asynchronously in a low state
1	1	3	SDRAM1. 1 = Enable, 0 = Output disabled asynchronously in a low state
0	1	2	SDRAM0. 1 = Enable, 0 = Output disabled asynchronously in a low state

Note:
4. These bits will be ignored in DDR mode. See *Table 1* on page 1.

Byte 2: Output Register (1 = Enable, 0 = Disable)[4]

Bit	@Pup	Pin #	Description
7	1		Reserved for device test.
6	1		Select drive strength for SDR outputs. 1 = Low drive, 0 = High drive
5	1		Reserved
4	1	21	SDRAM12. 1 = Enable, 0 = Output disabled asynchronously in a low state
3	1	18	SDRAM11. 1 = Enable, 0 = Output disabled asynchronously in a low state
2	1	17	SDRAM10. 1 = Enable, 0 = Output disabled asynchronously in a low state
1	1	16	SDRAM9. 1 = Enable, 0 = Output disabled asynchronously in a low state
0	1	15	SDRAM8. 1 = Enable, 0 = Output disabled asynchronously in a low state

Byte 3: Silicon Register (Read Only)

Bit	@Pup	Pin #	Description
7	1		Vendor ID 1000 Cypress
6	0		
5	0		
4	0		
3	0		Revision ID
2	0		
1	0		
0	0		

Maximum Ratings[5]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.5V

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} + 0.7V

Storage Temperature: .....–65°C to + 150°C

Operating Temperature: .....0°C to +70°C

Maximum ESD Protection:.....2000V

Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters[6]: TA = 0°C to +70°C

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	SDATA, SCLK			1.0	V
V_{IH}	Input High Voltage		2.2			V
V_{IL}	CLKIN Input Low Voltage (SDR Mode, VDD_3.3V = 3.3V)	CLKIN, FBIN_SDR	–0.3		0.8	V
V_{IL}	CLKIN Input Low Voltage (DDR Mode, VDD_2.5V = 2.5V)	CLKIN, FBIN_DDR	–0.3		0.7	V
V_{IH}	CLKIN Input High Voltage (SDR Mode, VDD_3.3V = 3.3V)	CLKIN, FBIN_SDR	2.0		V_{DD} + 0.3	V
V_{IH}	CLKIN Input High Voltage (DDR Mode, VDD_2.5V = 2.5V)	CLKIN, FBIN_DDR	1.7		V_{DD} + 0.3	V
I_{OZ}	High-Impedance Output Current	V_O = GND or V_O = VDD	–10		10	mA
I_{DDQ}	Dynamic Supply Current[7]	F_O = 133 MHz		235	300	ma
C_{in}	Input Pin Capacitance			4		pF

Table 5. AC Parameters for DDRT/C (0:5): VDD_2.5V = 2.5V ±5%, AVDD_3.3V = 3.3V ±5%, TA = 0°C to +70°C

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
fCLK	Operating Clock Frequency	VDD_2.5V = 2.5V ±5%	99		170	MHz
tDCI	Input Clock Duty Cycle		45		55	%
tDCO	Output Clock Duty Cycle		47	50	53	%
tLOCK[9]	Maximum PLL Lock Time				1.5	ms
Tr/Tf	Output Clocks Slew Rate	20% to 80% of VDD_2.5V	1.0		2.3	V/ns
tpZL, tpZH	Output Enable Time[8](all outputs)			3	5	ns
tpLZ, tpHZ	Output Disable Time[8](all outputs)			3	5	ns
tHPJ	Half-Period Jitter	@100 MHz and 133 MHz		90	125	ps
tPHASE	Phase Error	@133 MHz			200	ps
tSKEW	Any Output to Any Output Skew[7]				150	ps
VOUT	Output Voltage Swing[7]		1.1		V_{DD} – 0.4	V
Vx	Output Crossing Voltage[7]		(V_{DD}/2) – 0.2	V_{DD}/2	(V_{DD}/2) + 0.2	V

Notes:

5. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
6. Unused inputs must be held high or low to prevent them from floating.
7. All differential output terminals are terminated with 120Ω/16 pF as shown in *Figure 4*.
8. Refers to the transition of non-inverting output.
9. Time required for the integrated PL circuit to obtain phase lock of its feed back signal to its reference signal. For Phase lock specifications for propagation delay, skew and jitter parameters given in the switching characteristics table are not applicable.

Table 6. AC Parameters for SDRAM Outputs: VDD_3.3V = 2.5V ±5%, AVDD_3.3V = 3.3V ±5%, TA = 0°C to +70°C

Parameter	Description	Condition	Min	Typ	Max	Unit
fCLK	Operating Clock Frequency	VDD_3.3V = 3.3V ±5%	99		133	MHz
tDCI	Input Clock Duty Cycle		45		55	%
tLOCK[9]	Maximum PLL Lock Time				1.5	ms
tDCO	Output Clock Duty Cycle	100 MHz, 133 MHz	45	50	55	%
Tr/Tf[10, 11, 12]	Output Clocks Slew Rate		0.4		1.6	ps
tpZL, tpZH	Output Enable Time (all outputs)			3	5	ns
tpLZ, tpHZ	Output Disable Time (all outputs)			3	5	ns
tCCJ	Cycle-to-Cycle Jitter	@133 MHz		90	200	ps
tPHASE	Phase Error	@133 MHz			400	ps
tSKEW	Any Output to Any Output Skew[11]				200	ps
VOUT	Output Voltage Swing[11]		1.1		V_{DD} – 0.4	V
Vx	Output Crossing Voltage[11]		(V_{DD}/2) – 0.2	V_{DD}/2	(V_{DD}/2) + 0.2	V

Notes:
10. The tSKEW specification is only valid for equal loading of all outputs (30 pF lump-load). Measurement are acquired at 1.5V for 3.3V signals.
11. The test load is 30 pF lump-load.
12. TR/TF are measured at 0.4V to 2.4V.

Differential Parameter Measurement Information

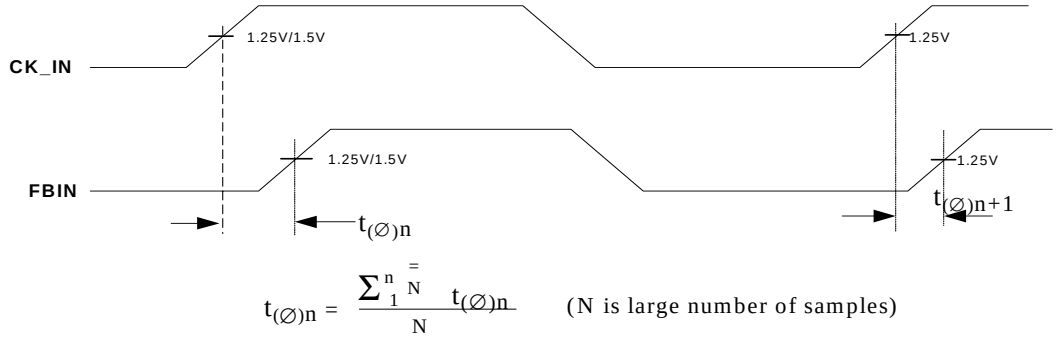


Figure 1. Phase Error

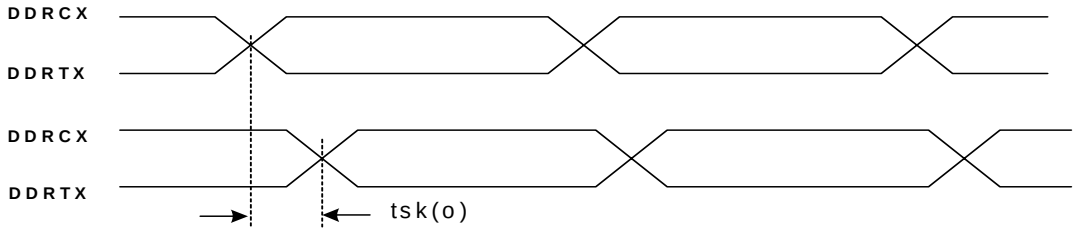


Figure 2. Output Skew

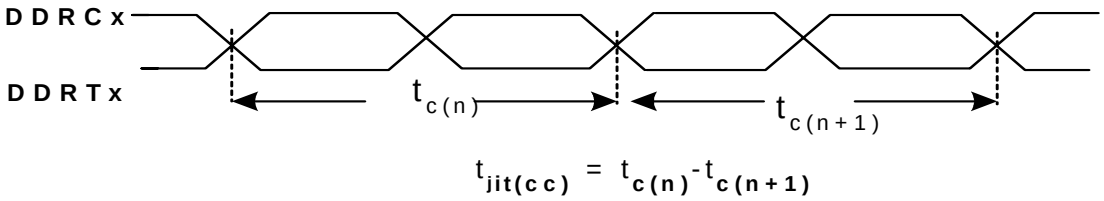


Figure 3. Cycle-to-Cycle Jitter

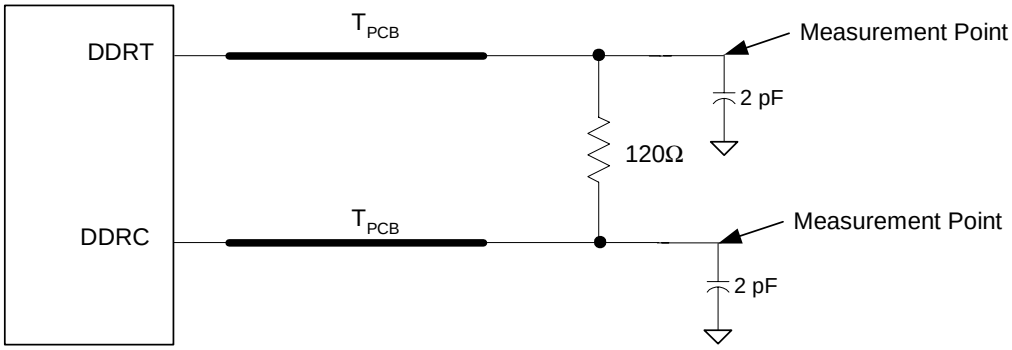


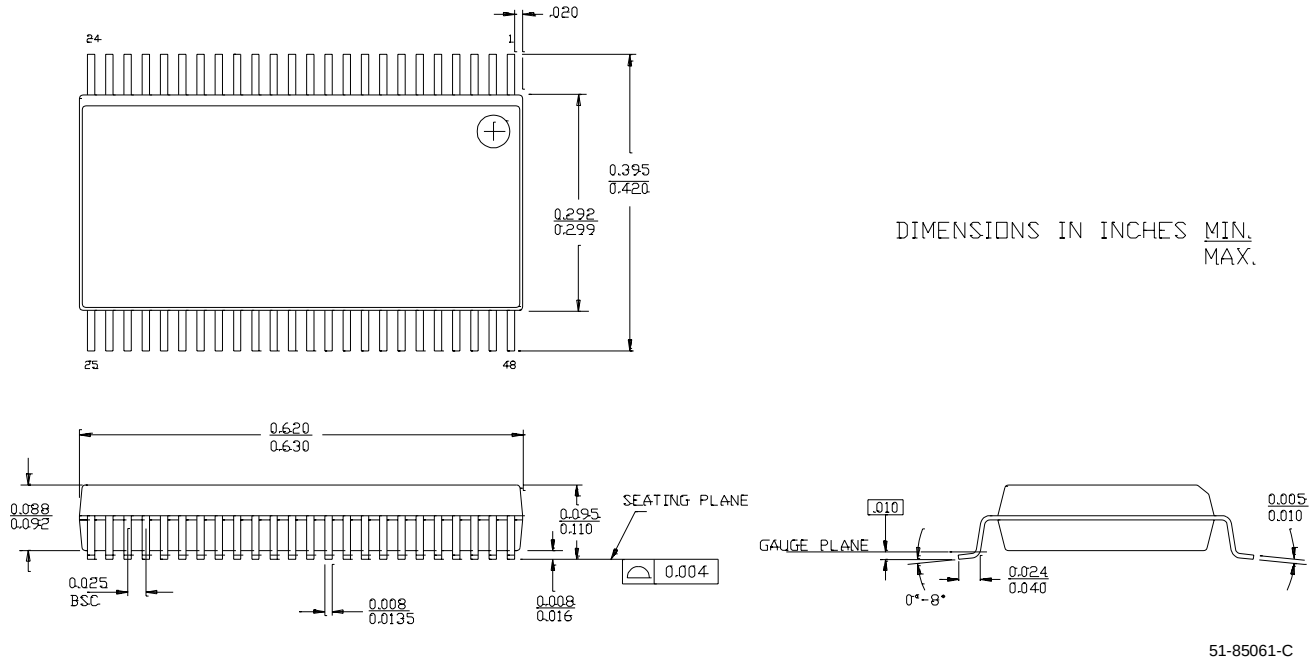
Figure 4. Differential Signal Using Direct Terminal Resistor

Ordering Information

Part Number	Package Type	Product Flow
CY28343OC	48-pin SSOP	Commercial, 0° to 70°C
CY28343OCT	48-pin SSOP - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

48-Lead Shrunk Small Outline Package O48



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Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	116671	08/22/02	DMG	New Data Sheet
*A	122909	12/26/02	RBI	Add power up requirements to maximum ratings information