
HD74HC283

4-bit Binary Full Adder

HITACHI

Description

The sum (S) outputs are provided for each bit and the resultant carry (C₄) is obtained from the fourth bit. This adder features full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation. The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- High Speed Operation: $t_{pd} = 19 \text{ ns typ (} C_L = 50 \text{ pF)}$
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: $1 \mu\text{A max}$
- Low Quiescent Supply Current: $I_{CC} \text{ (static)} = 4 \mu\text{A max (} T_a = 25^\circ\text{C)}$

HD74HC283

Function Table

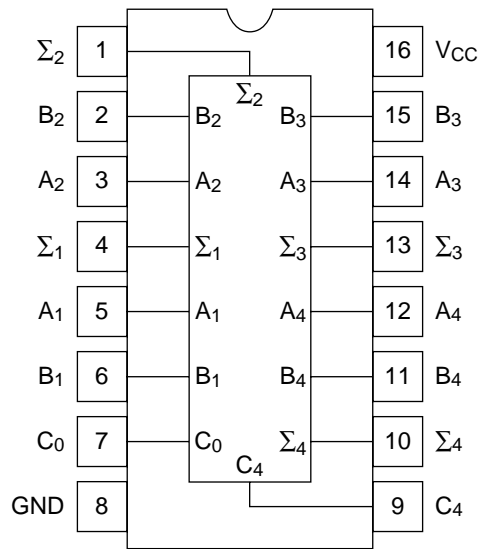
Inputs				Outputs					
				When $C_0 = L$ /When $C_2 = L$			When $C_0 = H$ /When $C_2 = H$		
A_1/A_3	B_1/B_3	A_2/A_4	B_2/B_4	Σ_1/Σ_3	Σ_2/Σ_4	C_2/C_4	Σ_1/Σ_3	Σ_1/Σ_4	C_2/C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H : high level

L : low level

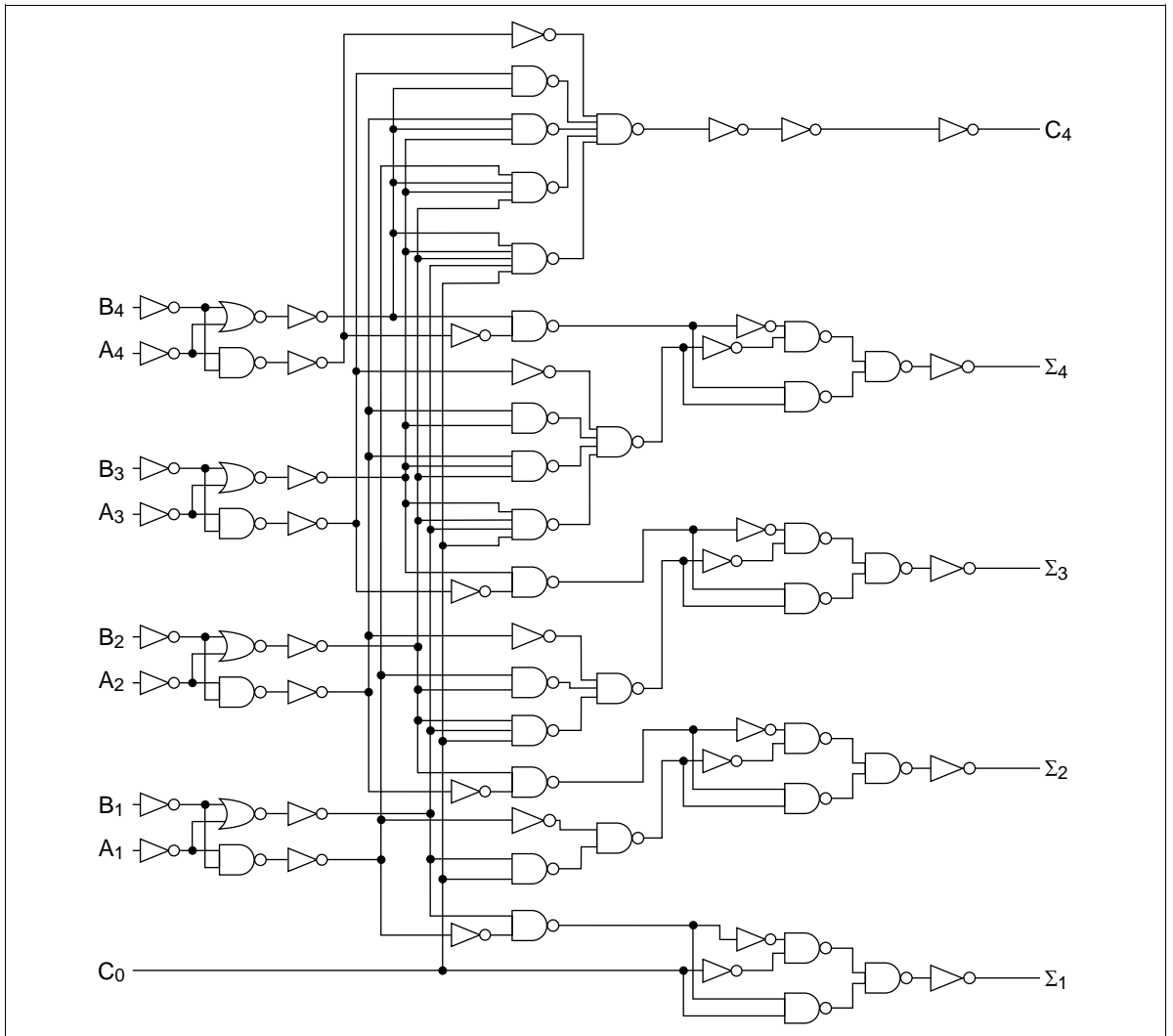
Note: Input conditions at A_1 , B_1 , A_2 , B_2 , and C_0 are used to determine outputs Σ_1 and Σ_2 and the value of the internal carry C_2 . The values at C_2 , A_3 , B_3 , A_4 and B_4 are then used to determine outputs Σ_3 , Σ_4 and C_4 .

Pin Arrangement



(Top view)

Block Diagram



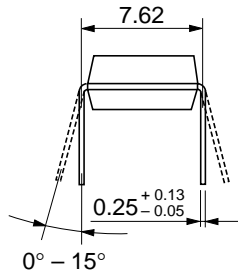
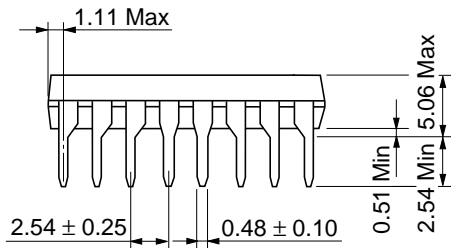
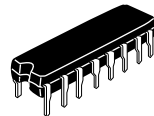
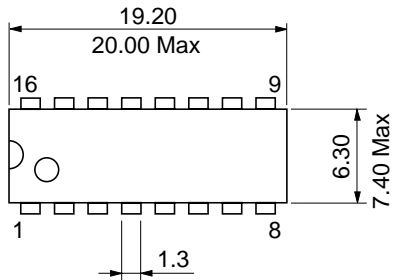
DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
		6.0	—	0.0	0.1	—	0.1			V
	4.5	—	0.0	0.1	—	0.1				
	6.0	—	0.0	0.1	—	0.1				
	4.5	—	—	0.26	—	0.33	I _{OL} = 4 mA			
	6.0	—	—	0.26	—	0.33	I _{OL} = 5.2 mA			
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

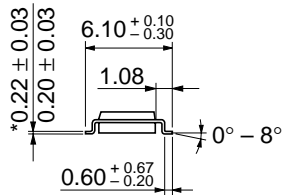
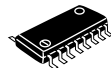
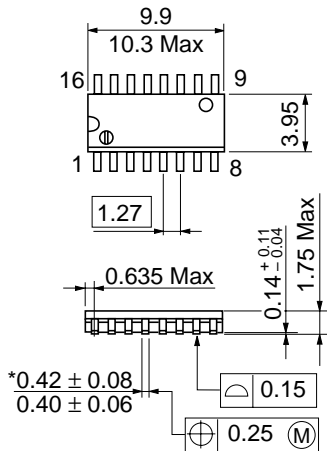
HD74HC283

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$		$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Propagation delay time	t_{PLH}	2.0	—	—	150	—	190	ns	C_0 to Σ_1
		4.5	—	19	30	—	38		
		6.0	—	—	26	—	33		
	t_{PHL}	2.0	—	—	150	—	190	ns	A_1 or B_1 to Σ_1
		4.5	—	19	30	—	38		
		6.0	—	—	26	—	33		
	t_{PLH}	2.0	—	—	150	—	190	ns	C_0 to C_4
		4.5	—	19	30	—	38		
		6.0	—	—	26	—	33		
	t_{PHL}	2.0	—	—	150	—	190	ns	A_1 or B_1 to C_4
		4.5	—	19	30	—	38		
		6.0	—	—	26	—	33		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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