MC141620

Advance Information

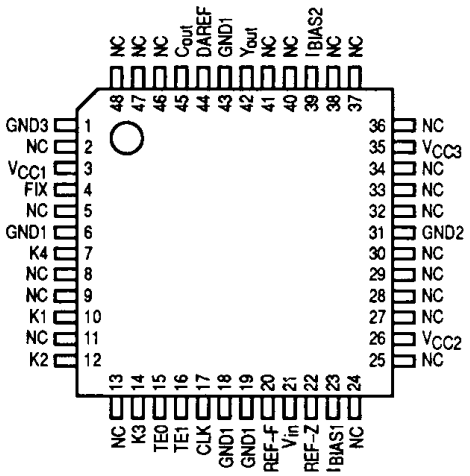
Enhanced Comb Filter
CMOS

The enhanced comb filter is a video signal processor for television and video recorder applications. The device separates the luminance Y and chrominance C from the NTSC composite video signal by using digital signal processing techniques. This filter allows an extended frequency bandwidth of the luminance signal while minimizing the common comb-filter problems such as dot-crawl and cross-color. This chip easily connects to analog TV and VCR chips due to the on-board A/D and D/A converters.

- Fast 8-Bit A/D Converter
- Two Line-Delay Memories
- Enhanced Combing Process
- Two 8-Bit D/A Converters
- Utilizes NTSC 4fsc (sub-carrier frequency) Clock

FU SUFFIX
QFP
CASE TBD

ORDERING INFORMATION
MC141620FU Quad Flat Package



NC = NO CONNECTION

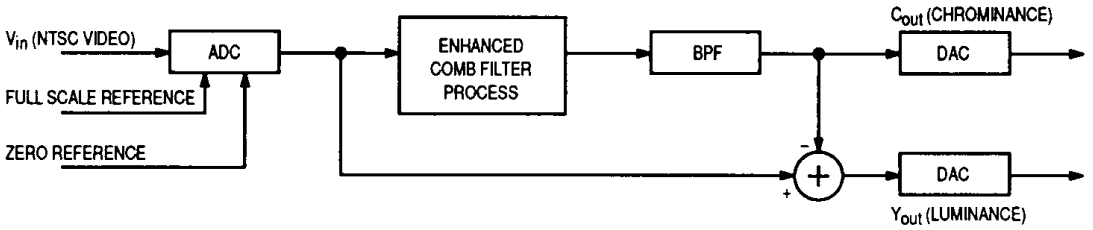


Figure 1. Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Characteristic	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current (per pin)	±20	mA
I_{out}	DC Output Current (per pin)	±25	mA
I_{CC}	DC Supply Current (V_{CC} and GND pins)	±100	mA
P_D	Power Dissipation	750	mW
T_{stg}	Storage Temperature	−65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

GENERAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C Unless Otherwise Noted)

Symbol	Characteristic	Min	Max	Unit
V_{CC}	Supply Voltage (V_{CC1}, V_{CC2}, V_{CC3})	4.5	5.5	V
I_{CC}	Operating Supply Current	—	75	mA
P_D	Operating Power Dissipation	—	420	mW
T_A	Ambient Operating Temperature	−20	80	°C
t_d	Total Signal Delay	—	64.95*	µs

*Nominal value. System clock for 930.5 cycles.

ADC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Typ*	Max	Unit
Resolution	8	—	—	Bits
Integral Nonlinearity	—	—	±1.5	LSB
Differential Nonlinearity	—	—	±1.0	LSB
Analog Input Level	—	—	3.0	V p-p
Full-Scale Reference Level	REF-Z	V_{CC2} − 0.4	V_{CC2} − 0.3	V
Zero Reference Level	1.4	1.6	REF-F	V
Reference Resistor Value (between REF-F & REF-Z)	—	380	600	Ω
Bias Current (Resistor = 10 kΩ)	—	120	—	µA
Input Capacitance (Design Ref. Value)	—	35	—	pF

*Data labeled "typ" is not guaranteed.

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CLOCK INPUT ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Max	Unit
Clock Frequency (Note 1)	12	15	MHz
Clock Jitter	—	2.0	ns
Input Level (Figure 8)	0.20	5.0	V p-p

Note 1 — This signal is usually 14.31818 MHz

FILTERING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Max	Unit
Y/C Separation (clock jitter < 2.0 ns)	—	40*	dB

*Typical value. Not guaranteed.

DAC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Max	Unit
Resolution	8	—	Bits
Output Bandwidth (at –3.0 dB)	5.5	—	MHz
Integral Nonlinearity	—	±1.0	LSB
Differential Nonlinearity	—	±0.3	LSB
Differential Gain	—	5.0	%
Differential Phase	—	5.0	Deg
Analog Output Voltage, Y_{out}	1.1	1.3	V p-p
Analog Output Voltage, C_{out}	1.1	1.3	V p-p
Full Scale Voltage, Y_{out}	1.3	1.7	V
Full Scale Voltage, C_{out}	1.3	1.7	V
Zero Scale Voltage, Y_{out}	0.1	0.5	V
Zero Scale Voltage, C_{out}	0.1	0.5	V
Bias Current [DAC only] — Resistor = 10 kΩ	120*	—	µA
Output Impedance	—	300	Ω

*Typical value. Not guaranteed.

DIGITAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Characteristic	Min	Max	Unit
V_{IH}	High Level Input Voltage (K1 ~ K4, FIX)	3.15	—	V
V_{IL}	Low Level Input Voltage (K1 ~ K4, FIX)	—	1.1	V
I_{IH}	High Level Input Current (K1 ~ K4, FIX)	—	0.1	µA
I_{IL}	Low Level Input Current (K1 ~ K4, FIX)	—	0.1	µA

PIN DESCRIPTIONS

V_{CC1} (Pin 3)
+5.0 V ± 10% dc power supply for the digital circuits.

V_{CC2} (Pin 26)
+5.0 V ± 10% dc power supply for the ADC.

V_{CC3} (Pin 35)
+5.0 V ± 10% dc power supply for the DAC.

GND1 (Pins 6, 18, 19, 43)
Ground for the digital circuits. For optimum performance, all pins must be tied to ground.

GND2 (Pin 31)
Ground for the ADC.

GND3 (Pin 1)
Ground for the DAC.

CLK (Pin 17)
4fsc (sub-carrier frequency) 14.31818 MHz input. This signal is usually ac-coupled through an external capacitance. See User Information. The clock signal must synchronize with the NTSC video signal.

V_{In} (Pin 21)
Composite video signal input. The composite video signal, clamped externally, should be supplied with dc coupling. The video input level should be nominally 3.0 V p-p. Input signal bandwidth should be limited to less than 1/2 of the frequency of the sampling clock by anti-aliasing filtering, etc.

REF-F (Pin 20)
ADC reference for the full-scale voltage.

REF-Z (Pin 22)
ADC reference for the zero input voltage.

DAREF (Pin 44)
Reference for the luminance and chrominance DACs. Insert a capacitor of 0.1 µF between DAREF and GND3.

I_{BIAS1} (Pin 23)
ADC bias circuit current control. Insert a resistor of 10 kΩ between I_{BIAS1} and GND2.

I_{BIAS2} (Pin 39)
DAC bias circuit current control. Insert a resistor of 10 kΩ between I_{BIAS2} and GND3.

Y_{out} (Pin 42)
Luminance output. This output signal is fed into the general analog VCR/TV system. Typical output voltage is 1.2 V p-p swinging from 0.3 V to 1.5 V.

C_{out} (Pin 45)
Chrominance output. This output signal is fed into the general analog VCR/TV system. Typical output voltage is 1.2 V p-p swinging from 0.3 V to 1.5 V.

TE0 (Pin 15)
Test enable pin. If this pin is a high level, the test mode is enabled. This pin must be grounded by the user.

TE1 (Pin 16)
Test select pin. This pin must be grounded by the user.

FIX (Pin 4)
Filter mode select pin. It must be a high level for the normal mode. Comb filter/bandpass filter fixed mode can be selected by the K1 pin. Each mode is shown below.

FIX	K1	MODE
H	H	Normal mode
H	L	Normal mode
L	H	Bandpass filter fixed mode
L	L	Comb filter fixed mode

K1, K2, K3, and K4 (Pins 10, 12, 14, 7)
K factor inputs. These pins are provided to set up the K value for the select control circuit, and to set up the threshold level of comb filter and bandpass filter. Each input (K1 ~ K4) are assigned to b1 ~ b4 of the K factor. Input must be at CMOS levels. The assignment of K pins are shown below. Also, when the FIX pin is at a low level, the K1 pin becomes a filter mode select pin. If the K1 pin is low, the comb filter is enabled; otherwise, the bandpass filter is enabled.

b0	b1	b2	b3	b4	b5	b6	b7
L	K1	K2	K3	K4	H	H	L

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OVERVIEW

The enhanced comb filter is a high performance HCMOS digital filter combined with A/D and D/A converters. The basic functions of this chip are the separation of the luminance Y and chrominance C signals from the NTSC video signal which is composed of luminance and chrominance components interleaved with each other in the same frequency band.

The visual performance advantages of the enhanced comb filter are that the chip eliminates the sub-carrier dot-crawl from the luminance channel in large color areas and eliminates the cross color from the chrominance in high frequency luminance areas. Also, the horizontal resolution of the picture is allowed from zero to an arbitrary high by this chip. The Y/C separation is performed by a combination of a digital 2H comb filter and a digital bandpass filter.

To perform the enhanced combing process, two horizontal scan line delay memories for a 2H comb filter, several pairs of latches for a bandpass filter, and selective control circuitry are provided. The 2H comb filter separates the chrominance components from the composite video signal by integration of 3 successive lines. However, when the comb filter is performing the line integration, the horizontal color smears on the boundary. This chip solves the color smear and dot-crawl problems while keeping the advantages of 2H comb filter by selecting one filter process from the bandpass filter or the 2H comb filter at a particular picture transition.

Enhanced Comb Filter Description

Figure 1 shows the block diagram of the enhanced comb filter chip. There are three major functions on this block diagram.

The first is the analog-to-digital conversion block. One 8-bit binary A/D converter is provided for digitizing the incoming analog video signal to 8-bit binary data. The conversion frequency is 14.3 MHz which is four times the color sub-carrier frequency. The analog video input is nominally 3.0 V p-p.

The second is the digital filters and selective control block. There are two digital filters on this block which are vertical filter (2H comb filter) and horizontal filter (bandpass filter). The selective control determines which type of filter should be chosen for the current process.

The third is the digital-to-analog conversion block. Two 8-bit D/A converters are provided for the luminance and chrominance analog output. The conversion frequency is four times the sub-carrier signal (14.3 MHz). The chrominance analog output has a dc offset bias of half the maximum output voltage.

Algorithm of Enhanced Comb Filter

Figure 2 illustrates the basic principles of the Y/C separation algorithm. The NTSC video signal has an alternate relationship in the horizontal and vertical direction on the sampled data array. V1 through V9 in Figure 2 represent a sampled data array of an appropriate area of the screen. The sampling frequency is four times the sub-carrier frequency (14.3 MHz). There are four data samples in one sub-carrier cycle, and the sub-carrier phase is reversed every scan line. In other words, V1 and V7 have same phase and V4 is reversed; V2 and V8 have same phase and V5 is reversed. Also, the sampled data V1 through V3 are placed on scan line N, V4 through V6 are on N-1, and so on. On the individual lines, every four data samples have the same phase — for instance, V1 and V3, V4 and V6, and so forth.

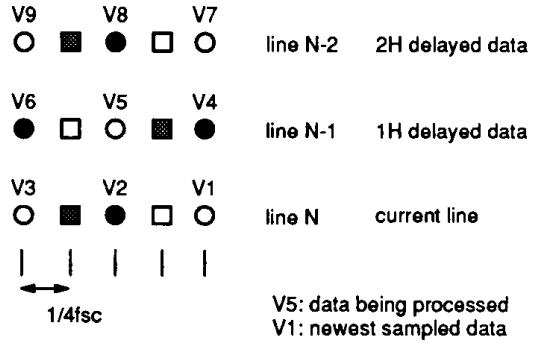

Figure 2.

Vertical Filtering

The typical vertical filter is a comb filter which may use 1H or 2H scan line delay. The comb filter integrates successive scan line data to separate Y and C. The formula is:

$$\text{Chrominance} = (V5 - (V2 + V8) / 2) / 2 \times H_{BPF}$$

$$\text{Luminance} = V5 - \text{Chrominance}$$

Where H_{BPF} is the BPF transfer function.

The combing process allows the luminance signal separation for the extension of the frequency bandwidth. However, the integration of the successive lines causes a loss of vertical resolution. The combing process causes color smears on the line, if there is color transition between the lines. It can be observed as color smear on the color boundary or horizontal running dot-crawl.

Horizontal Filtering

The conventional filtering, such as a bandpass filter, has typical dot-crawl and cross-color problems. Even the digital horizontal filtering has similar problems. However, the MC141620's digital horizontal filtering yields superior performance over a regular bandpass filter. The formula is:

$$\text{Chrominance} = (V5 - (V4 + V6) / 2) / 2 \times H_{BPF}$$

$$\text{Luminance} = V5 - \text{Chrominance}$$

Where H_{BPF} is the BPF transfer function.

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Enhanced Comb Filtering (Combination of Vertical and Horizontal Filtering)

This is a combination approach of the vertical filtering and horizontal filtering so that the overall filtering can take advantage of both filters. The algorithm of this filter is as follows:

If $|V8 - V2| + K \leq |V6 - V4|$
(Vertical Transition ≤ Horizontal Transition)
K: constant value
then Chrominance = $(V5 - (V2 + V8) / 2) / 2 \times H_{BPF}$
— Vertical Filter

If $|V8 - V2| + K > |V6 - V4|$
(Vertical Transition > Horizontal Transition)

then Chrominance = $(V5 - (V6 + V4) / 2) / 2 \times H_{BPF}$
Luminance = V5 – Chrominance — Horizontal Filter

This algorithm determines the amount of Y/C separation according to the result of comparison between the value change V2 to V8 and V4 to V6. Measurement of this data array allows minimization of the problems caused by horizontal and vertical filtering, such as dot-crawl or color smear. Also, it can give a weight to select a filter, vertical or horizontal, according to the K factor set up.

OPERATIONAL DESCRIPTION

A/D Converter

The clamped external composite-video signal is converted to 8-bit binary code by this fast A/D converter. The input video voltage is expected to be 3.0 V p-p nominal. The sampling clock frequency is 14.3 MHz which is four times the color subcarrier signal.

Comb Filter Function

The comb filter consists of a delay-line memory, absolute value function, latches, and 8-bit adders. The basic functions of the filtering are additions and subtractions by the adders. The calculations for each sampled data are expected to be completed within one clock cycle, about 70 ns. Each adder has latches to hold the value calculated. If the speed of the adders is not fast enough, other latches may be inserted into the adders to save the partial value of the calculations. These latches are counted as the digital process delay of the filter. There are two major data passes in this filter: chrominance and luminance. Both data passes are designed such that all delays match when they output.

Vertical Filter

The basic structure of this filter is a 2H line-delay comb filter. The simplified functional block diagram is shown in Figure 3.Two 1H scan delay lines are provided for vertical filtering. Video memory structure can be used for the line delay component. The cycle time of this memory has to be less than 70 ns, and total delay time is 1 scan line time for each.

Horizontal Filter

The other basic function of this filter is called horizontal filtering which has the same function as a bandpass filter. The horizontal filter consists of a 4th order FIR filter which has a bandpass characteristic. Figure 4 shows the simplified functional block diagram of the horizontal filter.

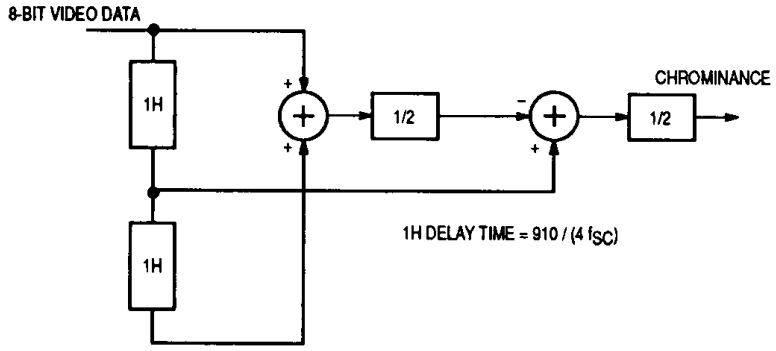

Figure 3. Vertical Filter

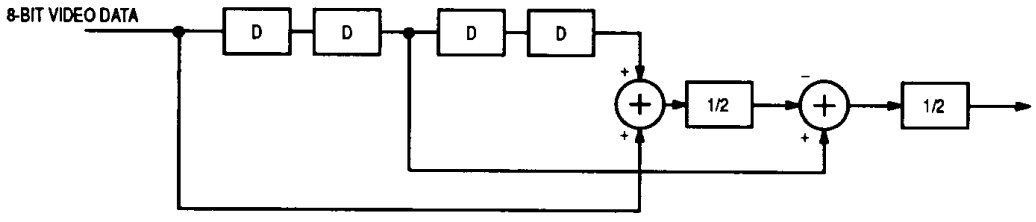

Figure 4. Horizontal Filter

Selective Control

The selective control checks the horizontal transition and vertical transition of the picture in order to select a filtering method that minimizes the dot-crawl, cross color, and color smear. The major filtering algorithm of the chip is performed in this block.

Horizontal transition = |V6 – V4|

Vertical transition = |V8 – V2|

The difference of the transition = |V8 – V2| – |V6 – V4| + K

If |V8 – V2| – |V6 – V4| + K > 0 then Horizontal Filter

If |V8 – V2| – |V6 – V4| + K ≤ 0 then Vertical Filter

K factor

Selective control switches the filtering modes by the transit difference of horizontal and vertical direction. K factor assignment is shown below. If K1 through K4 are all low, a weighting factor is given to the comb filter side. If all are a high level, it gives a weighting factor of 50% comb and bandpass side. The recommended level is b1 = L, b2 through b4 = H.

b0	b1	b2	b3	b4	b5	b6	b7
L	K1	K2	K3	K4	H	H	L

b0, b5, b6, b7 are fixed.

Bandpass Filter (BPF)

This filter has the same functions as the horizontal filter. The bandpass filter reduces low and high frequency components in the chrominance signal.

Video Input Signal

The recommended video input signal for the comb filter is shown in Figure 5. The nominal video input is 3.0 V p-p.

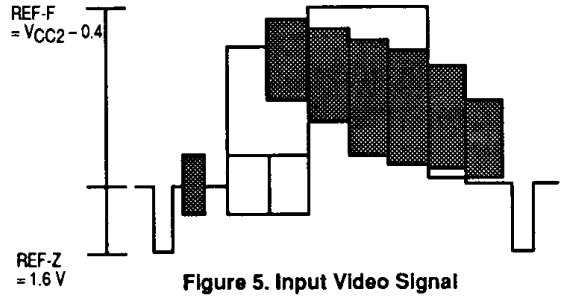

Figure 5. Input Video Signal

USER INFORMATION

V_{CC}, GND

Each of the V_{CC}/GND-pin pairs should be connected to separate power supplies in order to reduce noise problems. All V_{CC} pins should be by passed through 0.1 µF ceramic and 47 µF tantalum capacitors mounted as close as possible to the MC141620.

V_{in}

The video input signal must be clamped with an appropriate voltage level. It might be necessary to amplify the signal to drive this chip. In order to reduce noise effects, the wiring pattern on the V_{in} signal should be short as possible. V_{in} should be driven with a low-impedance source. The frequency bandwidth of the input signal should be limited to less than half of the sampling clock frequency (Nyquist criteria).

AD Reference Inputs

REF-F and REF-Z set the dynamic range of the ADC input. These should be by passed through 0.1 µF ceramic and 10 µF tantalum capacitors mounted close to GND2. The voltage supplied to REF-F and REF-Z must be stable within allowable time and temperature ranges.

Reference accuracy is ±0.5 LSB (voltage difference between REF-F and REF-Z), if all portions of circuit are not changed in compliance with temperature. But, most circuits are changed in compliance with the temperature. Therefore, in this case, the reference voltage accuracy should be less than ±0.5 LSB. A stable power supply is required for these reference inputs and the resistor value of the reference ladder is low (typically about 300 Ω).

Clock Input

Reference Figures 6, 7 and 8.

Clock (14.31818 MHz) must be synchronized with a subcarrier (NTSC) or horizontal sync signal. The clock line should be a short printed circuit board trace, and should be separated from other circuits in order to reduce crosstalk. TTL or CMOS levels may be connected by dc coupling. 5.0 V p-p sine waves may be ac coupled with a 0.1 µF ceramic capacitor.

A small signal, such as a 200 mV p-p or greater sine wave, may be ac coupled with a 0.1 µF ceramic capacitor, then biased to half of V_{CC1} by a pair of 330 kΩ resistors.

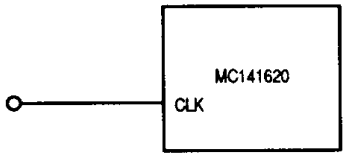

Figure 6. TTL Level

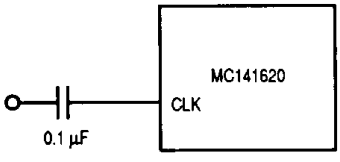

Figure 7. 5.0 V p-p Sine Wave

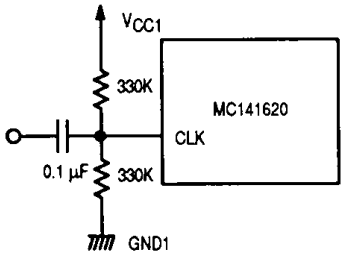

Figure 8. 200 mV p-p to 5.0 V p-p Sine Wave

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When the clock level is less than 200 mV p-p, it should be supplied to the circuit of Figure 8 after being increased to more than 200 mV p-p using a buffer amplifier.

I_{BIAS} Pins

The I_{BIAS} pins determine the bias current of the ADC and DAC by external resistors. I_{BIAS1} is associated with the ADC and I_{BIAS2} is for the DAC. In both cases, a 10 kΩ resistor is connected from each of these pins to the closest GND.

DA Reference

This is a bypass pin for the DA reference. Insert a bypass capacitor of about 0.1 µF between DAREF and GND3.

Power-On Sequence

The GND1, GND2, and GND3 pins are connected to a common ground. Power should be supplied sequentially to V_{CC1}, V_{CC2}, then V_{CC3}.

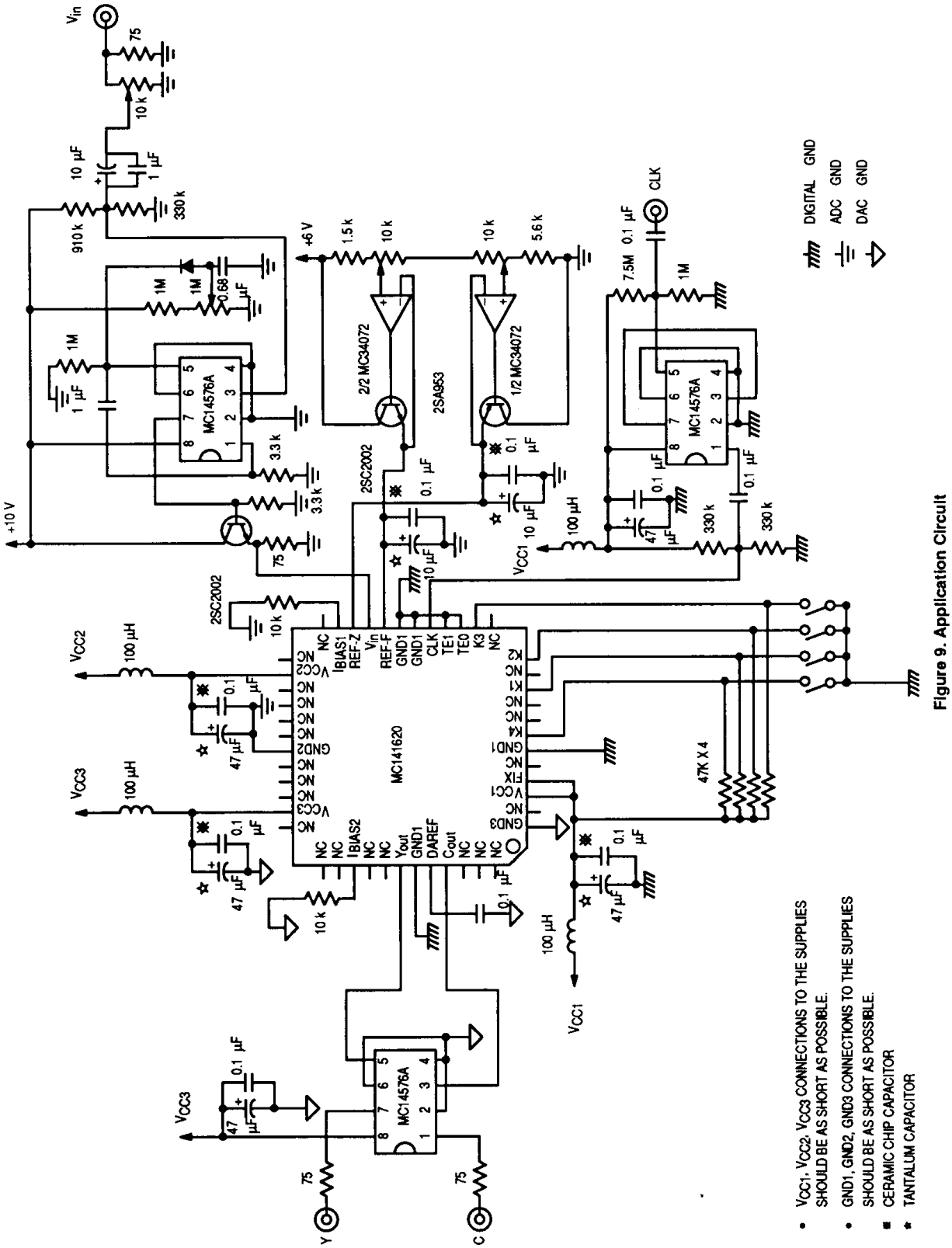

Figure 9. Application Circuit

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