## DESCRIPTION

The MC3410 series are 10-bit Multiplying Digital-to-Analog Converters. They are capable of high-speed performance, and are used as general-purpose building blocks in cost-effective D/A systems.
The Philips Semiconductors design provides complete 10-bit accuracy without laser trimming, and guaranteed monotonicity over temperature. Segmented current sources, in conjunction with an R-2R DAC provides the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

## FEATURES

- 10-bit resolution and accuracy ( $\pm 0.05 \%$ )
- Guaranteed monotonicity over temperature
- Fast settling time-250ns typical
- Digital inputs are TTL and CMOS compatible
- Wide output voltage compliance range
- High-speed multiplying input slew rate- $20 \mathrm{~mA} / \mu \mathrm{s}$
- Reference amplifier internally-compensated
- Standard supply voltages +5 V and -15 V


## APPLICATIONS

- Successive approximation A/D converters
- High-speed, automatic test equipment
- High-speed modems
- Waveform generators
- CRT displays
- Strip CHART and X-Y plotters
- Programmable power supplies
- Programmable gain and attenuation


## PIN CONFIGURATION



## BLOCK DIAGRAM



## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE | DWG \# |
| :--- | :---: | :---: | :---: |
| 16-Pin Ceramic Dual In-Line Package (CERDIP) | 0 to $+70^{\circ} \mathrm{C}$ | MC3410F | 0582 B |
| 16-Pin Ceramic Dual In-Line Package (CERDIP) | 0 to $+70^{\circ} \mathrm{C}$ | MC3410CF | 0582 B |

## ABSOLUTE MAXIMUM RATINGS

$\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ unless otherwise noted

| SYMBOL | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CC }}$ | Power supply | +7.0 | $V_{D C}$ |
| $\mathrm{V}_{\mathrm{EE}}$ |  | -18 | $V_{D C}$ |
| $V_{1}$ | Digital input voltage | +15 | $V_{D C}$ |
| $\mathrm{V}_{\mathrm{O}}$ | Applied output voltage | 0.5, -5.0 | $V_{D C}$ |
| $\mathrm{I}_{\text {REF (16) }}$ | Reference current | 2.5 | mA |
| $\mathrm{V}_{\text {REF }}$ | Reference amplifier inputs | $\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{EE}}$ | $V_{D C}$ |
| $\mathrm{V}_{\text {REF ( } \mathrm{D})}$ | Reference amplifier differential inputs | 0.7 | $V_{D C}$ |
| $\mathrm{T}_{\text {A }}$ | Operating ambient temperature range MC3410, 3410C | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{J}$ | Junction temperature, ceramic package | +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{P}_{\mathrm{D}}$ | Maximum power dissipation, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}(\text { still-air })^{1}$ <br> F package | 1190 | mW |

## NOTES:

1. Derate above $25^{\circ} \mathrm{C}$, at the following rates:

F package at $9.5 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$

## ELECTRICAL CHARACTERISTICS

$\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{VDC}, \mathrm{V}_{\mathrm{EE}}=-15 \mathrm{DC}, \quad \frac{\mathrm{V}_{\mathrm{REF}}}{\mathrm{R} 16}=2.0 \mathrm{~mA}$, all digital inputs at high logic level. MC 3410 Series: $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$, unless otherwise noted.

| SYMBOL | PARAMETER | TEST CONDITIONS | MC3410 |  |  | MC3410C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\mathrm{E}_{\mathrm{r}}$ | Relative accuracy (error relative to full-scale lo) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  |  | $\pm 0.05$ |  |  | $\pm 0.1$ | \% |
|  |  |  |  |  | 1/4 |  |  | 1/2 | LSB |
| TCE ${ }_{r}$ | Relative accuracy drift (relative to full-scale $\mathrm{l}_{\mathrm{O}}$ ) |  |  | 2.5 |  |  | 2.5 |  | ppm/ ${ }^{\circ} \mathrm{C}$ |
|  | Monotonicity | Over temperature | 10 |  |  | 10 |  |  | Bits |
| ts | Settling time to within $\pm$ LSB (all bits LOW-to-HIGH) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 250 |  |  | 250 |  | ns |
| $\begin{aligned} & \mathrm{t}_{\mathrm{tPLH}} \\ & \mathrm{t}_{\mathrm{PHL}} \end{aligned}$ | Propagation delay time | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | $\begin{aligned} & 35 \\ & 20 \end{aligned}$ |  |  | $\begin{aligned} & 35 \\ & 20 \\ & \hline \end{aligned}$ |  | ns |
| TClo | Output full scale current drift |  |  |  | 60 |  |  | 70 | $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{IH}}$ | Digital input logic levels (all bits) HIGH-level, Logic "1" LOW-level, Logic "0" |  | 2.0 |  | 0.8 | 2.0 |  | 0.8 | $V_{D C}$ |
| $\left\lvert\, \begin{aligned} & I_{I H} \\ & I_{I L} \end{aligned}\right.$ | Digital input current (all bits) HIGH-level, $\mathrm{V}_{\mathrm{IH}}=5.5 \mathrm{~V}$ LOW-level, $\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{~V}$ |  |  | -0.05 | $\begin{aligned} & +.04 \\ & -0.4 \end{aligned}$ |  | -0.05 | $\begin{aligned} & +.04 \\ & -0.4 \end{aligned}$ | mA |
| IREF (15) | Reference input bias current (Pin 15) |  |  | -1.0 | -5.0 |  | -1.0 | -5.0 | $\mu \mathrm{A}$ |
| IOR | Output current range |  |  | 4.0 | 5.0 |  | 4.0 | 5.0 | mA |
| IOH | Output current (all bits high) | $\begin{gathered} \hline \mathrm{V}_{\mathrm{REF}}=2.000 \mathrm{~V}, \\ \mathrm{R}_{16}=1000 \Omega \end{gathered}$ | 3.8 | 3.996 | 4.2 | 3.8 | 3.996 | 4.2 | mA |
| $\mathrm{l}_{\mathrm{OL}}$ | Output current (all bits low) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 0 | 2.0 |  | 0 | 4.0 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{0}$ | Output voltage compliance | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  |  | $\begin{array}{r} -2.5 \\ +0.2 \end{array}$ |  |  | $\begin{aligned} & \hline-2.5 \\ & +0.2 \end{aligned}$ | $V_{\text {DC }}$ |
| SR I ${ }_{\text {REF }}$ | Reference amplifier slew rate |  |  | 20 |  |  | 20 |  | $\mathrm{mA} / \mu \mathrm{s}$ |
| ST I REF | Reference amplifier settling time | 0 to $4.0 \mathrm{~mA}, \pm 0.1 \%$ |  | 2.0 |  |  | 2.0 |  | $\mu \mathrm{s}$ |
| PSRR(-) | Output current power supply sensitivity |  |  | 0.003 | 0.01 |  | 0.003 | 0.02 | \%/\% |
| $\mathrm{C}_{0}$ | Output capacitance | $\mathrm{V}_{\mathrm{O}}=0$ |  | 25 |  |  | 25 |  | pF |
| $\mathrm{Cl}_{1}$ | Digital input capacitance <br> (all bits high) |  |  | 4.0 |  |  | 4.0 |  | pF |
| $\begin{aligned} & \mathrm{I}_{\mathrm{CC}} \\ & \mathrm{I}_{\mathrm{FF}} \end{aligned}$ | Power supply current (all bits low) |  |  | -11.4 | $\begin{aligned} & +18 \\ & -20 \end{aligned}$ |  | -11.4 | $\begin{aligned} & +18 \\ & -20 \end{aligned}$ | mA |
| $\begin{array}{\|l} \hline \mathrm{v}_{\mathrm{CC}} \\ \mathrm{~V}_{\mathrm{EE}} \end{array}$ | Power supply voltage range | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\begin{gathered} \hline+4.75 \\ -14.25 \end{gathered}$ | $\begin{gathered} \hline+5.0 \\ -15 \end{gathered}$ | $\begin{gathered} +5.25 \\ -15.75 \end{gathered}$ | $\begin{aligned} & \hline+4.75 \\ & -14.25 \end{aligned}$ | $\begin{gathered} \hline+5.0 \\ -15 \end{gathered}$ | $\begin{aligned} & +5.25 \\ & -15.75 \end{aligned}$ | $\mathrm{V}_{\mathrm{DC}}$ |
|  | Power consumption <br> (all bits low) <br> (all bits high) |  |  | $\begin{aligned} & 220 \\ & 200 \\ & \hline \end{aligned}$ | 380 |  | $\begin{aligned} & 220 \\ & 200 \\ & \hline \end{aligned}$ | 380 | mW |

## 10-Bit high-speed multiplying D/A converter



Figure 1. Output Current vs Output Compliance Voltage


Figure 2. Maximum Output Compliance Voltage vs Temperature


Figure 3. Power Supply Current vs Temperature


Figure 4. Reference Amplifier Frequency Response

## CIRCUIT DESCRIPTION

The MC3410 consists of four segment current sources which generate the two most significant bits (MSBs), and an R-2R DAC implemented with ion-implanted resistors for scaling the remaining eight least significant bits (LSBs) (See Figure 5). This approach provides complete 10-bit accuracy without trimming.
The individual bit currents are switched ON or OFF by fully differential current switches. The switches use current steering for speed.
An on-chip high-slew reference current amplifier drives the R-2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times $1023 / 1024$ of the reference amplifier current, or nominally 3.996 mA for a 2.000 mA reference input current. The reference amplifier allows the user to provide a voltage input. Out-board resistor $\mathrm{R}_{16}$ (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0 V and a $1 \mathrm{k} \Omega$ resistor tied to Pin 16 , the full-scale current is approximately 4.0 mA . This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, $\mathrm{R}_{15}$ can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, $\mathrm{R}_{16}$ should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3 V above the $\mathrm{V}_{\mathrm{EE}}$ supply voltage for best operation. Bipolar input signals may be handled by connecting $R_{16}$ to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5 V logic supply is not recommended as a reference voltage. If a well regulated 5.0 V supply, which drives logic, is to be used as the reference, $\mathrm{R}_{16}$ should be decoupled by connecting it to the +5.0 V logic supply through another resistor and bypassing the junction of the two resistors with a $0.1 \mu \mathrm{~F}$ capacitor to ground.
The reference amplifier is internally-compensated with a 10 pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of $R_{16}$ and reference voltages which supply 2.0 mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0 mA . As $\mathrm{R}_{16}$ increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of $1.0 \mathrm{M} \Omega$, the bandwidth of the reference amplifier is approximately half what it is in the case of $R_{16}=1.0 \mathrm{k} \Omega$, and settling time is $\approx 10 \mu \mathrm{~s}$. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5 mA for stability.

## OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from -2.5 to +0.2 V . As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $\mathrm{V}_{\mathrm{EE}}>-15 \mathrm{~V}$.

## ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full-scale current drift with temperature.
The MC3410 are accurate to within $\pm 0.05 \%$ at $25^{\circ} \mathrm{C}$ with a reference current of 2.0 mA on Pin 16.


Figure 5. MC3410 Equivalent Circuit


Figure 6. Basic Connections

## MONOTONICITY

The MC3410 and MC3410C are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5 mA .

## SETTLING TIME

The worst-case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250 ns for the output to settle to within $\pm 1 / 2$ LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small ( $<0.7 \mathrm{~V}$ ) swing and the external output capacitance is under 25 pF .

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of $625 \Omega$ is connected to ground, allowing the output to swing to -2.5 V , the settling time increases to $1.5 \mu \mathrm{~s}$.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, $100 \mu \mathrm{~F}$ supply bypassing, and minimum scope lead length are all necessary.
A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2 V , and using a $500 \Omega$ load resistor $R_{L}$.



Figure 7. Settling Time


Figure 8. Propagation Delay Time


