Preliminary

OKI Semiconductor

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MSM7731-01

Multifunction PCM CODEC (Voice Signal Processor)

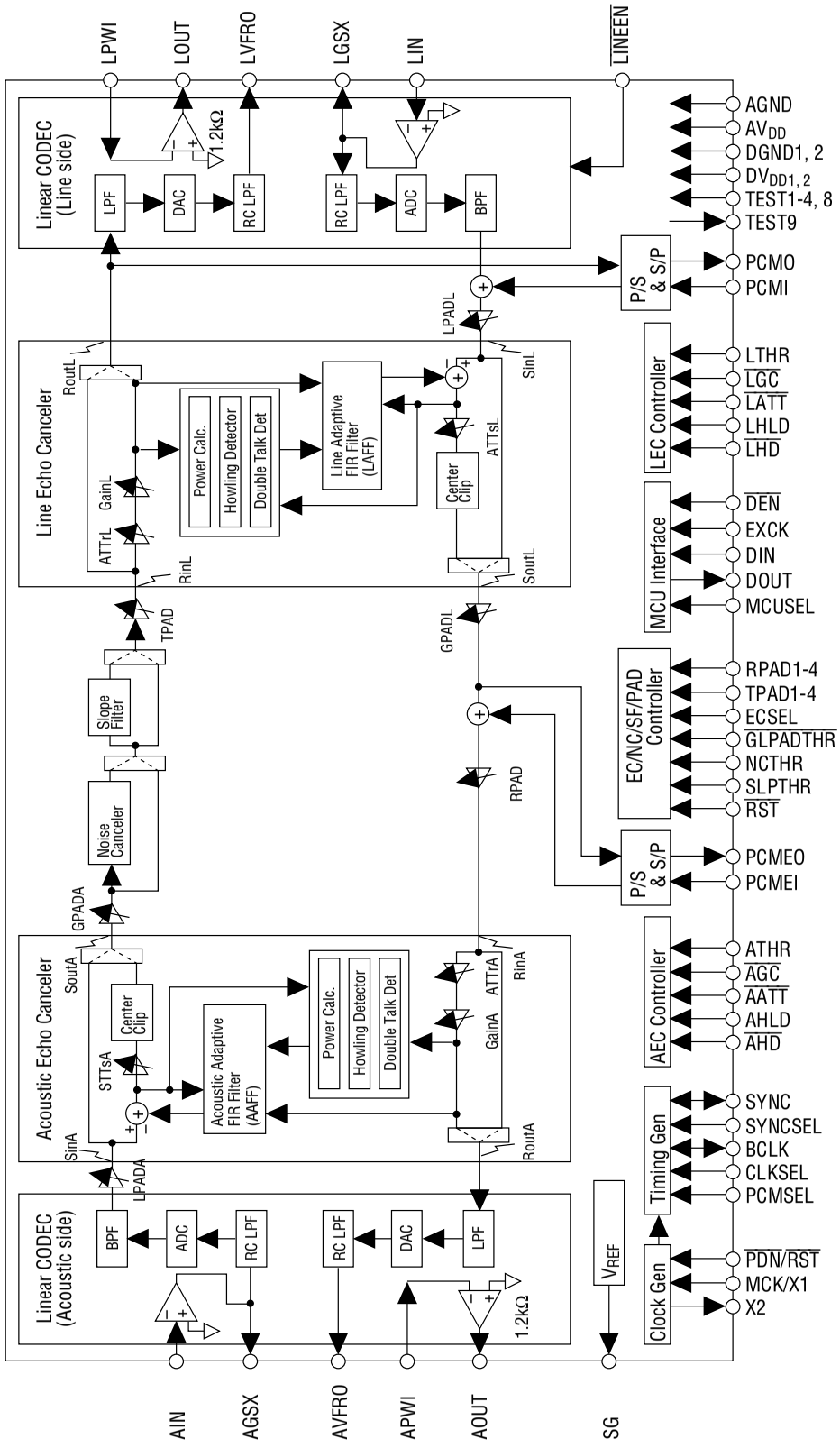
GENERAL DESCRIPTION

The MSM7731 is an LSI device developed for portable, handsfree communication with built-in line echo canceler, acoustic echo canceler, and transmission signal noise canceler. Built-in to the voice signal interface is a linear CODEC for the analog interface on the acoustic-side, and a linear CODEC for the analog interface on the line-side. On the line-side, in addition to the analog interface, there is also a μ-law PCM/16-bit linear digital interface.
Equipped with gain and mute controls for data transmission and reception, a μ-law PCM/16-bit linear digital interface for memo recording and message output, and transfer clock and sync clock generators for digital communication, this device is ideally suited for a handsfree system.

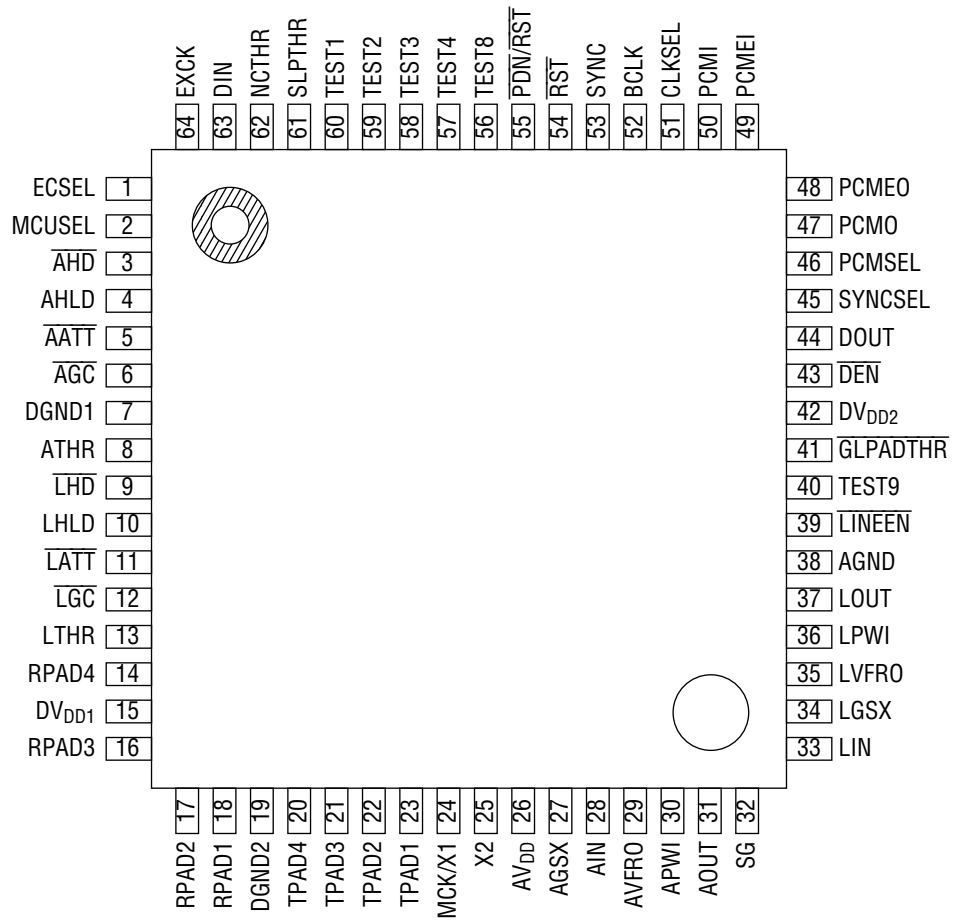
FEATURES

- Single 3 V power supply operation (2.7 V to 3.6 V)
- Built-in 2-channel (line and acoustic) echo canceler
  - Echo attenuation : 35 dB (typ.)
  - Cancelable echo delay time :
    - Line echo canceler + acoustic echo canceler : Tlined = 27 ms (max.), Tacoud = 59 ms – Tlined (max.)
    - Acoustic echo canceler only : Tacoud = 59 ms (max.)
- Built-in transmission signal noise canceler
  - Noise attenuation: 13 dB (typ.) for white noise
    40 dB (typ.) for single tone
- Built-in 2-channel CODEC
  Synchronous transmission and reception enables full duplex operation
- Built-in analog input gain amp stage (max. gain = 30 dB)
- Analog output configuration: Push-pull drive (can drive a 1.2 kΩ load)
- Built-in transmit slope filter
- Digital interface coding formats: μ-law PCM, 16-bit linear (2's complement)
- Digital interface sync formats: Normal-sync, short-frame-sync
- Built-in digital transmission clock generators
  - Sync clock (SYNC): 8 kHz output
  - Transmission clock (BCLK): 64 kHz output (μ-law PCM)/128 kHz output (16-bit linear)
- Digital transmission rate
  - External input: 64 kbps to 2048 kbps
  - Internal generation: 64 kbps (μ-law PCM)/128 kbps (16-bit linear)
- Fixed digital interface sync clock (SYNC) enables automatic power-down
- Master clock frequency: 19.2 MHz
  - Compatible with crystal oscillator and crystal
- Low power consumption
  - Operating mode: typ. 105mW (when V_{DD} = 3.0 V)
  - Power-down mode: typ. 0.3mW (when V_{DD} = 3.0 V)
- Control by both the serial microcomputer interface and parallel port is possible
- Transmit/receive mute function, transmit/receive programmable gain setting
- Package: 64-pin plastic QFP (QFP64-P-1414-0.80-BK) (Product name: MSM7731-01GA)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Pin	Symbol	Type
1	ECSEL	I	33	LIN	I
2	MCUSEL	I	34	LGSX	O
3	$\overline{\text{AHD}}$	I	35	LVFRO	O
4	AHLD	I	36	LPWI	I
5	$\overline{\text{AATT}}$	I	37	LOUT	O
6	$\overline{\text{AGC}}$	I	38	AGND	I
7	DGND1	I	39	$\overline{\text{LINEEN}}$	I
8	ATHR	I	40	TEST9	O
9	$\overline{\text{LHD}}$	I	41	$\overline{\text{GLPADTHR}}$	I
10	LHLD	I	42	DV_{DD2}	I
11	$\overline{\text{LATT}}$	I	43	$\overline{\text{DEN}}$	I
12	$\overline{\text{LGC}}$	I	44	DOUT	O
13	LTHR	I	45	SYNCSEL	I
14	RPAD4	I	46	PCMSEL	I
15	DV_{DD1}	I	47	PCMO	O
16	RPAD3	I	48	PCMEO	O
17	RPAD2	I	49	PCMEI	I
18	RPAD1	I	50	PCMI	I
19	DGND2	I	51	CLKSEL	I
20	TPAD4	I	52	BCLK	I/O
21	TPAD3	I	53	SYNC	I/O
22	TPAD2	I	54	$\overline{\text{RST}}$	I
23	TPAD1	I	55	$\overline{\text{PDN/RST}}$	I
24	MCK/X1	I	56	TEST8	I
25	X2	O	57	TEST4	I
26	AV_{DD}	I	58	TEST3	I
27	AGSX	O	59	TEST2	I
28	AIN	I	60	TEST1	I
29	AVFRO	O	61	SLPTHR	I
30	APWI	I	62	NCTHR	I
31	AOUT	O	63	DIN	I
32	SG	O	64	EXCK	I

PIN FUNCTIONAL DESCRIPTION

AIN, AGSX
These are the acoustic analog input and level adjusting pins. The AIN pin is connected to the inverting input of the internal amp and the AGSX pin is connected to the amp output. For level adjustment, refer to the diagram below (Figure 1). At power-down reset, the AGSX pin goes to a high impedance state.

AVFRO, AOUT, APWI
These are the acoustic analog output and level adjusting pins. The AVFRO pin is an audio output and can directly drive 20 kΩ. The AOUT pin is an analog output and can directly drive a load of 1.2 kΩ. For level adjustment, refer to the diagram below (Figure 1). At power-down reset, these output pins go to a high impedance state.

LIN, LGSX
These are the line analog input and level adjusting pins. The LIN pin is connected to the inverting input of the internal amp and the LGSX pin is connected to the amp output. For level adjustment, refer to the diagram below (Figure 1). At power-down reset, the LGSX pin goes to a high impedance state. If LIN is not used, short the LIN and LGSX pins together.

LVFRO, LOUT, LPWI
These are the line analog output and level adjusting pins. The LVFRO pin is an audio output and can directly drive 20 kΩ. The LOUT pin is an analog output and can directly drive a load of 1.2 kΩ. For level adjustment, refer to the diagram below (Figure 1). At power-down reset, these output pins go to a high impedance state. If LOUT is not used, short the LPWI and LOUT pins together.

$\overline{\text{LINEEN}}$
This is the power-down control pin for the line CODEC. A logic "0" continues normal operation and a logic "1" powers down only the line CODEC. If the line CODEC is not used, power down the line CODEC and short the LIN pin to the LGSX pin and the LPWI pin to the LOUT pin. This procedure results in the low consumption of electrical power. At power-down, the output pins go to a high impedance state. Since this pin is ORed with CR0-B5 of the control register, set the pin to a logic "0" when controlling power-down by the control register. If the pin setting is changed, reset must be activated by either the $\overline{\text{PDN}}$/$\overline{\text{RST}}$ pin or the PDN/RST bit (CR0-B7).

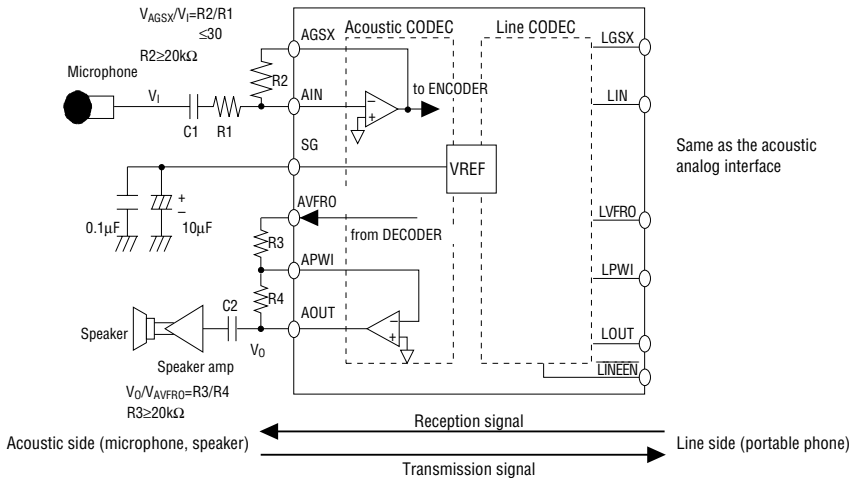


Figure 1 Analog Interface

AGND
This is the analog ground pin.

DGND1, DGND2
These are the digital ground pins.

AV_{DD}
This is the analog +3 V power supply pin.

DV_{DD1}, DV_{DD2}
These are the digital +3 V power supply pins.

SG
This is the output pin for the analog signal ground potential. The output voltage is approximately 1.4 V. Insert 10 µF and 0.1 µF ceramic bypass capacitors between the AGND and SG pins. At power-down reset, this output becomes 0 V.

$\overline{PDN}/\overline{RST}$
This is the power-down reset control input pin. If a logic "0" is input to this pin, the device enters the power-down state. At this time, all control register bits and internal variables will be reset. After the power-down reset state is released, the device enters the initial mode (refer to the CR0 control register description). During normal operation, set this pin to a logic "1". Since the $\overline{PDN}/\overline{RST}$ pin is ORed (negative logic) with CR0-B7 of the control register, set the pin to a logic "1" when controlling power-down reset by the control register.

MCK/X1
This is the master clock input pin. The clock frequency is 19.2 MHz. The input clock may be asynchronous with respect to the SYNC signal or the BCLK signal. Refer to Figure 2 (a) for an example application of an external clock and Figure 2 (b) for an example oscillator circuit.

X2
This is the crystal oscillator output pin. If an existing external clock is to be used, leave this pin open and input the clock to the MCK pin. Refer to Figure 2 (b) for an example oscillator circuit.

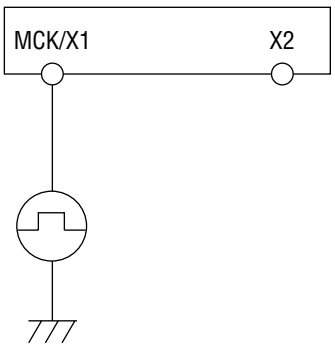


Figure 2 (a) External Clock Application Example

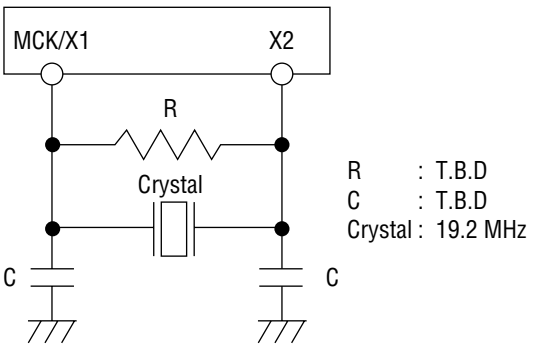


Figure 2 (b) Oscillator Circuit Example

SYNC
This is the 8 kHz sync signal I/O pin for digital data communication. This pin is switched to function as an input or output by the CLKSEL pin. If the internal clock mode is selected by the CLKSEL pin, an 8 kHz clock synchronized to the BCLK signal is output and digital data communication is performed. If the external clock mode is selected by the CLKSEL pin, this pin becomes an input that requires an 8 kHz clock input synchronized to the BCLK pin, and digital data communication is performed based on this input clock. Fixing this signal to a logic "1" or logic "0" causes this device to internally write a logic "1" to the PDN/RST (CR0-B7) bit of the control register, and to enter the power-down reset state. This automatic power-down control is valid when external clock mode is selected by the CLKSEL pin and automatic power-down control has been turned ON by the SYPDN (CR11-B0) bit of the control register.

BCLK
This is the shift clock I/O pin for digital data communication. This pin is switched to function as an input or output by the CLKSEL pin. If the internal clock mode is selected by the CLKSEL pin, a 64 kHz or 128 kHz clock synchronized to the SYNC signal is output and digital data communication is performed. Switching between 64 kHz and 128 kHz is performed by the PCMSEL pin. If μ-law PCM is selected by the PCMSEL pin, a 64 kHz clock is output. Or, if 16-bit linear mode is selected, a 128 kHz clock is output. If the external clock mode is selected by the CLKSEL pin, this pin becomes an input that requires a clock input synchronized to the SYNC. In this case, the clock frequency range is from 64 kHz to 2048 kHz.

CLKSEL
This pin selects internal or external clock modes for the SYNC and BCLK signals. A logic "0" selects the internal clock mode. At this time, SYNC and BCLK pins are configured as output pins and each internally generated clock is output to perform digital data communication. A logic "1" selects the external clock mode and configures the SYNC and BCLK pins as input pins. At this time, digital data communication is performed with the externally input SYNC and BCLK clocks. If digital data communication is not used, set this pin to a logic "0" to select internal clocks. If the pin setting is changed, reset must be activated by either the $\overline{\text{PDN}}/\overline{\text{RST}}$ pin or the PDN/RST bit (CR0-B7).

PCMI
This is the digital receive signal input pin on the line-side. This input signal is shifted at the rising edge of the BCLK signal and input. The beginning of digital data is identified on the rising edge of the SYNC signal. The coding format can be selected as μ-law PCM or 16-bit linear (2's complement) by the PCMSEL pin. If the PCMI pin is not used, set it to a logic "1" if μ-law PCM has been selected, or a logic "0" if 16-bit linear mode has been selected. The sync format can be selected as normal-sync or short-frame-sync by the SYNCSEL pin. Refer to Figure 3 for the timing. This digital input signal is added internally to the CODEC digital output signal. Be careful of overflow when using the CODEC.

PCMO
This is the digital transmit signal output pin on the line-side. This output signal is synchronized to the rising edge of the BCLK and SYNC signals and then output. When not used for output, this pin is in the high impedance state. It is also at high impedance during the power-down reset and the initial modes. The coding format can be selected as μ-law PCM or 16-bit linear (2's complement) by the PCMSEL pin. The sync format can be selected as normal-sync or short-frame-sync by the SYNCSEL pin. Refer to Figure 3 for the timing.

PCMEI

This is the message signal input pin. Use this pin when a message is output to the speaker on the acoustic-side. This input signal is shifted at the rising edge of the BCLK signal and then input. The beginning of digital data is identified on the rising edge of the SYNC signal. The coding format can be selected as μ-law PCM or 16-bit linear (2's complement) by the PCMSEL pin. If the PCMEI pin is not used, set it to a logic "1" if μ-law PCM has been selected, or a logic "0" if 16-bit linear mode has been selected. The sync format can be selected as normal-sync or short-frame sync by the SYNCSEL pin. Timing is the same as for the PCMI pin (refer to Figure 3). This digital input signal is added internally to the echo canceler output signal. Be careful of overflow during telephone conversations.

PCMEO

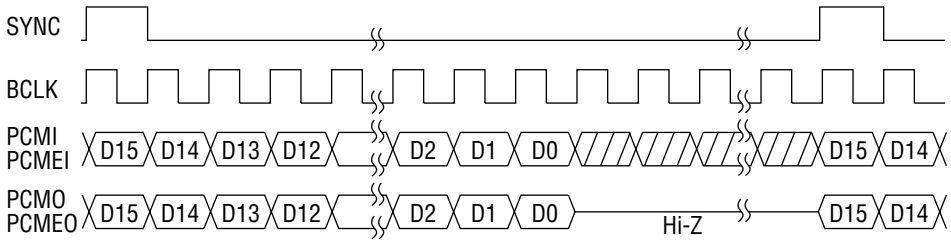
This output pin is for memo recording. Use it with the memo function. This output signal is synchronized to the rising edge of the BCLK and SYNC signals and then output. When not used for output, this pin is in the high impedance state. It is also at high impedance during the power-down reset and the initial modes. The coding format can be selected as μ-law PCM or 16-bit linear (2's complement) by the PCMSEL pin. The sync format can be selected as normal-sync or short-frame-sync by the SYNCSEL pin. Timing is the same as for the PCMO pin (refer to Figure 3).

SYNCSEL

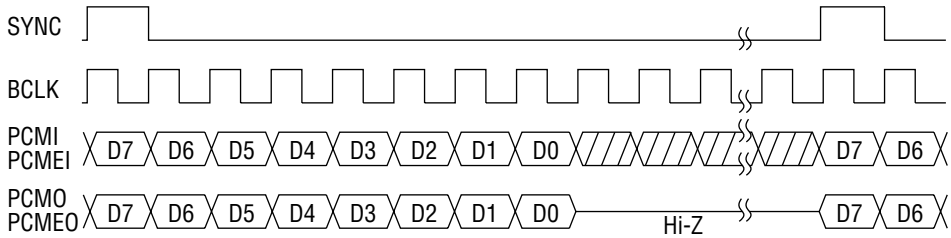
This is the sync timing selection pin for digital data communication. A logic "0" selects normal-sync timing and a logic "1" selects short-frame-sync timing. Refer to Figure 3 for the timing. If the pin setting is changed, reset must be activated by either the $\overline{\text{PDN}}/\overline{\text{RST}}$ pin or the PDN/RST bit (CR0-B7).

PCMSEL

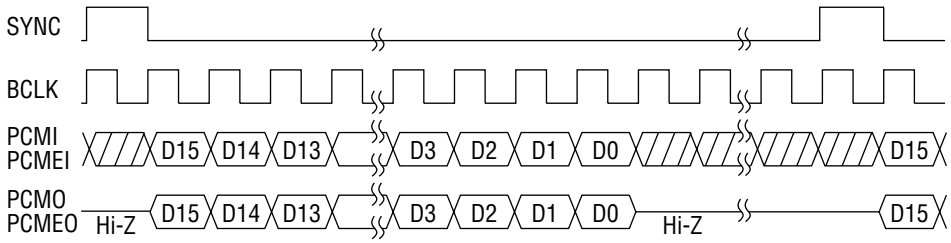
This is the coding format selection pin for digital data communication. A logic "1" selects μ-law PCM and a logic "0" selects 16-bit linear (2's complement) coding format. When an internal clock is selected, the BCLK signal determines the output clock frequency. If the digital interface is not used, set this pin to logic "0" to select 16-bit linear coding format.
Since this pin is logically ORed with the PCMSEL bit (CR11-B1), set the pin to a logic "0" when controlling by the control register.
If the pin setting is changed, reset must be performed by either the $\overline{\text{PDN}}/\overline{\text{RST}}$ pin or the PDN/RST bit (CR0-B7).



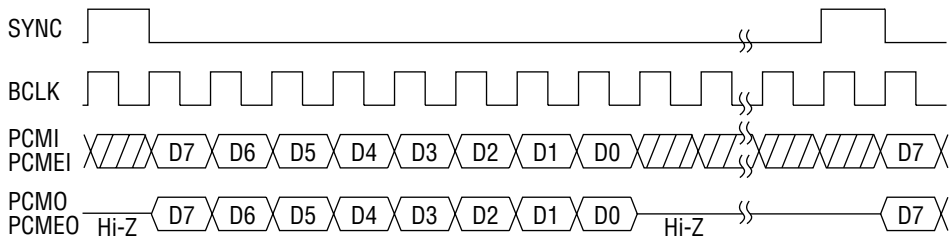
(a) 16-bit linear coding format timing (normal sync)



(b) μ-law PCM coding format timing (normal sync)



(c) 16-bit linear coding format timing (short-frame sync)



(c) μ-law PCM coding format timing (short-frame sync)

Figure 3 Digital Interface Timing

ECSEL
This is the echo canceler mode selection pin. A logic "1" selects the single echo canceler mode and a logic "0" selects the dual echo canceler mode. Since this pin is ORed with the CR0-B0 bit of the control register, set the pin to a logic "0" when controlling by the control register. If the pin setting is changed, reset must be activated by either the $\overline{PDN}/\overline{RST}$ pin or the PDN/RST bit (CR0-B7). If the single echo canceler mode is selected, echo canceler control on the line-side is unnecessary.

LTHR/ATHR
This is the "through mode" control pin for the echo canceler. In the "through mode", SinL/A and RinL/A data is directly output to SoutL/A and RoutL/A respectively while each respective echo coefficient is maintained. A logic "0" selects the normal mode (echo canceler operation) and a logic "1" selects the "through mode." Since this pin is ORed with the CR4-B7 and CR5-B7 bits of the control register, set the pin to a logic "0" when controlling the "through mode" by the control register. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer. For further details, refer to the electrical characteristics.

$\overline{LHD}/\overline{AHD}$
This pin turns ON or OFF the function to detect and cancel the howling that occurs in an acoustic system such as a handsfree communication system. A logic "0" turns the function ON and a logic "1" turns the function OFF. Since this pin is ORed with the CR4-B4 and CR5-B4 bits of the control register, set the pin to a logic "0" when controlling by the control register. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer. For further details, refer to the electrical characteristics.

LHLD/AHLD
This pin controls the updating of adaptive FIR filter coefficients for the echo canceler. A logic "0" selects the normal mode (coefficient updating) and a logic "1" selects the fixed coefficient mode. Since this pin is ORed with the CR4-B2 and CR5-B2 bits of the control register, set the pin to a logic "0" when controlling by the control registers. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer. For further details, refer to the electrical characteristics.

$\overline{LATT}/\overline{AATT}$
This pin turns ON or OFF the ATT function to prevent howling by means of attenuators (ATTsL/A, ATTrL/A) provided in the RinL/A inputs and SoutL/A outputs of the echo canceler. If input is only to RinL/A, the ATTsL/A for SoutL/A is activated. If input is only to SinL/A, or if there is input to both SinL/A and RinL/A, the ATTrL/A for RinL/A input is activated. The ATT value of each attenuator is approximately 6 dB. A logic "0" turns ON and a logic "1" turns OFF the ATT function. Since this pin setting is logically ORed with the CR4-B1 and CR5-B1 bits of the control register, set the pin to a logic "0" when controlling by the control register. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer. For further details, refer to the electrical characteristics.

$\overline{\text{LGC/AGC}}$

This pin turns ON or OFF the gain control function to control the input level and prevent howling by means of gain controls (GainL/A) provided in the RinL/A inputs of the echo canceler. The gain controller adjusts the RIN input level when it is –10 dBm0 or above, and it has the control range of 0 to –8.5 dB. A logic "0" turns the function ON and a logic "1" turns the function OFF. Since this pin is ORed with the CR4-B0 and CR5-B0 bits of the control register, set the pin to a logic "0" when controlling by the control register. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer. For further details, refer to the electrical characteristics.

Notes:

Lxx/Axx: In the above, Lxx refers to line echo canceler control pins and Axx to acoustic echo canceler control pins.

xxL/xxA: In the above pin descriptions, xxL refers to line echo canceler functions and xxA to acoustic echo canceler functions.

$\overline{\text{GLPADTHR}}$

This is the mode control pin for the attenuators (LPADL/A) provided in the SinL/A inputs and the amplifiers (GPADL/A) provided in the SoutL/A outputs of the echo canceler. A logic "0" selects the "through mode" and a logic "1" selects the normal mode (PAD operation). The levels are set by the CR10 register. Settings of ±18, ±12, ±6 and 0 dB are possible. The default setting is ±12 dB. If the echo return loss (value of returned echo) is amplified, set the LPAD level such that echo return loss will be attenuated. It is recommended to set the GPAD level to the positive level equal to the LPAD level. Since this pin is ORed with the CR1-B2 bit of the control register, set the pin to a logic "0" when controlling by the control register. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer. For further details, refer to the electrical characteristics.

NCTHR

This is the noise canceler "through mode" control pin. In the "through mode" the noise canceler is halted and data is directly output. A logic "0" selects the normal mode (noise canceler operation) and a logic "1" selects the "through mode". Since this pin is ORed with the CR1-B0 bit of the control register, set the pin to a logic "0" when controlling by the control register. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer. For further details, refer to the electrical characteristics. When this pin is changed from normal mode to "through mode", approximately 20 ms of data dropout will occur.

SLPTHR

This is the "through mode" control pin for the transmit slope filter. In the "through mode", the filter is halted and data is directly output. A logic "0" selects the normal mode (slope filter operation) and a logic "1" selects the "through mode". Since this pin is ORed with the CR1-B1 bit of the control register, set the pin to a logic "0" when controlling by the control register. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer. For further details, refer to the electrical characteristics.

$\overline{\text{RST}}$

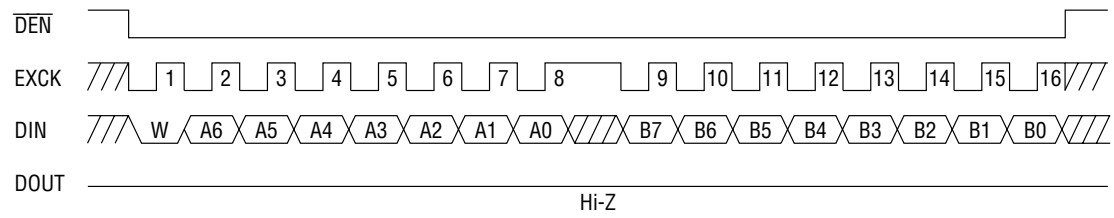
This input pin resets coefficients of the echo canceler and noise canceler. A logic "0" causes the reset state to be entered. At this time, the filter coefficients for the echo canceler and noise canceler are reset. Control register contents are preserved. While reset is being processed, there is no sound. During normal operation, set this pin to a logic "1". Since this pin is ORed (negative logic) with the CR0-B6 bit of the control register, set the pin to a logic "1" when controlling by the control register. Use this pin in cases where the echo path changes (due to line switching during a telephone conversation, etc.), or when resuming telephone communication. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer.
For further details, refer to the electrical characteristics.

$\overline{\text{DEN}}$, EXCK, DIN, DOUT

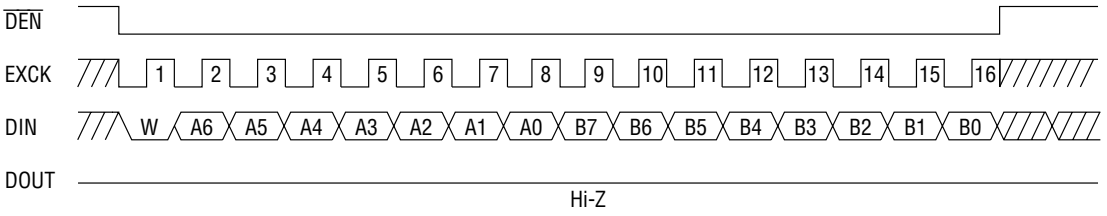
This is the serial port for the microcomputer interface. 13 bytes of control registers are provided in this LSI device. These pins are used to write and read data from an external microcomputer. The $\overline{\text{DEN}}$ pin is an enable signal input pin, the EXCK pin is a clock signal input pin for data shifting, the DIN pin is an address and data input pin, and the DOUT pin is a data output pin. If the microcomputer interface is not used, set the $\overline{\text{DEN}}$ pin to a logic "1" and the EXCK and DIN pins to a logic "0". In addition, use the MCUSEL pin to specify the "unused" setting of the microcomputer interface. Figure 4 shows the input timing.

MCUSEL

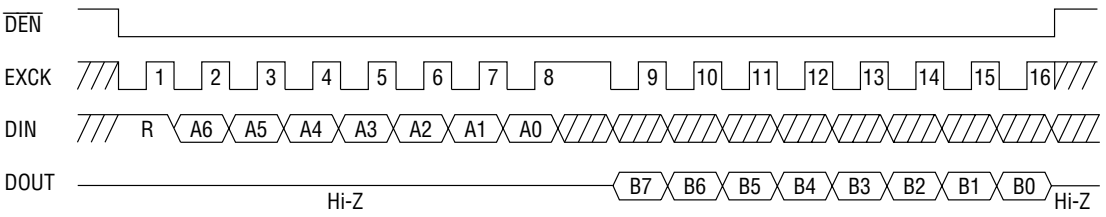
This pin selects whether the microcomputer interface is used or unused. A logic "0" specifies that the microcomputer interface is used and a logic "1" specifies that it is not used. If the microcomputer interface is not used, this pin must be set to a logic "1". This pin is ORed with the CR0-B1 bit of the control register.



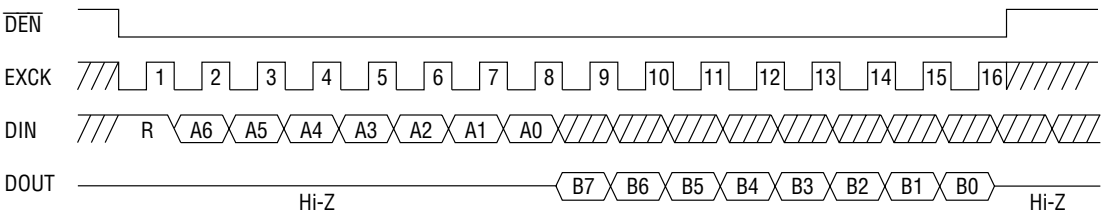
(a) Data Write Timing 1 (8-Bit MCU)



(b) Data Write Timing 2 (16-Bit MCU)



(c) Data Read Timing 1 (8-Bit MCU)



(d) Data Read Timing 2 (16-Bit MCU)

Figure 4 Microcomputer Interface I/O Timing

RPAD4, RPAD3, RPAD2, RPAD1
These are the receive signal gain adjusting and mute setting pins. Refer to Table 1 for the settings. Set these pins to a logic "0" when controlling by the control register. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer. For further details, refer to the electrical characteristics.

TPAD4, TPAD3, TPAD2, TPAD1
These are the transmit signal gain adjusting and mute setting pins. Refer to Table 1 for the settings. Set these pins to a logic "0" when controlling by the control register. Because data is shifted into this pin in synchronization with the rising edge of the SYNC signal, hold the data at the pin for 250 µs or longer. For further details, refer to the electrical characteristics.

Table 1 RPAD/TPAD Settings

RPAD4	RPAD3	RPAD2	RPAD1	TPAD4	TPAD3	TPAD2	TPAD1	Level
0	1	1	1	0	1	1	1	21 dB
0	1	1	0	0	1	1	0	18 dB
0	1	0	1	0	1	0	1	15 dB
0	1	0	0	0	1	0	0	12 dB
0	0	1	1	0	0	1	1	9 dB
0	0	1	0	0	0	1	0	6 dB
0	0	0	1	0	0	0	1	3 dB
0	0	0	0	0	0	0	0	0 dB
1	1	1	1	1	1	1	1	–3 dB
1	1	1	0	1	1	1	0	–6 dB
1	1	0	1	1	1	0	1	–9 dB
1	1	0	0	1	1	0	0	–12 dB
1	0	1	1	1	0	1	1	–15 dB
1	0	1	0	1	0	1	0	–18 dB
1	0	0	1	1	0	0	1	–21 dB
1	0	0	0	1	0	0	0	MUTE

TEST1-4, 8
Test inputs. Set these pins to a logic "0".

TEST9
Test output.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +5.0	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD}+0.3	V
Digital Output Voltage	V_{OUT}	—	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply voltage	V_{DD}	—	2.7	—	3.6	V
Operating Temperature	Ta	—	–40	+25	+85	°C
Input High Voltage	V_{IH}	SYNC, BCLK input pins	0.5×V_{DD}	—	V_{DD}	V
		MCK/X1 input pin	0.65×V_{DD}			
		Other digital input pins	0.45×V_{DD}			
Input Low Voltage	V_{IL}	MCK/X1 input pin	0	—	0.35×V_{DD}	V
		Other digital input pins			0.16×V_{DD}	
Digital Input Rise Time	t_{IR}	All digital inputs	—	—	20	ns
Digital Input Fall Time	t_{If}	All digital inputs	—	—	20	ns
Master Clock Frequency	F_{MCK}	MCK/X1	–100 ppm	+19.2	+100 ppm	MHz
Master Clock Duty Ratio	D_{MCK}	MCK/X1	40	50	60	%
Bit Clock Frequency	F_{BCK}	BCLK (during input)	64	—	2048	kHz
Bit Clock Duty Ratio	D_{CK}	BCLK (during input)	40	50	60	%
Synchronous Signal Frequency	F_{SYNC}	SYNC (during input)	–100 ppm	8	+100 ppm	kHz
Synchronous Signal Width	t_{WS}	SYNC (during input)	1 BCLK	—	100	µs
Transmit/Receive Sync Signal	t_{BS}	BCLK to SYNC (during input)	100	—	—	ns
Setting Time	t_{SB}	SYNC to BCLK (during input)	100	—	—	ns
Digital Output Load	R_{DL}	DOUT, PCMO, PCMEO	1	—	—	kΩ
	C_{DL1}	DOUT, PCMO, PCMEO	—	—	50	pF
	C_{DL2}	SYNC, BCLK (during output)	—	—	20	pF
Bypass Capacitor for SG	C_{SG}	SG to AG	10+0.1	—	—	µF

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 2.7 V to 3.6 V Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current 1	I_{DD1}	Operating, no signal (V_{DD} = 3.0 V)	—	35	45	mA
Power Supply Current 2	I_{DD2}	Power down mode (V_{DD} = 3.0 V, MCK = 0 V)	—	0.1	1	mA
Input Leakage Current	I_{IH}	$V_I = V_{DD}$	—	—	2	µA
	I_{IL}	V_I = 0 V	—	—	2	µA
High Level Digital Output Voltage	V_{OH}	I_{OH} = 0.4 mA	0.5×V_{DD}	—	V_{DD}	V
Low Level Digital Output Voltage	V_{OL}	I_{OL} = 3.2 mA	0	0.2	0.4	V
Digital Output Leakage Current	I_O	DOUT, PCMO, PCMEO	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF

Analog Interface

(V_{DD} = 2.7 V to 3.6 V Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{INA}	AIN, APWI		10	—	—	MΩ
	R_{INL}	LIN, LPWI		10	—	—	MΩ
Output Load Resistance	R_{LA1}	AGSX, AVFRO		20	—	—	kΩ
	R_{LA2}	AOUT		1.2	—	—	kΩ
	R_{LL1}	LGSX, LVFRO		20	—	—	kΩ
	R_{LL2}	LOUT		1.2	—	—	kΩ
Output Load Capacitance	C_{LA1}	AGSX, AVFRO, AOUT		—	—	100	pF
	C_{LL1}	LGSX, LVFRO, LOUT		—	—	100	pF
Output Voltage Level (*1)	V_{OA1}	AGSX, AVFRO	R_L = 20 kΩ	—	—	1.3	Vpp
	V_{OA2}	AOUT	R_L = 1.2 kΩ	—	—	2.6	Vpp
	V_{OL1}	LGSX, LVFRO	R_L = 20 kΩ	—	—	1.3	Vpp
	V_{OL2}	LOUT	R_L = 1.2 kΩ	—	—	2.6	Vpp
Offset Voltage	V_{OFA1}	AVFRO		–100	—	+100	mV
	V_{OFA2}	AOUT		–20	—	+20	mV
	V_{OFL1}	AVFRO		–100	—	+100	mV
	V_{OFL2}	LOUT		–20	—	+20	mV
SG Output Voltage	V_{SG}	SG		—	1.4	—	V
SG Output Impedance	R_{SG}	SG		—	40	80	kΩ

*1 0.320 Vrms = 0 dBm0, +3.14 dBm0 = 1.30 Vpp

Digital Interface

(V_{DD} = 2.7 V to 3.6 V Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-down Reset Signal Pulse Width	t_{RSTW}	$\overline{PDN}/\overline{RST}$ pin	1	—	—	µs
		PDN/RST control bit	1.6			
Power-down Reset Start Time	t_{PDND}	$\overline{PDN}/\overline{RST}$ pin and PDN/RST control bit	—	—	50	ns
Power-down Reset End Time	t_{PDNH}	$\overline{PDN}/\overline{RST}$ pin and PDN/RST control bit	—	—	200+α (*2)	ms
Power-down Reset Internal Setting Time	t_{PDNS}	SYNC pin (input mode)	140	—	180	µs
Control Pulse Width	t_{PARW}	(*3)	250	—	—	µs
Control Start Time	t_{PARD}		—	—	250	µs
Control End Time	t_{PARH}		—	—	250	µs
Bit Clock Frequency	F_{BCK}	C_{DL} = 20 pF (output mode, PCM)	—	64	—	kHz
		C_{DL} = 20 pF (output mode, linear)	—	128	—	kHz
Bit Clock Duty Ratio	D_{CK}	C_{DL} = 20 pF (output mode)	40	50	60	%
Synchronous Signal Frequency	F_{SYNC}	C_{DL} = 20 pF (output mode)	—	8	—	kHz
Sync Signal Duty Ratio	D_{SYNC}	C_{DL} = 20 pF (output mode)	40	50	60	%
Transmit/Receive Sync Signal Setting Time	t_{BS}	BCLK to SYNC (output mode)	100	—	—	ns
	t_{SB}	SYNC to BCLK (output mode)	100	—	—	ns
Input Setup Time	t_{DS}	—	100	—	—	ns
Input Hold Time	t_{DH}	—	100	—	—	ns
Digital Output Delay Time	t_{SDX}	R_{DL} = 1 kΩ, C_{DL} = 50 pF	—	—	100	ns
	t_{XD1}	R_{DL} = 1 kΩ, C_{DL} = 50 pF	—	—	100	ns
	t_{XD2}	R_{DL} = 1 kΩ, C_{DL} = 50 pF	—	—	100	ns
	t_{XD3}	R_{DL} = 1 kΩ, C_{DL} = 50 pF	—	—	100	ns
MCU Interface Digital Input/Output Setting Timing	t_{M1}		20	—	—	ns
	t_{M2}		20	—	—	ns
	t_{M3}		50	—	—	ns
	t_{M4}		100	—	—	ns
	t_{M5}		50	—	—	ns
	t_{M6}		50	—	—	ns
	t_{M7}	R_{DL} = 1 kΩ, C_{DL} = 20 pF	—	—	30	ns
	t_{M8}		0	—	—	ns
	t_{M9}		50	—	—	ns
	t_{M10}	R_{DL} = 1 kΩ, C_{DL} = 20 pF	—	—	30	ns
	t_{M11}		100	—	—	ns
EXCK Clock Frequency	f_{ECK}		—	—	10	MHz

*2 α : Crystal activation time

*3 Applies to the following pins/control bits:
$\overline{LINEEN}$, SLPTHR, NCTHR, $\overline{GLPADTHR}$, TPAD6-1, RPAD6-1, $\overline{RST}$, ATHR, $\overline{AATT}$, AHLD, $\overline{AHD}$, $\overline{AGC}$, LTHR, $\overline{LATT}$, LHLD, $\overline{LHD}$, and $\overline{LGC}$

AC Characteristics (Line CODEC/Acoustic CODEC)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)	Others				
Transmit Frequency Response	L_{OSS} T1	0 to 60	0	—	25	—	—	dB
	L_{OSS} T2	300 to 3000			–0.15	—	+0.20	dB
	L_{OSS} T3	1020			Reference			dB
	L_{OSS} T4	3300			–0.15	—	+0.80	dB
	L_{OSS} T5	3400			0	—	0.80	dB
	L_{OSS} T6	3968.75			13	—	—	dB
Receive Frequency Response	L_{OSS} R1	0 to 3000	0	—	–0.15	—	+0.20	dB
	L_{OSS} R2	1020			Reference			dB
	L_{OSS} R3	3300			–0.15	—	+0.80	dB
	L_{OSS} R4	3400			0	—	0.80	dB
	L_{OSS} R5	3968.75			13	—	—	dB
Transmit Signal to Distortion Ratio	SD T1	1020	3	(*4)	35	—	—	dB
	SD T2		0		35	—	—	dB
	SD T3		–30		35	—	—	dB
	SD T4		–40		28	—	—	dB
	SD T5		–45		23	—	—	dB
Receive Signal to Distortion Ratio	SD R1	1020	3	(*4)	35	—	—	dB
	SD R2		0		35	—	—	dB
	SD R3		–30		35	—	—	dB
	SD R4		–40		28	—	—	dB
	SD R5		–45		23	—	—	dB
Transmit Gain Tracking	GT T1	1020	3	—	–0.2	—	+0.2	dB
	GT T2		–10		Reference			dB
	GT T3		–40		–0.2	—	+0.2	dB
	GT T4		–50		–0.5	—	+0.5	dB
	GT T5		–55		–1.2	—	+1.2	dB
Receive Gain Tracking	GT R1	1020	3	—	–0.2	—	+0.2	dB
	GT R2		–10		Reference			dB
	GT R3		–40		–0.2	—	+0.2	dB
	GT R4		–50		–0.5	—	+0.5	dB
	GT R5		–55		–1.2	—	+1.2	dB
Idle Channel Noise	N_{IDLT}	—	—	(*4)	—	—	–68 (–75.7)	dBm0p (dBmp)
	N_{IDLR}	—	—	(*4)	—	—	–72 (–79.7)	
Absolute Signal Amplitude	A_{VT}	1020	0	A/LGSX	0.285	0.320	0.359	Vrms
	A_{VR}			A/LVFRO	0.285	0.320	0.359	Vrms
Power Supply Noise Rejection Ratio	P_{SRRT}	Noise Freq.: 0 to 50 kHz	Noise Level: 50 mV_{PP}	—	30	—	—	dB
	P_{SRRR}				30	—	—	dB

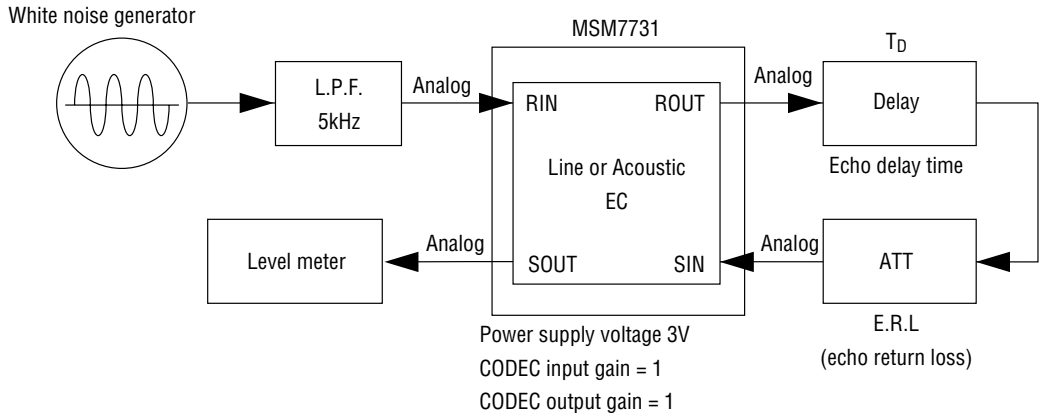
*4 P-message weighted filter used
0.320 Vrms = 0 dBm0 = –7.7 dBm

Echo Canceler Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo Attenuation	Eres	Acoustic side Line side (when CODEC or 16-bit linear data interface is used)	—	35	—	dB
		Line side (μ-law PCM used)		30		
Cancelable Echo Delay Time	Tacoud	Single mode	—	—	59	ms
	Tacoud	Dual mode (acoustic side)	—	—	59–Tlined	ms
	Tlined	Dual mode (line side)	—	—	27	ms

Measurement System Block Diagram

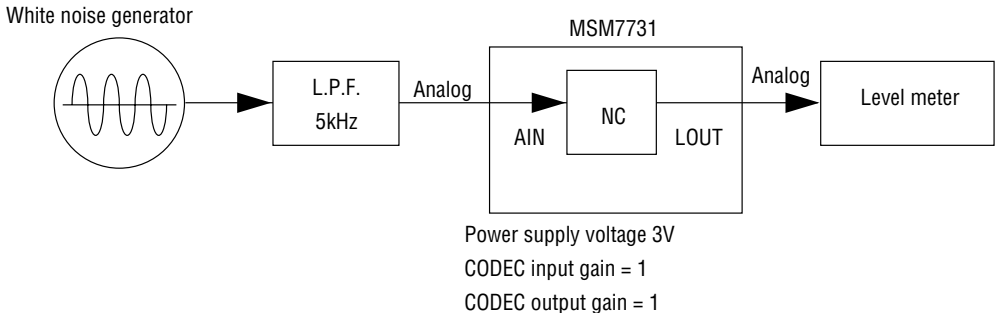


Noise Canceler Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

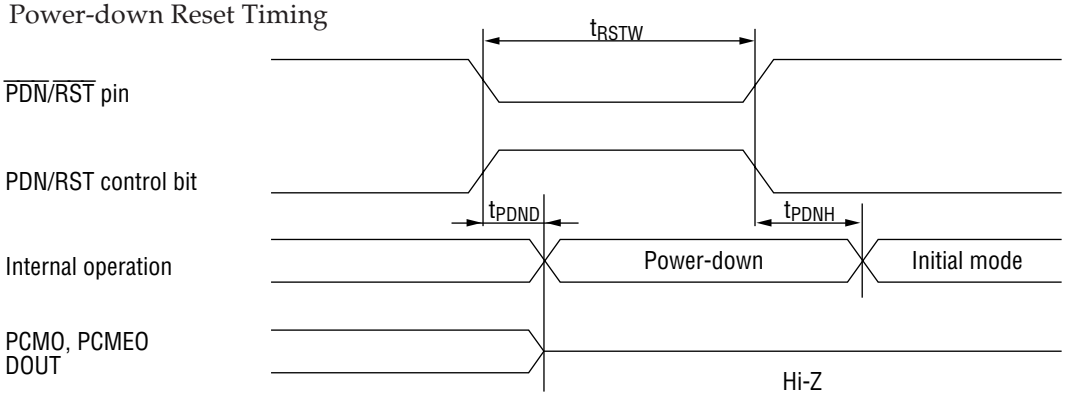
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Noise Attenuation	Nres	White noise, voice band	—	13	—	dB

Measurement System Block Diagram

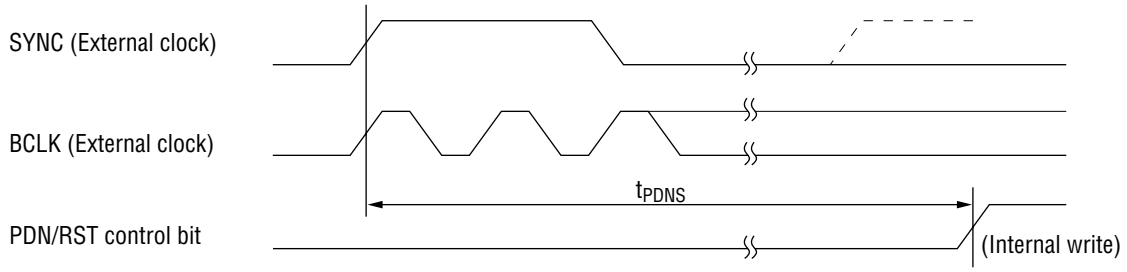


TIMING DIAGRAM

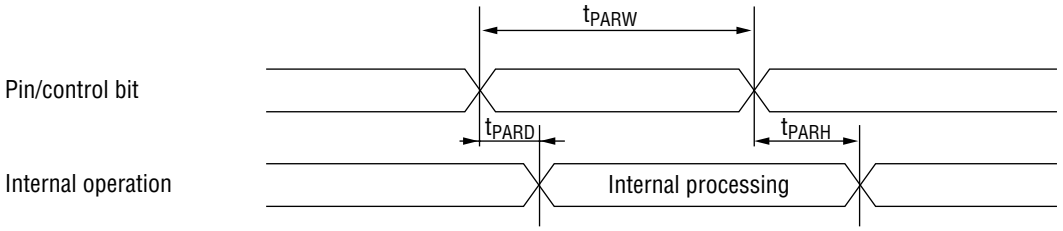
Power-down Reset Timing



Power-down Reset Setting Timing

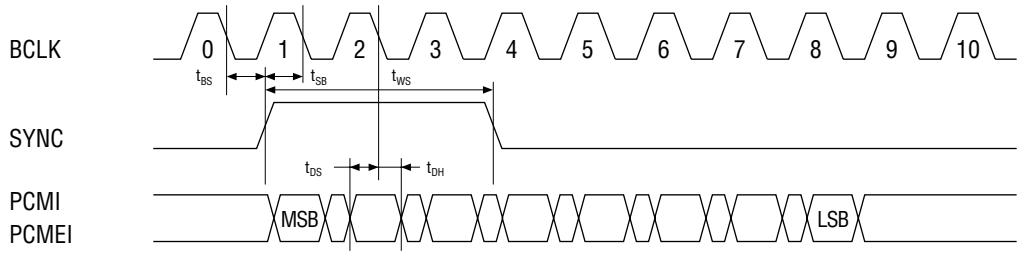


Control Timing

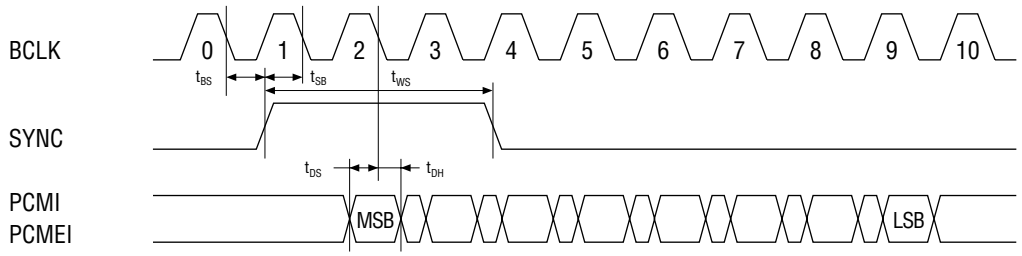


Note: Applies to the following pins/control bits:
$\overline{\text{LINEEN}}$, SLPTHR, NCTHR, $\overline{\text{GLPADTHR}}$, TPAD6-1, RPAD6-1, $\overline{\text{RST}}$, ATHR, $\overline{\text{AATT}}$, AHLD, $\overline{\text{AHD}}$, $\overline{\text{AGC}}$, LTHR, $\overline{\text{LATT}}$, LHLD, $\overline{\text{LHD}}$, and $\overline{\text{LGC}}$

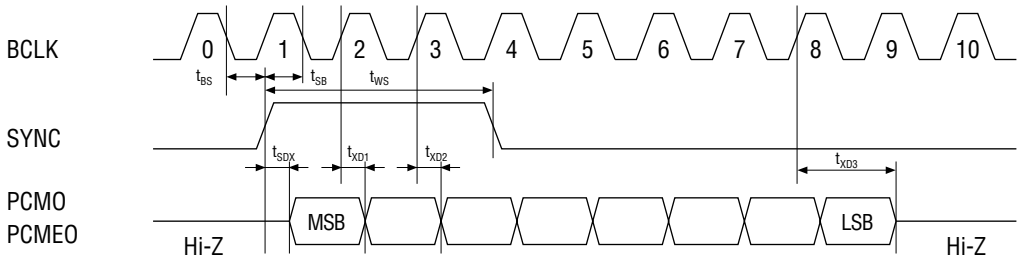
Digital Input Timing (Normal-sync)



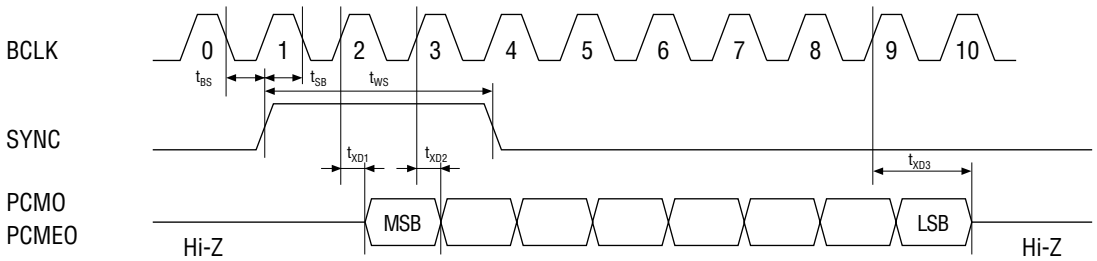
Digital Input Timing (Short-frame-sync)



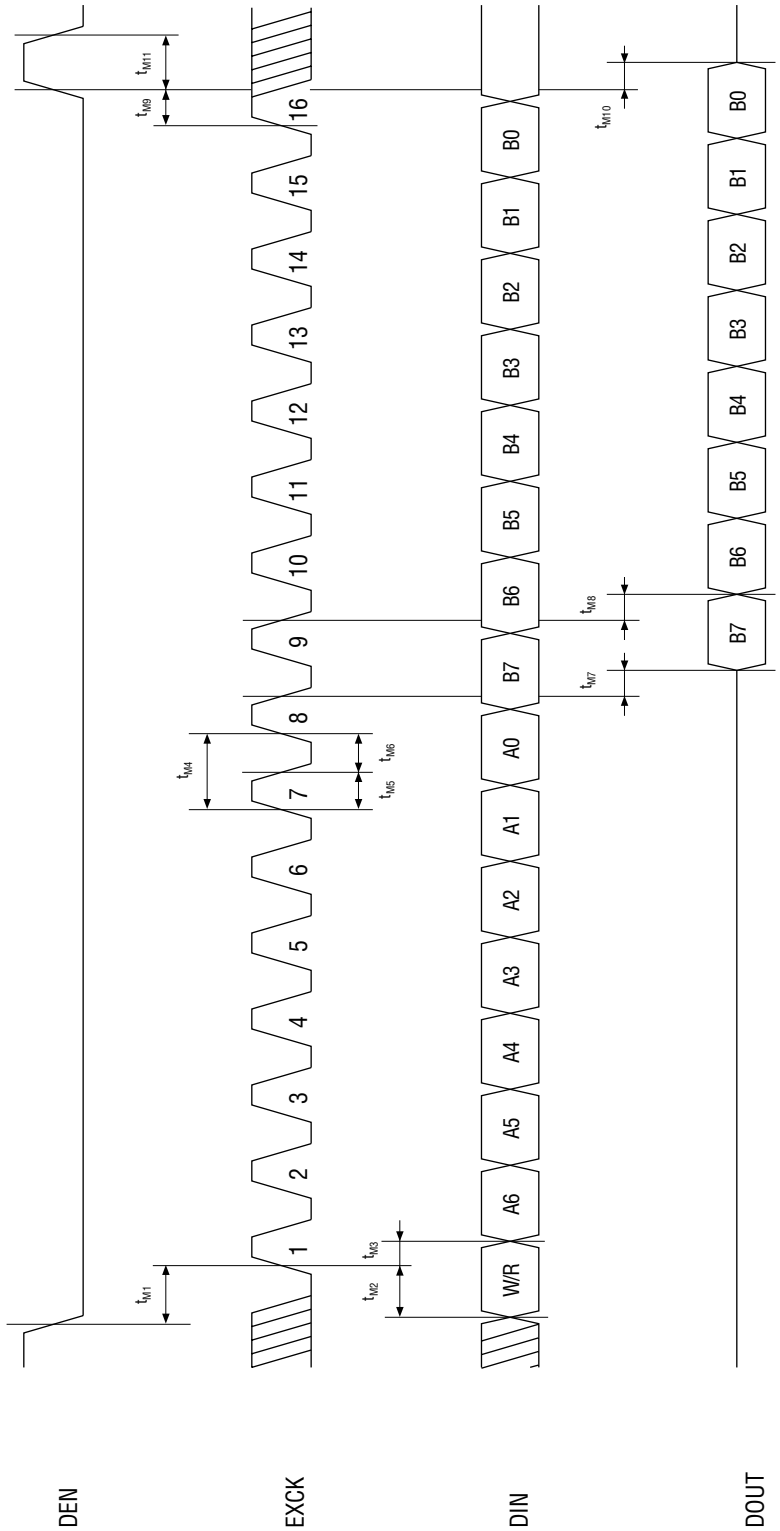
Digital Output Timing (Normal-sync)



Digital Output Timing (Short-frame-sync)

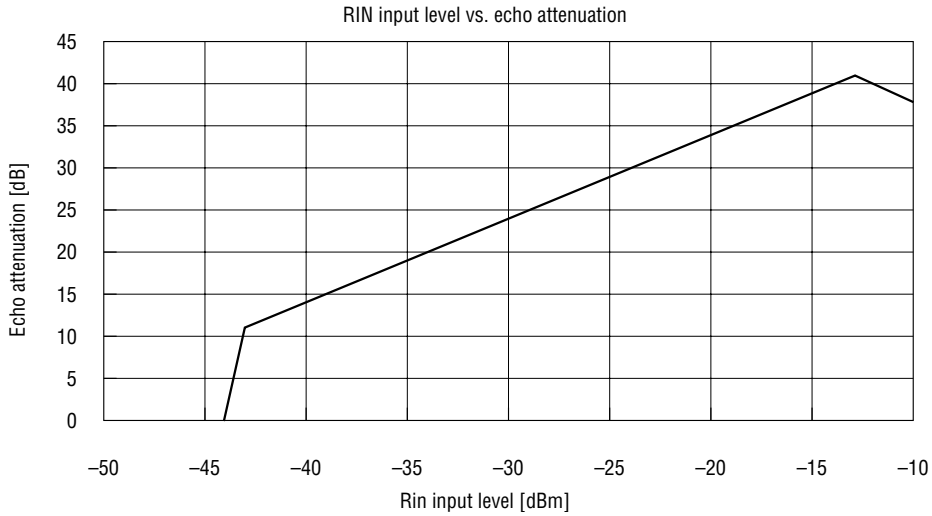


Microcomputer Interface I/O Timing



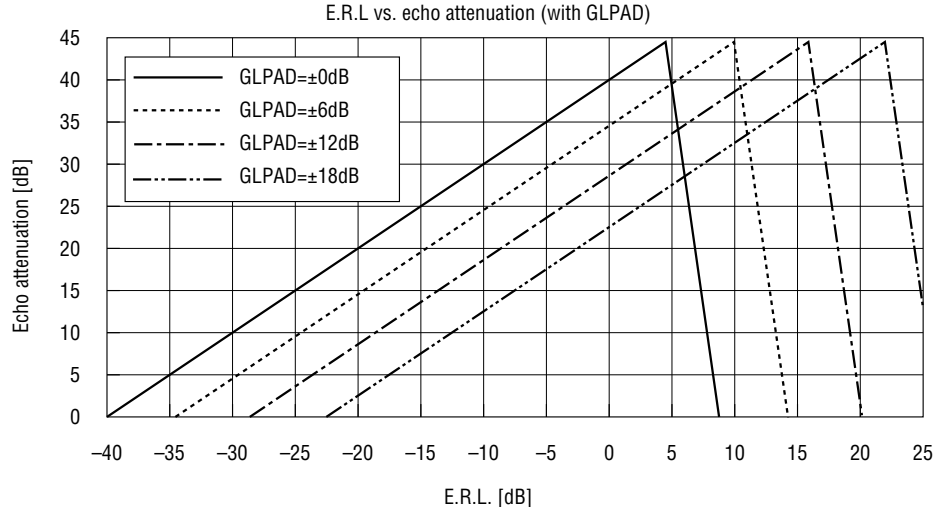
Rin input level vs. echo attenuation

(Measuring conditions) Rin signal : 5 kHz band white noise
E.R.L : –6dB
Delay time : 4ms
ATT, GC : OFF
Noise floor : –60dBm (P-message filter unused)



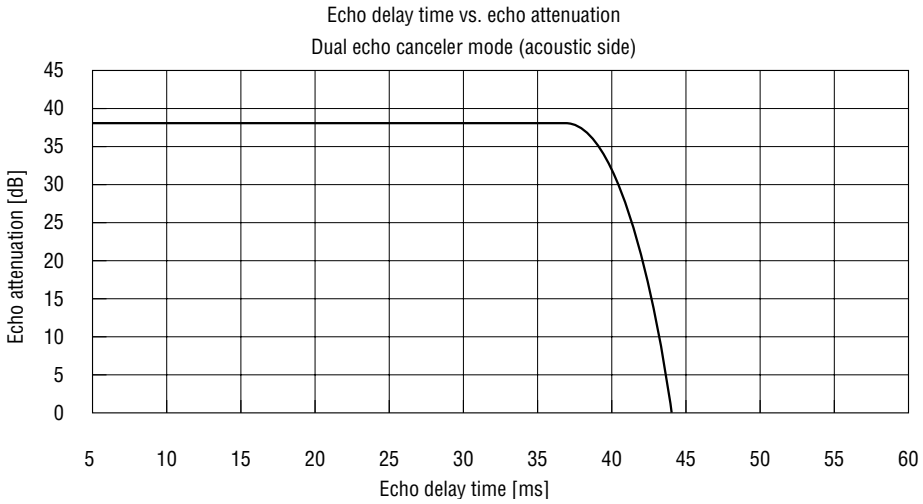
E.R.L. level vs. echo attenuation (with GLPAD)

(Measuring conditions) Rin signal : 5 kHz band white noise
Rin input level : –20dBm (with GLPAD=±0dB)
: –26dBm (with GLPAD=±6dB)
: –32dBm (with GLPAD=±12dB)
: –38dBm (with GLPAD=±18dB)
Delay time : 4ms
ATT, GC : OFF
Noise floor : –60dBm (P-message filter unused)



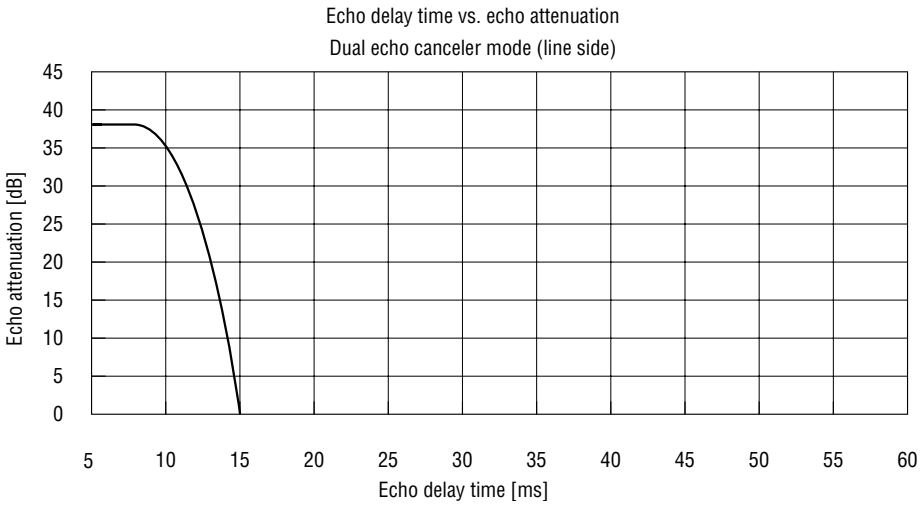
Echo delay time vs. echo attenuation (Dual echo canceler mode/acoustic side)

(Measuring conditions) Rin signal : 5 kHz band white noise
Rin input level : –16dBm
E.R.L : –6dB
ATT, GC : OFF
Noise floor : –60dBm (P-message filter unused)



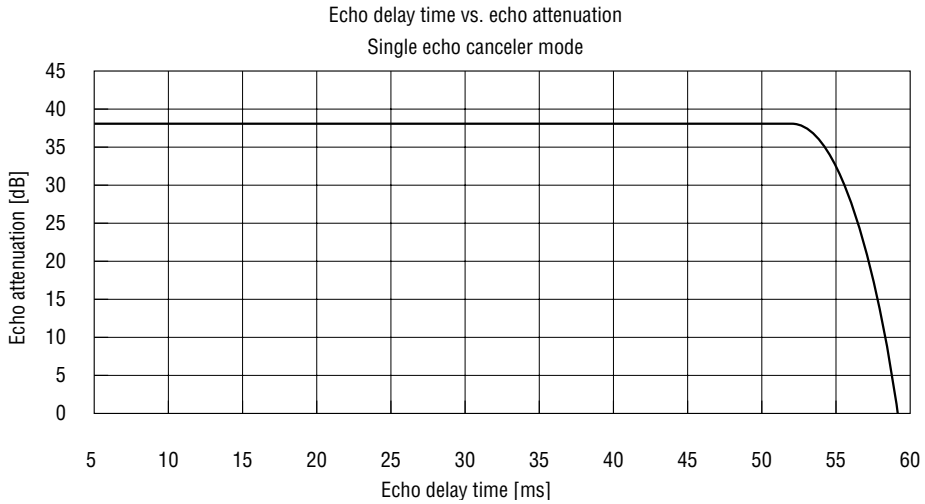
Echo delay time vs. echo attenuation (Dual echo canceler mode/line side)

(Measuring conditions) Rin signal : 5 kHz band white noise
Rin input level : –16dBm
E.R.L : –6dB
ATT, GC : OFF
Noise floor : –60dBm (P-message filter unused)



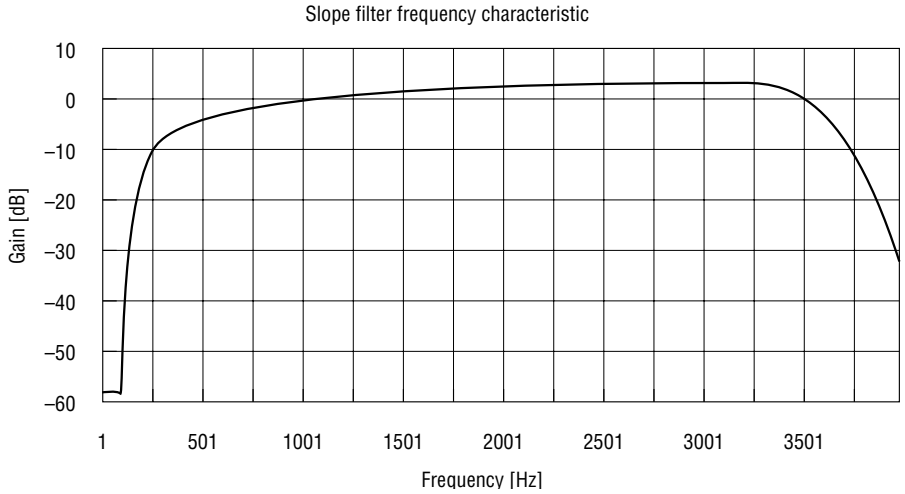
Echo delay time vs. echo attenuation (Single echo canceler mode)

(Measuring conditions) Rin signal : 5 kHz band white noise
Rin input level : –16dBm
E.R.L : –6dB
ATT, GC : OFF
Noise floor : –60dBm (P-message filter unused)



Slope filter frequency characteristic (with CODEC frequency characteristic)

(Measuring conditions) Rin input level : –16dBm
Noise floor : –60dBm (P-message filter unused)



Echo Canceler Characteristics Data 1 (Line Echo, White Noise)

(Measuring conditions) Rin signal : 5 kHz band white noise
Rin input level : –20dBm
E.R.L : 0dB
ATT, GC : OFF
Noise floor : –60dBm (P-message filter unused)
Echo attenuation=40dB

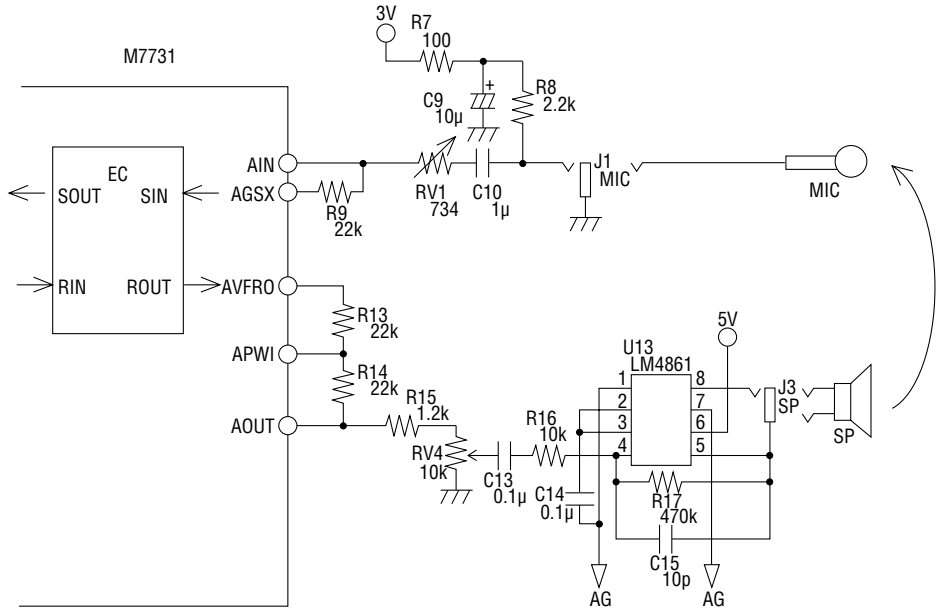
Echo Canceler Characteristics Data 2 (Line Echo, Voice)

(Measuring conditions) Rin signal : Voice
Rin input level : about –20dBm
E.R.L : 0dB
ATT, GC : OFF
Noise floor : –60dBm (P-message filter unused)
Echo attenuation=34dB

Echo Canceler Characteristics Data 3 (Acoustic Echo, Voice)

(Measuring conditions) Rin signal : Voice
Rin input level : about –20dBm
Speaker output level : 80dBa (at 1m)
Distance from microphone and speaker : 5cm
GC : OFF
ATT, Noise Canceller : ON
Noise floor : –60dBm (P-message filter unused)
Echo attenuation=34dB

Measurement System Block Diagram (Acoustic Echo)



FUNCTIONAL DESCRIPTION

Control Registers

Table 2 Control Register Map

Reg	Address							Contents								R/W
Name	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	0	0	0	0	*PDN/RST	*RST	*$\overline{\text{LINEEN}}$	$\overline{\text{CLKEN}}$	$\overline{\text{PCMEN}}$	$\overline{\text{PCMEEN}}$	OPE *MCUSEL	OPE *ECSEL	R/W
CR1	0	0	0	0	0	0	1	DMWR	—	—	—	—	*$\overline{\text{GLPADTHR}}$	*SLPTHR	*NCTHR	R/W
CR2	0	0	0	0	0	1	0	—	—	RPAD6	RPAD5	RPAD4	RPAD3	RPAD2	RPAD1	R/W
CR3	0	0	0	0	0	1	1	—	—	TPAD6	TPAD5	TPAD4	TPAD3	TPAD2	TPAD1	R/W
CR4	0	0	0	0	1	0	0	*LTHR	—	—	*$\overline{\text{LHD}}$	LCLP	*LHLD	*$\overline{\text{LATT}}$	*$\overline{\text{LGC}}$	R/W
CR5	0	0	0	0	1	0	1	*ATHR	—	—	*$\overline{\text{AHD}}$	ACLP	*AHLD	*$\overline{\text{AATT}}$	*$\overline{\text{AGC}}$	R/W
CR6	0	0	0	0	1	1	0	A15	A14	A13	A12	A11	A10	A9	A8	R/W
CR7	0	0	0	0	1	1	1	A7	A6	A5	A4	A3	A2	A1	A0	R/W
CR8	0	0	0	1	0	0	0	D15	D14	D13	D12	D11	D10	D9	D8	R/W
CR9	0	0	0	1	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	R/W
CR10	0	0	0	1	0	1	0	GPADA2	GPADA1	LPADA2	LPADA1	GPADL2	GPADL1	LPADL2	LPADL1	R/W
CR11	0	0	0	1	0	1	1	READY	—	—	—	—	—	PCMSEL	SYPDN	R/W
CR12	0	0	0	1	1	0	0	—	—	—	—	—	—	—	—	R/W

*: Shared control bit with port (pin)
—: Reserved bit. Do not change the initial value ("0").

(1) CR0 (basic operating mode settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	PDN/RST	RST	$\overline{\text{LINEEN}}$	$\overline{\text{CLKEN}}$	$\overline{\text{PCMEN}}$	$\overline{\text{PCMEEN}}$	OPE MCUSEL	OPE ECSEL
Initial value (*4)	0	0	0	0	0	0	0	0

Note: *4. Initial values are the values set when reset is activated by the $\overline{\text{PDN}}$/$\overline{\text{RST}}$ pin. (Initial values are also set in the same manner, except for CR0-B7, when reset by the PDN/RST bit of B7).

B7 ..... Power-down reset 0: power-on, 1: power-down reset
During power-down reset, this device enters the power-down state. At this time, all control register bits and internal variables are reset. After power-down reset is released, this device enters the initial mode. This bit is internally ORed with the inverted $\overline{\text{PDN}}$/$\overline{\text{RST}}$ signal.

B6 ..... Reset control 0: normal operation, 1: reset
At reset, the coefficients for the echo canceler and noise canceler are reset. Control register contents are preserved. While reset is being processed, there is no sound. Use this bit in cases where the echo path changes (due to line switching during a telephone conversation, etc.), or when resuming telephone communicaion. This bit is internally ORed with the inverted $\overline{\text{RST}}$ signal.

B5 ..... Line CODEC I/O control 0: ON, 1: OFF
When OFF, the line CODEC is in the power-down state, the line CODEC output pin is at high impedance and line CODEC input pin is internally processed as an idle pattern input. This bit is internally ORed with the $\overline{\text{LINEEN}}$ pin. When the line CODEC is not used, this control results in low consumption of electrical power.
This bit can only be set to "0" or "1" during power-down reset and the initial mode.

B4 ..... SYNC, BCLK output control 0: ON, 1: OFF
When OFF, the SYNC and BCLK output pins are in the high impedance state. This control is valid when the CLKSEL pin is at a logic "0" and has selected the internal clock mode. When the SYNC and BCLK clocks are not used externally, this control results in low consumption of electrical power.
This bit can only be set to "0" or "1" during power-down reset and the initial mode.

B3 ..... PCM I/O control 0: ON, 1: OFF
When OFF, the PCMO output pin is in the high impedance state and the PCMI input pin is internally processed as an idle pattern input. When the line digital interface is not used, this control results in low consumption of electrical power.
This bit can only be set to "0" or "1" during power-down reset and the initial mode.

B2 ..... PCME I/O control 0: ON, 1: OFF
When OFF, the PCMEO output pin is in the high impedance state and the PCMEI input pin is internally processed as an idle pattern input. When not used for message output and memo recording, this control results in low consumption of electrical power.
This bit can only be set to "0" or "1" during power-down reset and the initial mode.

B1, B0 ... Operating mode selection

(0, 0): Initial mode

Approximately 200 ms after power-down reset is released, the initial mode is entered.

Only in this mode can the contents of the internal default value store memory be modified and CR0-B5 to CR0-B0, CR1-B7, CR11-B1 and CR11-B0 be set. In this mode, digital signal output pins are at high impedance, digital communication input pins are internally processed as idle pattern inputs, and neither the echo canceler nor the noise canceler operates. This mode is skipped when the MCUSEL pin is "1". This mode is released by setting the modes shown below. Refer to the flowchart of Figure 5.

(1, 0): Dual echo canceler mode

The acoustic echo canceler, line echo canceler and other functions can be operated by control from the control registers. Refer to Figure 6.

The initial setting for cancelable echo delay time is as follows:

Acoustic delay time (Tacoud) = 44 ms

Line delay time (Tlined) = 15 ms

(1, 1): Single echo canceler mode

The acoustic echo canceler and other functions can be operated by control from the control registers. Control of the line echo canceler is unnecessary in this mode. Refer to Figure 7.

(Other): Reserved bit (cannot be used)

Note: The MCUSEL pin is internally ORed with B1, and the ECSEL pin is internally ORed with B0. To return to the initial mode after it has been released, activate power-down reset.

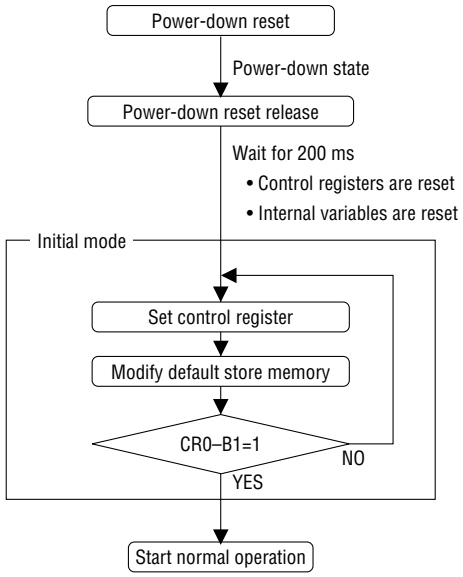


Figure 5 Initial Mode Flowchart

Note: During the initial mode, the READY bit (CR11-B7) is "1", at all other times it is "0".

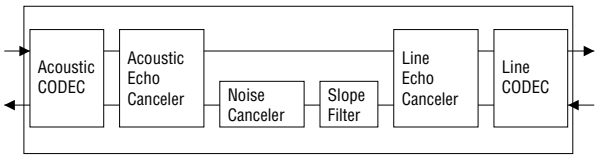


Figure 6 Dual Echo Canceler Mode

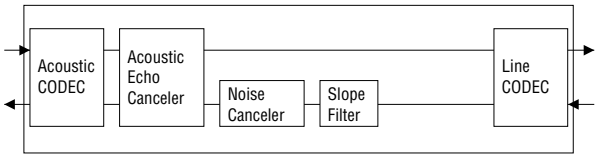


Figure 7 Single Echo Canceler Mode

(2) CR1

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	DMWR	—	—	—	—	$\overline{\text{GLPADTHR}}$	SLPTHR	NCTHR
Initial value	0	0	0	0	0	0	0	0

B7 ..... Internal data memory write control 0: write inhibited, 1: write
In internal data memory, the data set in CR8 (D15 to D8) and CR9 (D7 to D0) is written to the memory address set in CR6 (A15 to A8) and CR7 (A7 to A0). Writing is possible only during the initial mode.
For further details, refer to the internal data memory access method.

B6, B5, B4, B3 .. Reserved bits Modification of initial values is inhibited

B2 ..... Echo canceler I/O PAD control 0: "through mode", 1: normal mode
This bit controls the attenuators (LPADL/A) provided in the SinL/A inputs and the amplifiers (GPADL/A) provided in the SoutL/A outptus of the echo canceler. Levels are set by the CR10 register. Use this bit when the echo return loss (value of returned echo) is amplified. This bit is internally ORed with the $\overline{\text{GLPADTHR}}$ pin.

B1 ..... Slope filter control 0: normal mode (slope filter operation), 1: "through mode"
This bit controls operation of the transmit slope filter. In the "through mode", the filter is halted and data is output directly. This bit is internally ORed with the SLPTHR pin.

B0 ..... Noise canceler control 0: normal mode (noise canceler operation), 1: "through mode"
This bit controls operation of the noise canceler. In the "through mode", the noise canceler is halted and data is output directly. This bit is internally ORed with the NCTHR pin. If this bit is changed to the normal mode, approximately 20 ms of data dropout will occur.

(3) CR2 (Receive side level control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	—	—	RPAD6	RPAD5	RPAD4	RPAD3	RPAD2	RPAD1
Initial value	0	0	0	0	0	0	0	0

B7, B6 ... Reserved bits Modification of initial values is inhibited

B5, B4, B3, B2, B1, B0 ..... Receive side level setting (RPAD)

These bits adjust the receive signal gain and set the mute level. Notice that only the mute level setting differs from pin control.

When using this register, set the RPAD4, 3, 2, 1 pins to a logic "0".

(0, 0, 1, 0, 1, 0):	30 dB
(0, 0, 1, 0, 0, 1):	27 dB
(0, 0, 1, 0, 0, 0):	24 dB
(0, 0, 0, 1, 1, 1):	21 dB
(0, 0, 0, 1, 1, 0):	18 dB
(0, 0, 0, 1, 0, 1):	15 dB
(0, 0, 0, 1, 0, 0):	12 dB
(0, 0, 0, 0, 1, 1):	9 dB
(0, 0, 0, 0, 1, 0):	6 dB
(0, 0, 0, 0, 0, 1):	3 dB
(0, 0, 0, 0, 0, 0):	0 dB
(1, 1, 1, 1, 1, 1):	–3 dB
(1, 1, 1, 1, 1, 0):	–6 dB
(1, 1, 1, 1, 0, 1):	–9 dB
(1, 1, 1, 1, 0, 0):	–12 dB
(1, 1, 1, 0, 1, 1):	–15 dB
(1, 1, 1, 0, 1, 0):	–18 dB
(1, 1, 1, 0, 0, 1):	–21 dB
(1, 1, 1, 0, 0, 0):	–24 dB
(1, 1, 0, 1, 1, 1):	–27 dB
(1, 1, 0, 1, 1, 0):	–30 dB
(1, 1, 0, 1, 0, 1):	–33 dB
(1, 1, 0, 1, 0, 0):	–36 dB
(1, 1, 0, 0, 1, 1):	–39 dB
(1, 1, 0, 0, 1, 0):	–42 dB
(1, 1, 0, 0, 0, 1):	–45 dB
(1, 1, 0, 0, 0, 0):	–48 dB
(1, 0, 1, 1, 1, 1):	–51 dB
(1, 0, 1, 1, 1, 0):	–54 dB
(1, 0, 1, 1, 0, 1):	–57 dB
(1, 0, 1, 1, 0, 0):	–60 dB
(1, 0, 1, 0, 1, 1):	MUTE

(4) CR3 (Transmit side level control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	—	—	TPAD6	TPAD5	TPAD4	TPAD3	TPAD2	TPAD1
Initial value	0	0	0	0	0	0	0	0

B7, B6 ... Reserved bits Modification of initial values is inhibited

B5, B4, B3, B2, B1, B0 ..... Transmit side level setting (TPAD)

These bits adjust the transmit signal gain and set the mute level. Notice that only the mute level setting differs from pin control.

When using this register, set the RPAD4, 3, 2, 1 pins to a logic "0".

(0, 0, 1, 0, 1, 0):	30 dB
(0, 0, 1, 0, 0, 1):	27 dB
(0, 0, 1, 0, 0, 0):	24 dB
(0, 0, 0, 1, 1, 1):	21 dB
(0, 0, 0, 1, 1, 0):	18 dB
(0, 0, 0, 1, 0, 1):	15 dB
(0, 0, 0, 1, 0, 0):	12 dB
(0, 0, 0, 0, 1, 1):	9 dB
(0, 0, 0, 0, 1, 0):	6 dB
(0, 0, 0, 0, 0, 1):	3 dB
(0, 0, 0, 0, 0, 0):	0 dB
(1, 1, 1, 1, 1, 1):	–3 dB
(1, 1, 1, 1, 1, 0):	–6 dB
(1, 1, 1, 1, 0, 1):	–9 dB
(1, 1, 1, 1, 0, 0):	–12 dB
(1, 1, 1, 0, 1, 1):	–15 dB
(1, 1, 1, 0, 1, 0):	–18 dB
(1, 1, 1, 0, 0, 1):	–21 dB
(1, 1, 1, 0, 0, 0):	–24 dB
(1, 1, 0, 1, 1, 1):	–27 dB
(1, 1, 0, 1, 1, 0):	–30 dB
(1, 1, 0, 1, 0, 1):	–33 dB
(1, 1, 0, 1, 0, 0):	–36 dB
(1, 1, 0, 0, 1, 1):	–39 dB
(1, 1, 0, 0, 1, 0):	–42 dB
(1, 1, 0, 0, 0, 1):	–45 dB
(1, 1, 0, 0, 0, 0):	–48 dB
(1, 0, 1, 1, 1, 1):	–51 dB
(1, 0, 1, 1, 1, 0):	–54 dB
(1, 0, 1, 1, 0, 1):	–57 dB
(1, 0, 1, 1, 0, 0):	–60 dB
(1, 0, 1, 0, 1, 1):	MUTE

(5) CR4 (Line echo canceler settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	LTHR	—	—	$\overline{\text{LHD}}$	LCLP	LHLD	$\overline{\text{LATT}}$	$\overline{\text{LGC}}$
Initial value	0	0	0	0	0	0	0	0

B7 ..... "Through mode" control 1: "through mode", 0: normal mode (echo cnaceler operation)
This is the "through mode" control bit for the line echo canceler. In the "through mode", RinL and SinL data is output directly to RoutL and SoutL respectively. Coefficients are not reset.
This bit is internally ORed with the LTHR pin.

B6, B5 ... Reserved bits Modification of initial values is inhibited

B4 ..... Howling detector control 1: OFF, 0: ON
This bit controls the function to detect and cancel the howling that occurs in an acoustic system such as a handsfree communication system.
This bit is internally ORed with the $\overline{\text{LHD}}$ pin.

B3 ..... Center clip control 1: ON, 0: OFF
When the SoutL output of the line echo canceler is –57 dBm0 or less, the center clip function forcibly sets it to the minimum positive value.

B2 ..... Coefficient update control 1: fixed coefficients, 0: updated coefficients
This bit selects whether the adaptive FIR filter (AFR) coefficients for the line echo canceler will be updated.
This bit is internally ORed with the LHLD pin.

B1 ..... Attenuator control 1: ATT OFF, 0: ATT ON
This bit turns ON or OFF the ATT function to prevent howling by means of attenuators (ATTsL, ATTrL) provided in the RinL input and SoutL output of the line echo canceler.
If input is only to RinL, the ATT for SoutL (ATTsL) is activated. If input is only to SinL, or if there is input to both SinL and RinL, the ATT for RinL input (ATTrL) is activated. The ATT value of each attenuator is approximately 6 dB.
This bit is internally ORed with the $\overline{\text{LATT}}$ pin.

B0 ..... Gain controller 1: GC OFF, 0: GC ON
This bit turns ON or OFF the gain control function to control the RinL input level and prevent howling by means of a gain controller (GainL) provided in the RinL input of the line echo canceler.
The gain controller adjusts the RIN input level when it is –10 dBm0 or above, and it has the control range of 0 to –8.5 dB.
This bit is internally ORed with the $\overline{\text{LGC}}$ pin.

(6) CR5 (Acoustic echo canceler settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	ATHR	—	—	$\overline{\text{AHD}}$	ACLP	AHLD	$\overline{\text{AATT}}$	$\overline{\text{AGC}}$
Initial value	0	0	0	0	0	0	0	0

B7 ..... "Through mode" control 1: "through mode", 0: normal mode (echo cnaceler operation)
This is the "through mode" control bit for the acoustic echo canceler. In the "through mode", RinA and SinA data is output directly to RoutA and SoutA respectively. Coefficients are not reset.
This bit is internally ORed with the ATHR pin.

B6, B5 ... Reserved bits Modification of initial values is inhibited

B4 ..... Howling detector control 1: OFF, 0: ON
This bit controls the function to detect and cancel the howling that occurs in an acoustic system such as a handsfree communication system.
This bit is internally ORed with the $\overline{\text{AHD}}$ pin.

B3 ..... Center clip control 1: ON, 0: OFF
When the SoutA output of the acoustic echo canceler is –57 dBm0 or less, the center clip function forcibly sets it to the minimum positive value.

B2 ..... Coefficient update control 1: fixed coefficients, 0: updated coefficients
This bit selects whether the adaptive FIR filter (AFR) coefficients for the acoustic echo canceler will be updated.
This bit is internally ORed with the AHLD pin.

B1 ..... Attenuator control 1: ATT OFF, 0: ATT ON
This bit turns ON or OFF the ATT function to prevent howling by means of attenuators (ATTsA, ATTrA) provided in the RinA input and SoutA output of the acoustic echo canceler.
If input is only to RinA, the ATT for SoutA (ATTsA) is activated. If input is only to SinA, or if there is input to both SinA and RinA, the ATT for RinA input (ATTrA) is activated. The ATT value of each attenuator is approximately 6 dB.
This bit is internally ORed with the $\overline{\text{AATT}}$ pin.

B0 ..... Gain controller 1: GC OFF, 0: GC ON
This bit turns ON or OFF the gain control function to control the RinA input level and prevent howling by means of a gain controller (GainA) provided in the RinA input of the acoustic echo canceler.
The gain controller adjusts the RIN input level when it is –10 dBm0 or above, and it has the control range of 0 to –8.5 dB.
This bit is internally ORed with the $\overline{\text{AGC}}$ pin.

(7) CR6 (Internal data memory write register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	A15	A14	A13	A12	A11	A10	A9	A8
Initial value	0	0	0	0	0	0	0	0

B7 to B0 ..... Memory upper address control

This register sets the upper address of memory. For the writing method, refer to the Method of Internal Data Memory Access section.

(8) CR7 (Internal data memory write register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	A7	A6	A5	A4	A3	A2	A1	A0
Initial value	0	0	0	0	0	0	0	0

B7 to B0 ..... Memory lower address control

This register sets the lower address of memory. For the writing method, refer to the Method of Internal Data Memory Access section.

(9) CR8 (Internal data memory write register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR8	D15	D14	D13	D12	D11	D10	D9	D8
Initial value	0	0	0	0	0	0	0	0

B7 to B0 ..... Memory upper data control

This register sets the memory's upper data. For the writing method, refer to the Method of Internal Data Memory Access section.

(10) CR9 (Internal data memory write register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR9	D7	D6	D5	D4	D3	D2	D1	D0
Initial value	0	0	0	0	0	0	0	0

B7 to B0 ..... Memory lower data control

This register sets the memory's lower data. For the writing method, refer to the Method of Internal Data Memory Access section.

(11) CR10 (Echo canceler I/O level settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR10	GPADA2	GPADA1	LPADA2	LPADA1	GPADL2	GPADL1	LPADL2	LPADL1
Initial value	0	0	0	0	0	0	0	0

B7, B6 ... Acoustic output level control

These bits control the PAD level of the gain of the acoustic echo canceler's SoutA output. PAD is turned ON or OFF by either the $\overline{\text{GLPADTHR}}$ pin or the $\overline{\text{GLPADTHR}}$ control register bit (CR1-B2). It is recommended to set the level to the positive level equal to LPADA2 and LPADA1.

(0, 1) : +18 dB
(0, 0) : +12 dB
(1, 1) : +6 dB
(1, 0) : 0 dB

B5, B4 ... Acoustic input level control

These bits control the PAD level of the loss of the acoustic echo canceler's SinA input. PAD is turned ON or OFF by either the $\overline{\text{GLPADTHR}}$ pin or the $\overline{\text{GLPADTHR}}$ control register bit (CR1-B2). Set the level such that echo return loss (value of returned echo) will be attenuated.

(0, 1) : −18 dB
(0, 0) : −12 dB
(1, 1) : −6 dB
(1, 0) : 0 dB

B3, B2 ... Line output level control

These bits control the PAD level of the gain of the line echo canceler's SoutL output. PAD is turned ON or OFF by either the $\overline{\text{GLPADTHR}}$ pin or the $\overline{\text{GLPADTHR}}$ control register bit (CR1-B2). It is recommended to set the level to the positive level equal to LPADL2 and LPADL1.

(0, 1) : +18 dB
(0, 0) : +12 dB
(1, 1) : +6 dB
(1, 0) : 0 dB

B1, B0 ... Line input level control

These bits control the PAD level of the loss of the line echo canceler's SinL output. PAD is turned ON or OFF by either the $\overline{\text{GLPADTHR}}$ pin or the $\overline{\text{GLPADTHR}}$ control register bit (CR1-B2). Set the level such that echo return loss (value of returned echo) will be attenuated.

(0, 1) : −18 dB
(0, 0) : −12 dB
(1, 1) : −6 dB
(1, 0) : 0 dB

(12) CR11 (SYNC power-down control register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR11	READY	—	—	—	—	—	PCMSEL	SYPDN
Initial value	0	0	0	0	0	0	0	0

B7 ..... Data write flag 1: write enabled, 0: write disabled
After power-down reset is released, this device enters the initial mode. This bit becomes "1" only during the initial mode, enabling access to the internal data memory. Checking this bit will detect whether writing by an external microcomputer is possible.

B6 to B2 ..... Reserved bits Modification of initial values is inhibited

B1 ..... PCM coding format control 1: μ-law PCM, 0: 16-bit linear
This is the coding format selection bit for digital data communication. A logic "1" selects μ-law PCM and a logic "0" selects 16-bit linear (2's complement) coding format. When an internal clock is selected, the BCLK signal determines the output clock frequency to be used when internal clock is selected.
If the digital interface is not used, set this bit to logic "0" to select 16-bit linear coding format. Since this bit is ORed with the PCMSEL pin, set this bit to logic "0" when controlling by the pin. If this bit setting is changed, reset must be activated by either the $\overline{\text{PDN}}/\overline{\text{RST}}$ pin or the PDN/RST bit (CR0-B7).

B0 ..... SYNC power-down 1: SYNC power-down ON, 0: SYNC power-down OFF
This bit turns ON or OFF the function that automatically enters the power-down reset state when the SYNC signal is fixed to a logic "1" or "0". This function is valid when the external clock mode has been selected by the CLKSEL pin. If the SYNC signal is fixed at 8kHz or longer, this device automatically writes a logic "1" to the control register PDN/RST bit (CR0-B7) and enters the power-down reset state. For timing details, refer to the electrical characteristics.

(13) CR12 (Reserved register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR12	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7 to B0 ..... Reserved bits Modification of initial value is inhibited.

RELATIONSHIP BETWEEN PINS AND CONTROL REGISTERS

In this device, the same function is controlled by either a pin or a control retister.
For example, when a function is controlled by a pin, setting of the corresponding control register is important. Table 3 shows the relationship between settings of pins when functions are controlled by control registers and settings of control registers when functions are controlled by pins. The setting value of a control register when a function is controlled by a pin is equal to its initial value when the device is reset by the PDN/RST pin or the $\overline{PDN}/\overline{RST}$ bit (CR0-B7).

Table 3 Relationship between pins and control registers

Function	Setting of pin when function is controlled by control register	Setting of control register when function is controlled by pin
$\overline{LINEEN}$	Logic "0"	0
$\overline{PDN/RST}$	Logic "1"	0
PCMSEL	Logic "0"	0
ECSEL	Logic "0"	0
LTHR/ATHR	Logic "0"	0
LHD/AHD	Logic "0"	0
LHLD/AHLD	Logic "0"	0
LATT/AATT	Logic "0"	0
LGC/AGC	Logic "0"	0
GLPADTHR	Logic "0"	0
NCTHR	Logic "0"	0
SLPTHR	Logic "0"	0
RST	Logic "1"	0
MCUSEL	Logic "0"	0
RPAD4-1	Logic "0"	0
TPAD4-1	Logic "0"	0

Method of Internal Data Memory Access

So that the default values such as the cancelable echo delay time can be changed, contents of the memory that stores default values can be modified during the initial mode (CR0-B1, CR0-B0 = "00").
Refer to the procedure below.

1. Set the address of the default value store memory. (CR6, CR7)
2. Set the modified values (data). (CR8, CR9)
3. Set the write command. (CR1-B7 = "1")

After the write operation is complete, the write command (CR1-B7) is cleared to "0". Consecutive writes are possible.

Echo Canceler Delay Time

Cancelable echo delay time is as follows.

(1) Single echo canceler mode
- Acoustic echo canceler
  - Default: 59 ms
  - Variable range: 0.5 to 59 ms (in 0.5 ms steps)
- Line echo canceler operation is halted.

(2) Dual echo canceler mode (operation of acoustic and line echo cancelers)
Condition: acoustic delay time + line delay time ≤ 59 ms
- Acoustic echo canceler
  - Default: 44 ms
  - Variable range: 0.5 to 58.5 ms (in 0.5 ms steps)
- Line echo canceler
  - Default: 15 ms
  - Variable range: 0.5 to 27 ms (in 0.5 ms steps)

Memory addresses are shown below.

(1) Single echo canceler mode
Memory address of acoustic echo canceler delay time: 009DH

(2) Dual echo canceler mode
Memory address of acoustic echo canceler delay time: 009BH
Memory address of line echo canceler delay time: 009CH

The method for calculating delay time is shown below.

delay time [s] × 8000 = delay time data (HEX)

Example of 30 ms:

$0.03 \times 8000 = 240$ (DEC)
$= 00F0$ (HEX)

Noise Attenuation

There is a trade-off between noise attenuation and sound quality. In other words, increasing the noise attenuation deteriorates sound quality, and decreasing the noise attenuation improves sound quality. The following three types of noise attenuation levels can be selected with this device.

	Noise attenuation	Sound quality
Type 1	approx. 13 dB (typ.)	Typ.
Type 2	approx. 10 dB (typ.)	Better than Type 1
Type 3	approx. 9 dB (typ.)	Better than Type 2

Note: Only type 1 is compatible with pin control.

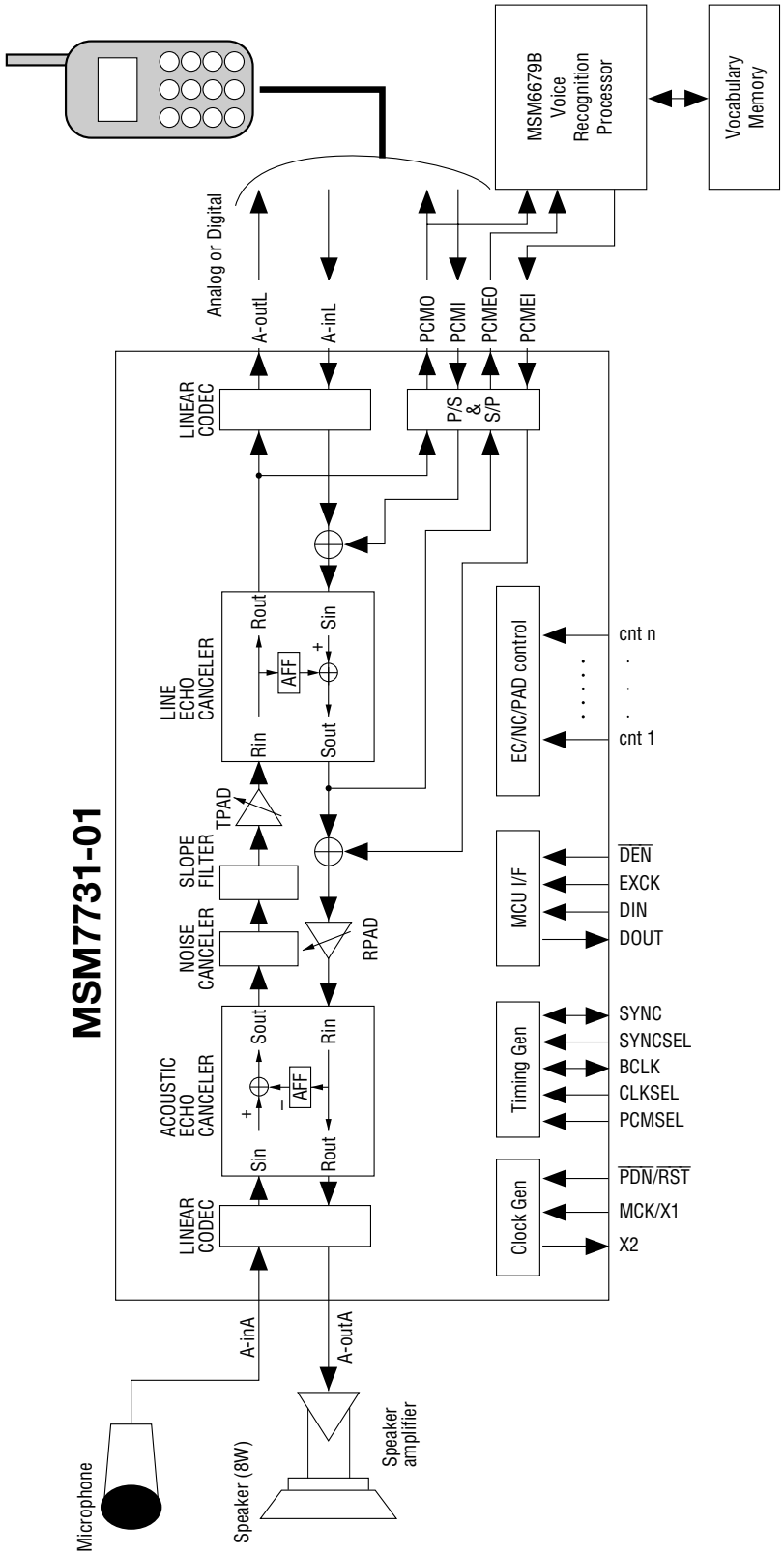
Memory address: 01C8H
Data to be stored:

	Data
Type 1	2000H
Type 2	3333H
Type 3	4666H

NOTES ON USE

1. Use a stabilized power supply with a low level of noises (especially spike noises and pulse noises of high frequencies) in order to prevent this device from malfunction or degradation in characteristics.
2. Place a good characteristics of bypass-capacitor for the power supply near the pins of this device in order to assure its electrical characteristics.
3. Place a good characteristics of bypass-capacitor for the analog signal ground (SG pin) near the pins of this device in order to assure its electrical characteristics.
4. Connect the AGND, DGND1 and DGND2 to the system ground at a shortest distance and in a low impedance state.
5. Use a separate power supply for an external speaker amplifier so as not to be disturbed by externally generated noises.
6. When an external speaker amplifier is used, do gain adjusting without overflow (saturation) of speaker amplifier output.
   The overflow of speaker amplifier output decreases the echo attenuation.
7. Set the analog signal input level to less than $1.3V_{PP}$ to prevent overflow.
   Otherwise, voice will be distorted.
8. Set the echo return loss (ERL) to be attenuated. If the echo return loss is to be amplified, the GLPAD function should be used.
   The ERL refers to echo attenuation (loss) between the echo canceler output (RoutA/RoutL) and the echo canceler input (SinA/SinL).
   Refer to Characteristics Diagram for the ERL vs. echo attenuation.
9. The input level should be –10 to –20dBm0.
   Refer to Characteristics Diagram for the RIN input level vs. echo attenuation.
10. Adjust the volume at the position of the echo canceler input (RinA/RinL).
    When in Dual Echo Canceler mode : Adjust the volume with TPAD and RPAD.
    When in Signal Echo Canceler mode : Adjust the volume with TPAD and RPAD, or with the analog input (LIN) that is set at less than $1.3V_{PP}$.
11. When the echo path is changed (when resuming telephone communication), reset the device with the PDN/RST pin or the PDN/RST bit.
12. After turning on the power, be sure to reset the device with PDN/RST pin or the $\overline{\text{PDN}}/\overline{\text{RST}}$ bit.
13. In order to get the highest performance of this device, the following functions should be used.
    $\overline{\text{AATT}}/\overline{\text{LATT}}$: ON
    $\overline{\text{AGC}}/\overline{\text{LGC}}$: ON
    SLPTHR : Normal mode (slope filter operation)
    NCTHR : Normal mode (noise canceler operation)
    RPAD6-1 : Adjusting the volume of receive signal.
    TPAD6-1 : Adjusting the volume of transmit signal.

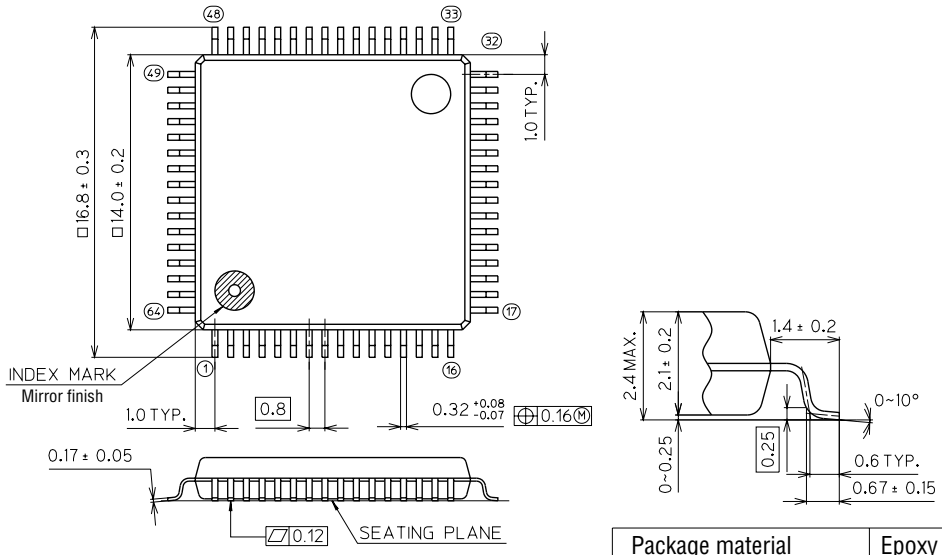
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit : mm)

QFP64-P-1414-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.87 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).