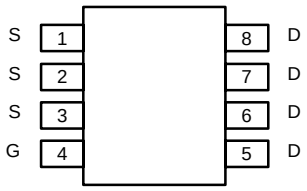
N-Channel 80-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
80	0.035 @ V_{GS} = 10 V	6.2
	0.040 @ V_{GS} = 6.0 V	5.8

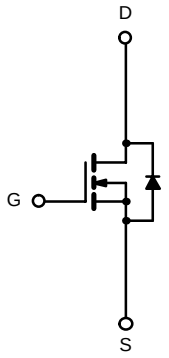
175°C Rated Maximum Junction Temperature TrenchFET® Power MOSFETs

SO-8



Top View

Ordering Information: Si4480EY
Si4480EY-T1 (with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 175°C)[a, b]	T_A = 25°C	I_D	6.2	A
	T_A = 70°C		5.2	
Pulsed Drain Current		I_{DM}	40	
Continuous Source Current (Diode Conduction)[a, b]		I_S	2.5	
Maximum Power Dissipation[a, b]	T_A = 25°C	P_D	3	W
	T_A = 70°C		2.1	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	40	50	°C/W
	Steady State		85	100	
Maximum Junction-to-Lead	Steady State	R_{thJL}	20	24	

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.
b. t ≤ 10 sec.

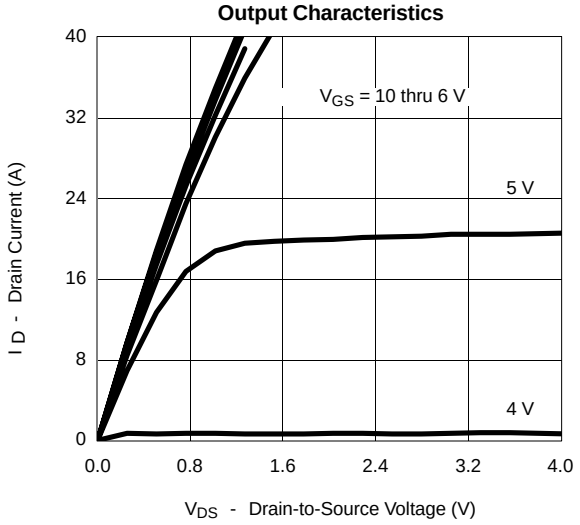
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ[b]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			1	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55°C			20	
On-State Drain Curren[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 6.2 A		0.026	0.035	Ω
		V_{GS} = 6.0 V, I_D = 5.8 A		0.030	0.040	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 6.2 A		25		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.1 A, V_{GS} = 0 V			1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 40 V, V_{GS} = 10 V, I_D = 6.2 A		30	50	nC
Gate-Source Charge	Q_{gs}			9		
Gate-Drain Charge	Q_{gd}			5.6		
Gate Resistance	R_g		1.5		4.0	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 40 V, R_L = 30 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		12.5	25	ns
Rise Time	t_r			12.5	25	
Turn-Off Delay Time	$t_{d(off)}$			52	80	
Fall Time	t_f			22	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.1 A, di/dt = 100 A/µs		50	80	

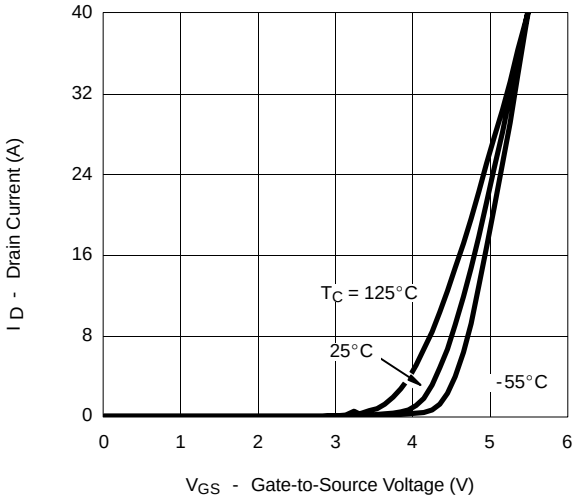
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

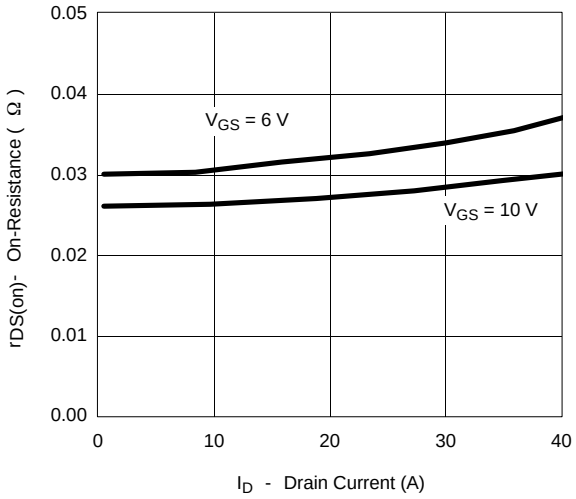


Transfer Characteristics

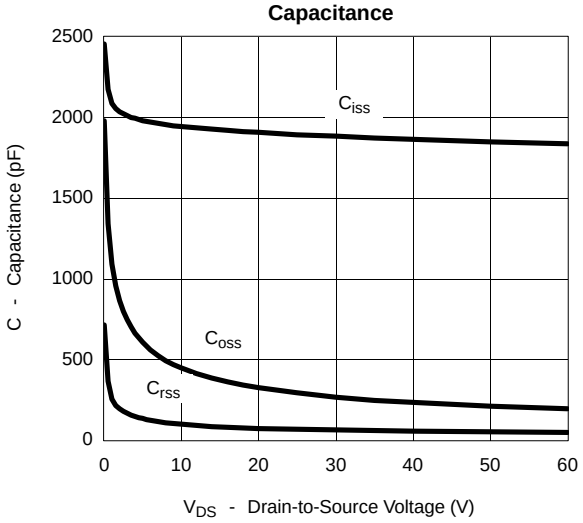


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

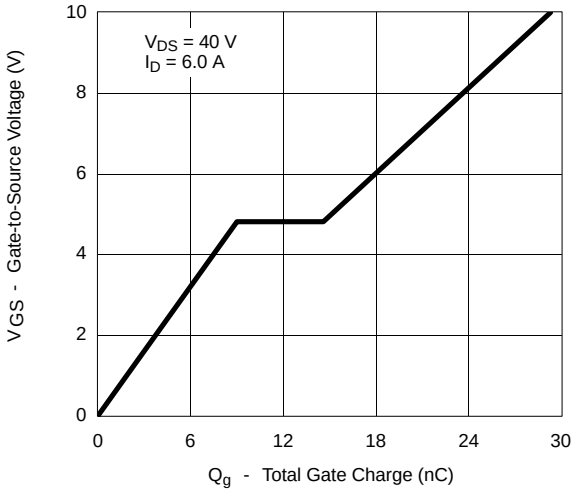
On-Resistance vs. Drain Current



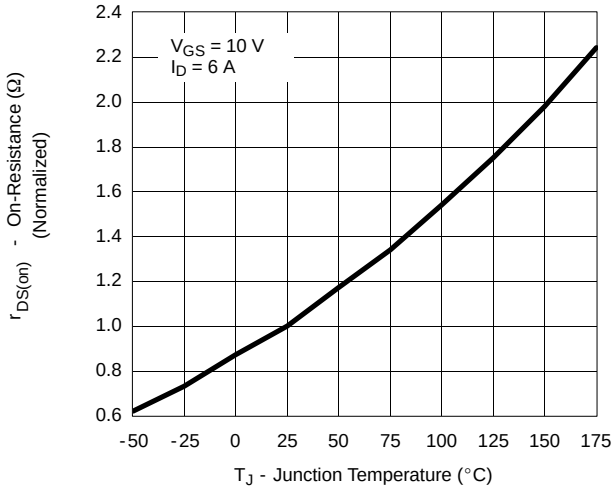
Capacitance



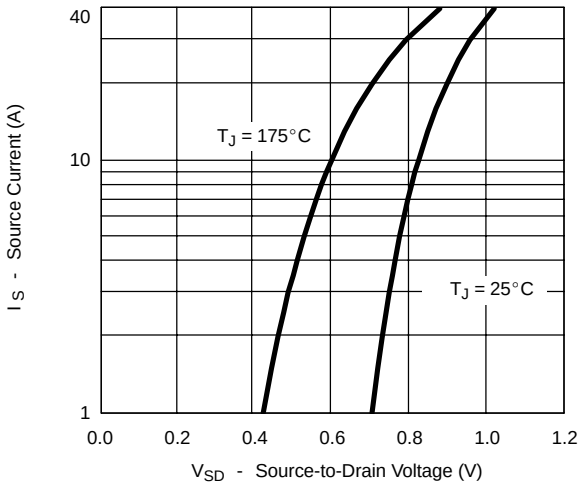
Gate Charge



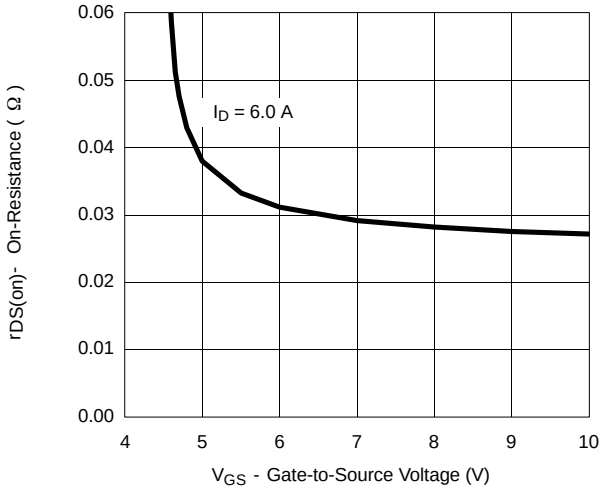
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

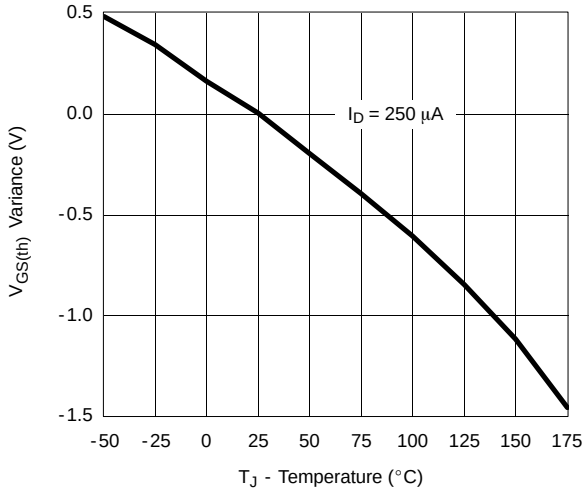


On-Resistance vs. Gate-to-Source Voltage

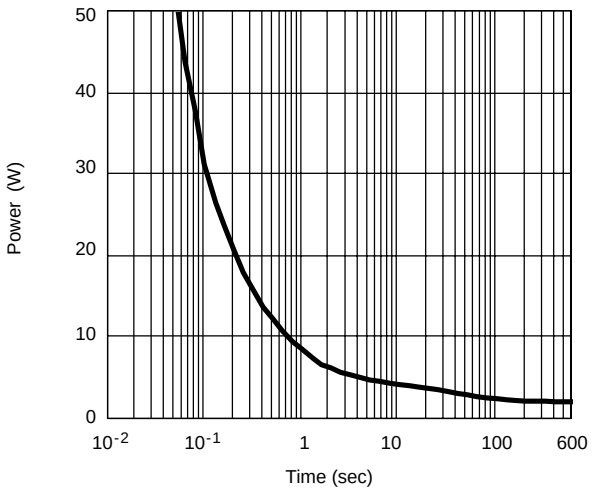


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

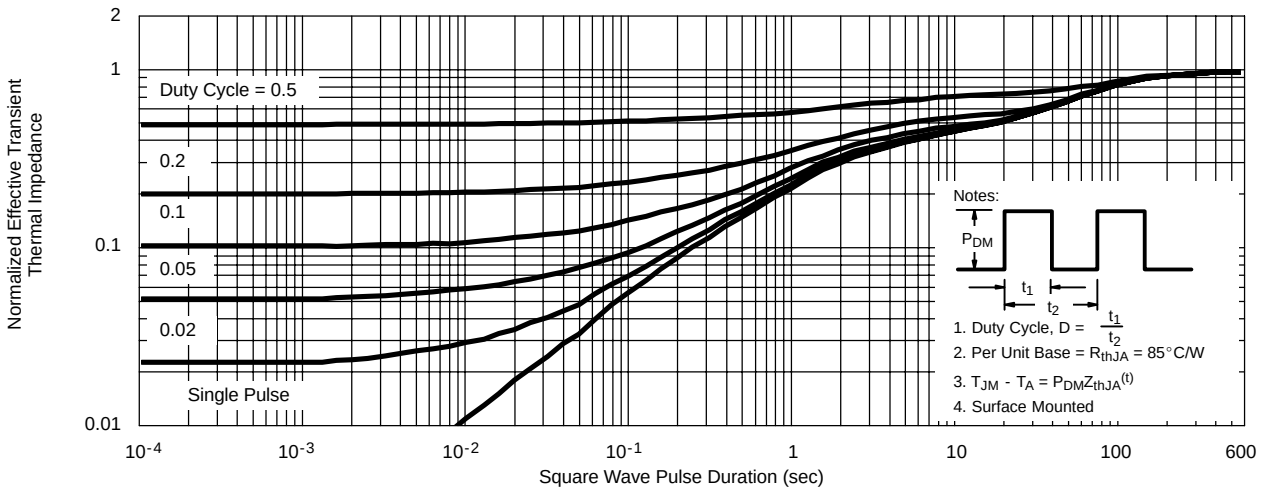
Threshold Voltage



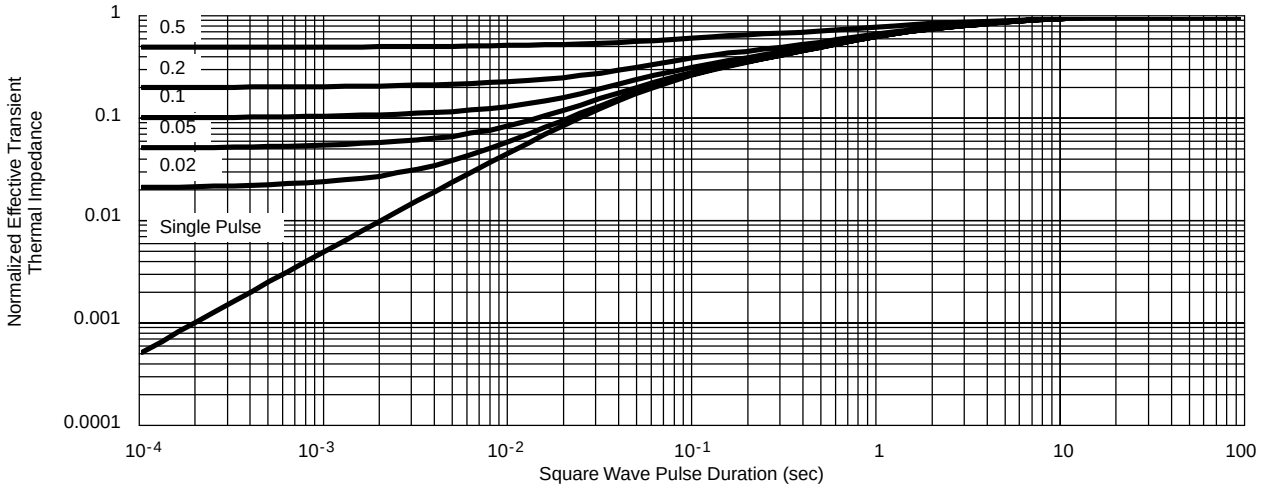
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



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