

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

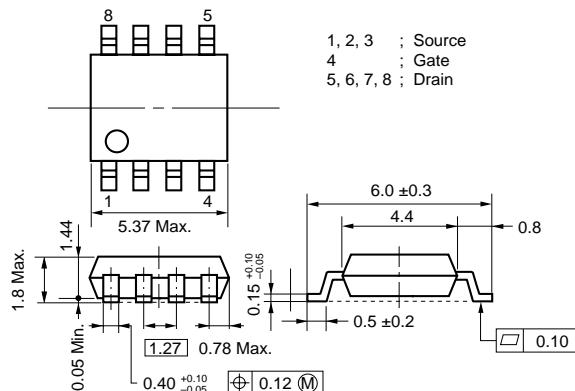
DESCRIPTION

The μ PA1728 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Single chip type
- Low On-state Resistance
- ★ $R_{DS(on)1} = 19 \text{ m}\Omega$ (TYP.) ($V_{GS} = 10 \text{ V}$, $I_D = 4.5 \text{ A}$)
- ★ $R_{DS(on)2} = 23 \text{ m}\Omega$ (TYP.) ($V_{GS} = 4.5 \text{ V}$, $I_D = 4.5 \text{ A}$)
- ★ $R_{DS(on)3} = 24 \text{ m}\Omega$ (TYP.) ($V_{GS} = 4.0 \text{ V}$, $I_D = 4.5 \text{ A}$)
- ★ • Low C_{iss} : $C_{iss} = 1700 \text{ pF}$ (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



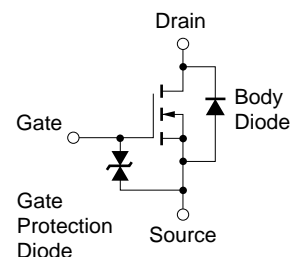
ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1728	Power SOP8

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 9	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 36	A
Total Power Dissipation ($T_A = 25 \text{ }^\circ\text{C}$) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	9	A
Single Avalanche Energy ^{Note3}	E_{AS}	8.1	mJ

EQUIVALENT CIRCUIT



Notes 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1 \%$

- ★ 2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
- 3. Starting $T_{ch} = 25 \text{ }^\circ\text{C}$, $R_G = 25 \Omega$, $T_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

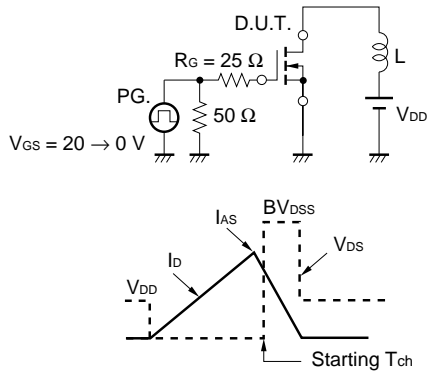
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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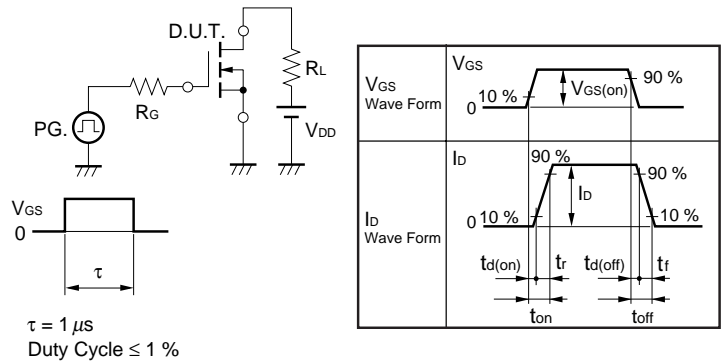
★ ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 4.5 A		19	26	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 4.5 A		23	29	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 4.5 A		24	34	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.5 A	6.0	12		S
Drain Leakage Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iSS}	V _{DS} = 10 V		1700		pF
Output Capacitance	C _{oSS}	V _{GS} = 0 V		270		pF
Reverse Transfer Capacitance	C _{rSS}	f = 1 MHz		130		pF
Turn-on Delay Time	t _{d(on)}	I _D = 4.5 A		17		ns
Rise Time	t _r	V _{GS(on)} = 10 V		69		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 30 V		77		ns
Fall Time	t _f	R _G = 10 Ω		31		ns
Total Gate Charge	Q _G	I _D = 9 A		31		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 48 V		4.4		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		9.1		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 9 A, V _{GS} = 0 V		0.82		V
Reverse Recovery Time	t _{rr}	I _F = 9 A, V _{GS} = 0 V		41		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs		76		nC

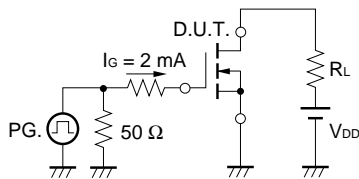
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



[MEMO]

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