FAIRCHILD SEMICONDUCTOR™

July 1988
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100323
Low Power Hex Bus Driver

General Description

The 100323 is a monolithic device containing six bus drivers capable of driving terminated lines with terminations as low as 25Ω. To reduce crosstalk, each output has its own respective ground connection. Transition times were designed to be longer than on other F100K devices. The driver itself performs the positive logic AND of a data input (D_1–D_6) and the OR of two select inputs (E and either DE_1, DE_2, or DE_3).

Enabling of data is possible in multiples of two, i.e., 2, 4 or all 6 paths. All inputs have 50 kΩ pull-down resistors.

The output voltage LOW level is designed to be more negative than normal ECL outputs (cut off state). This allows an emitter-follower output transistor to turn OFF when the termination supply is –2.0V and thus present a high impedance to the data bus.

Features

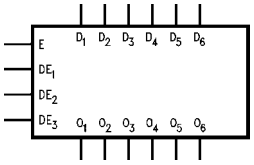
- 50% power reduction of the 100123
- 2000V ESD protection
- –4.2V to –5.7V operating range
- Drives 25Ω load

Ordering Code:

Order Number	Package Number	Package Description
100323PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100323QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

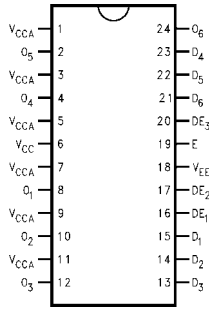


Pin Descriptions

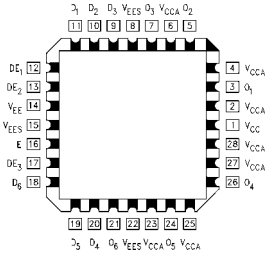
Pin Names	Description
D_1–D_6	Data Inputs
DE_1–DE_3	Dual Enable Inputs
E	Common Enable Input
O_1–O_6	Data Outputs

Connection Diagrams

24-Pin DIP



28-Pin PLCC

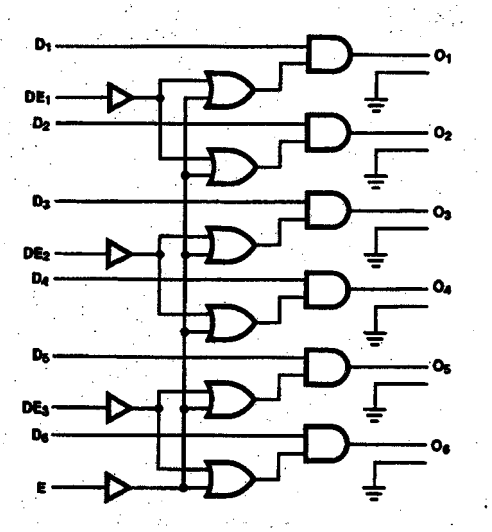


Truth Table

E	DE_n	D_n	D_{n+1}	O_n	O_{n+1}
L	L	X	X	Cutoff	Cutoff
X	H	L	L	Cutoff	Cutoff
X	H	L	H	Cutoff	H
X	H	H	L	H	Cutoff
X	H	H	H	H	H
H	X	L	L	Cutoff	Cutoff
H	X	L	H	Cutoff	H
H	X	H	L	H	Cutoff
H	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Cutoff = Lower-than-LOW State

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output High)	−50 mA
ESD	≥2000V

Recommended Operating Conditions

Case Temperature	0°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

DC Electrical Characteristics (Note 3)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed High Signal for ALL Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed Low Signal for ALL Inputs	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$	Loading with 25Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$	Loading with 25Ω to −2.0V
V_{OLZ}	Cut-Off LOW Voltage			−1950	mV	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$	Loading with 25Ω to −2.0V
I_{IL}	Input LOW Current	0.50			µA	V_{IN} = $V_{IL\ (min)}$	
I_{IH}	Input HIGH Current			240	µA	V_{IN} = $V_{IH\ (max)}$	
I_{EE}	Power Supply Current	−121	−91	−57	mA	Inputs Open	

Note 3: The specified limits represent "worst case" values for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics (Note 4)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PZH}	Propagation Delay	1.90	3.60	1.90	3.60	2.00	3.80	ns	Figures 1, 2
t_{PHZ}	Data to Output	1.30	2.70	1.30	2.70	1.50	2.70		
t_{PZH}	Propagation Delay	1.90	3.60	1.90	3.60	2.00	3.90	ns	
t_{PHZ}	Dual Enable to Output	1.60	3.00	1.60	3.00	1.70	3.40		
t_{PZH}	Propagation Delay	1.80	3.50	1.80	3.50	2.00	3.80	ns	
t_{PHZ}	Common Enable to Output	1.50	2.90	1.50	2.90	1.60	3.00		
t_{TZH}	Transition Time	0.50	1.80	0.50	1.80	0.50	1.80	ns	
t_{THZ}	20% to 80%, 80% to 20%	0.35	1.40	0.35	1.40	0.35	1.40		

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

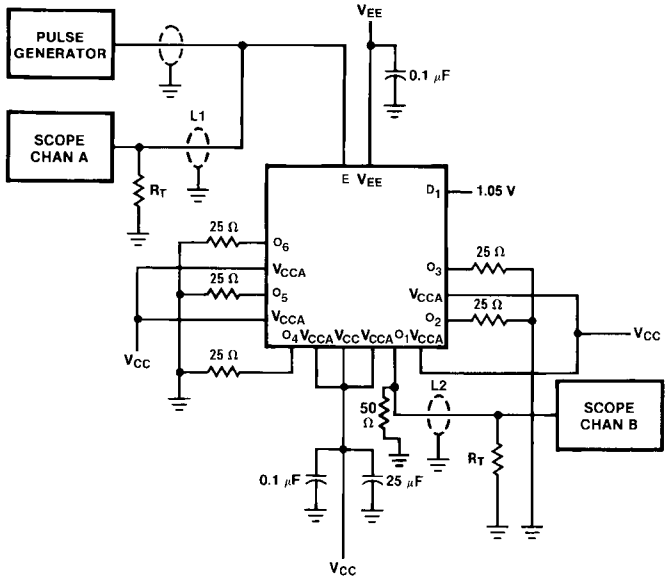
PLCC AC Electrical Characteristics (Note 5)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PZH}	Propagation Delay	1.90	3.40	1.90	3.40	2.00	3.60	ns	Figures 1, 2
t_{PHZ}	Data to Output	1.30	2.50	1.30	2.50	1.50	2.70		
t_{PZH}	Propagation Delay	1.90	3.40	1.90	3.40	2.00	3.70	ns	
t_{PHZ}	Dual Enable to Output	1.60	2.80	1.60	2.80	1.70	3.00		
t_{PZH}	Propagation Delay	1.80	3.30	1.80	3.30	2.00	3.60	ns	
t_{PHZ}	Common Enable to Output	1.50	2.70	1.50	2.70	1.60	2.80		
t_{TZH}	Transition Time	0.50	1.70	0.50	1.70	0.50	1.70	ns	
t_{THZ}	20% to 80%, 80% to 20%	0.35	1.30	0.35	1.20	0.35	1.30		

Note 5: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Test Circuitry



Note:

- V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 25Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

Timing Waveform

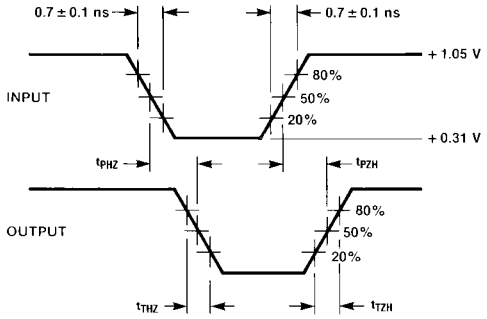
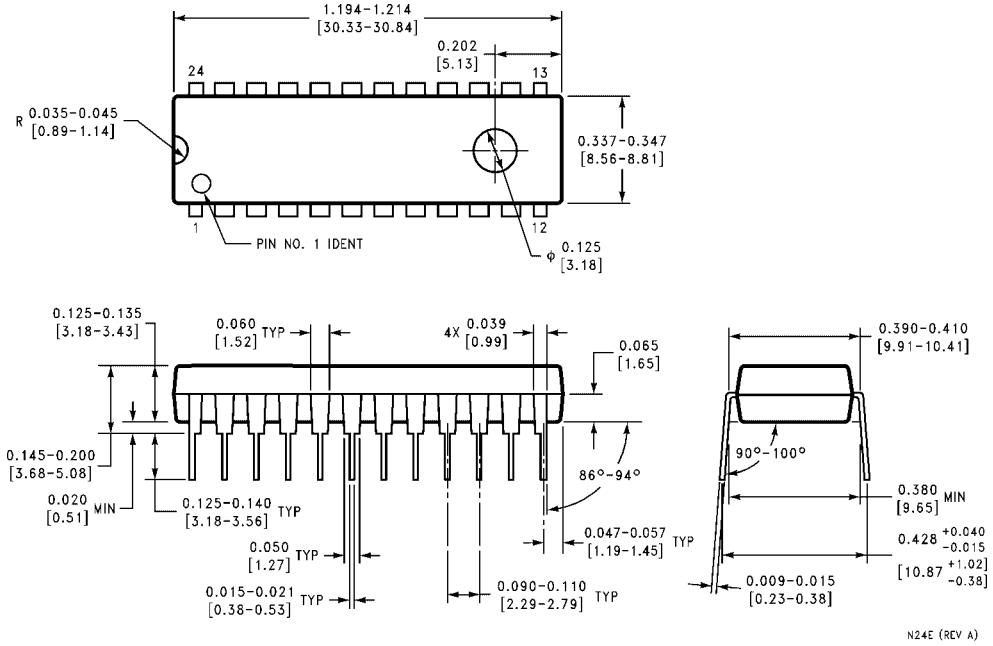


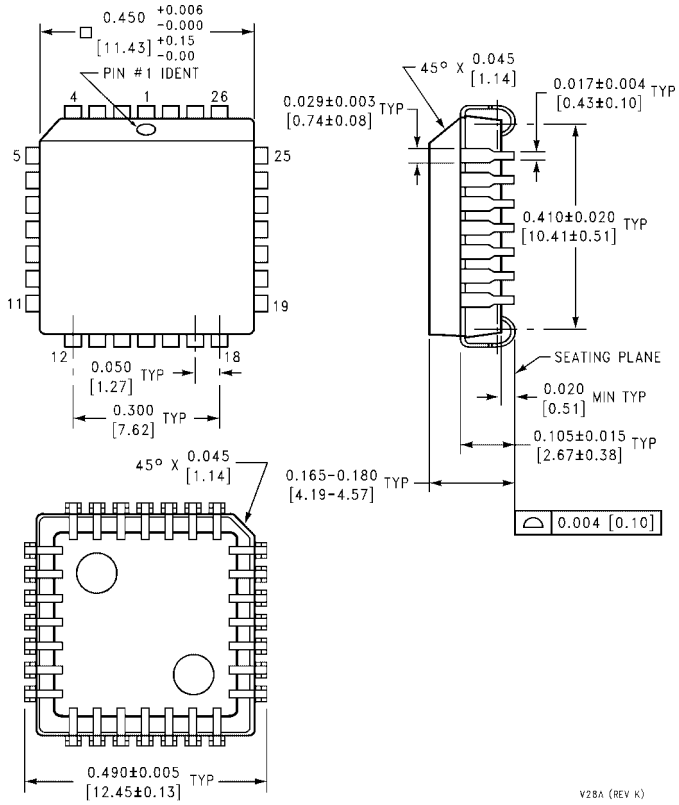
FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A