SONY

CXA2543R

Decoder/Driver/Timing Generator for Color LCD Panels

Description

The CXA2543R is an IC designed exclusively to drive the color LCD panel DCX501BK and LCX018AK.

This IC greatly reduces the number of circuits and parts required to drive LCD panels by incorporating RGB decoder functions for video signals, driver functions, and a timing generator for driving panels onto a single chip.

This chip has a built-in serial interface circuit and electronic attenuators which allow various mode settings and adjustments to be performed through direct control from an external microcomputer, etc.

Features

- Color LCD panel DCX501BK and LCX018AK driver
- Supports NTSC and PAL signals
- Supports 16:9 wide display
- Supports composite inputs, Y/C inputs and Y/color difference inputs
- Serial interface circuit
- Electronic attenuators (D/A converter)
- BPF, trap and delay line
- Sharpness function
- 2-point γ correction circuit
- R, G, B signal delay time adjustment circuit
- Polarity inversion circuit (line inverted mode)
- Supports external RGB input
- Supports AC drive for LCD panel during no signal

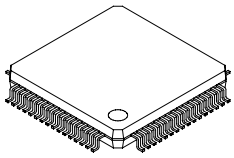
Applications

- Compact LCD monitors
- LCD viewfinders
- Compact liquid crystal projectors, etc.

Structure

Bipolar CMOS IC

64 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	$V_{CC}1$ – GND1	6	V
	$V_{CC}2$ – GND2	14	V
	$V_{CC}3$ – GND3	14	V
	$V_{DD}1$ – $V_{SS}1$	4.5	V
	$V_{DD}1$ – $V_{SS}2$	4.5	V
• Analog input pin voltage	VINA	–0.3 to V_{CC}	V
• Digital input pin voltage	VIND	–0.3 to $V_{DD}1$ + 0.3	V
• Operating temperature	Topr	–15 to +75	°C
• Storage temperature	Tstg	–40 to +125	°C
• Allowable power dissipation*1			
	P_D (Ta ≤ 75°C)	350	mW

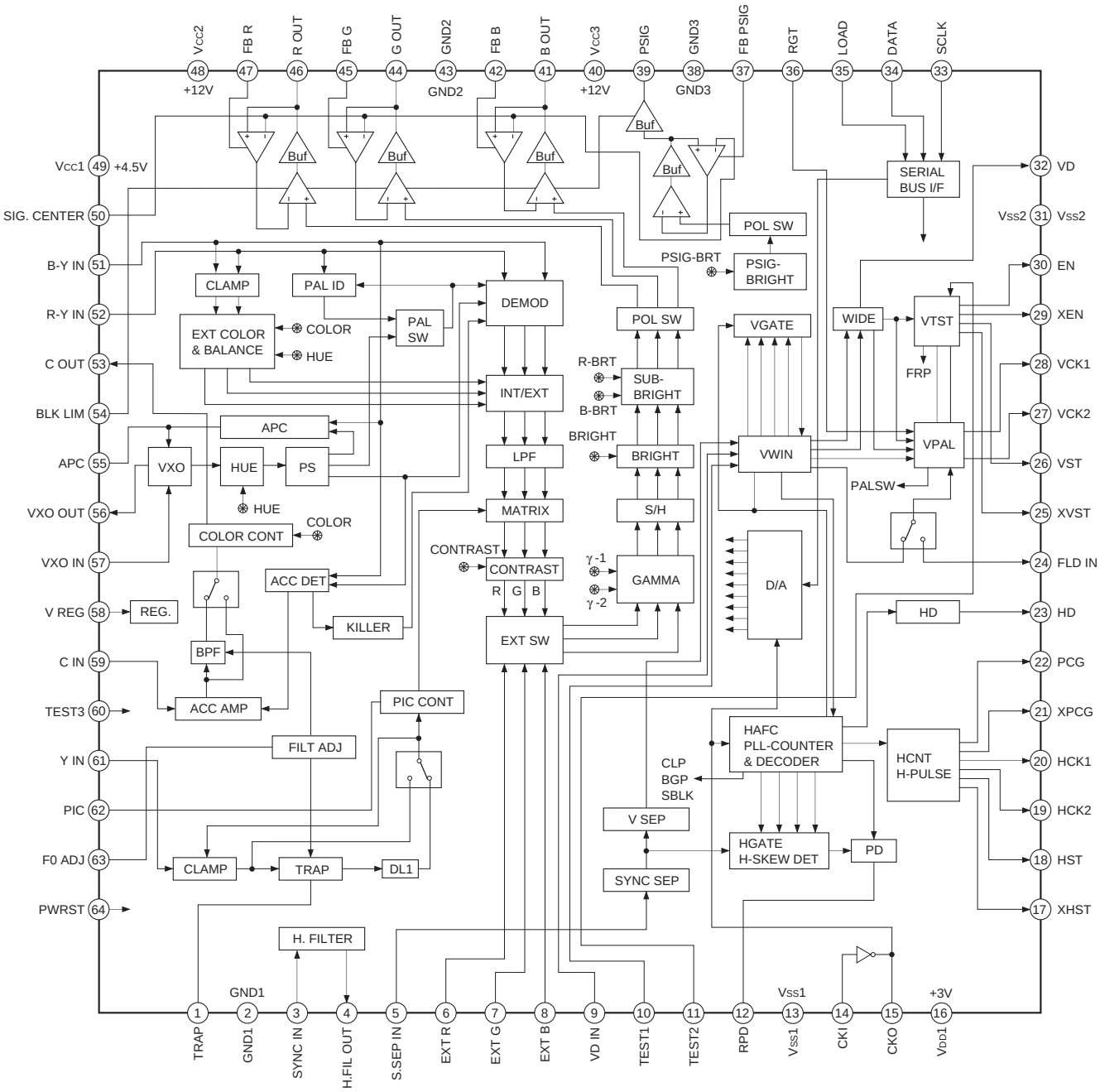
Operating conditions

Supply voltage	$V_{CC}1$ – GND1	4.25 to 5.25	V
	$V_{CC}2$ – GND2	11.0 to 13.5	V
	$V_{CC}3$ – GND3	11.0 to 13.5	V
	$V_{DD}1$ – $V_{SS}1$	2.7 to 3.6	V
	$V_{DD}1$ – $V_{SS}2$	2.7 to 3.6	V

*1 With substrate Size: 30 × 30 × 1.6mm
Material: Glass fabric base epoxy

E98403-PS

Block Diagram



Pin Description

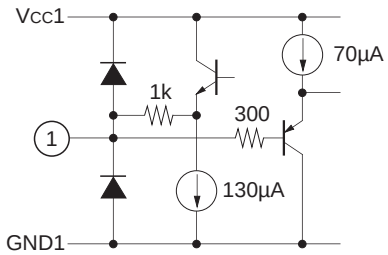
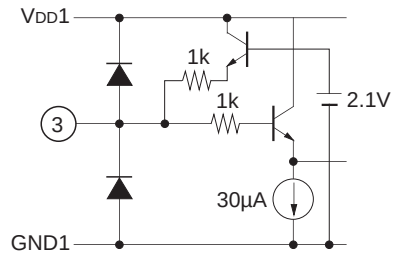
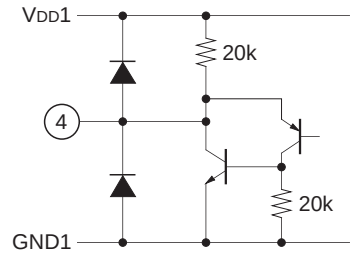
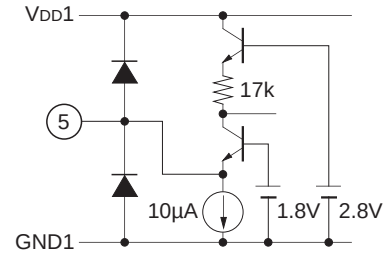
Pin No.	Symbol	I/O	Description	Input pin for open status
1	TRAP		External trap connection	
2	GND1		Analog (4.5V) GND	
3	SYNC IN	I	Video input for sync separation	
4	H.FIL OUT	O	Video output for sync input	
5	S.SEP IN	I	Sync separation circuit input	
6	EXT R	I	External digital input R	
7	EXT G	I	External digital input G	
8	EXT B	I	External digital input B	
9	VD IN	I	External vertical sync input	H
10	TEST1		Test (Leave this pin open.)	
11	TEST2		Test (Leave this pin open.)	
12	RPD	O	Phase comparator output	
13	$V_{SS}1$		Digital (3V) GND for oscillation cell	
14	CKI	I	Oscillation cell input	
15	CKO	O	Oscillation cell output	
16	$V_{DD}1$		Digital 3V power supply	
17	XHST	O	XH start pulse output (HST reversed polarity)	
18	HST	O	H start pulse output	
19	HCK2	O	H clock pulse 2 output	
20	HCK1	O	H clock pulse 1 output	
21	XPCG	O	XPCG pulse output (PCG reversed polarity)	
22	PCG	O	PCG pulse output	
23	HD	O	HD pulse output	
24	FLD IN	I	Field identification input	H
25	XVST	O	XV start pulse output (VST reversed polarity)	
26	VST	O	V start pulse output	
27	VCK2	O	V clock pulse 2 output	
28	VCK1	O	V clock pulse 1 output	
29	XEN	O	XEN pulse output (EN reversed polarity)	
30	EN	O	EN pulse output	
31	$V_{SS}2$		Digital (3V) GND	
32	VD	O	VD pulse output	

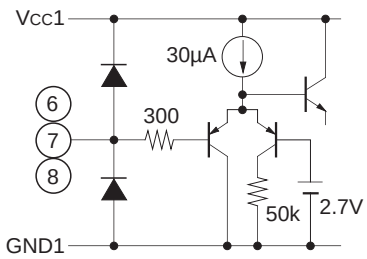
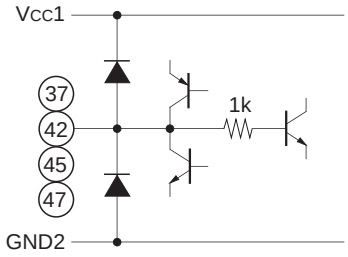
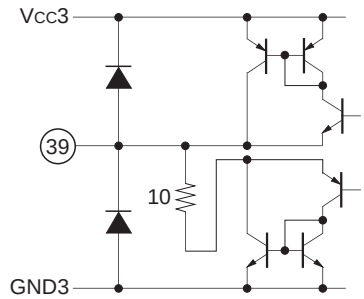
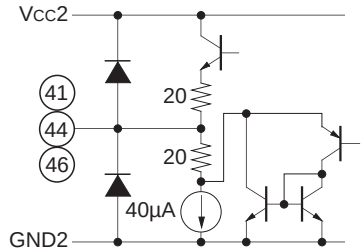
(H: Pull up)

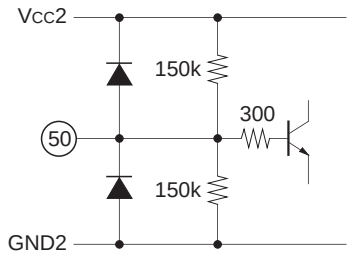
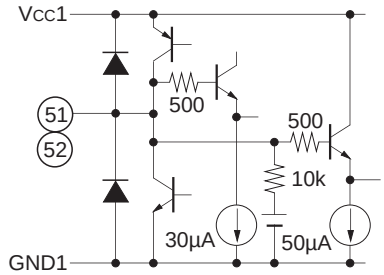
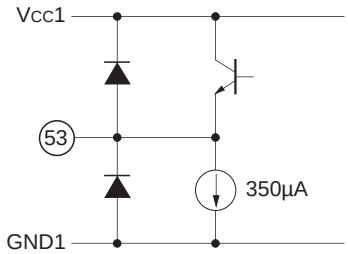
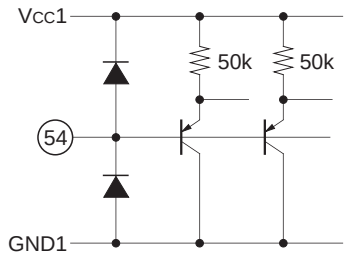
Pin No.	Symbol	I/O	Description	Input pin for open status
33	SCLK	I	Serial interface clock input	H
34	DATA	I	Serial interface data input	H
35	LOAD	I	Serial interface load input	H
36	RGT	I	Switches between Normal scan (H) and Reverse scan (L)	H
37	FB PSIG	O	PSIG signal DC voltage feedback circuit capacitor connection	
38	GND3		Analog (12V) GND for PSIG	
39	PSIG	O	PSIG output	
40	Vcc3		Analog 12V power supply for PSIG	
41	B OUT	O	B signal output	
42	FB B	O	B signal DC voltage feedback circuit capacitor connection	
43	GND2		Analog (12V) GND	
44	G OUT	O	G signal output	
45	FB G	O	G signal DC voltage feedback circuit capacitor connection	
46	R OUT	O	R signal output	
47	FB R	O	R signal DC voltage feedback circuit capacitor connection	
48	Vcc2		Analog 12V power supply	
49	Vcc1		Analog 4.5V power supply	
50	SIG.CENTER	I	R, G, B and PSIG output DC voltage adjustment	
51	B-Y IN	I	B-Y demodulator input (or B-Y color difference signal input)	
52	R-Y IN	I	R-Y demodulator input (or R-Y color difference signal input)	
53	C OUT	O	Chroma signal output	
54	BLK LIM	I	Black peak limiter level adjustment	
55	APC	O	APC detective filter connection	
56	VXO OUT	O	VXO output	
57	VXO IN	I	VXO input	
58	V REG	O	Constant voltage capacitor connection	
59	C IN	I	Chroma signal input	
60	TEST3	I	Test (Connect to GND.)	
61	Y IN	I	Y signal input	
62	PIC	I	Y signal frequency response adjustment	
63	F0 ADJ	O	Internal filter adjusting resistor connection	
64	PWRST	—	System reset	

(H: Pull up)

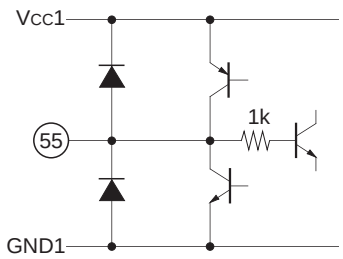
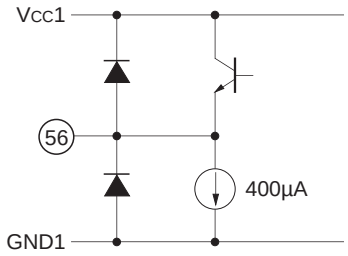
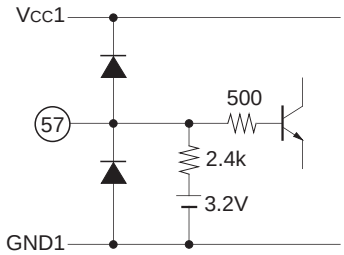
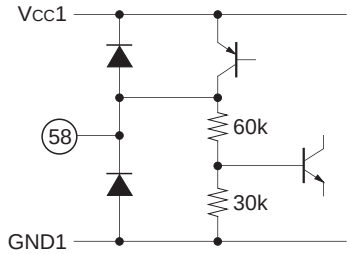
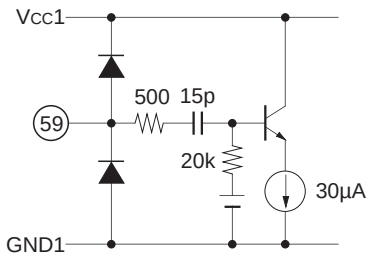
Analog Block Pin Description

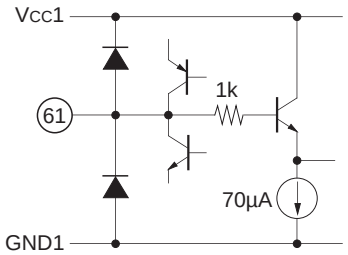
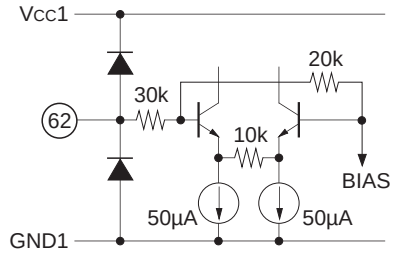
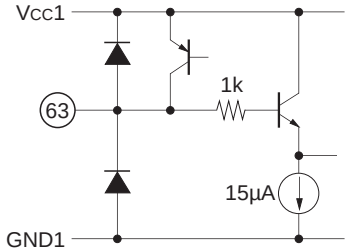
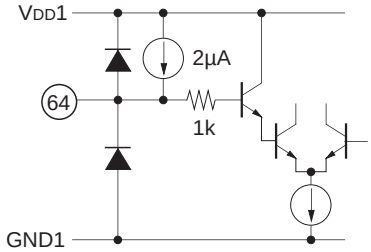
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	TRAP	—		External trap connection. Connect the trap between this pin and GND to remove the chroma component. Leave this pin open when using Y/C and Y/color difference input.
2	GND1	0V		Analog (4.5V) GND.
3	SYNC IN	1.5V		Sync input. Normally inputs the Y signal. The standard signal input level is 0.5Vp-p (100% white level from the sync tip).
4	H.FIL OUT	0.8V		Outputs the video signal for input to the sync separation circuit.
5	S.SEP IN	2.1V		Sync separation circuit input. Input the H.FIL OUT (4pin) signal.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	EXT-R	—		External digital signal inputs. There are two threshold values: Vth1 (= 1.0V) and Vth2 (= 2.0V). When one of the RGB signals exceeds Vth1, all of the RGB outputs go to black level; when an input exceeds Vth2, only the corresponding output goes to white level.
7	EXT-G			
8	EXT-B			
37	FB PSIG	2.0V		Smoothing capacitor connection for the feedback circuit of R, G, B and PSIG output DC level control. Use a low-leakage capacitor because of high impedance.
42	FB B			
45	FB G			
47	FB GR			
38	GND3	0V		Analog (12V) GND for the PSIG circuit.
39	PSIG	$\frac{Vcc2}{2}$		PSIG signal outputs.
40	Vcc3	12V		12V power supply for the PSIG circuit.
41	B OUT	$\frac{Vcc2}{2}$		RGB signal outputs.
44	G OUT			
46	R OUT			
43	GND2	0V		Analog (12V) GND.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
48	Vcc2	12V		12V power supply.
49	Vcc1	4.5V		4.5V power supply.
50	SIG. CENTER	6.0V		RGB output DC voltage control. When used with a Vcc2 and Vcc3 of 12V or more, apply 6V from an external source.
51	B-Y IN	—		Color difference demodulation circuit inputs. Color difference signal is input when using Y/color difference input. At this time, the standard signal input level is 0.3Vp-p and the clamp level is approximately 2.8V. Pin 53 signal is input in other modes (except D-PAL*). At this time, the DC level is approximately 1.6V.
52	R-Y IN			
53	C OUT	1.6V		Color adjusted chroma signal output. The burst level is 180mVp-p (typ.). (540mVp-p during D-PAL.) Leave this pin open when using Y/color difference input.
54	BLK LIM	—		Sets the RGB output amplitude (black-black) clip level and the blanking black level for during wide display.

* D-PAL is a demodulation method that uses an external delay line during demodulation;
S-PAL is a demodulation method that internally processes chroma demodulation.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
55	APC	2.7V		APC detective filter connection. Leave this pin open when using Y/color difference input.
56	VXO OUT	2.9V		VXO output. Leave this pin open when using Y/color difference input.
57	VXO IN	3.2V		VXO input. Leave this pin open when using Y/color difference input.
58	V REG	3.6V		Smoothing capacitor connection for the internally generated constant voltage source circuit. Connect a capacitor of 1µF or more.
59	C IN	—		Video signal input when using composite input. Chroma signal input when using Y/C signal input. Leave this pin open when using Y/color difference input.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
61	Y IN	3.1V		Y signal input. The standard signal input level is 0.5Vp-p (100% white level from the sync tip). Input at low impedance (75Ω or less).
62	PIC	—		Adjusts frequency response of luminance signal. Increasing the voltage emphasizes contours.
63	F0 ADJ	3.0V		Connect resistance of 15kΩ between this pin and GND1 to adjust the internal filters using the outflow current value. Connect to +4.5V power supply when using Y/C or Y/color difference input.
64	PWRST	—		TG block system reset pin. The system is reset when this pin is connected to GND. Connect a capacitor between this pin and GND.

Setting Conditions for Measuring Electrical Characteristics

Use the electrical characteristics measurement circuit on page 30 when measuring electrical characteristics. Also, the TG (timing generator) block must be initialized by performing Settings 1 and 2 below.

Setting 1. System reset

After turning on the power, set SW64 to ON and start up V64 from GND in order to activate the TG block system reset. (See Fig. 1-1.)

The serial bus will be set to default values.

Setting 2. Horizontal AFC adjustment

Input SIG5 (VL = 0mV) to (A) and adjust V14 so that WL and WH of the TP12 output waveform are the same. (See Fig. 1-2.)

Note) When measuring a band of 2MHz or more for Y signal frequency response or sharpness response among the items being measured, the measurement must be made with sample-and-hold timing (serial bus) set to through (sample-and- hold not performed).

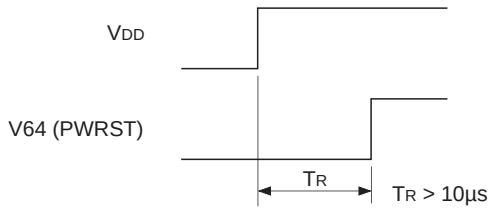


Fig. 1-1. System reset

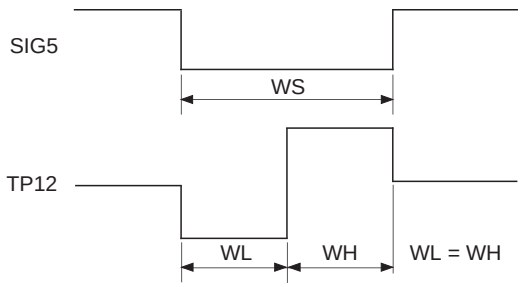


Fig. 1-2. Horizontal AFC adjustment

Electrical Characteristics — DC Characteristics

Unless otherwise specified, Settings 1 and 2 and the following setting conditions are required.
$V_{CC}1$ = 4.5V, $V_{CC}2$ = 12.0V, $V_{CC}3$ = 12.0V, GND1 = GND2 = GND3 = 0V, $V_{DD}1$ = 3.0V, $V_{SS}1$ = $V_{SS}2$ = 0V, Ta = 25°C
SW54, SW62, SW64 = ON
SW6, SW7, SW8, SW59 = A
SW51, SW52 = B
V54 = 0V, V62 = 2.2V
Set the serial bus registers to the "Serial Bus Register Initial Settings". Unspecified the serial bus registers should be set to default settings.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply characteristics						
Current consumption $V_{CC}1$	$I_{CC}11$	Input SIG4 to (A) and SIG2 (0dB) to (B). Measure the $I_{CC}1$ current value. COMP input mode	23	30	37	mA
	$I_{CC}12$	Input SIG4 to (A) and SIG2 (0dB) to (B). Measure the $I_{CC}1$ current value. Y/C input mode	21	28	35	mA
	$I_{CC}13$	Input SIG4 to (A), (D) and (E). Measure the $I_{CC}1$ current value. SW51, SW52 = A, SW59 = B Y/color difference input mode	17	23	29	mA
Current consumption $V_{CC}2$, 3	$I_{CC}2A$	Input SIG4 to (A) and SIG2 (0dB) to (B). Measure the $I_{CC}2$ current value. PSIG load capacity CLP = 0pF	6	8	10	mA
	$I_{CC}2B$	Input SIG4 to (A) and SIG2 (0dB) to (B). Adjust PSIG-BRT of the serial bus and measure the $I_{CC}2$ current value when TP39 output is set to 5Vp-p. PSIG load capacity CLP = 10000pF	6	8.3	10.5	mA
Current consumption V_{DD}	$I_{DD}1$	Input SIG4 to (A) and SIG2 (0dB) to (B). Measure the I_{DD} current value. DCX501 and LCX018 (4:3) mode	6	8	10	mA
	$I_{DD}2$	Input SIG4 to (A) and SIG2 (0dB) to (B). Measure the I_{DD} current value. LCX018 (16:9) mode	7.5	10	12.5	mA

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Digital block I/O characteristics						
Low level input voltage	VIL	Digital block input pin*1			0.3V_{DD}	V
High level input voltage	VIH	Digital block input pin*1	0.7V_{DD}			V
Input current	II1	Input pin with pull-up resistor*2 VIN = V_{SS}2	–145	–60	–24	µA
CKI pin low input current	II2	VIN = V_{SS}	–10			µA
CKI pin high input current	II3	VIN = V_{DD}1			10	µA
High level output voltage Output pins except CKO and RPD	VOH1	IOH = –1mA*3	2.8			V
Low level output voltage Output pins except CKO and RPD	VOL1	IOL = 1mA*3			0.3	V
High level output voltage CKO pin	VOH2	IOH = –3mA	0.5V_{DD}			V
Low level output voltage CKO pin	VOL2	IOL = 3mA			0.5V_{DD}	V
High level output voltage RPD pin	VOH3	IOH = –0.5mA	V_{DD} – 1.2			V
Low level output voltage RPD pin	VOL3	IOL = 0.7mA			1.0	V
Output off leak current RPD pin	IOFF	High impedance status VOUT = V_{SS} or VOUT = V_{DD}1	–40		40	µA

*1 Digital block input pins: SCLK, DATA, LOAD, VDIN, RGT, FLDIN, CKI

*2 Input pins with pull-up resistors: SCLK, DATA, LOAD, VDIN, RGT, FLDIN

*3 Output pins except CKO and RPD: XHST, HST, HCK1, HCK2, XPCG, PCG, HD, XVST, VST, VCK1, VCK2, XEN, EN, VD

Electrical Characteristics — AC Characteristics

Unless otherwise specified, Settings 1 and 2 and the following setting conditions are required.
$V_{CC}1$ = 4.5V, $V_{CC}2$ = 12.0V, $V_{CC}3$ = 12.0V, GND1 = GND2 = GND3 = 0V, $V_{DD}1$ = 3.0V, $V_{SS}1$ = $V_{SS}2$ = 0V, Ta = 25°C
SW54, SW62, SW64 = ON
SW6, SW7, SW8 = A
SW51, SW52, SW59 = B
V54 = 0V, V62 = 2.2V
Set the serial bus registers to the "Serial Bus Register Initial Values". Unspecified serial bus registers should be set to default settings.
Unless otherwise specified, measure the non-inverted outputs for TP41, TP44 and TP46.

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Y signal block							
Video maximum gain	GV	Input SIG4 to (A) and measure the ratio between the output amplitude (white-black) and input amplitude at TP44.		19	22	25	dB
Contrast characteristics TYP	GCNTTP	Input SIG4 to (A) and measure the ratio between the output amplitude (white-black) and input amplitude at TP44.		13	17	21	dB
Contrast characteristics MIN	GCNTMN	Input SIG4 to (A) and measure the ratio between the output amplitude (white-black) and input amplitude at TP44.		–9	–5	–1	dB
Y signal frequency response 1	FCYYC	Assume the output amplitude at TP44 when SIG7 (0dB, no burst, 100kHz) is input to (A) as 0dB. Vary the frequency of the input signal to obtain the frequency with an output amplitude of –3dB. V62 = 1.5V	Y/C input	5.0			MHz
	FCYCMN		Composite input (NTSC)	2.5			MHz
	FCYCMP		Composite input (PAL)	3.0			MHz
Y signal frequency response 2	FCL	Assume the output amplitude at TP44 when SIG7 (0dB, no burst, 100kHz) is input to (A) as 0dB. Vary the frequency of the input signal to obtain the frequency with an output amplitude of –3dB. V62 = 1.5V, Load 500pF		5.0			MHz
Picture quality adjustment variable amount 1 (Y/C input)	GSHP1X	Assume the output amplitude at TP44 when SIG7 (100kHz) is input to (A) as 0dB. Set SIG7 to 2.5MHz and measure GSHP1X and GSHP1N as the amounts by which the output amplitude at TP44 changes when V62 = 4V and 0V, respectively.		10	14		dB
	GSHP1N				–2	0	dB
Picture quality adjustment variable amount 2 (composite input)	GSHP2X	Assume the output amplitude at TP44 when SIG7 (100kHz) is input to (A) as 0dB. Set SIG7 to 2.0MHz and measure GSHP2X and GSHP2N as the amounts by which the output amplitude at TP44 changes when V62 = 4V and 0V, respectively.		6	9		dB
	GSHP2N				–4	–2	dB
Carrier leak (residual carrier)	CRLEKY	Input SIG2 (0dB) to (A). Using a spectrum analyzer, measure the input and the 3.58MHz or 4.43MHz component of TP44, and obtain CRLEKY = 150mV × $10^{\Delta CLK/20}$ using their difference ΔCLK.				30	mV
Y signal I/O delay time	TDYYC	Input SIG9 (VL = 150mV) to (A). Measure the delay time from the 2T pulse peak of the input signal to the peak of the non-inverted output at TP44.	Y/C input	250	350	450	ns
	TDYCMN		Composite input (NTSC)	570	670	770	ns
	TDYCMP		Composite input (PAL)	570	670	770	ns

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Chroma signal block							
ACC amplitude characteristics 1	ACC1	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB/+6dB/–20dB, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B). Measure the output amplitude at TP53, assuming the output corresponding to 0dB, +6dB and –20dB as V0, V1 and V2, respectively. ACC1 = 20 log (V1/V0) ACC2 = 20 log (V2/V0) SW59 = A	NTSC	–3	0	3	dB
			PAL	–3	0	3	dB
ACC amplitude characteristics 2	ACC2		NTSC	–4	–1	2	dB
			PAL	–4	–1	2	dB
APC pull-in range	FAPCN	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B). Changing the SIG2 burst frequency, measure the frequency f1 at which the TP44 output appears (the killer mode is canceled). NTSC: FAPCN = f1 – 3579545Hz PAL: FAPCP = f1 – 4433619Hz SW59 = A	NTSC	±500			Hz
	FAPCP		PAL	±500			Hz
Color adjustment characteristics MAX	GCOLMX	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz burst/chroma phase = 180°) to (B). Assume the chroma output amplitude when serial bus register COLOR = 80H, 0FFH and 0H as V0, V1 and V2, respectively. GCOLMX = 20 log (V1/V0) GCOLMN = 20 log (V2/V0) SW59 = A		4	6		dB
Color adjustment characteristics MIN	GCOLMN				–25	–15	dB
HUE adjustment range MAX	HUEMX	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, burst/chroma phase variable) to (B). Assume the phase at which the output amplitude at TP44 reaches a minimum when serial bus register HUE = 80H, 0FFH and 0H as θ0, θ1 and θ2, respectively. HUEMX = θ1 – θ0 HUEMN = θ2 – θ0 SW59 = A		–30	–40		deg
HUE adjustment range MIN	HUEMN			30	60		deg
Killer operation input level	ACKN	Input SIG5 (VL = 150mV) to (A) and SIG2 (level variable, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B), and measure the output amplitude at TP44. Gradually reduce the SIG3 amplitude level and measure the level at which the killer operation is activated. SW59 = A	NTSC		–37	–31	dB
	ACKP		PAL		–34	–28	dB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Demodulation output amplitude ratio (NTSC)	VRBN	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz) to (B) and change the chroma phase. Assume the maximum amplitude at TP41 as VB, the maximum amplitude at TP44 as VG, and the maximum amplitude at TP46 as VR. VRBN = VR/VB, VGBN = VG/VB SW59 = A	0.53	0.63	0.73	
	VGBN		0.25	0.32	0.39	
Demodulation output phase difference (NTSC)	θRBN	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz) to (B) and change the chroma phase. Assume the phase at which the amplitude at TP41, TP44 and TP46 reaches a maximum as θB, θG and θR, respectively. θRBN = θR – θB, θGBN = θG – θB SW59 = A	99	109	119	deg
	θGBN		230	242	254	deg
Demodulation output amplitude ratio (PAL)	VRBP	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 4.43MHz) to (B) and change the chroma phase. Assume the maximum amplitude at TP41 as VB, the maximum amplitude at TP44 as VG, and the maximum amplitude at TP46 as VR. VRBP = VR/VB, VGBP = VG/VB SW59 = A	0.65	0.75	0.85	
	VGBP		0.33	0.40	0.47	
Demodulation output phase difference (PAL)	θRBP	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 4.43MHz) to (B) and change the chroma phase. Assume the phase at which the amplitude at TP41, TP44 and TP46 reaches a maximum as θB, θG and θR, respectively. θRBP = θR – θB, θGBP = θG – θB SW59 = A	80	90	100	deg
	θGBP		232	244	256	deg
Color difference input color adjustment characteristics MAX	GEXCMX	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D). Assume the output amplitude at TP41 (100kHz) when serial bus register COLOR = 80H as VC0, when COLOR = 0H as VC2, and when SIG1 is set to -10dB and COLOR = 0FFH as VC1. GEXCMX = 20 log (VC1/VC0) + 10 GEXCMN = 20 log (VC2/VC0) SW51, SW52 = A	4	6		dB
Color difference input color adjustment characteristics MIN	GEXCMN			–20	–15	dB
Color difference balance	VEXCBL	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D) and (E). Assume the output amplitude at TP41 (100kHz) as VB and the output amplitude at TP46 (100kHz) as VR. VEXCBL = VR/VB SW51, SW52 = A	0.8	1.0	1.2	
Color difference input balance adjustment R	GEXRMX	Input SIG5 (VL = 150mV) to (A) and SIG1 (–6dB, 100kHz, no burst) to (D) and (E). Assume the output amplitude at TP46 (100kHz) and TP41 (100kHz) when serial bus register HUE = 80H as VR0 and VB0, respectively, when HUE = 0FFH as VR1 and VB1, respectively, and when HUE = 0H as VR2 and VB2, respectively. GEXRMX = 20 log (VR1/VR0) GEXRMN = 20 log (VR2/VR0) GEXBMX = 20 log (VB1/VB0) GEXBMN = 20 log (VB2/VB0) SW51, SW52 = A	2	3		dB
	GEXRMN			–3	–2	dB
Color difference input balance adjustment B	GEXBMX			–3	–2	dB
	GEXBMN		2	3		dB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
G-Y matrix characteristics (NTSC)	VEXGBN	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D). Assume the output amplitude at TP41 (100kHz) as VEXB and the output amplitude at TP44 (100kHz) as VEXBG. VEXGBN = VEXBG/VEXB SW51, SW52 = A	0.22	0.25	0.28	
	VEXGRN	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (E). Assume the output amplitude at TP46 (100kHz) as VEXR and the output amplitude at TP44 (100kHz) as VEXRG. VEXGRN = VEXRG/VEXR SW51, SW52 = A	0.47	0.53	0.58	
G-Y matrix characteristics (PAL)	VEXGBP	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D). Assume the output amplitude at TP41 (100kHz) as VEXB and the output amplitude at TP44 (100kHz) as VEXBG. VEXGBP = VEXBG/VEXB SW51, SW52 = A	0.16	0.19	0.22	
	VEXGRP	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (E). Assume the output amplitude at TP46 (100kHz) as VEXR and the output amplitude at TP44 (100kHz) as VEXRG. VEXGRP = VEXRG/VEXR SW51, SW52 = A	0.48	0.53	0.58	
RGB signal output block						
RGB signal and PSIG output DC voltage	VOUT	Input SIG5 (VL = 0mV) to (A). Adjust serial bus register BRIGHT so that the output (black-black) at TP44 is 9Vp-p and measure the DC voltage at TP39, TP41, TP44 and TP46.	5.85	6.00	6.15	V
RGB signal and PSIG output DC voltage difference	ΔVOUT	Input SIG5 (VL = 0mV) to (A). Adjust serial bus register BRIGHT so that the output (black-black) at TP44 is 9Vp-p, measure the DC voltage at TP39, TP41, TP44 and TP46, and obtain the maximum difference between each of these values.		0	100	mV
RGB and PSIG output limiter operation voltage	VLIMMX	Input SIG3 to (A). Vary V54 and measure the maximum value VLIMMX and minimum value VLIMMN of the voltage range (black-black) over which the black limiter operates for the TP39, TP41, TP44 and TP46 outputs. Assume the value whenV54 = 0V as VLIMMX, and when V54 = 4.5V as VLIMMN.	9.0			Vp-p
	VLIMMN				5.2	Vp-p
Amount of change in brightness	BRTMX	Input SIG5 (VL = 0mV) to (A) and measure the output (black-black) at TP41, TP44 and TP46 when serial bus register BRIGHT = 0H.	9.0			Vp-p
	BRTMN	Input SIG5 (VL = 0mV) to (A) and measure the output (black-black) at TP41, TP44 and TP46 when serial bus register BRIGHT = 0FFH.			4.0	Vp-p

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Amount of change in PSIG	PSIGMX	Input SIG5 (VL = 0mV) to (A) and measure the output (black-black) at TP39 when serial bus register PSIG-BRT = 0H.			1.5	Vp-p
	PSIGMN	Input SIG5 (VL = 0mV) to (A) and measure the output (black-black) at TP39 when serial bus register PSIG-BRT = 0FFH.	9.0			Vp-p
Amount of change in sub-brightness	SBBRT	Input SIG5 (VL = 0mV) to (A) and measure the difference between the outputs (black-black) at TP41 and TP46 and the output (black-black) at TP44 when serial bus registers R-BRT = B-BRT = 0H and when R-BRT = B-BRT = 0FFH.	±1.5	±2.0		V
Difference in gain between RGB output signals	ΔGRGB	Input SIG4 to (A) and obtain the level difference between the maximum and minimum non-inverted output amplitudes (white-black) at TP41, TP44 and TP46.	–0.5	0	0.5	dB
Difference in RGB output inverted/non-inverted gain	ΔGINV	Input SIG4 to (A) and obtain the level difference between the non-inverted output amplitudes (white-black) and the inverted output amplitudes at TP41, TP44 and TP46.	–0.5	0	0.5	dB
Difference in black level potential between RGB output signals	ΔVBL	Input SIG4 to (A) and obtain the level difference between the maximum and minimum black levels of both the inverted and non-inverted outputs at TP41, TP44 and TP46.			300	mV
γ gain	Gγ1	Input SIG8 to (A). Adjust the non-inverted output black level at TP44 to 6.0 - 4.5V with serial bus register BRIGHT and the non-inverted output amplitude (white-black) at TP44 to 3.5V with serial bus register CONTRAST. Measure VG1, VG2 and VG3. Gγ1 = 20 log (VG1/0.0357) Gγ2 = 20 log (VG2/0.0357) Gγ3 = 20 log (VG3/0.0357) (See Fig. 5 for definitions of VG1, VG2 and VG3.)	23.0	26.0	29.0	dB
	Gγ2		12.0	15.0	18.0	dB
	Gγ3		18.0	21.0	25.0	dB
γ1 adjustment variable range	Vγ1MN	Input SIG8 to (A) and adjust serial bus register BRIGHT so that the output at TP44 is 9Vp-p (black-black). Read the point where the gain of the non-inverted output at TP44 changes when serial bus register γ1 = 0H and 0FFH from the input signal IRE level. Vγ1MN when γ1 = 0H, and Vγ1MX when γ1 = 0FFH.			0	IRE
	Vγ1MX		100			IRE
γ2 adjustment variable range	Vγ2MN	Input SIG8 to (A) and adjust serial bus register BRIGHT so that the output at TP44 is 9Vp-p (black-black). Read the point where the gain of the non-inverted output at TP44 changes when serial bus register γ2 = 0H and 0FFH from the input signal IRE level. Vγ2MN when γ2 = 0H, and Vγ2MX when γ2 = 0FFH.	100			IRE
	Vγ2MX				0	IRE
PSIG transition time	tPSIGH	Input SIG4 to (A) and adjust serial bus register PSIG-BRT so that the output at TP39 is 9Vp-p (black-black). Measure the time it takes to change to an amplitude of 9Vp-p. tPSIGH: rising edge, tPSIGL: falling edge		1.5	3.0	µs
	tPSIGL			1.5	3.0	µs
RGB output white limiter operation voltage	VWLIM	Input SIG5 (VL = 350mV) to (A) and measure the voltage (white-white) at which the white limiter activates for inverted output and non-inverted output at TP41, TP44 and TP46, respectively.	1.3	1.5	1.7	V
Black limiter DC voltage difference	ΔVBLIM	Input SIG5 (VL = 0mV) to (A) and adjust V54 so that the output at TP44 is 9Vp-p (black-black). Measure the DC voltage at TP41, TP44 and TP46 and obtain the difference versus the RGB output voltage VOUT.		0	100	mV

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
White limiter DC voltage difference	ΔVWLIM	Input SIG5 (VL = 350mV) to (A). Measure the DC voltage at TP41, TP44 and TP46 and obtain the difference versus the RGB output voltage VOUT.			0	100	mV
RGB output range when FRP polarity reverse is stopped	VDROFF	Input SIG8 to (A). Assume the black limiter level of the output at TP41, TP44 and TP46 when serial bus register BRIGHT = 0H as VDRB and the white limiter level when BRIGHT = OFFH as VDRW. VDROFF = VDRW – VDRB		3.0			V
Filter characteristics							
Amount of BPF attenuation	ATBPF	Assume the chroma amplitude at TP53 when SIG5 (VL = 0mV) is input to (A) and SIG1 (0dB at input center frequency (3.58Hz or 4.43Hz)) is input to (B) as 0dB. Obtain the amount by which the output at TP53 is attenuated when the frequencies noted on the right are input. SW59 = A	NTSC 1.5MHz		–16	–10	dB
			PAL 2.0MHz		–16	–10	dB
			NTSC 5.5MHz		–7	–2	dB
			PAL 6.8MHz		–8	–3	dB
Amount of TRAP attenuation	ATRAPN	Input SIG2 (0dB, 3.58Hz and 4.43Hz) to (A) and measure the output at TP44. Assume the amplitude at TP44 during Y/C input mode as 0dB, and obtain the amount of attenuation during COMP input mode.	NTSC		–40	–30	dB
	ATRAPP		PAL		–40	–30	dB
R-Y, B-Y and LPF characteristics	DEMLPF	Assume the amplitude of the 100kHz component of the output at TP44 when SIG5 (VL = 150mV) is input to (A) and SIG1 (0dB, 3.58Hz + 100kHz) is input to (B) as 0dB. Obtain the frequency which attenuates the beat component of the output by 3dB when the SIG1 frequency is increased with respect to 3.58MHz. SW59 = A		0.8	1.0	1.3	MHz
Sync separation, TG block							
Input sync signal width sensitivity	WSSEP	Input SIG5 (VL = 0mV, VS = 143mV, WS variable) to (A) and confirm that it is synchronized with the HD output at TP23. Gradually narrow the WS of SIG5 from 4.7µs and obtain the WS at which synchronization with the HD output at TP23 is lost.		2.0			µs
Sync separation input sensitivity	VSSEP	Input SIG5 (VL = 0mV, WS = 4.7µs, VS = variable) to (A) and confirm that it is synchronized with the HD output at TP23. Gradually reduce the VS of SIG5 from 143mV and obtain the VS at which synchronization with the HD output at TP23 is lost.			40	60	mV
Sync separation output delay time	TDSYL	Input SIG5 (VL = 0mV, WS = 4.7µs, VS = 143mV) to (A) and measure the delay time with the RPD output at TP12. TDSYL is from the falling edge of the input HSYNC to the falling edge of the RPD output at TP12, and TDSYH is from the falling edge of the input HSYNC to the rising edge of the RPD output at TP12.		430	630	830	ns
	TDSYH			4.7	5.0	5.3	µs
Horizontal pull-in range	HPLLN	Input SIG5 (VL = 0mV, WS = 4.7µs, VS = 143mV, horizontal frequency variable) to (A) and confirm that it is synchronized with the HD output at TP23. Obtain the frequency f_H at which the input and output are synchronized by changing the horizontal frequency of SIG5 from the non-synchronized condition. HPLLN = f_H – 15734 HPLLP = f_H – 15625	NTSC	±500			Hz
	HPLLP		PAL	±500			Hz

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output transition time (P12*3 pin)	tTLH	Input SIG5 (VL = 0mV) to (A). Measure the transition time for each output. Load = 30pF (See Fig. 3.)			30	ns
	tTHL				30	ns
Cross-point time difference	ΔT	Input SIG5 (VL = 0mV) to (A). Measure HCK1/HCK2. Load = 30pF (See Fig. 4.)			10	ns
HCK duty	DTYHC	Input SIG5 (VL = 0mV) to (A). Measure the HCK1/HCK2 duty. Load = 30pF	47	50	53	%
External I/O characteristics						
External RGB input threshold voltage	VTEXTB	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL variable) to (C). Raise the SIG6 amplitude (VL) from 0V and assume the voltage where the outputs at TP41, TP44 and TP46 go to black level as VTEXTB. Then raise the amplitude further and assume the voltage where these outputs go to white level as VTEXTW. SW6, SW7, SW8 = B	0.8	1.0	1.2	V
	VTEXTW		1.8	2.0	2.2	V
Propagation delay time between external RGB input and output	TDEXTH	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 3V) to (C). Measure the rise delay time TD1EXT and the fall delay time TD2EXT of the outputs at TP41, TP44 and TP46. (See Fig. 2.) SW6, SW7, SW8 = B	50	100	150	ns
	TDEXTL		50	100	150	ns
Output blanking level during external RGB input	EXTBK	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 1.7V) to (C). Measure the difference from the black level of the outputs at TP41, TP44 and TP46. SW6, SW7, SW8 = B			0	V
Output white level during external RGB input	EXTWT	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 2.7V) to (C). Measure the difference from the black level of the outputs at TP41, TP44 and TP46. SW6, SW7, SW8 = B	3.5			V
Minimum pulse width during external RGB input	TEXTMIN	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 2.7V) to (C). Measure the minimum pulse width at which each of the outputs at TP41, TP44 and TP46 reach the white limiter. SW6, SW7, SW8 = B			180	ns
Serial transfer block						
Data setup time	ts0	LOAD setup time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
	ts1	DATA setup time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
Data hold time	th0	LOAD hold time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
	th1	DATA hold time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
Minimum pulse width	tw1L	SCLK pulse width. (See Fig. 6.)		160		ns
	tw1H	SCLK pulse width. (See Fig. 6.)		160		ns
	tw2	LOAD pulse width. (See Fig. 6.)	1			µs

Description of Electrical Characteristics Measurement Methods

Serial Bus Register Initial Values

	Item	Symbol	Serial bus													
			Mode settings					DAC settings								
			Input	System	Panel	Aspect	S/H	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2	PSIG-BRT
Setting 2	Horizontal AFC adjustment		COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
Power supply characteristics	Current consumption $V_{CC}1$	$I_{CC}11$	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
		$I_{CC}12$	Y/C	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
		$I_{CC}13$	Y/color difference	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Current consumption $V_{CC}2,3$	$I_{CC}2A$	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
		$I_{CC}2B$	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	78H
	Current consumption V_{DD}	$I_{DD}1$	COMP	NTSC	—	4:3	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
		$I_{DD}2$	COMP	NTSC	LCX018	16:9	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
Digital block I/O characteristics	Low level input voltage	VIL	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	High level input voltage	VIH	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Input current	II1	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	CKI pin low input current	II2	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	CKI pin high input current	II3	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	High level output voltage	VOH1	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Low level output voltage	VOL1	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	High level output voltage	VOH2	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Low level output voltage	VOL2	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	High level output voltage	VOH3	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Low level output voltage	VOL3	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Output off leak current	IOFF	COMP	NTSC	—	—	SHS1	80H	80H	80H	80H	80H	80H	0H	0H	80H

(–: don't care, ADJ: adjustment, SET: setting)

	Item	Symbol	Serial bus													
			Mode settings					DAC settings								
			Input	System	Panel	Aspect	S/H	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2	PSIG-BRT
Y signal block	Video maximum gain	GV	COMP	NTSC	—	—	Through	80H	80H	0A0H	0FFH	80H	80H	0H	0H	80H
	Contrast characteristics TYP	GCNTTP	COMP	NTSC	—	—	Through	80H	80H	0A0H	80H	80H	80H	0H	0H	80H
	Contrast characteristics MIN	GCNTMN	COMP	NTSC	—	—	Through	80H	80H	0A0H	0H	80H	80H	0H	0H	80H
	Y signal frequency response 1	FCYYC	Y/C	NTSC	—	—	Through	80H	80H	0A0H	80H	80H	80H	0H	0H	80H
		FCYCMN	COMP	NTSC	—	—	Through	80H	80H	0A0H	80H	80H	80H	0H	0H	80H
		FCYCMP	COMP	PAL	—	—	Through	80H	80H	0A0H	80H	80H	80H	0H	0H	80H
	Y signal frequency response 2	FCL	Y/C	NTSC	—	—	Through	80H	80H	0A0H	80H	80H	80H	0H	0H	80H
	Picture quality adjustment variable amount 1	GSHP1X	Y/C	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
		GSHP1N	Y/C	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Picture quality adjustment variable amount 2	GSHP2X	COMP	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
		GSHP2N	COMP	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Carrier leak	CRLEKY	COMP	—	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Y signal I/O delay time	TDYYC	Y/C	—	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
		TDYCMN	COMP	NTSC	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
		TDYCMP	COMP	PAL	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H

(–: don't care, ADJ: adjustment, SET: setting)

Item		Symbol	Serial bus													
			Mode settings					DAC settings								
			Input	System	Panel	Aspect	S/H	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2	PSIG-BRT
Chroma signal block	ACC amplitude characteristics 1	ACC1	COMP	NTSC	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
		ACC1	COMP	PAL	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
	ACC amplitude characteristics 2	ACC2	COMP	NTSC	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
		ACC2	COMP	PAL	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
	APC pull-in range	FAPCN	COMP	NTSC	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
		FAPCP	COMP	PAL	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
	Color adjustment characteristics MAX	GCOLMX	COMP	NTSC	—	—	Through	80H	0FFH	96H	80H	80H	80H	0H	0H	80H
	Color adjustment characteristics MIN	GCOLMN	COMP	NTSC	—	—	Through	80H	0H	96H	80H	80H	80H	0H	0H	80H
	HUE adjustment range MAX	HUEMX	COMP	NTSC	—	—	Through	0FFH	80H	96H	80H	80H	80H	0H	0H	80H
	HUE adjustment range MIN	HUEMN	COMP	NTSC	—	—	Through	0H	80H	96H	80H	80H	80H	0H	0H	80H
	Killer operation input level	ACKN	COMP	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
		ACKP	COMP	PAL	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Demodulation output amplitude ratio NTSC	VRBN	COMP	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
		VGBN	COMP	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Demodulation output phase difference NTSC	θRBN	COMP	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
		θGBN	COMP	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Demodulation output amplitude ratio PAL	VRBP	COMP	PAL	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
		VGBP	COMP	PAL	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Demodulation output phase difference PAL	θRBP	COMP	PAL	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
		θGBP	COMP	PAL	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H

(–: don't care, ADJ: adjustment, SET: setting)

Item		Symbol	Serial bus													
			Mode settings					DAC settings								
			Input	System	Panel	Aspect	S/H	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2	PSIG-BRT
Chroma signal block	Color difference input color adjustment characteristics MAX	GEXCMX	Y/color difference	—	—	—	Through	80H	0FFH	96H	80H	80H	80H	0H	0H	80H
	Color difference input color adjustment characteristics MIN	GEXCMN	Y/color difference	—	—	—	Through	80H	0H	96H	80H	80H	80H	0H	0H	80H
	Color difference balance	VEXCBL	Y/color difference	—	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
	Color difference input balance adjustment R	GEXRMX	Y/color difference	—	—	—	Through	0FFH	80H	96H	80H	80H	80H	0H	0H	80H
		GEXRMN	Y/color difference	—	—	—	Through	0H	80H	96H	80H	80H	80H	0H	0H	80H
	Color difference input balance adjustment B	GEXBMX	Y/color difference	—	—	—	Through	0FFH	80H	96H	80H	80H	80H	0H	0H	80H
		GEXBMN	Y/color difference	—	—	—	Through	0H	80H	96H	80H	80H	80H	0H	0H	80H
	G-Y matrix characteristics NTSC	VEXGBN	Y/color difference	NTSC	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
		VEXGRN	Y/color difference	NTSC	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
	G-Y matrix characteristics PAL	VEXGBP	Y/color difference	PAL	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
		VEXGRP	Y/color difference	PAL	—	—	Through	80H	80H	96H	80H	80H	80H	0H	0H	80H
RGB signal output block	RGB signal and PSIG output DC voltage	VOUT	—	—	—	—	Through	80H	80H	ADJ	80H	80H	80H	0H	0H	64H
	RGB signal and PSIG output DC voltage difference	ΔVOUT	—	—	—	—	Through	80H	80H	ADJ	80H	80H	80H	0H	0H	64H
	RGB and PSIG output limiter operation voltage	VLIMMX	—	—	—	—	Through	80H	80H	0H	80H	80H	80H	0H	0H	0FFH
		VLIMMN	—	—	—	—	Through	80H	80H	0H	80H	80H	80H	0H	0H	0FFH
	Amount of change in brightness	BRTMX	—	—	—	—	Through	80H	80H	0H	80H	80H	80H	0H	0H	0FFH
		BRTMN	—	—	—	—	Through	80H	80H	0FFH	80H	80H	80H	0H	0H	0FFH
	Amount of change in PSIG	PSIGMX	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	0FFH
		PSIGMN	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	0H

(–: don't care, ADJ: adjustment, SET: setting)

	Item	Symbol	Serial bus													
			Mode settings					DAC settings								
			Input	System	Panel	Aspect	S/H	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2	PSIG-BRT
RGB signal output block	Amount of change in sub-brightness	SBBRT	—	—	—	—	Through	80H	80H	0B4H	80H	SET	SET	0H	0H	80H
	Difference in gain between RGB output signals	ΔGRGB	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Difference in RGB output inverted/non-inverted gain	ΔGINV	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Difference in black level potential between RGB output signals	ΔVBL	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
	γ gain	Gγ1	—	—	—	—	Through	80H	80H	ADJ	ADJ	80H	80H	78H	0D7H	80H
		Gγ2	—	—	—	—	Through	80H	80H	ADJ	ADJ	80H	80H	78H	0D7H	80H
		Gγ3	—	—	—	—	Through	80H	80H	ADJ	ADJ	80H	80H	78H	0D7H	80H
	γ1 adjustment variable range	Vγ1MN	—	—	—	—	Through	80H	80H	ADJ	46H	80H	80H	0H	0H	80H
		Vγ1MX	—	—	—	—	Through	80H	80H	ADJ	46H	80H	80H	0FFH	0H	80H
	γ2 adjustment variable range	Vγ2MN	—	—	—	—	Through	80H	80H	ADJ	46H	80H	80H	0H	0H	80H
		Vγ2MX	—	—	—	—	Through	80H	80H	ADJ	46H	80H	80H	0H	0FFH	80H
	PSIG transition time	tPSIGH	—	—	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	0FFH
		tPSIGL	—	—	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	0FFH
	RGB output white limiter operation voltage	VWLIM	—	—	—	—	Through	80H	80H	0B4H	0FFH	80H	80H	0H	0H	80H
	Black limiter DC voltage difference	ΔVBLIM	—	—	—	—	Through	80H	80H	0H	80H	80H	80H	0H	0H	80H
	White limiter DC voltage difference	ΔVWLIM	—	—	—	—	Through	80H	80H	0B4H	0FFH	80H	80H	0H	0H	80H
	RGB output range when FRP polarity reverse is stopped	VDROFF	—	—	—	—	Through	80H	80H	SET	80H	80H	80H	0H	0H	80H

(–: don't care, ADJ: adjustment, SET: setting)

	Item	Symbol	Serial bus													
			Mode settings					DAC settings								
			Input	System	Panel	Aspect	S/H	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2	PSIG-BRT
Filter characteristics	Amount of BPF attenuation	ATBPF	COMP	—	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Amount of TRAP attenuation	ATRAPN	SET	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
		ATRAPP	SET	PAL	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	R-Y, B-Y and LPF characteristics	DEMLPF	Y/C	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
Sync separation, TG block	Input sync signal width sensitivity	WSSEP	COMP	—	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Sync separation input sensitivity	VSSEP	COMP	—	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Sync separation output delay time	TDSYL	COMP	—	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
		TDSYH	COMP	—	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Horizontal pull-in range	HPLLN	COMP	NTSC	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
		HPLLP	COMP	PAL	—	—	Through	80H	80H	60H	80H	80H	80H	0H	0H	80H
	Output transition time	tTLH	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
		tTHL	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Cross-point time difference	ΔT	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
	HCK duty	DTYHC	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
External I/O characteristics	External RGB input threshold voltage	VTEXTB	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
		VTEXTW	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Propagation delay time between external RGB input and output	TDEXTH	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
		TDEXTL	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Output blanking level during external RGB input	EXTBK	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H
	Output white level during external RGB input	EXTWT	—	—	—	—	Through	80H	80H	64H	80H	80H	80H	0H	0H	80H
	Minimum pulse width during external RGB input	TEXTMIN	—	—	—	—	Through	80H	80H	80H	80H	80H	80H	0H	0H	80H

(–: don't care, ADJ: adjustment, SET: setting)

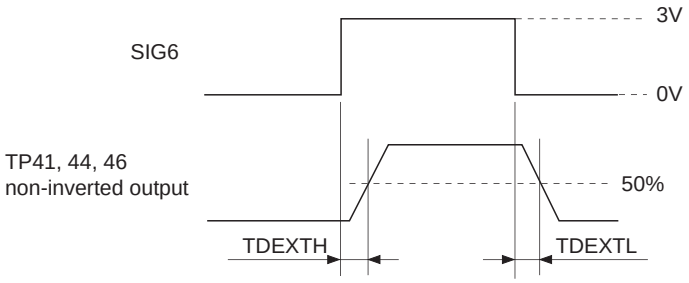


Fig. 2. Conditions for measuring the delay between external RGB input and output

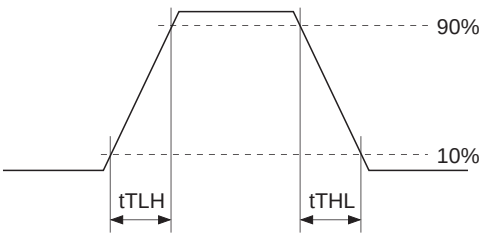


Fig. 3. Output transition time measurement conditions

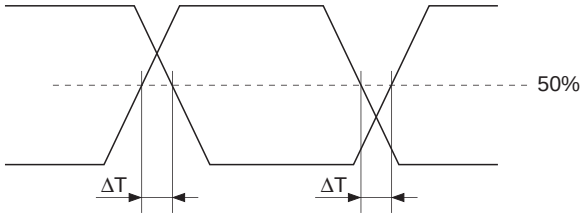


Fig. 4. Cross-point time difference measurement conditions

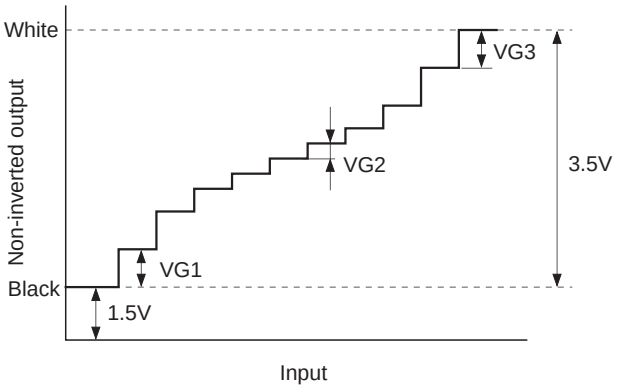


Fig. 5. γ characteristics measurement conditions

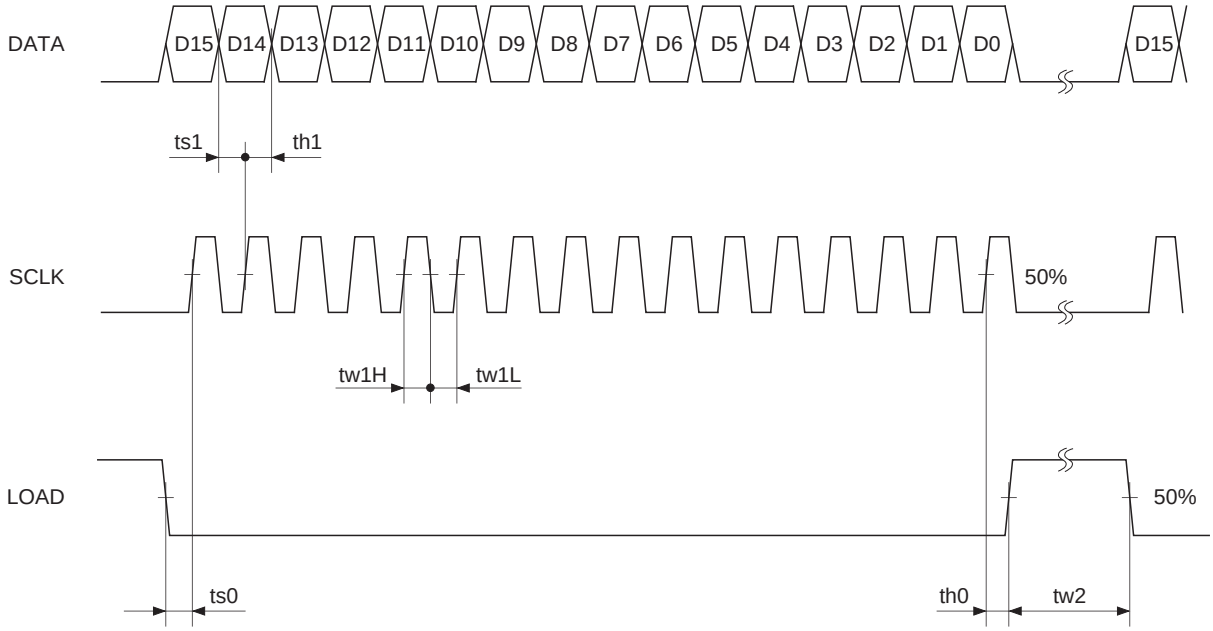
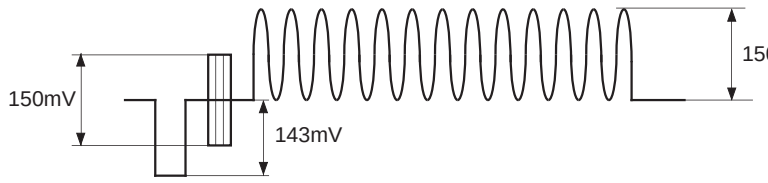
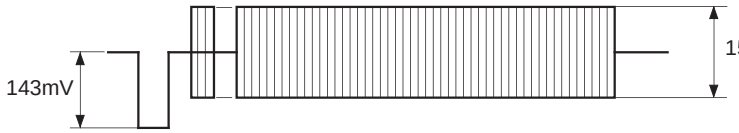
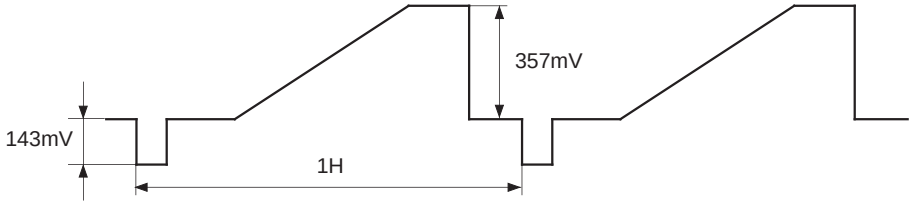
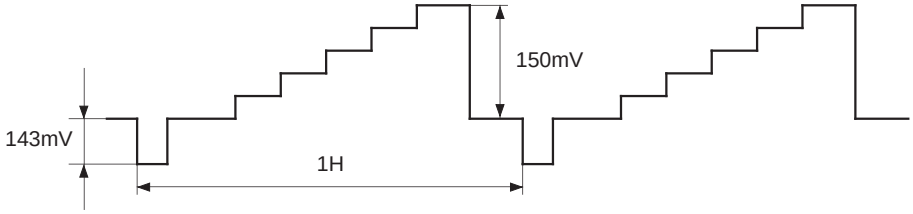
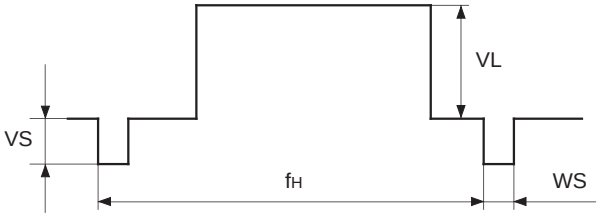
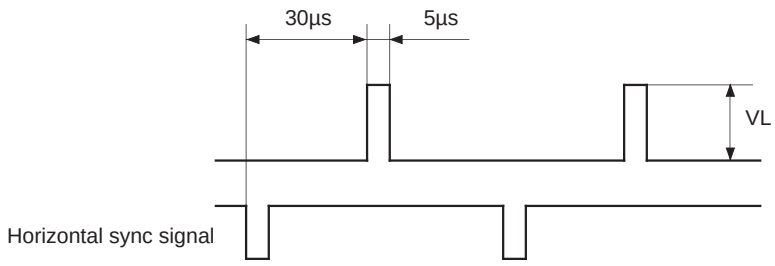
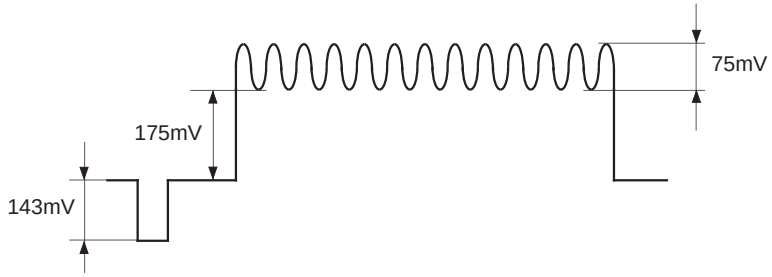
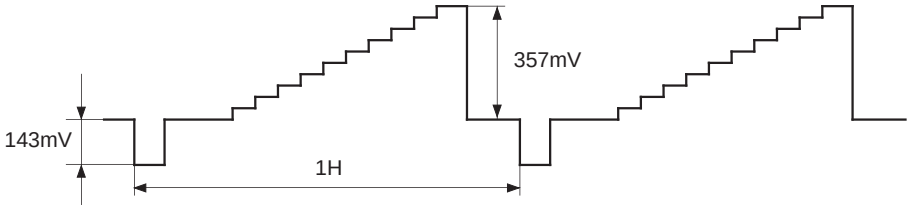
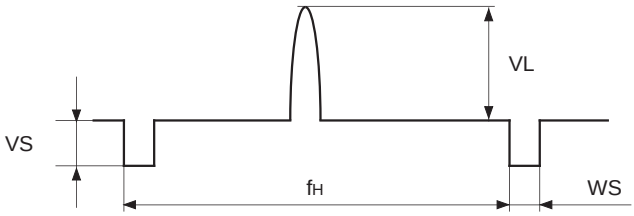


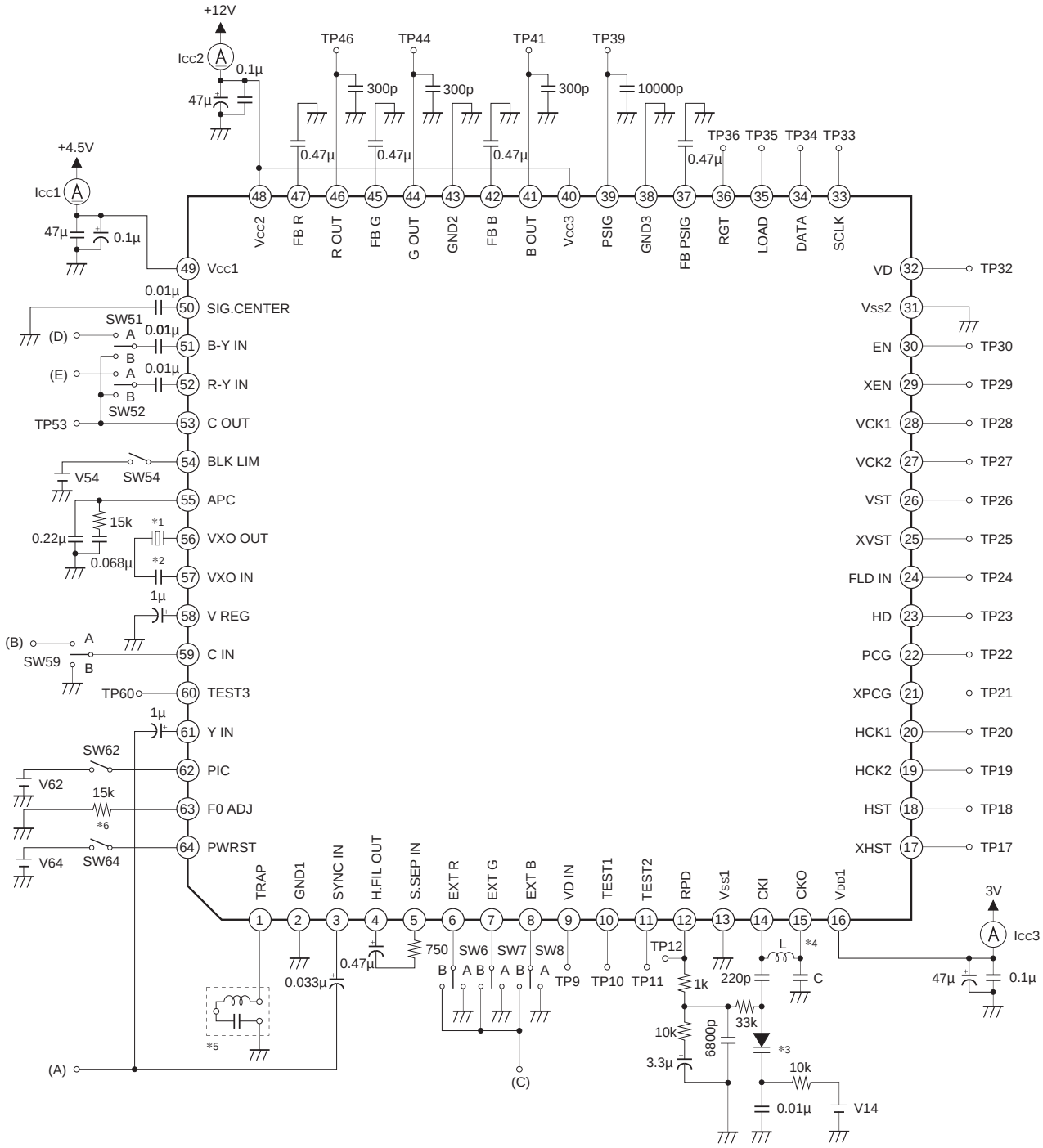
Fig. 6. Serial transfer block measurement conditions

Input Waveforms

SG No.	Waveform
SIG1	Sine wave video signal: With/without burst Amplitude and frequency variable  ← Value noted on left: 0dB
SIG2	Chroma signal: Burst, chroma frequency (3.579545MHz, 4.433619MHz) Chroma phase and burst frequency variable  ← Value noted on left: 0dB
SIG3	Ramp waveform 
SIG4	5-step staircase waveform 
SIG5	 VL amplitude variable VS variable: 143mV unless otherwise specified WS variable: 4.7µs unless otherwise specified fH variable: 15.734kHz (NTSC) or 15.625kHz (PAL) unless otherwise specified

SG No.	Waveform
SIG6	 VL amplitude variable
SIG7	 Frequency variable
SIG8	10-step staircase waveform 
SIG9	2T pulse waveform  VL amplitude variable VS variable: 143mV unless otherwise specified WS variable: 4.7µs unless otherwise specified fH variable: 15.734kHz (NTSC) or 15.625kHz (PAL) unless otherwise specified

Electrical Characteristics Measurement Circuit



*1 Used crystal: KINSEKI CX-5F
Frequency deviation: within ±30ppm, frequency temperature characteristics: within ±30ppm, load capacity: 16pF
NTSC: 3.579545MHz
PAL: 4.433619MHz

*2 NTSC: shorted, PAL: 18pF

*3 Variable Capcitance Diode: 1T369 (SONY)

*4 DCX501 mode: L value: 4.7µH, C value: 22pF
LCX018 (4:3) mode: L value: 4.7µH, C value: 22pF
LCX018 (16:9) mode: L value: 2.2µH, C value: 33pF

*5 Trap (TDK)
NTSC: NLT4532-S3R6B
PAL: NLT4532-S4R4

*6 Resistance value tolerance: ±2%,
temperature coefficient: ±200ppm or less

Description of Operation

The CXA2543R incorporates the three functions of an RGB decoder block, an RGB driver block and a timing generator (TG) block onto a single chip using Bi-CMOS technology.

1) RGB decoder block

- Input mode switching
  The input mode can be switched between composite input, Y/C input and Y/color difference input by the serial bus settings.
  During composite input: The composite signal is input to Pins 3, 59 and 61.
  During Y/C input: The Y signal is input to Pins 3 and 61, and the C signal to Pin 59.
  During Y/color difference input: The Y signal is input to Pins 3 and 61, the B-Y signal to Pin 51, and the R-Y signal to Pin 52.

- System switching
  The input system can be switched between NTSC and PAL (DPAL using external delay lines and SPAL) by the serial bus settings.

- Trap, BPF
  The center frequency of the built-in trap and BPF can be switched to 3.58Hz during NTSC and 4.43Hz during PAL.
  During composite input, the Y signal enters the trap circuit and the C signal enters the BPF. These signals do not pass through the trap or BPF during Y/C input and Y/color difference input.

- ACC detection, ACC amplifier
  The amplitude of the burst signal output from the ACC amplifier is detected and the ACC amplifier is controlled to maintain the burst signal amplitude at a constant level.

- VXO, APC detection
  The VXO local oscillation circuit is a crystal oscillation circuit. The phases of the input burst signal and the VXO oscillator output are compared in the APC detection block, and the detective output is used to form a PLL loop that controls the VXO oscillation frequency, which means that the need for adjustments is eliminated.

- External inputs
  These are digital inputs with two thresholds. When one of the RGB inputs is higher than the lower threshold Vth1 (≈ 1.0V), all RGB outputs go to black level. When the higher threshold Vth2 (≈ 2.0V) is exceeded, the output for only the signal in question goes to white level, while the other outputs remain at black level.

2) RGB driver block

• γ correction

In order to support the characteristics of LCD panels, the I/O characteristics are as shown in Fig. 1. The characteristics change as shown in Fig. 2 by adjusting the serial bus register γ1, and as shown in Fig. 3 by adjusting γ2.

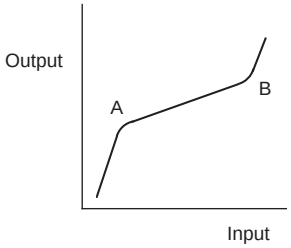


Fig. 1

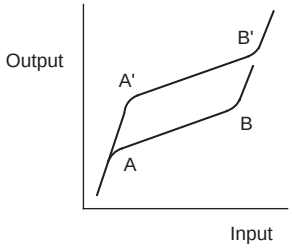


Fig. 2

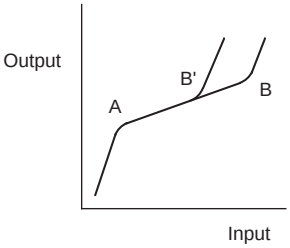
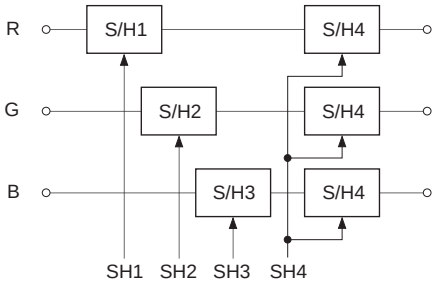
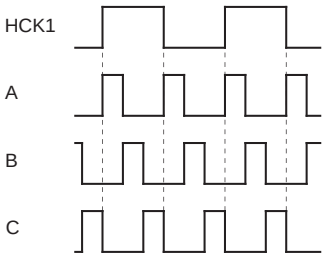


Fig. 3

• Sample-and-hold circuit

As LCD panels sample RGB signals simultaneously, RGB signals output from the CXA2543R must be sampled-and-hold in sync with the LCD panel drive pulses.





DCX501

RGT = H (normal)

	SHS1	SHS2	SHS3
SH1	B	A	C
SH2	Through	Through	Through
SH3	A	C	B
SH4	C	B	A

RGT = L (inverted)

	SHS1	SHS2	SHS3
SH1	B	A	C
SH2	A	C	B
SH3	Through	Through	Through
SH4	C	B	A

SH1: R signal SH pulse
SH2: G signal SH pulse
SH3: B signal SH pulse
SH4: RGB signal SH pulse

LCX018

RGT = H (normal)

	SHS1	SHS2	SHS3
SH1	A	C	B
SH2	B	A	C
SH3	Through	Through	Through
SH4	C	B	A

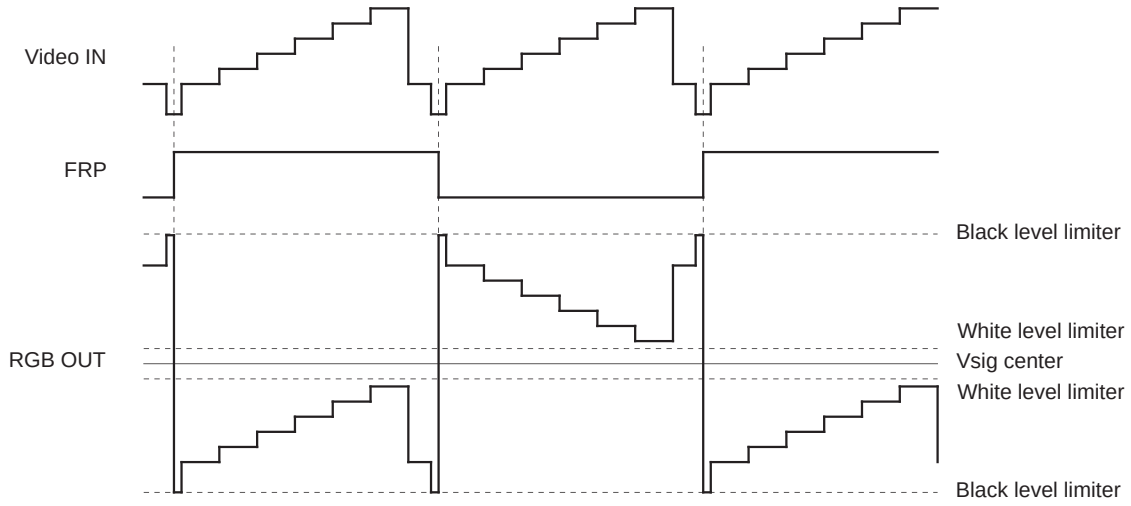
RGT = L (inverted)

	SHS1	SHS2	SHS3
SH1	Through	Through	Through
SH2	B	A	C
SH3	A	C	B
SH4	C	B	A

The sample-and-hold circuit performs sample-and-hold by receiving the SH1 to SH4 pulses from the TG block. Since LCD panels perform color coding using an RGB delta arrangement, each horizontal line must be compensated by 1.5 dots. This relationship is reversed during right/left inversion. This compensation timing is also generated by the TG block. The sample-and-hold timing changes according to the phase relationship with the HCK1 pulse, so the timing should be set to SHS1, 2 or 3 in accordance with the actual board.

• RGB output

RGB outputs (Pins 41, 44, and 46) are inverted each horizontal line by the FRP pulse supplied from the TG block as shown in the figure below. Feedback is applied so that the center voltage (Vsig center) of the output signal matches the reference voltage ($V_{CC}2$ + GND2)/2 (or the voltage input to SIG CENTER (Pin 50)). In addition, the white level output is clipped by the Vsig center ±0.7V, and the black level output is clipped by the limiter operation point that is adjusted at the BLKLIM (Pin 54).

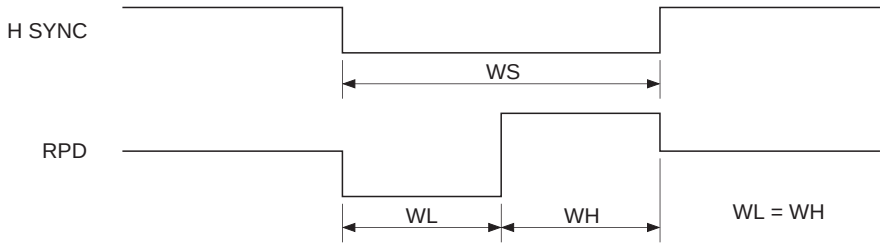


3) TG block

• PLL and AFC circuits

The TG block contains a PLL circuit phase comparator and frequency division counter, and a PLL circuit can be comprised by connecting an external VCO circuit.

The PLL error detection signal is generated at the following timing. The phase comparison output of the entire bottom of HSYNC and the internal frequency division counter becomes RPD. RPD output is converted to DC error with the lag-lead filter, and then it changes the capacitance of variable capacitance diode to stabilize the oscillation frequency at 1066f_H in the DCX501BK and LCX018AK (4:3) mode, 1417f_H in the LCX018AK (16:9) mode. The PLL of this system is adjusted by setting the the reverse bias voltage of the varicap diode (V14) so that the point at which RPD changes is at the center of the window depicted in the figure below.



• H position

The horizontal display position can be set at 2f_H intervals in 32 different ways by the serial bus settings.

The picture center is set at the internal default value, but because there is a difference between the RGB signal and the drive pulse delays on the actual board, the picture center may not match the design center. In this case, adjust with the serial bus.

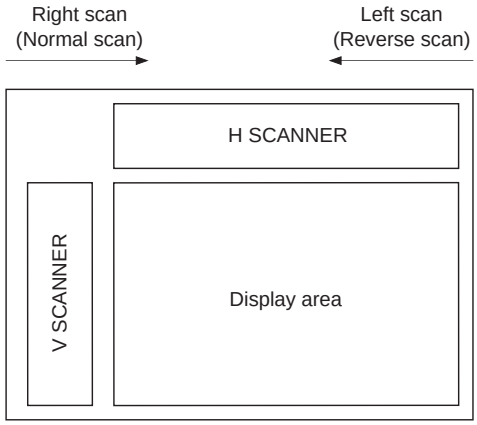
• Right/left inversion

The LCD panel is arranged in a delta arrangement, where identical signal lines are offset by 1.5 dots from adjoining lines. For this reason, a 1.5-bit offset is attached to the horizontal start pulse (HST) between odd lines and even lines. HCK and S/H are also 1.5-bit offset.

When the panel is driven by left scan (Reverse scan), this offset relationship is inverted for even and odd lines. Moreover, since the dot arrangement is asymmetrical, the HST position is also changed.

RGT = H: Right scan mode

RGT = L: Left scan mode



LCD panel

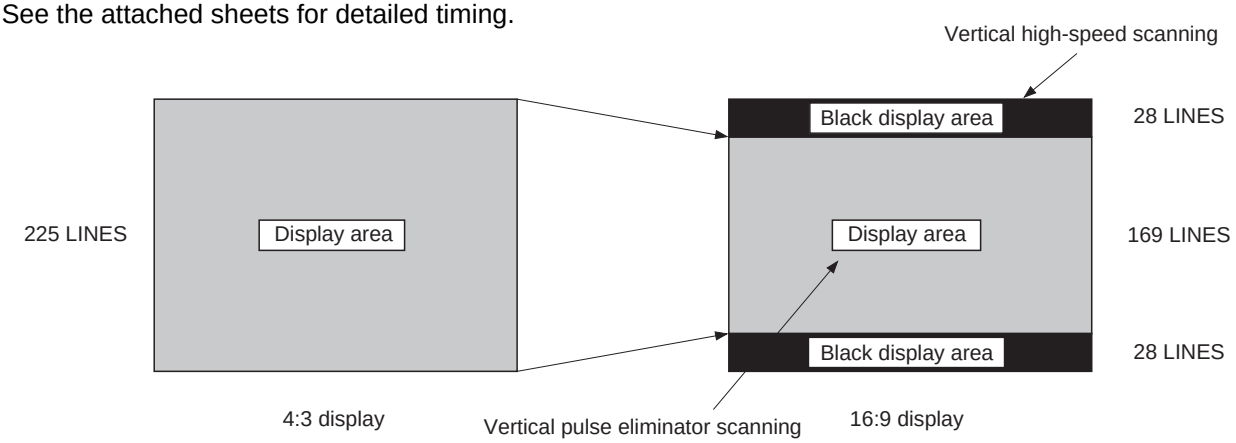
• WIDE mode (DCX501BK mode)

Setting the WIDE mode by switching the aspect with the serial bus shifts the unit to WIDE mode. In the DCX501BK mode, the aspect ratio is converted through pulse eliminator processing, allowing 16:9 quasi-WIDE display. During WIDE mode, vertical pulse eliminator scanning of 1/4 for NTSC or 1/2 and 1/4 for PAL are performed, and the video signal is compressed to achieve a 16:9 aspect ratio. In addition, in areas outside the display area, black is displayed in the 28 lines, respectively at the top and bottom of this display area by performing high-speed scanning

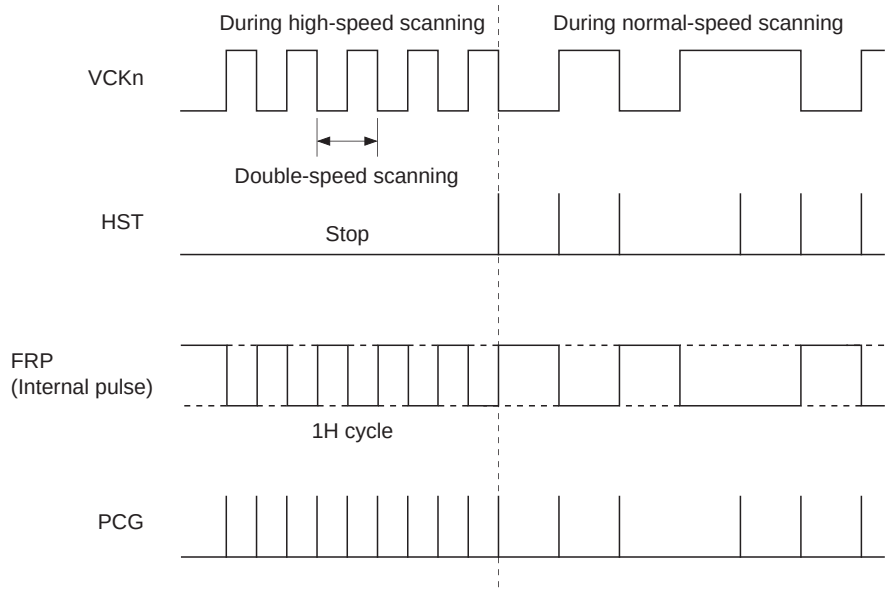
The method of black display is a writing method by PSIG. By setting PSIG level during high-speed scanning to black display level and writing this black display level at the PCG timing, reliable black display is realized within the limited V blanking period.

During this period, HST is masked and video signal input is limited.

See the attached sheets for detailed timing.



DCX501BK



• AC driving of LCD panels during no signal

HST, XHST, HCK1, HCK2, VST, XVST, VCK1, VCK2, PCG, XPCG, EN, XEN, HD, VD, and FRP are made to run freely so that the LCD panel is AC driven even when there is no composite sync from the SYNC IN pin. During this time, the HSYNC separation circuit stops and the PLL counter is made to run freely. In addition, the VSYNC separation circuit is also stopped, so the auxiliary V counter is used to create the reference pulse for generating VD, VST and XVST.

The cycle of this v counter is designed to be 525/2H for NTSC and 625/2H for PAL. However, when there is no vertical sync signal for 5 fields, the no signal state is assumed and the free running VD, VST and XVST pulses are generated from the next field.

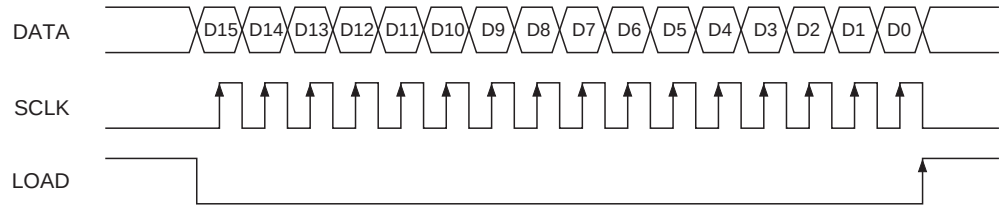
In addition, RPD is kept at high impedance when there is no signal in order to prevent the AFC circuit from causing errors due to phase comparison.

Description of Serial Control Operation

1) Control method

Control data consists of 16 bits of data which is loaded one bit at a time at the rising edge of SCLK. This loading operation starts from the falling edge of LOAD and is completed at the next rising edge. (D13 to D15 are dummy data.)

Digital block control data is established by the vertical sync signal and the LOAD "H". If data is transferred multiple times for the same item, the data immediately before the vertical sync signal is valid.
Analog (electronic attenuator) block control data becomes valid each time the LOAD signal is input.



Serial transfer timing

2) Serial data map

The serial data map is as follows.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	0	0	0	0	0	S/H phase		Aspect	Supported panel	System		Input switching	
*	*	*	0	0	0	0	1	FRP polarity	FRP256 inversion	Up/down inversion	SYNC GEN	Mode	Y/color difference clamp	VD polarity	HD polarity
*	*	*	0	0	0	1	0	0	0	0	0	0	PAL decima -tion	External V SYNC	FIELD determi -nation
*	*	*	0	0	0	1	1	0	0	0	H-POSITION				
*	*	*	0	0	1	0	0	0	0	0	HD-POSITION				
*	*	*	0	0	1	0	1	0	0	PCG width		0	0	PCG position	
*	*	*	0	0	1	1	0	0	0	EN width		0	0	EN position	
*	*	*	1	0	0	0	0	HUE							
*	*	*	1	0	0	0	1	COLOR							
*	*	*	1	0	0	1	0	BRIGHT							
*	*	*	1	0	0	1	1	CONTRAST							
*	*	*	1	0	1	0	0	R-BRT							
*	*	*	1	0	1	0	1	B-BRT							
*	*	*	1	0	1	1	0	γ1							
*	*	*	1	0	1	1	1	γ2							
*	*	*	1	1	0	0	0	PSIG-BRT							
*	*	*	1	1	1	1	1	TEST							

Note) Any data transfer performed when addresses D8, D9, D10, D11, D12 = 1, 1, 1, 1, 1 (shadowed portion) will result in test mode regardless of other data settings.
Do not transfer data with these addresses set this way.

3) Serial data mode settings (X: don't care)

- Input switching

D1	D0	
0	X	Composite input (default)
1	0	Y/C input
1	1	Y/color difference input

- System switching

D3	D2	
0	X	NTSC (default)
1	0	D-PAL
1	1	S-PAL

- Supported panel switching

D4	
0	DCX501BK (default)
1	LCX018AK

- Aspect switching

D5	
0	4:3 (default)
1	16:9

- Sample-and-hold timing switching

D7	D6	
0	0	SHS1 (default)
0	1	SHS2
1	0	SHS3
1	1	Through (sample-and-hold not performed)

- HD output polarity switching

D0	
0	Negative polarity (default)
1	Positive polarity

- VD output polarity switching

D1	
0	Negative polarity (default)
1	Positive polarity

- Y/color difference clamp position switching

This switches the position at which the R-Y and B-Y input signals are clamped during Y/color difference input mode.

D2	
0	Pedestal position (default)
1	SYNC position

- Mode switching

This is the test mode. Set to normal mode.

D3	
0	Normal mode (default)
1	Test mode

• Sync generator function
This stops outputs other than VD and HD of the TG block.

D4
0 OFF (default)
1 ON

Note) Make sure that Vcc2, 3 (12V) and LCD panel power supply should be turned OFF during sync generator ON.

• Up/down inversion function
This switches the up/down inverted display.

D5
0 DOWN (normal display) (default)
1 UP (up/down inverted display)

• FRP256 field inversion
This further inverts the polarity of the RGB output that is inverted every 1H for 256 fields.

D6
0 OFF (default)
1 ON

• FRP polarity inversion function

D7
0 ON (1H inversion) (default)
1 OFF (polarity not inverted)

• External field identification input switching
Internal field identification is not performed and an externally field input source is used.

D0
0 OFF (internal identification) (default)
1 ON (external input)

• External VSYNC input switching
Internal VSYNC separation is not performed and an externally input VSYNC is used.

D1
0 OFF (internal separation) (default)
1 ON (external input)

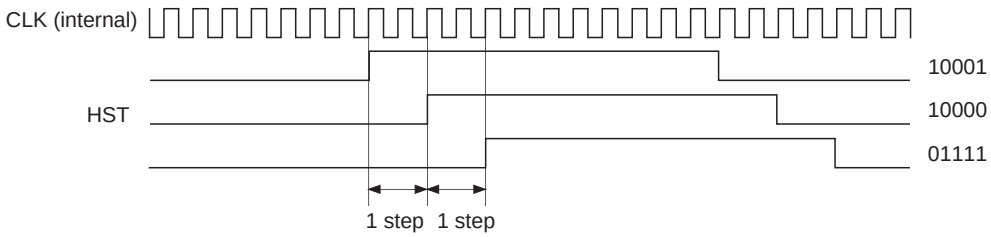
• PAL pulse elimination switching
This switches on/off the PAL pulse elimination function during PAL mode.

D2
0 ON (elimination performed) (default)
1 OFF (elimination not performed)

• H position setting

D4	D3	D2	D1	D0
0	0	0	0	0
:	:	:	:	:
1	0	0	0	0 (default)
:	:	:	:	:
1	1	1	1	1

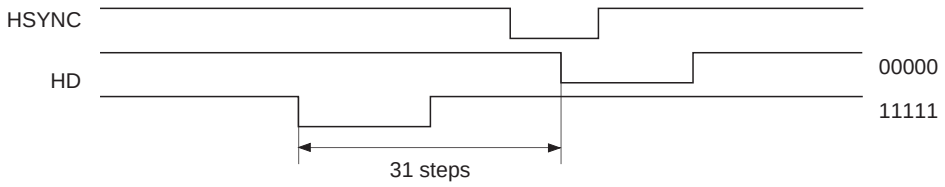
Variable in $2f_H$ (= 1 bit) increments



• HD phase setting

D4	D3	D2	D1	D0
0	0	0	0	0 (default)
:	:	:	:	:
1	1	1	1	1

Variable in $4f_H$ (= 1 bit) increments



• PCG pulse position

This sets the PCG pulse position (A in the figure below).

D1	D0	
0	0	(default)
1	1	

DCX501 and LCX018 (4:3) mode: variable in $6f_H$ (= 1 bit) increments

LCX018 (16:9) mode: variable in $9f_H$ (= 1 bit) increments

• PCG pulse width

This sets the PCG pulse width (B in the figure below).

D5	D4	
0	0	(default)
1	1	

DCX501 and LCX018 (4:3) mode: variable in $8f_H$ (= 1 bit) increments

LCX018 (16:9) mode: variable in $12f_H$ (= 1 bit) increments

• EN pulse position

This sets the EN pulse position (C in the figure below).

D1	D0	
0	0	(default)
1	1	

DCX501 and LCX018 (4:3) mode: variable in $4f_H$ (= 1 bit) increments

LCX018 (16:9) mode: variable in $6f_H$ (= 1 bit) increments

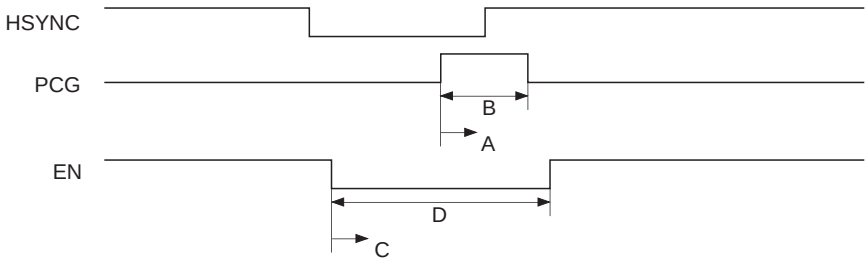
• EN pulse width

This sets the EN pulse width (D in the figure below).

D5	D4	
0	0	(default)
1	1	

DCX501 and LCX018 (4:3) mode: variable in $8f_H$ (= 1 bit) increments

LCX018 (16:9) mode: variable in $12f_H$ (= 1 bit) increments



Setting Correspondence Table

Set the positions and widths for the EN and PCG pulses as follows when driving the DCX501BK and the LCX018AK.

DCX501BK

	Width		Position	
	D5	D4	D1	D0
PCG pulse	0	0	0	0
EN pulse	0	0	0	0

LCX018AK

	Width		Position	
	D5	D4	D1	D0
PCG pulse	1	0	0	0
EN pulse	0	0	1	1

4) Serial data electronic attenuator (D/A converter) settings

• HUE

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• COLOR

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• BRIGHT

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• CONTRAST

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• R-BRT

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• B-BRT

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• $\gamma 1$

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0 (default)

• $\gamma 2$

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0 (default)

• PSIG-BRT

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0 (default)

5) Test mode

Test mode results if data is sent to the following addresses.
For this reason, do not perform data transfer using these addresses.

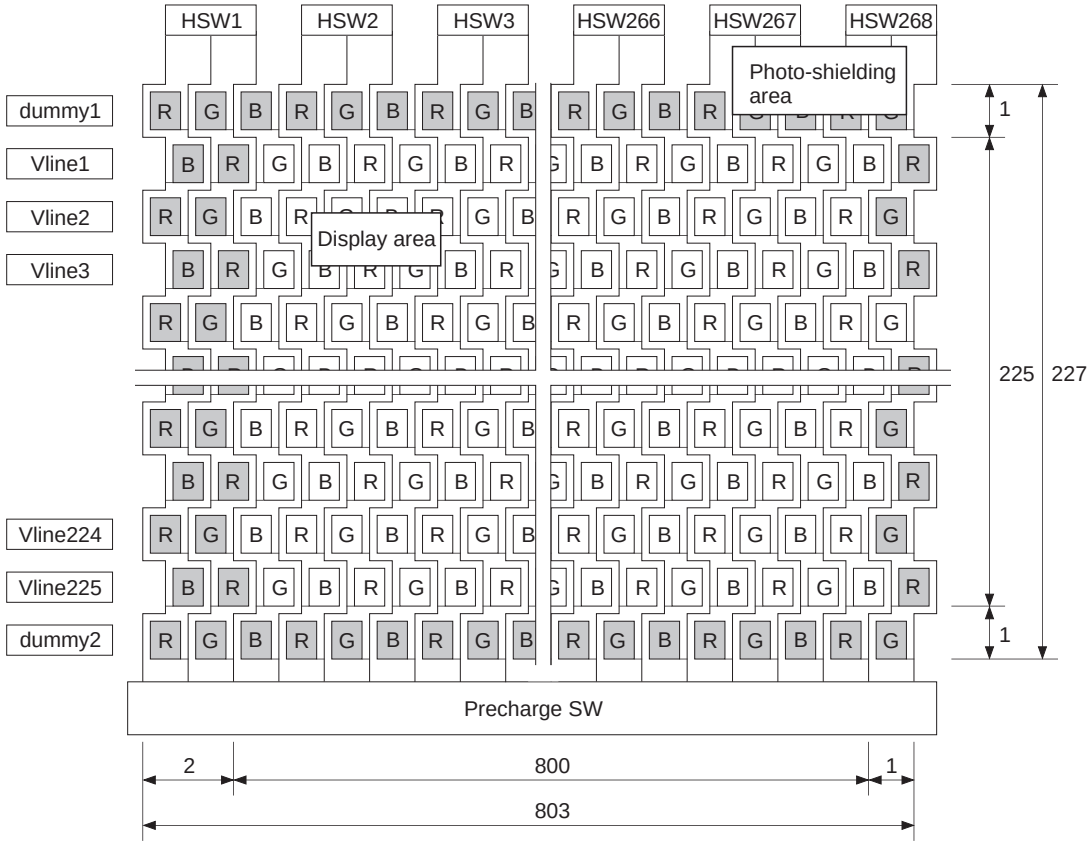
D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	*	*	*	*	*	*	*	*

Note) If data transfer is performed in these addresses, the chip will enter test mode regardless of the data set.

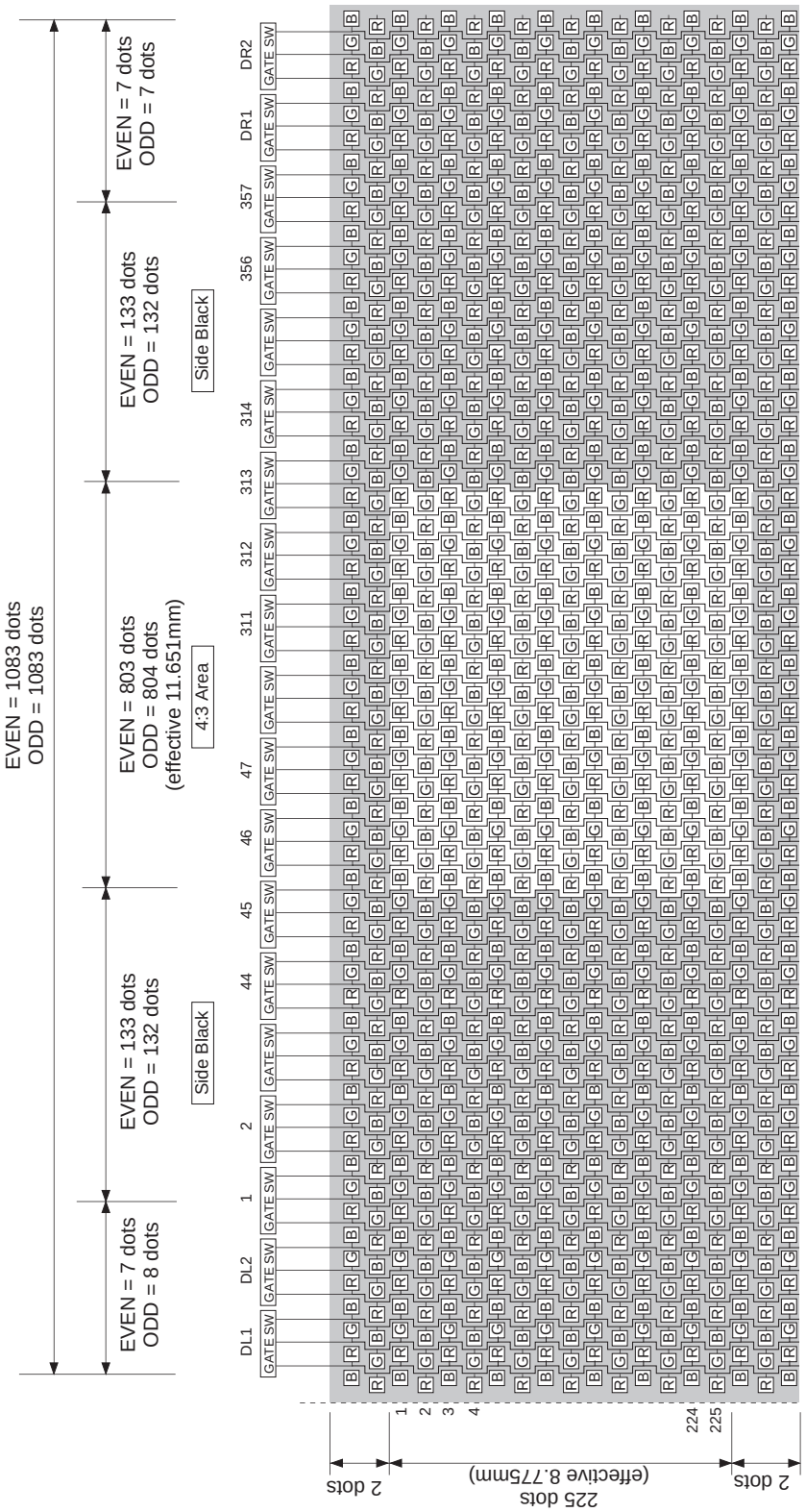
DCX501BK Color Coding Diagram

The delta arrangement is used for the color coding in the LCD panels with which this IC is compatible. Note that the shaded region within the diagram is not displayed.

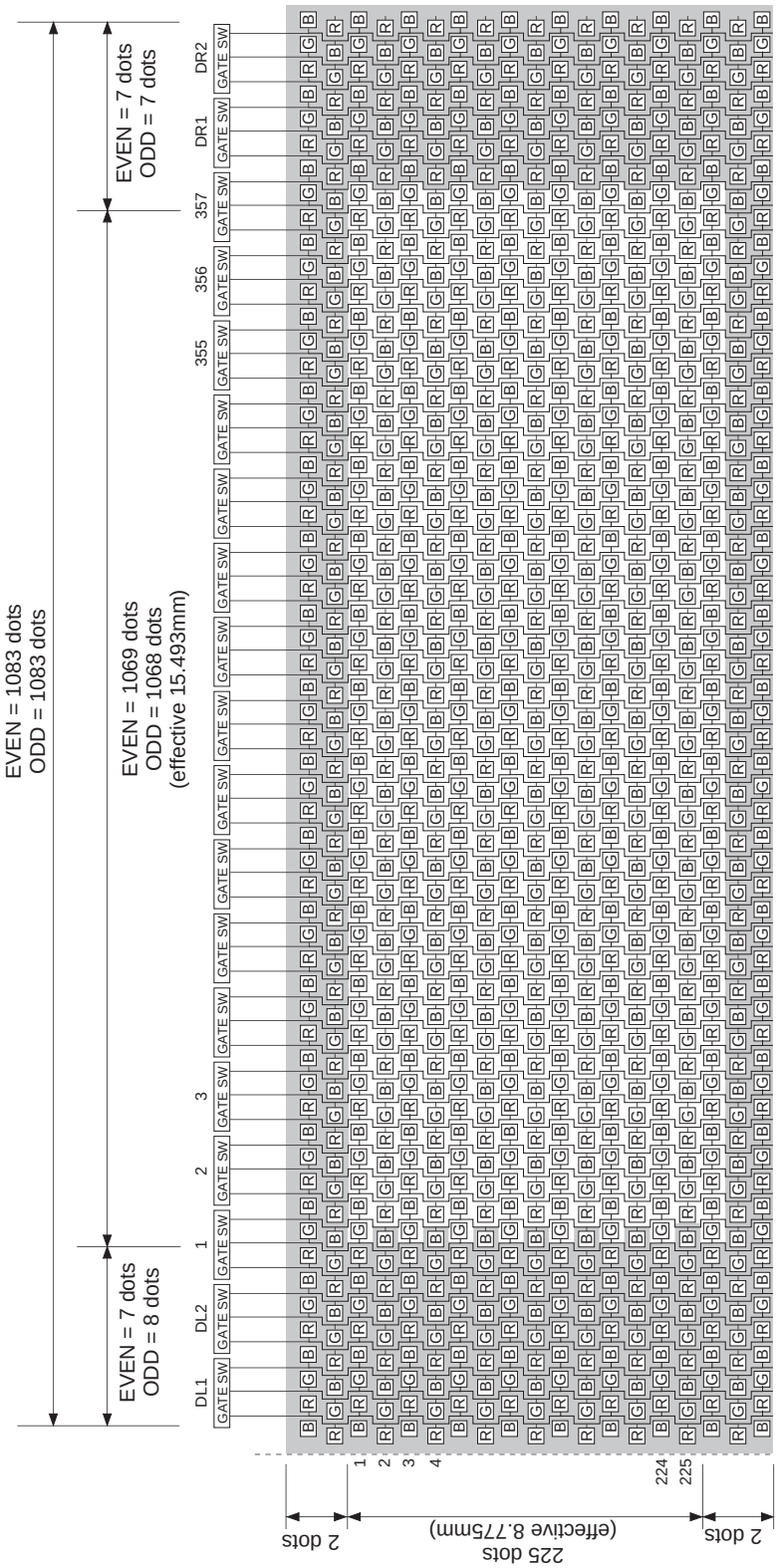
DCX501BK pixel arrangement



LCX018AK Pixel Arrangement (4:3)



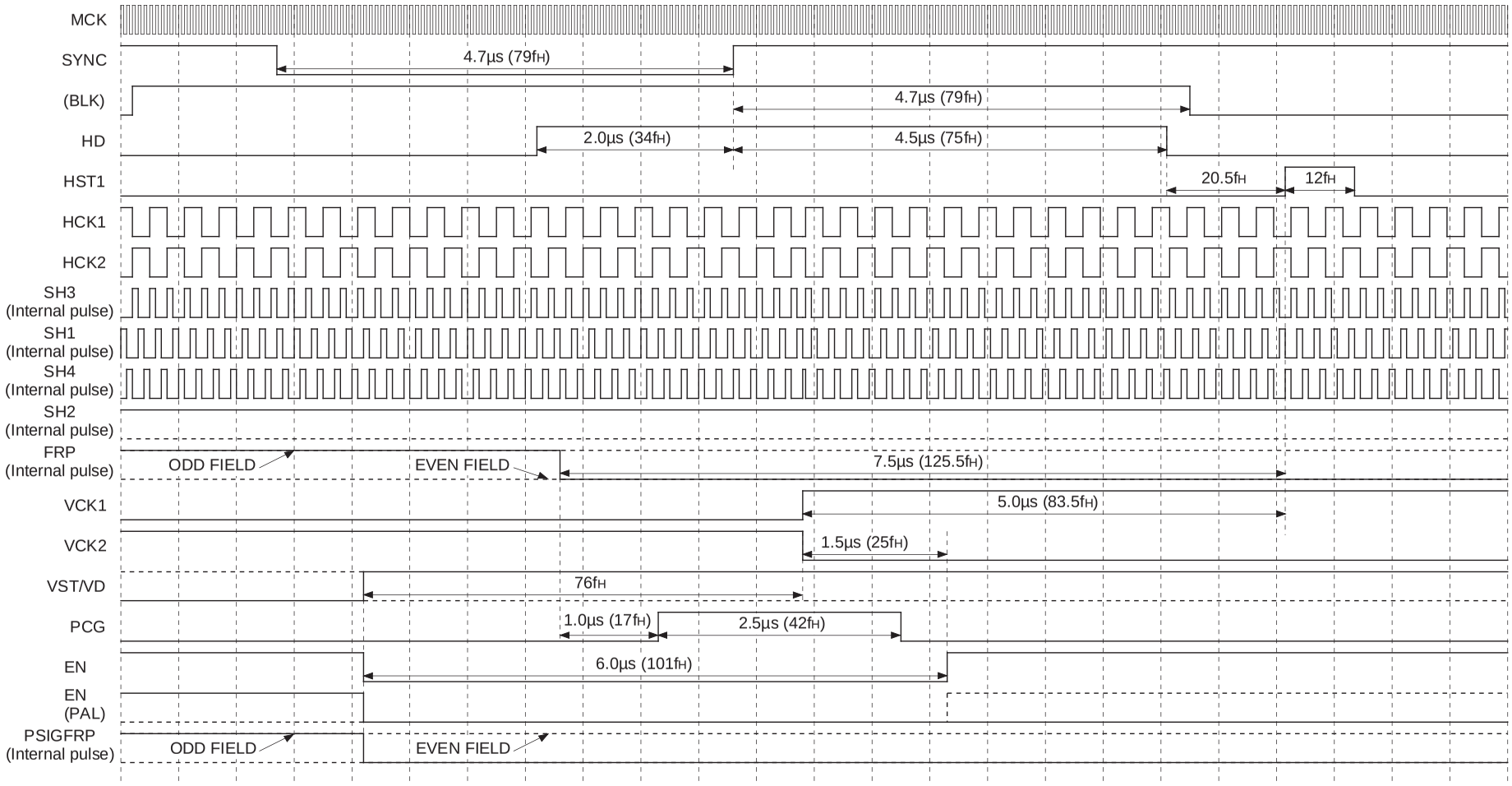
LCX018AK Pixel Arrangement (16:9)



DCX501BK Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: H (Normal scan)
1066f_H



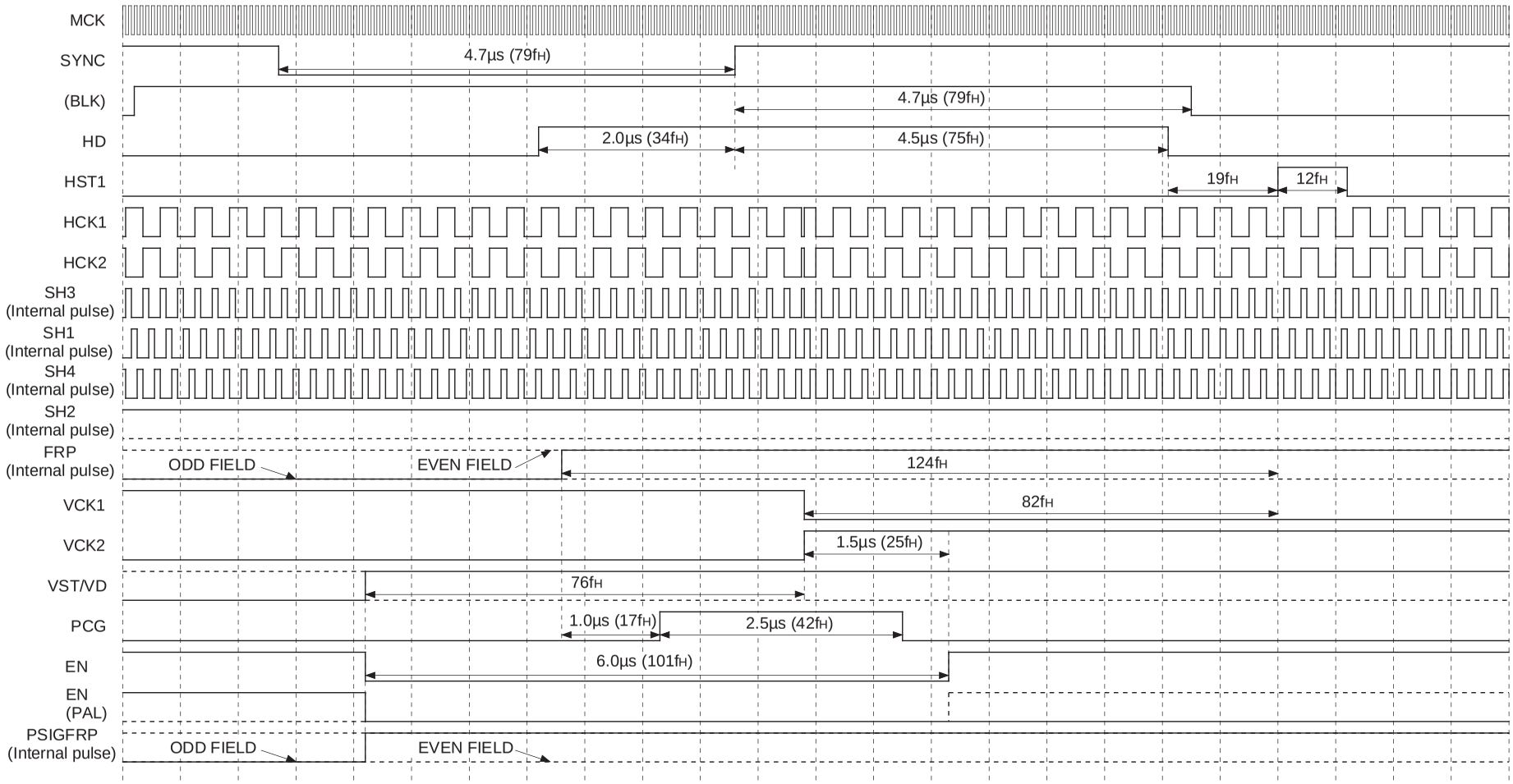
ODD LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: H (Normal scan)
1066f_H



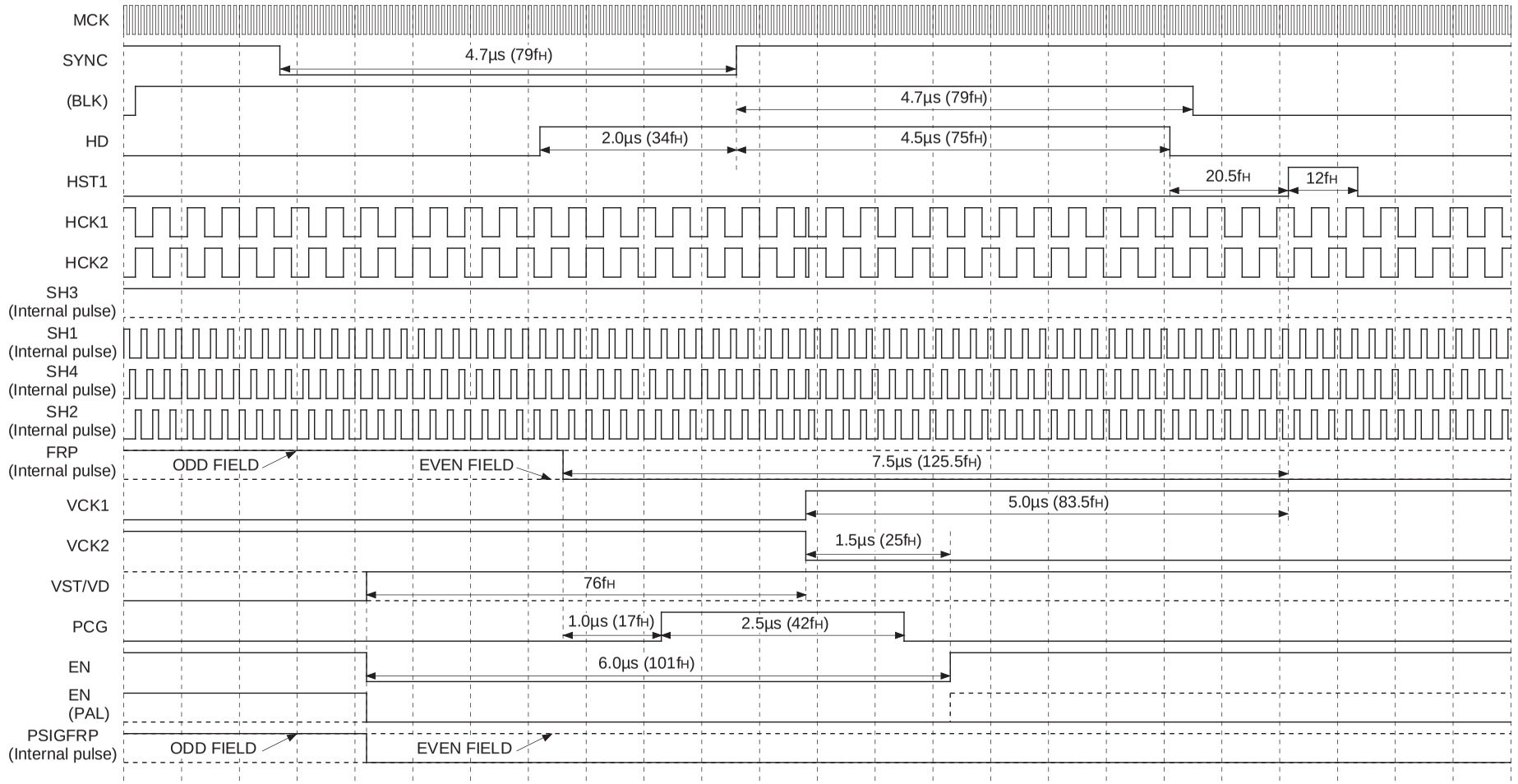
EVEN LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: L (Reverse scan)
1066fH

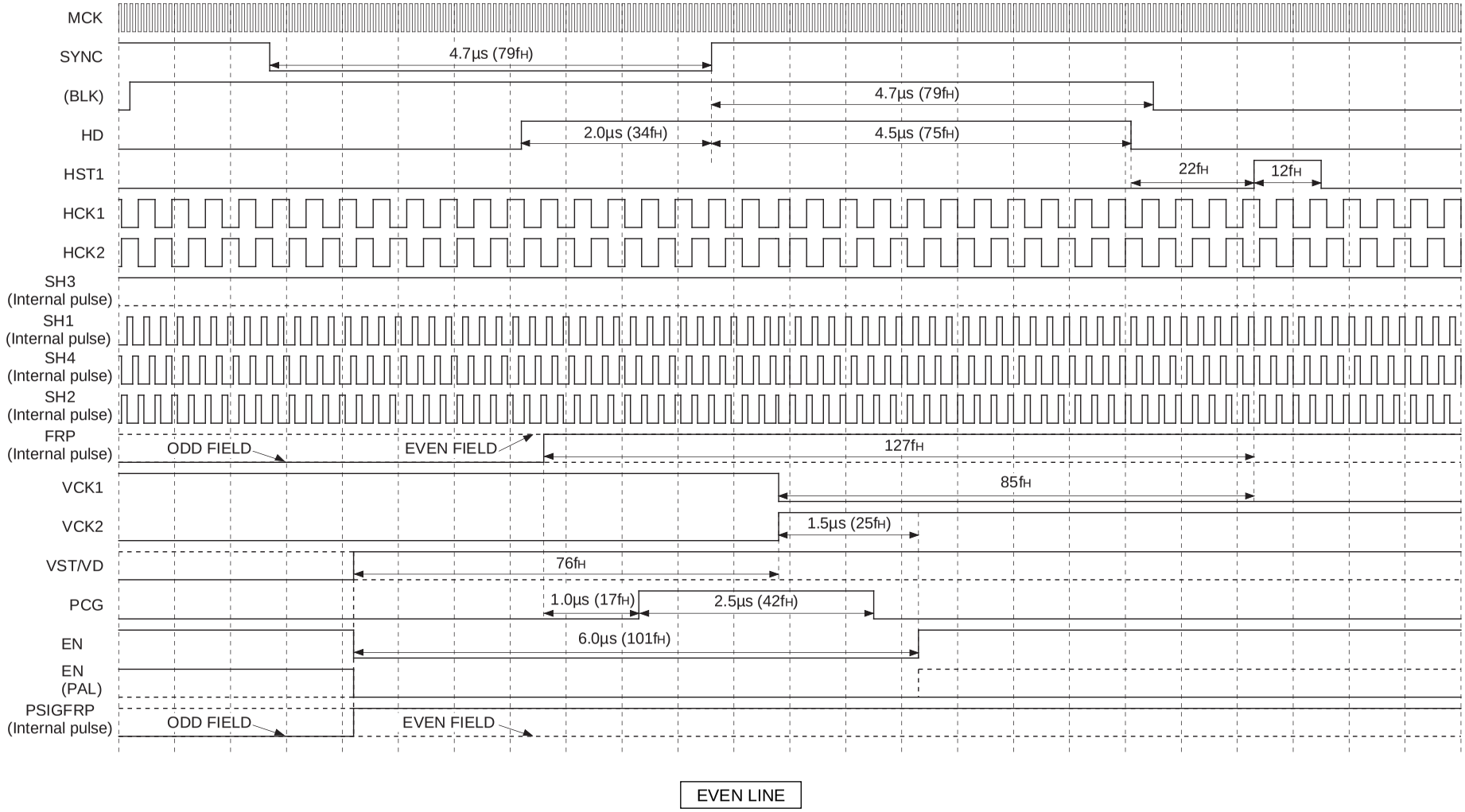


Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Horizontal Direction Timing Chart

NTSC/PAL

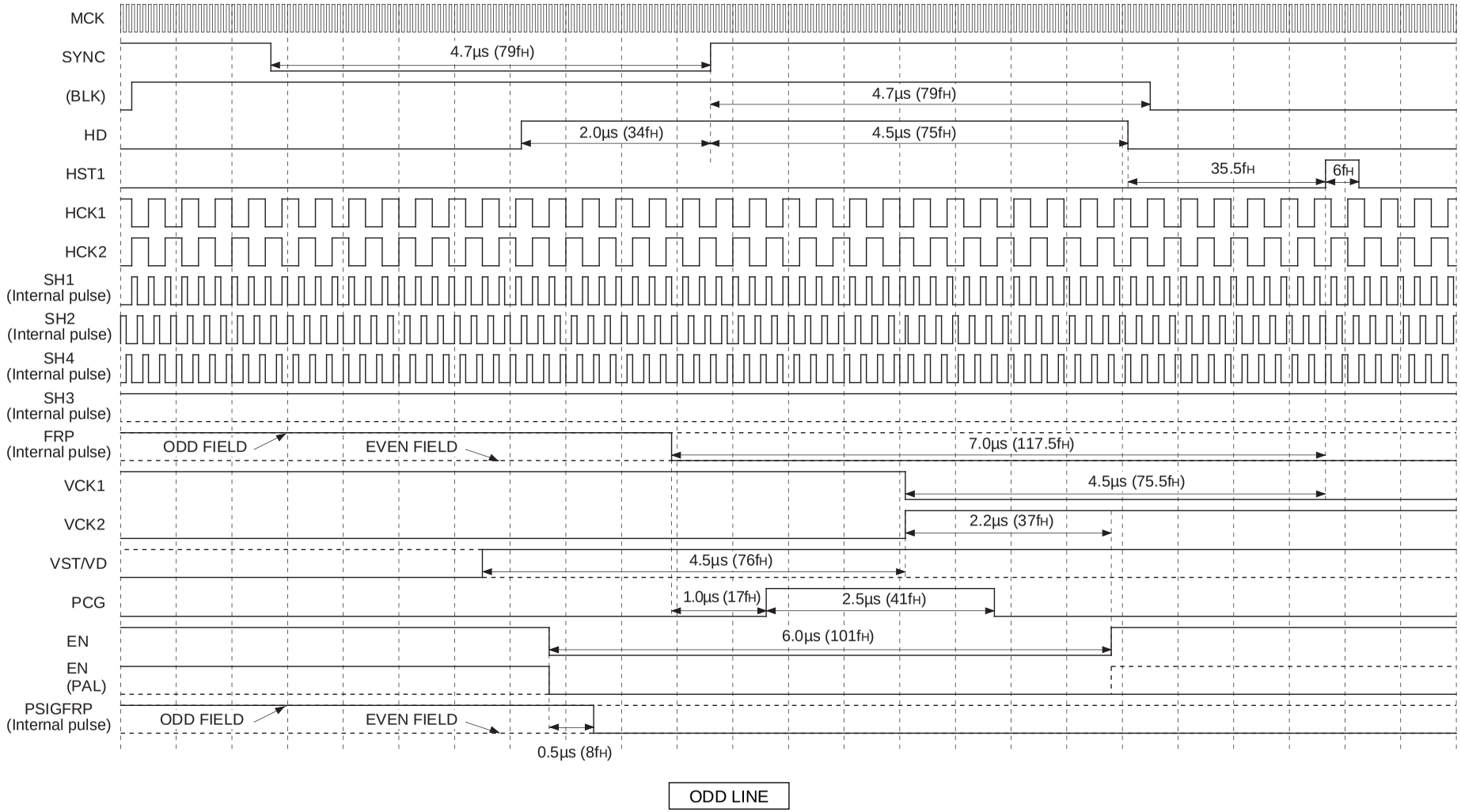
Unless otherwise specified, serial settings are the default values.
RGT: L (Reverse scan)
1066f_H



Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Horizontal Direction Timing Chart (4:3)
NTSC/PAL

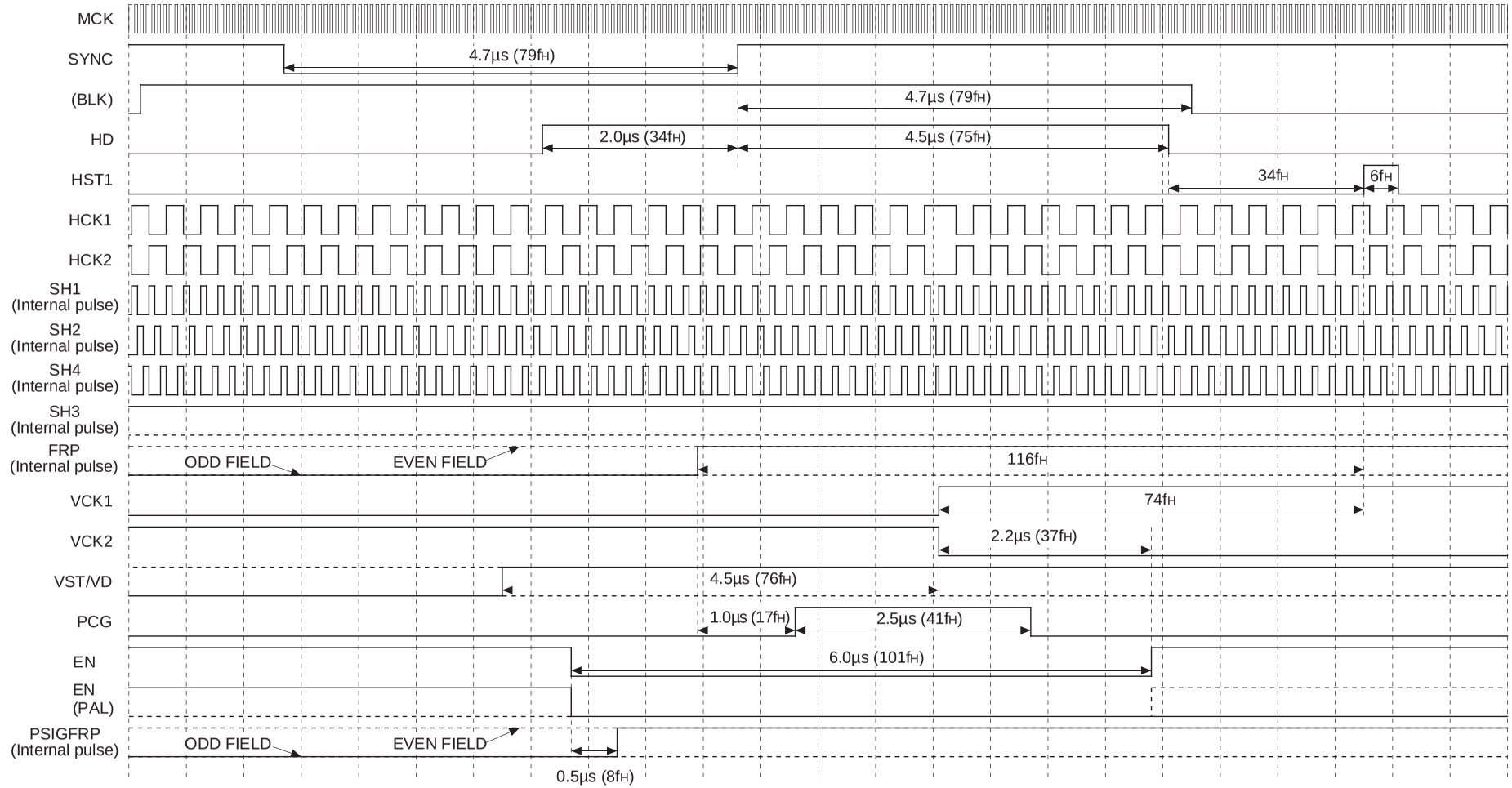
Unless otherwise specified, serial settings are the default values.
RGT: H (Normal scan), PCG width: LH, EN position: HH
Master Clock: 16.773MHz (NTSC) / 16.656MHz (PAL)
PLL Counter N: 1066f_H



Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Horizontal Direction Timing Chart (4:3)
NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: H (Normal scan), PCG width: LH, EN position: HH
Master Clock: 16.773MHz (NTSC) / 16.656MHz (PAL)
PLL Counter N: 1066f_H



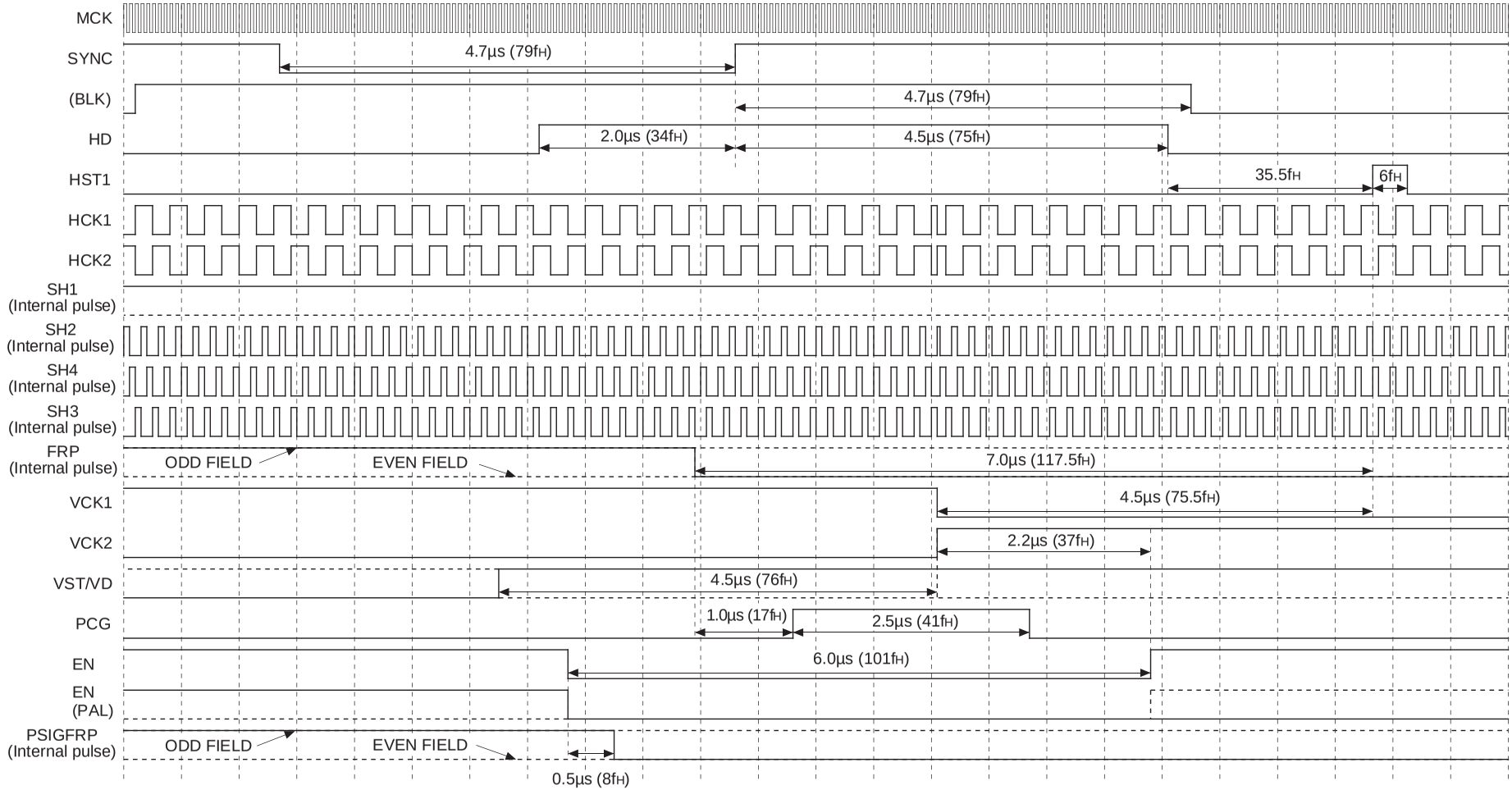
EVEN LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Horizontal Direction Timing Chart (4:3)

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: L (Reverse scan), PCG width: LH, EN position: HH
Master Clock: 16.773MHz (NTSC) / 16.656MHz (PAL)
PLL Counter N: 1066f_H



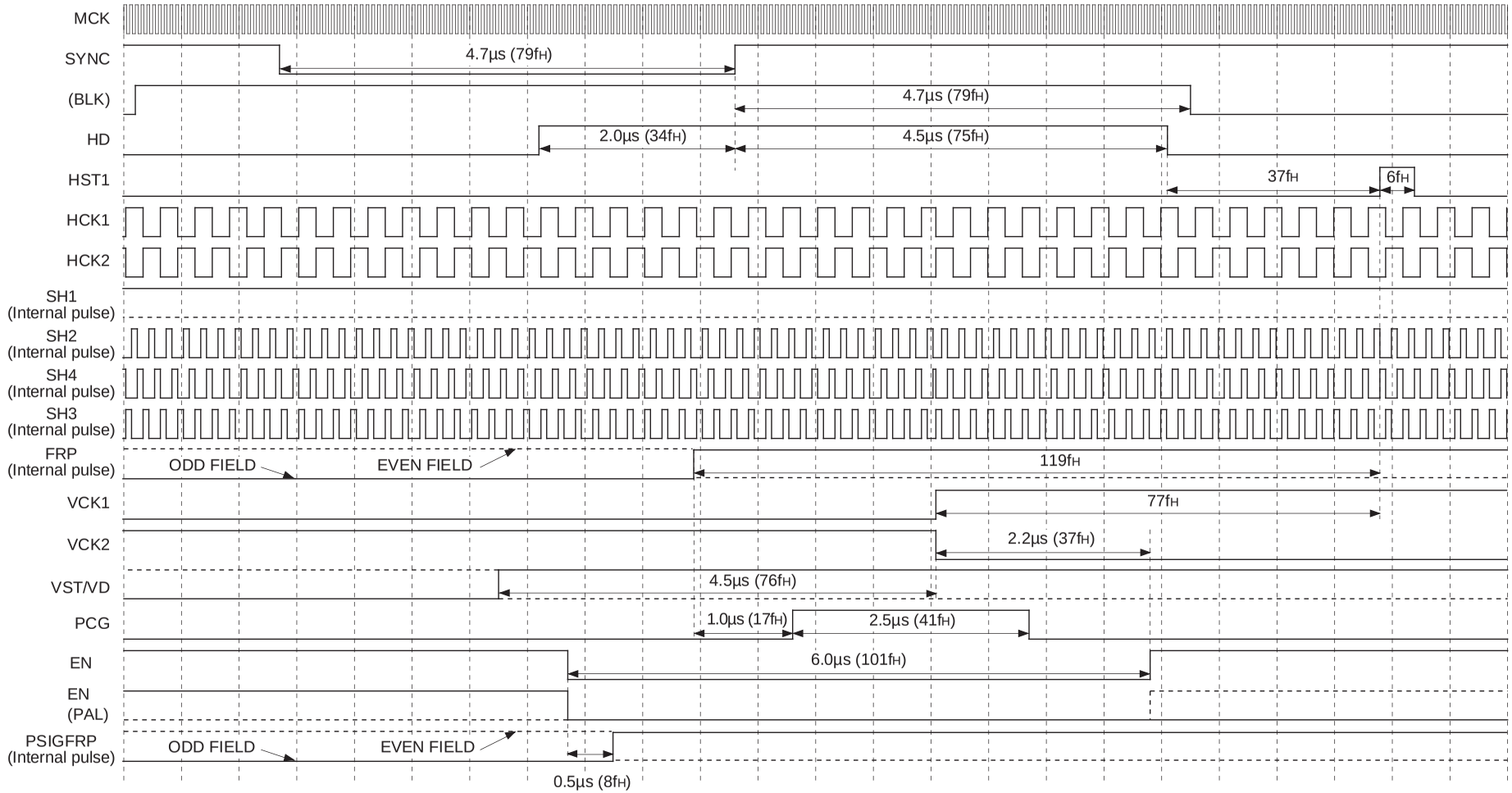
ODD LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Horizontal Direction Timing Chart (4:3)

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: L (Reverse scan), PCG width: LH, EN position: HH
Master Clock: 16.773MHz (NTSC) / 16.656MHz (PAL)
PLL Counter N: 1066f_H



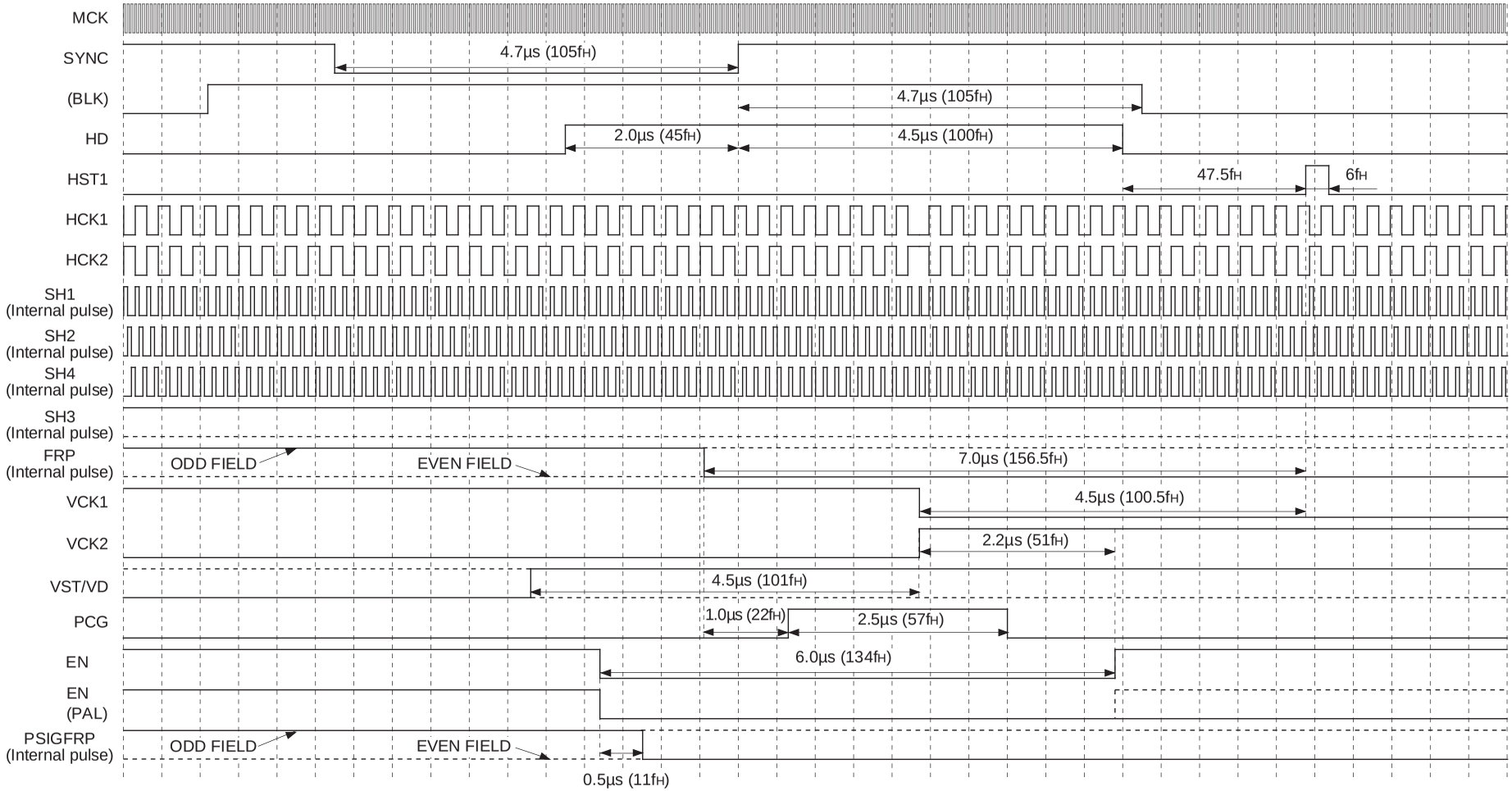
EVEN LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Horizontal Direction Timing Chart (16:9)

NTSC/PAL

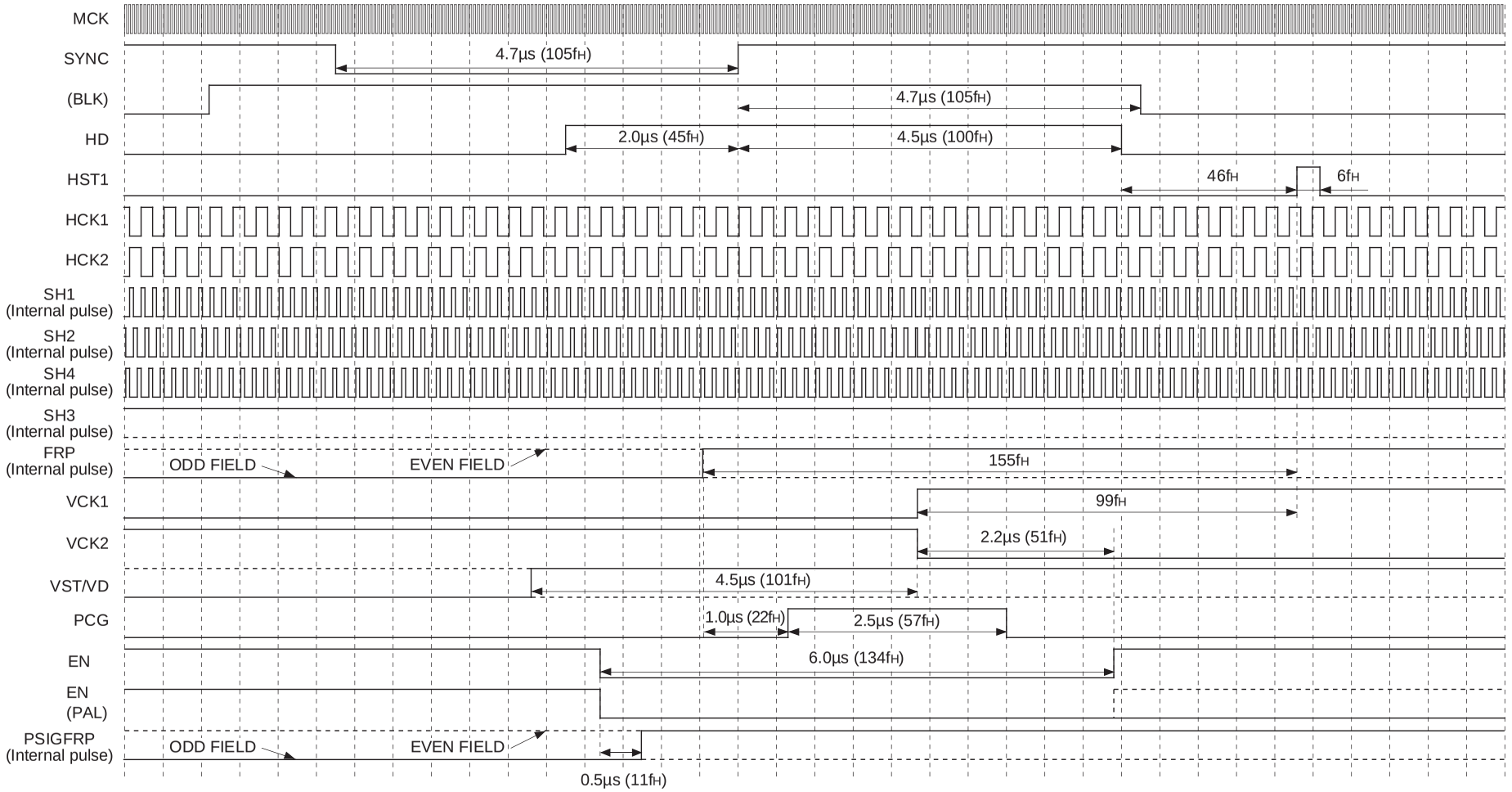
Unless otherwise specified, serial settings are the default values.
RGT: H (Normal scan), PCG width: LH, EN position: HH
Master Clock: 22.295MHz (NTSC) / 22.141MHz (PAL)
PLL Counter N: 1417fH



Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Horizontal Direction Timing Chart (16:9)
NTSC/PAL

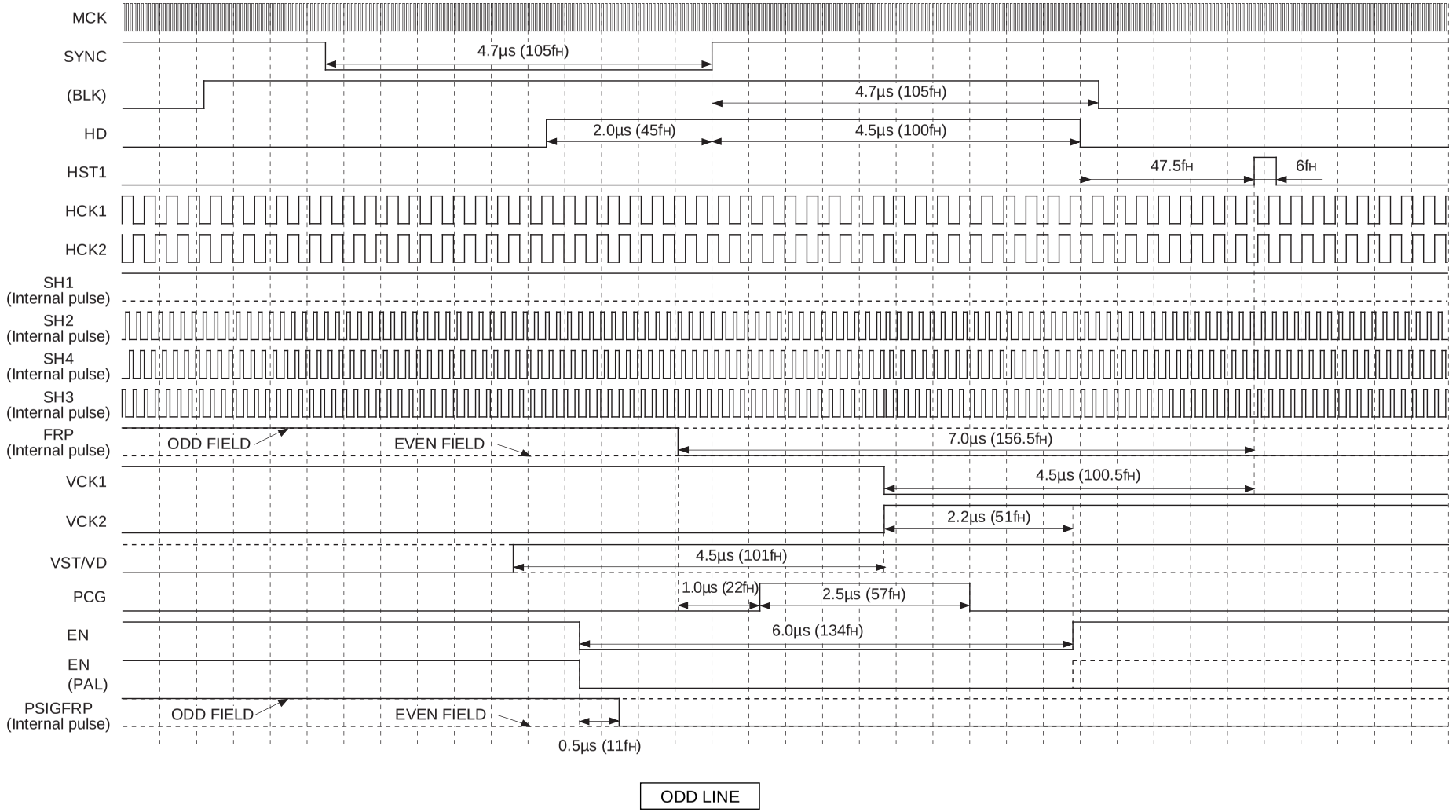
Unless otherwise specified, serial settings are the default values.
RGT: H (Normal scan), PCG width: LH, EN position: HH
Master Clock: 22.295MHz (NTSC) / 22.141MHz (PAL)
PLL Counter N: 1417fH



Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Horizontal Direction Timing Chart (16:9)
NTSC/PAL

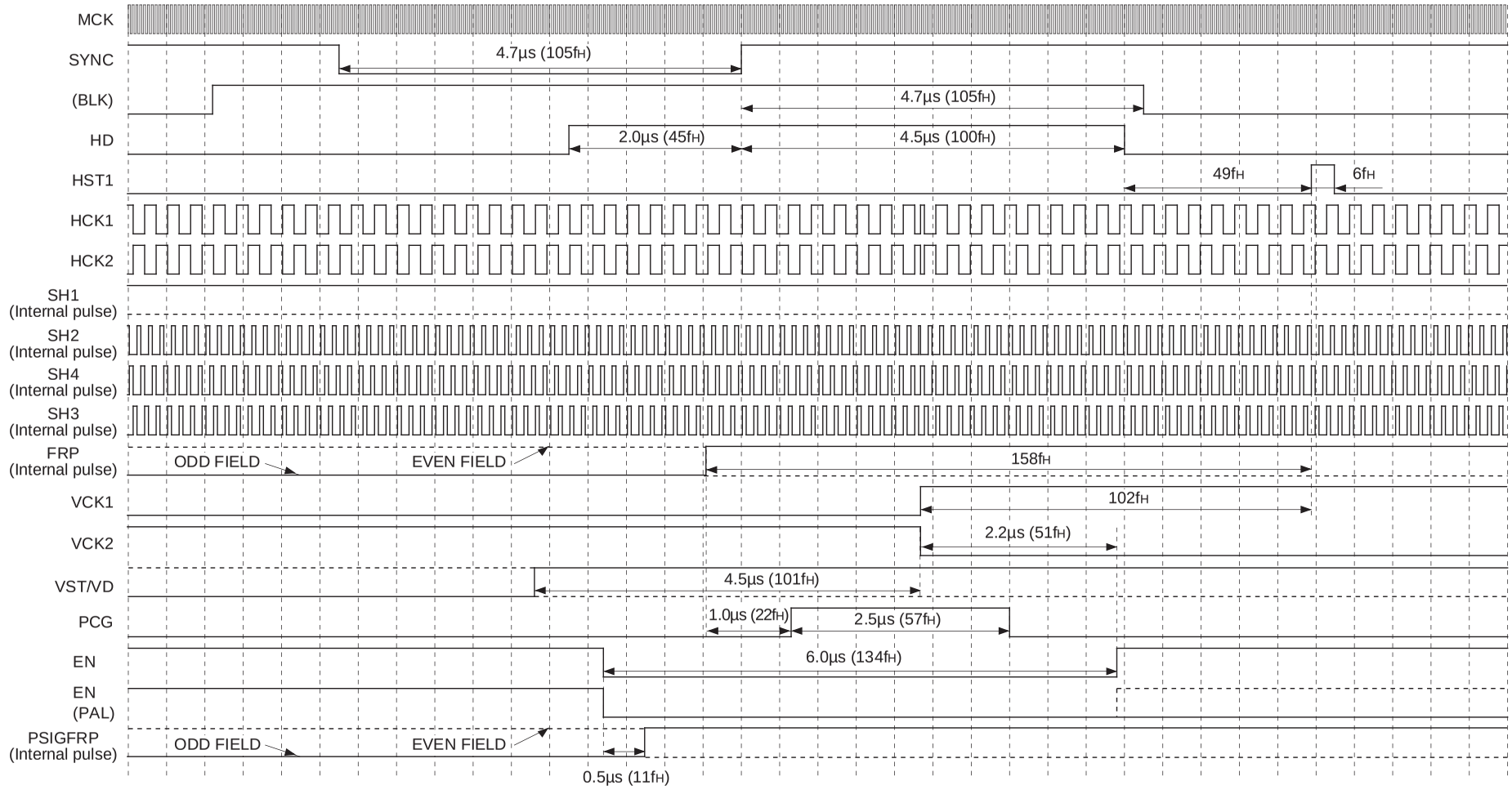
Unless otherwise specified, serial settings are the default values.
RGT: L (Reverse scan), PCG width: LH, EN position: HH
Master Clock: 22.295MHz (NTSC) / 22.141MHz (PAL)
PLL Counter N: 1417f_H



Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Horizontal Direction Timing Chart (16:9)
NTSC/PAL

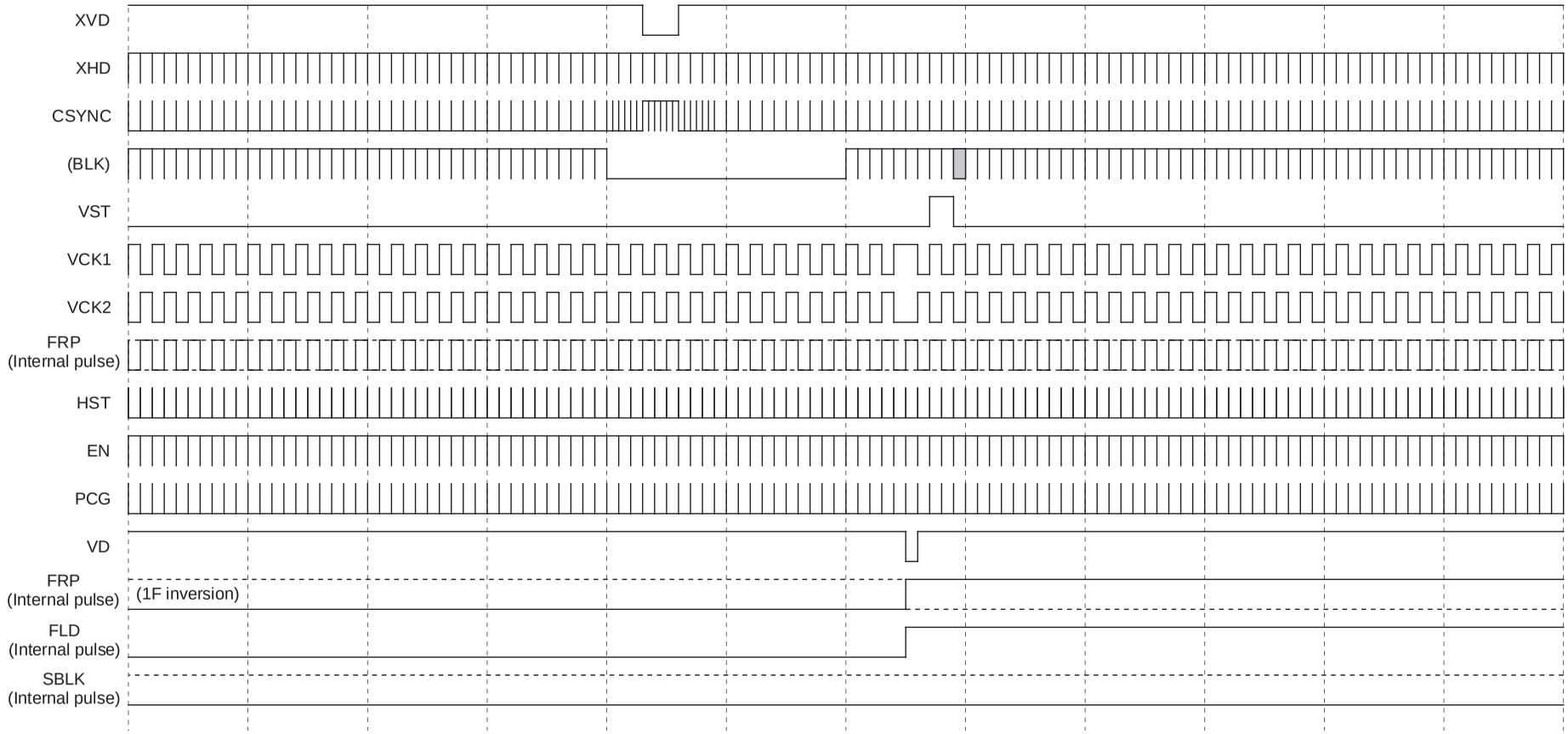
Unless otherwise specified, serial settings are the default values.
RGT: L (Reverse scan), PCG width: LH, EN position: HH
Master Clock: 22.295MHz (NTSC) / 22.141MHz (PAL)
PLL Counter N: 1417f_H



Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Vertical Direction Output Pulse

NTSC Vertical Direction Timing Chart

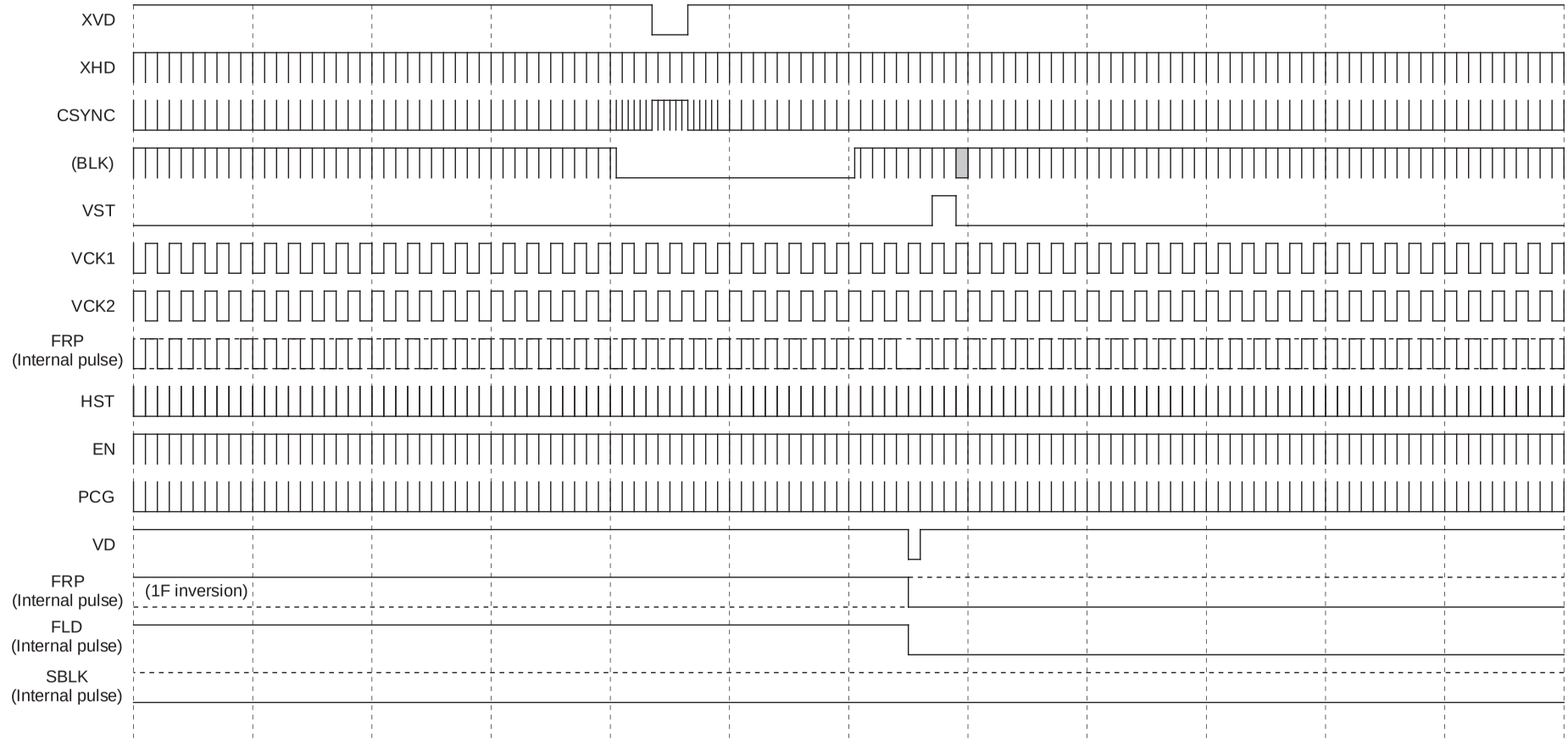


ODD FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Vertical Direction Output Pulse

NTSC Vertical Direction Timing Chart

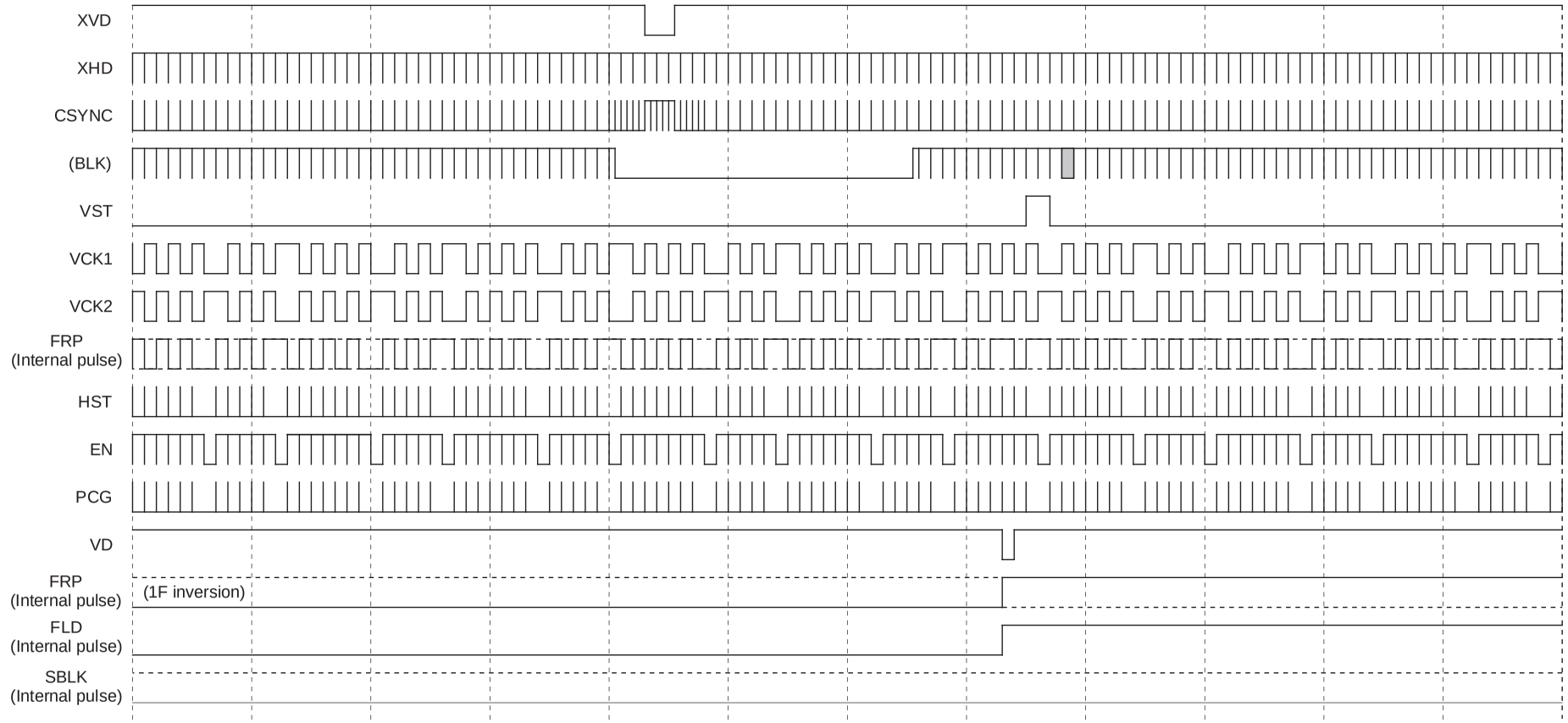


EVEN FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Vertical Direction Output Pulse

PAL Vertical Direction Timing Chart

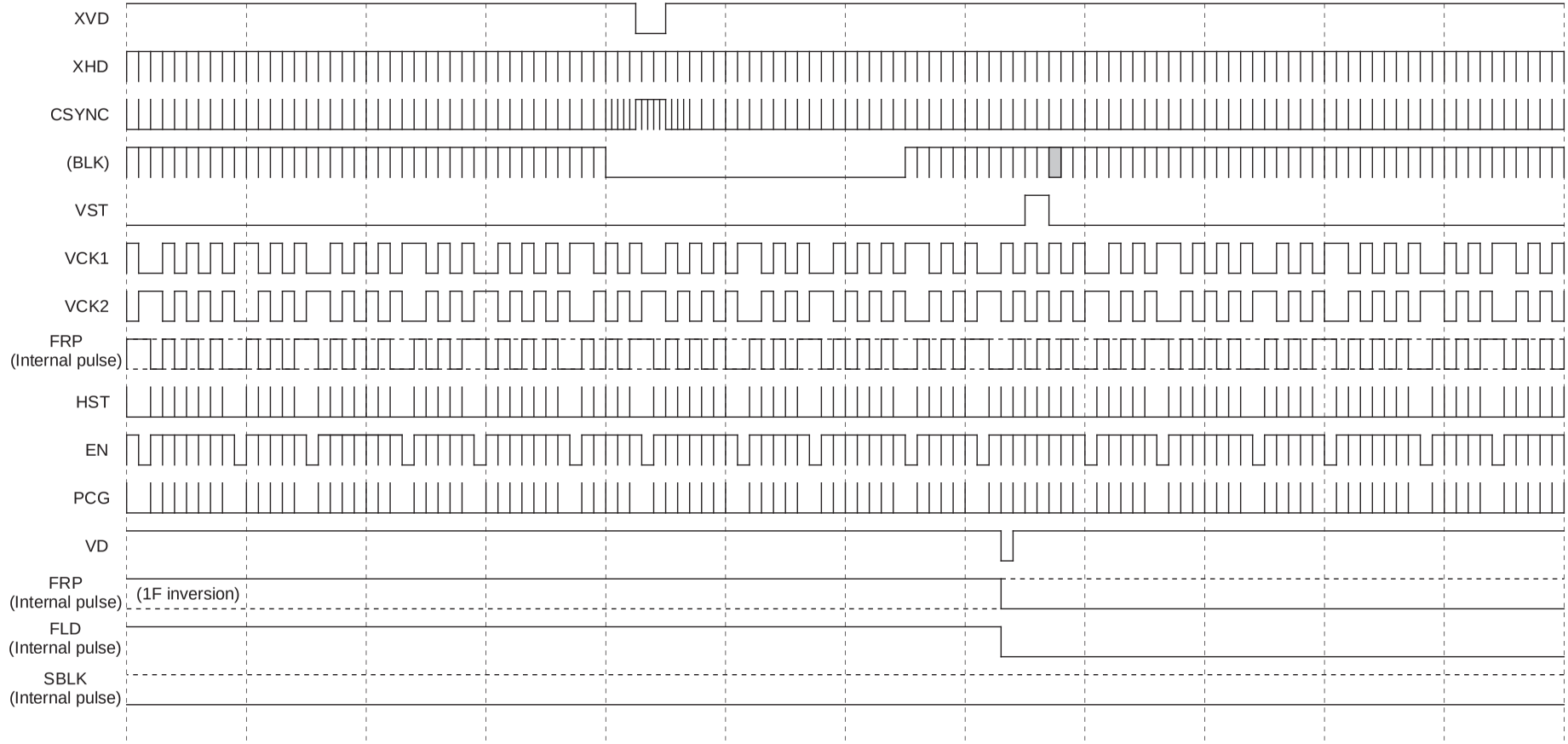


ODD FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Vertical Direction Output Pulse

PAL Vertical Direction Timing Chart



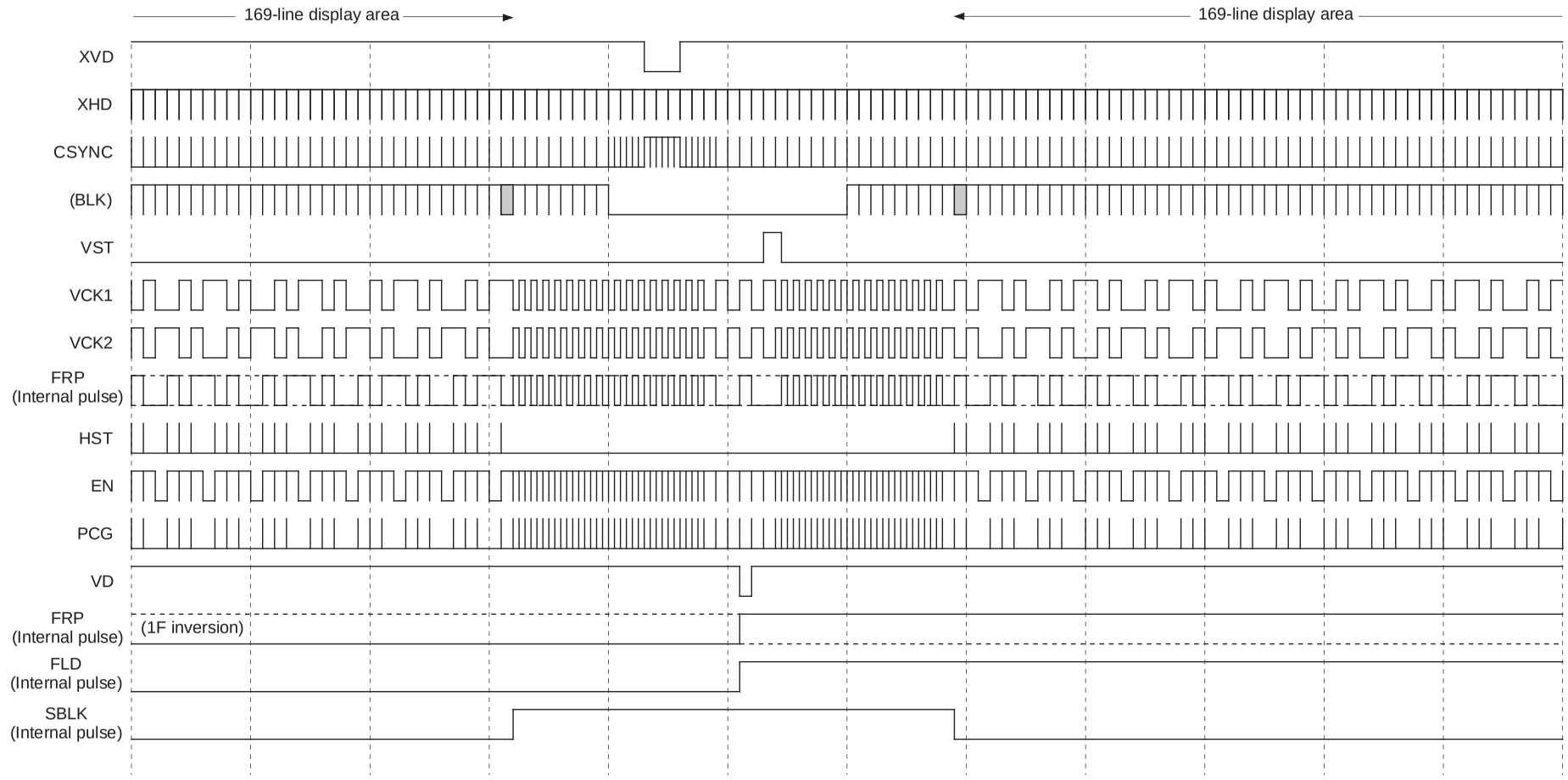
EVEN FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Vertical Direction Output Pulse

NTSC WIDE Vertical Direction Timing Chart

1/4 pulse eliminator



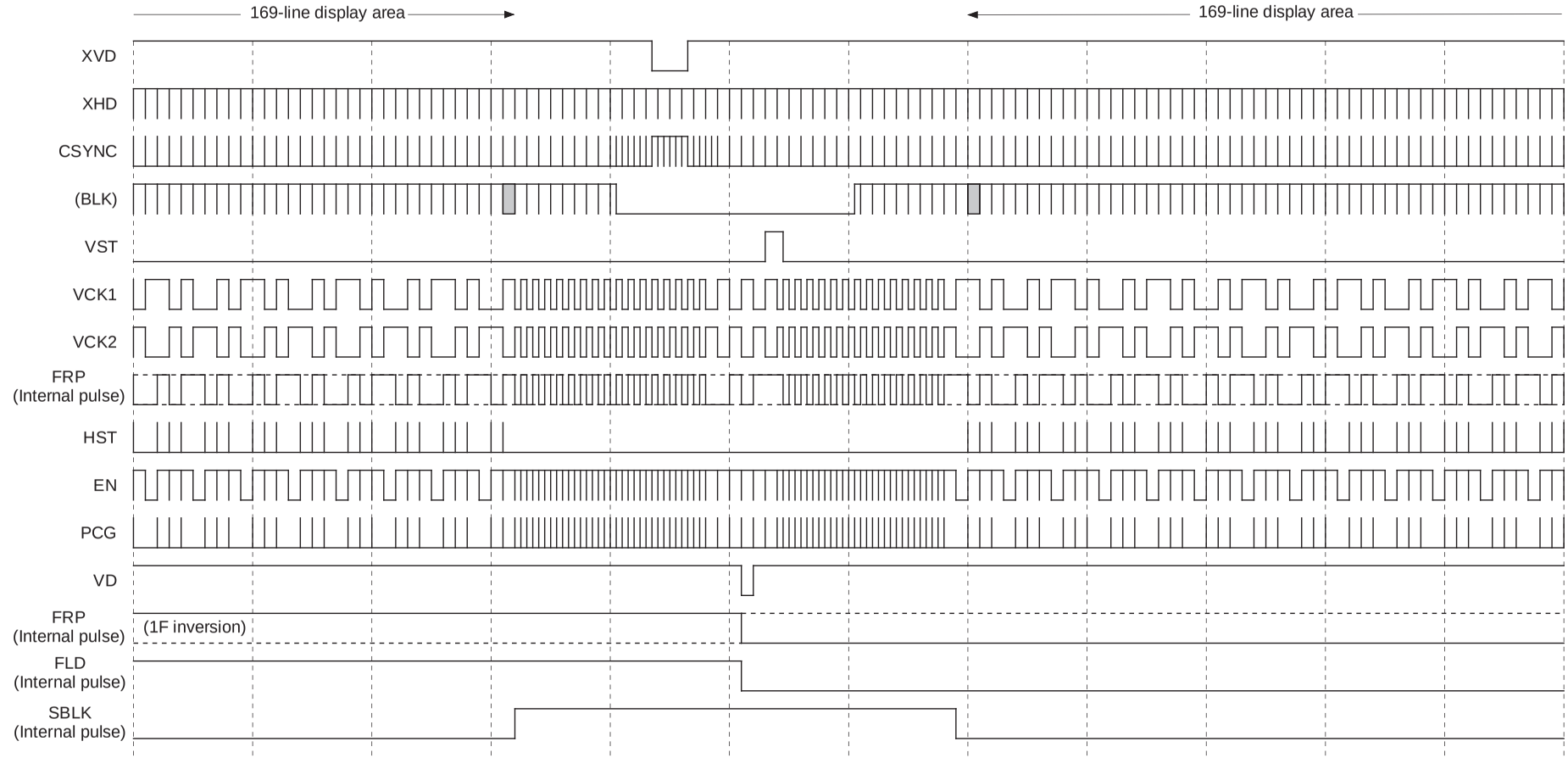
ODD FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Vertical Direction Output Pulse

NTSC WIDE Vertical Direction Timing Chart

1/4 pulse eliminator

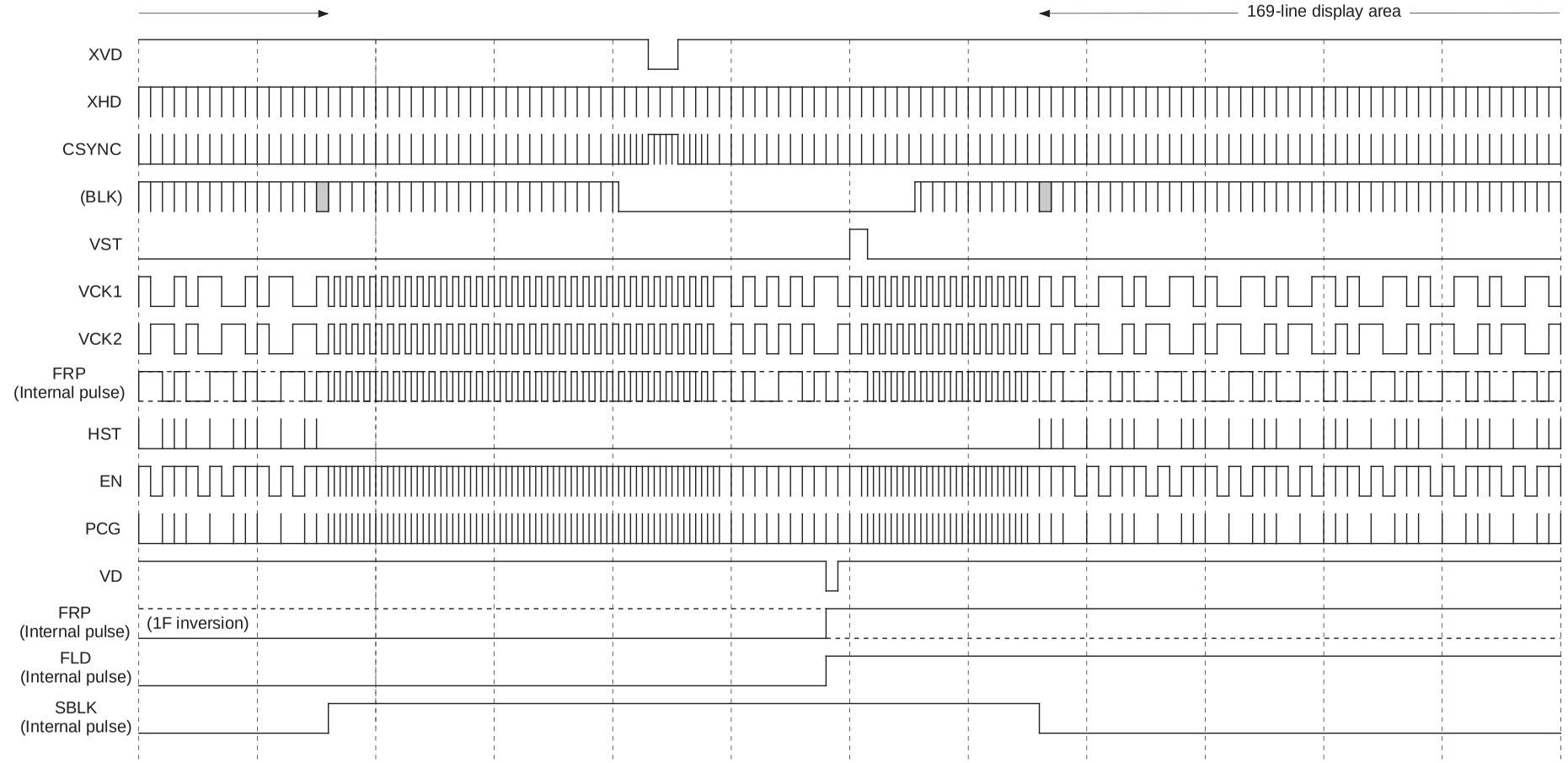


EVEN FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Vertical Direction Output Pulse

PAL WIDE Vertical Direction Timing Chart

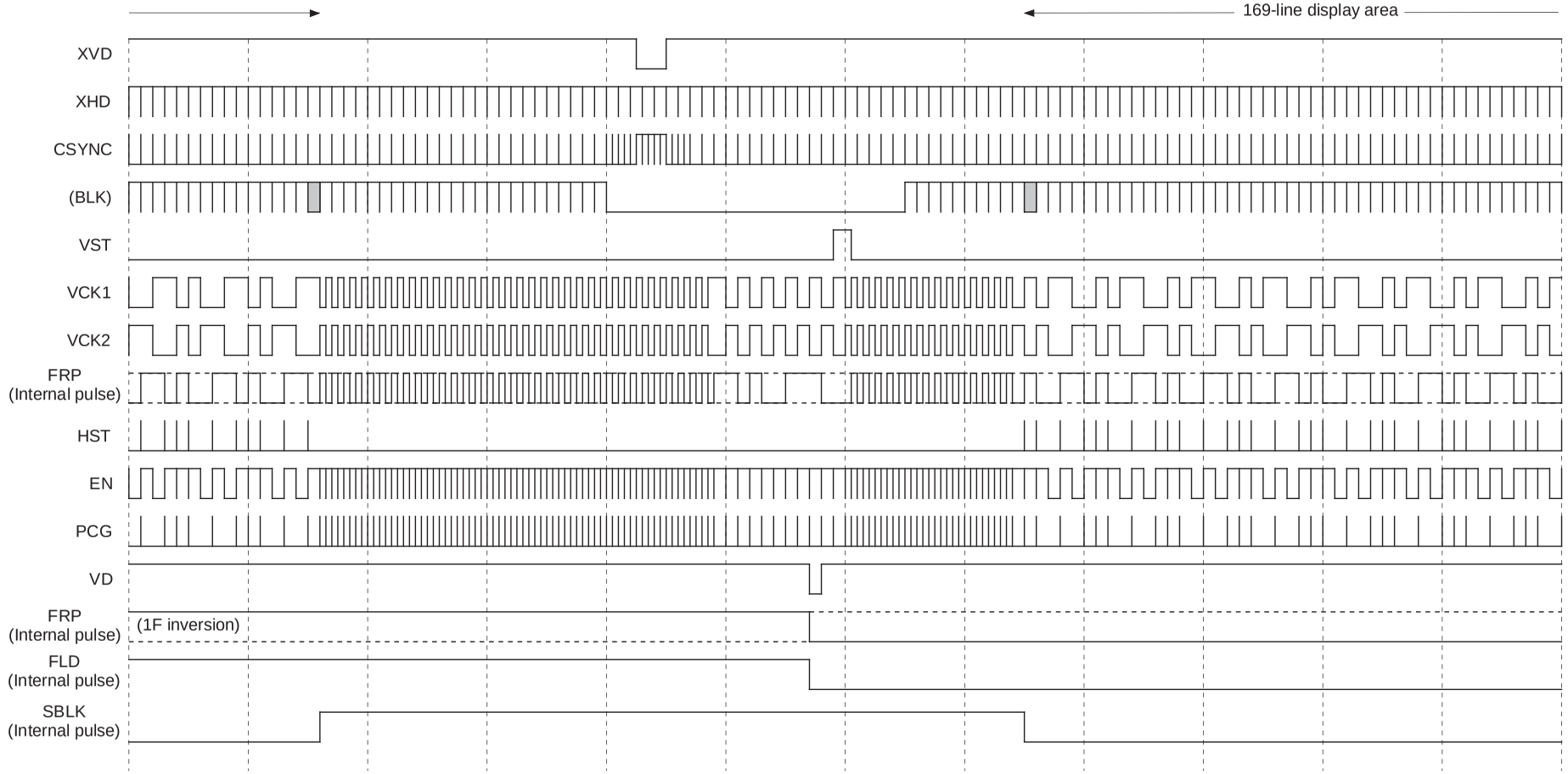


ODD FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

DCX501BK Vertical Direction Output Pulse
PAL WIDE Vertical Direction Timing Chart

1/2 and 1/4 pulse eliminator

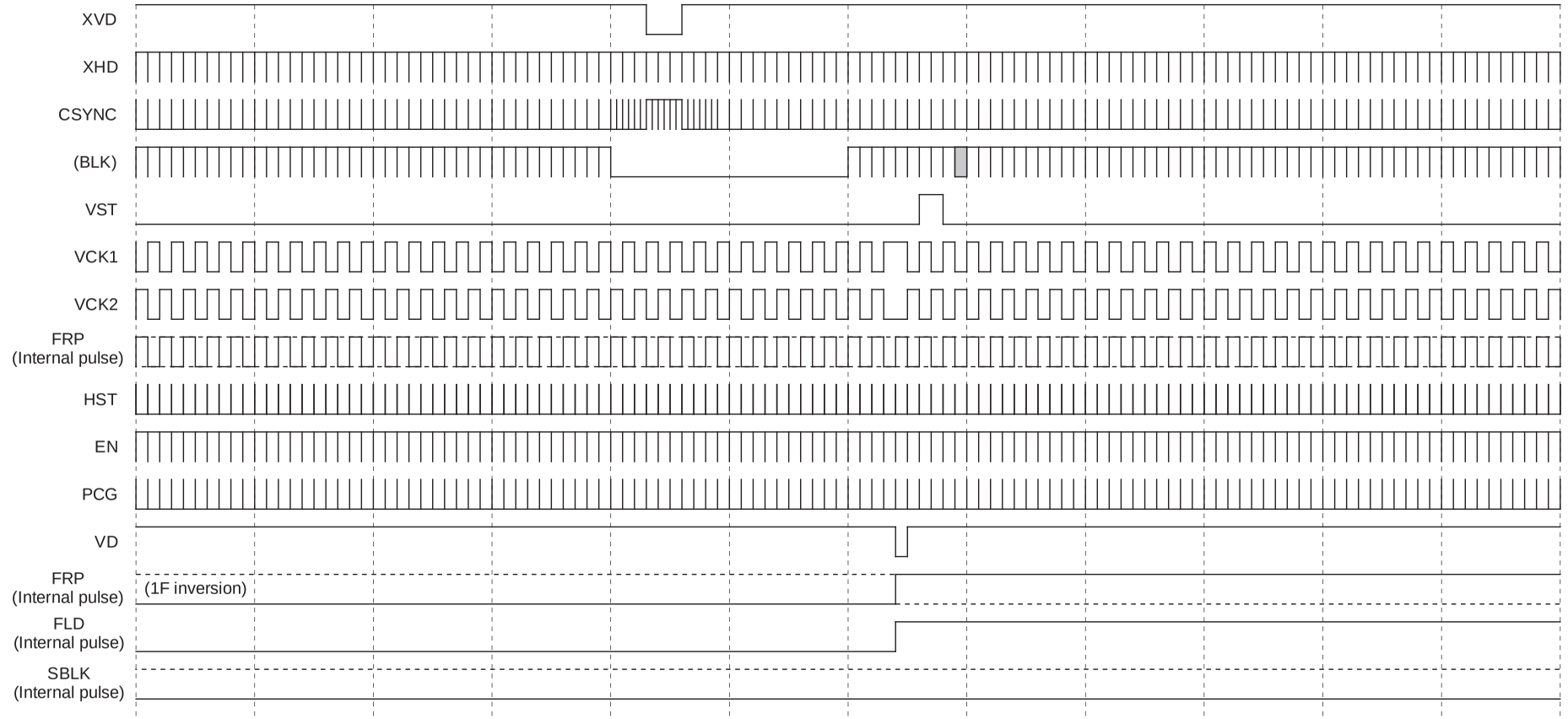


EVEN FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Vertical Direction Output Pulse

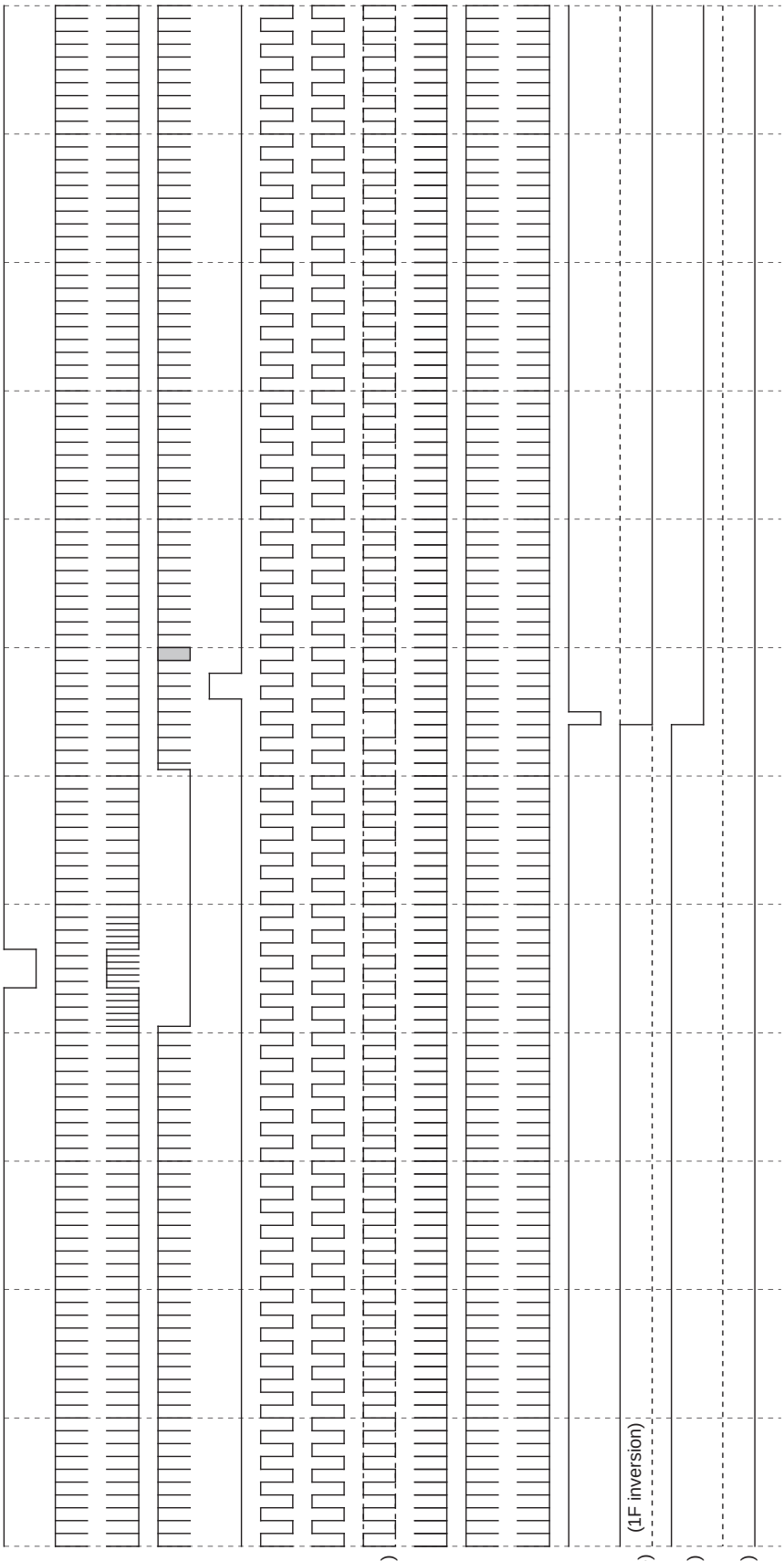
NTSC Vertical Direction Timing Chart (DOWN)



ODD FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

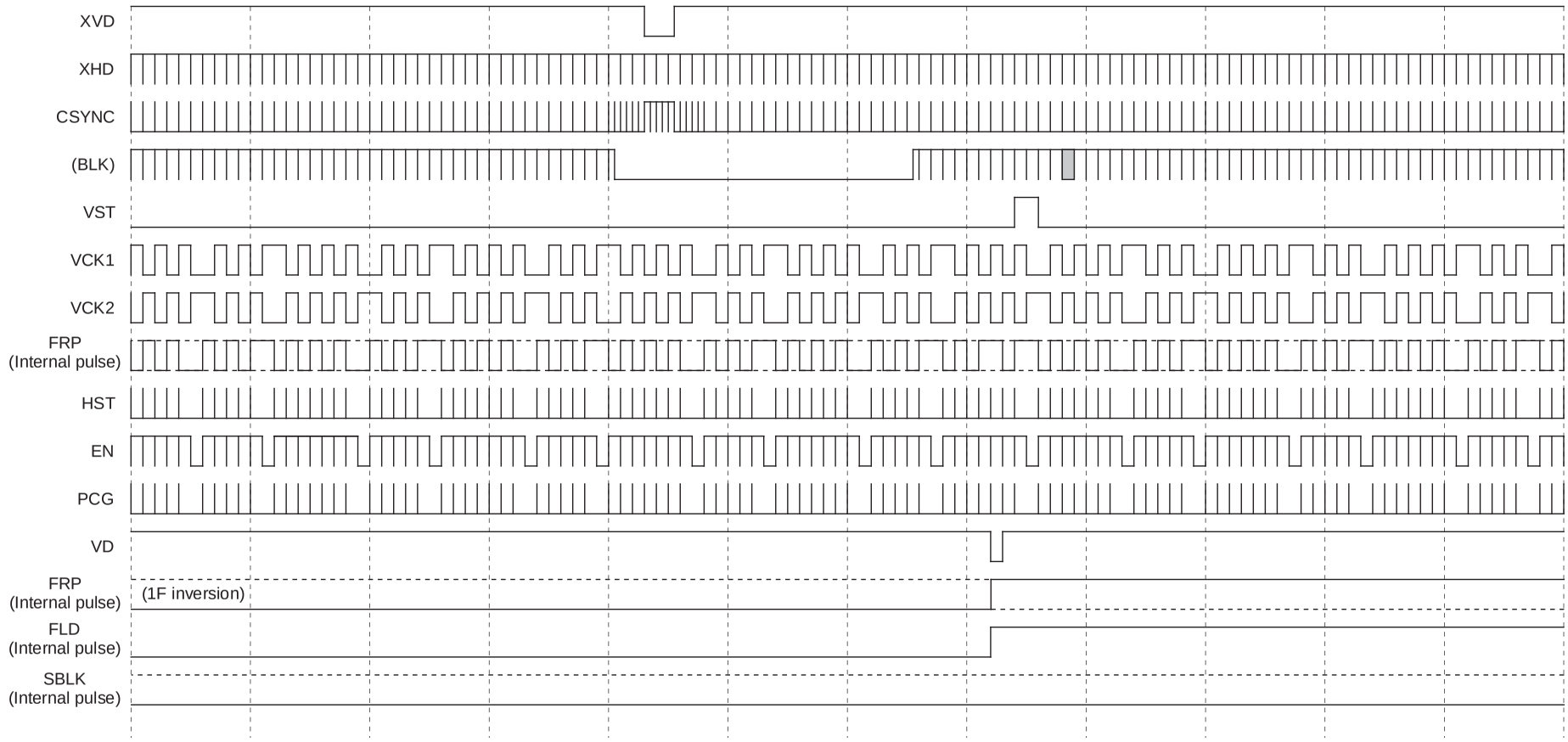
LCX018AK Vertical Direction Output Pulse
NTSC Vertical Direction Timing Chart (DOWN)



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Vertical Direction Output Pulse

PAL Vertical Direction Timing Chart (DOWN)

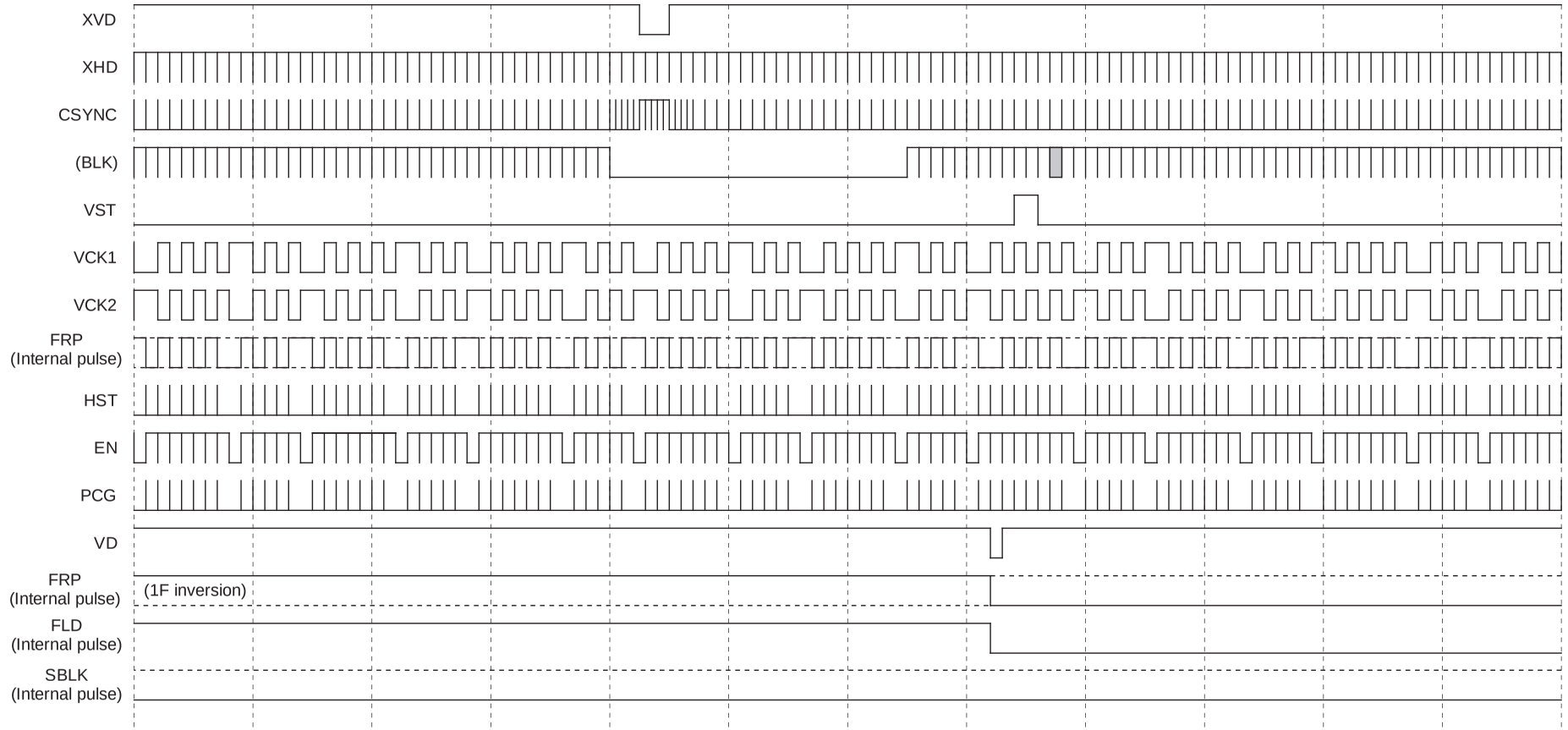


ODD FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Vertical Direction Output Pulse

PAL Vertical Direction Timing Chart (DOWN)

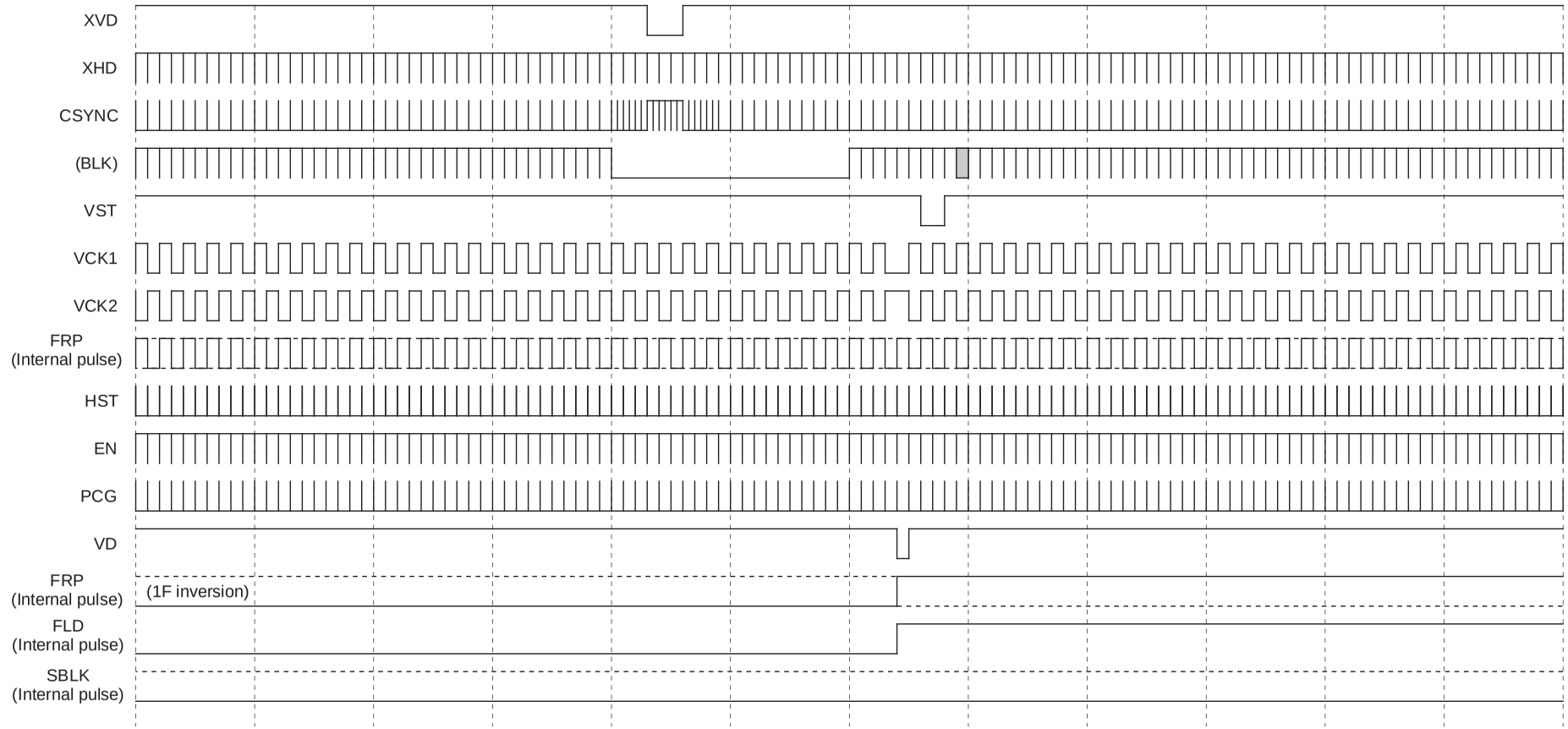


EVEN FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Vertical Direction Output Pulse

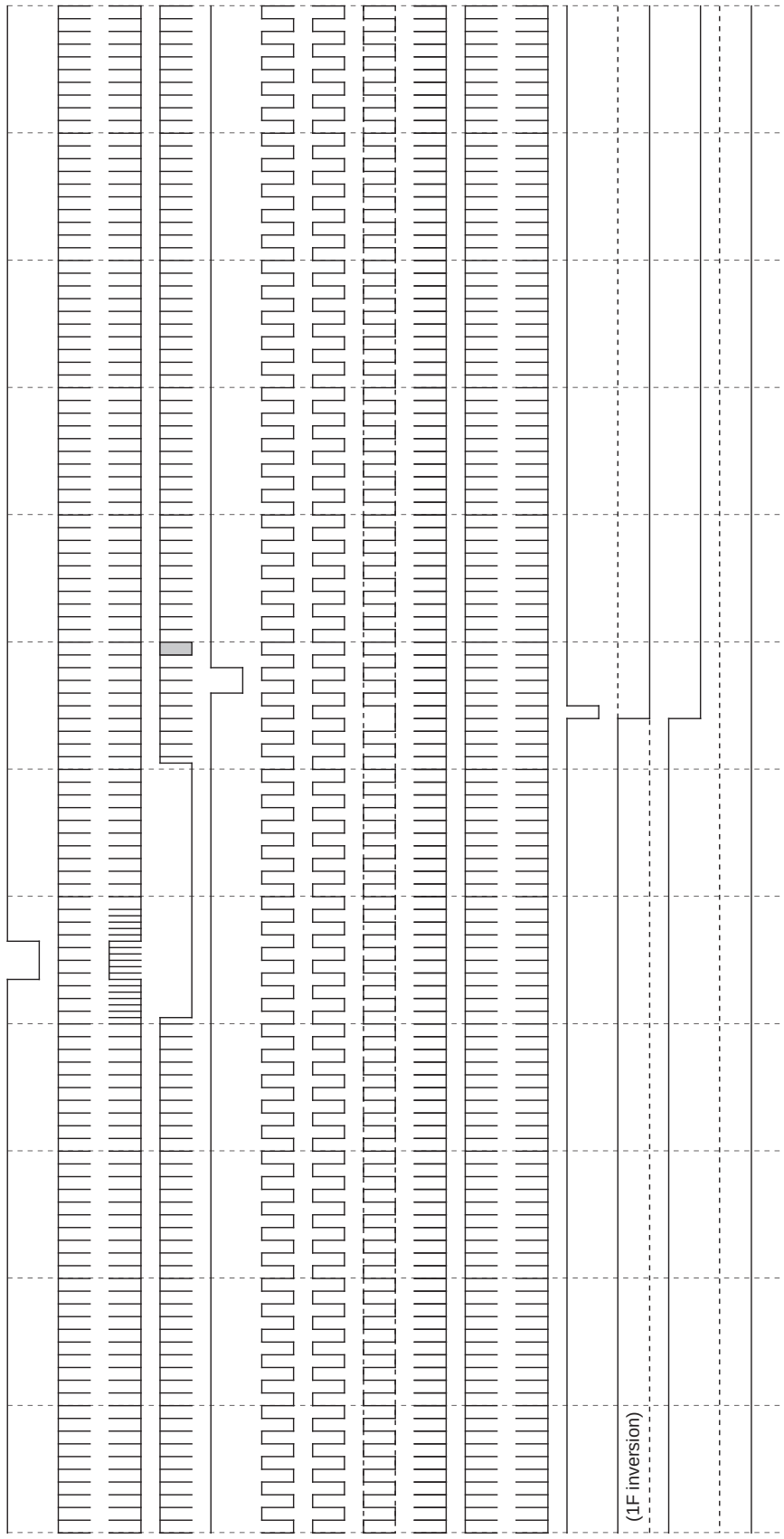
NTSC Vertical Direction Timing Chart (UP)



ODD FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Vertical Direction Output Pulse
NTSC Vertical Direction Timing Chart (UP)



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Vertical Direction Output Pulse

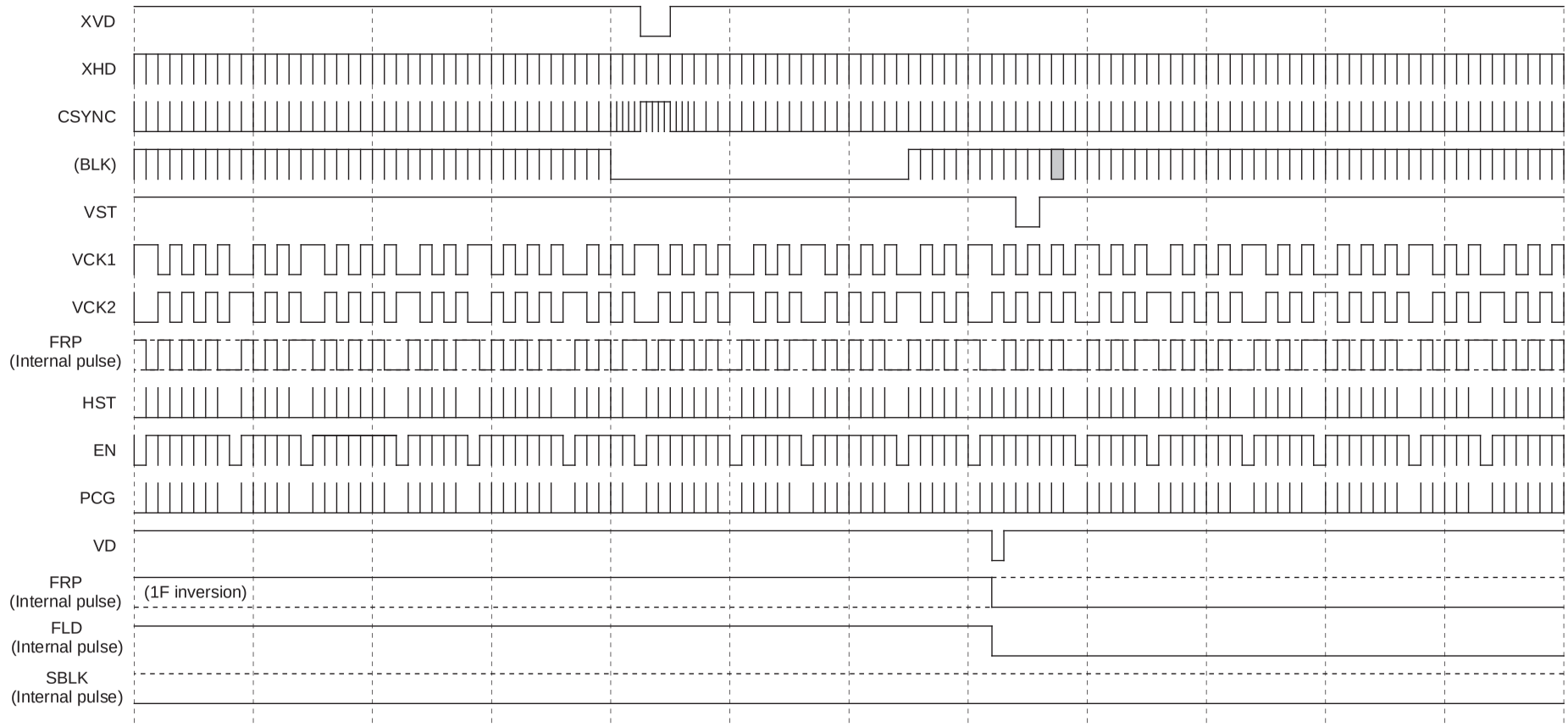
PAL Vertical Direction Timing Chart (UP)

ODD FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX018AK Vertical Direction Output Pulse

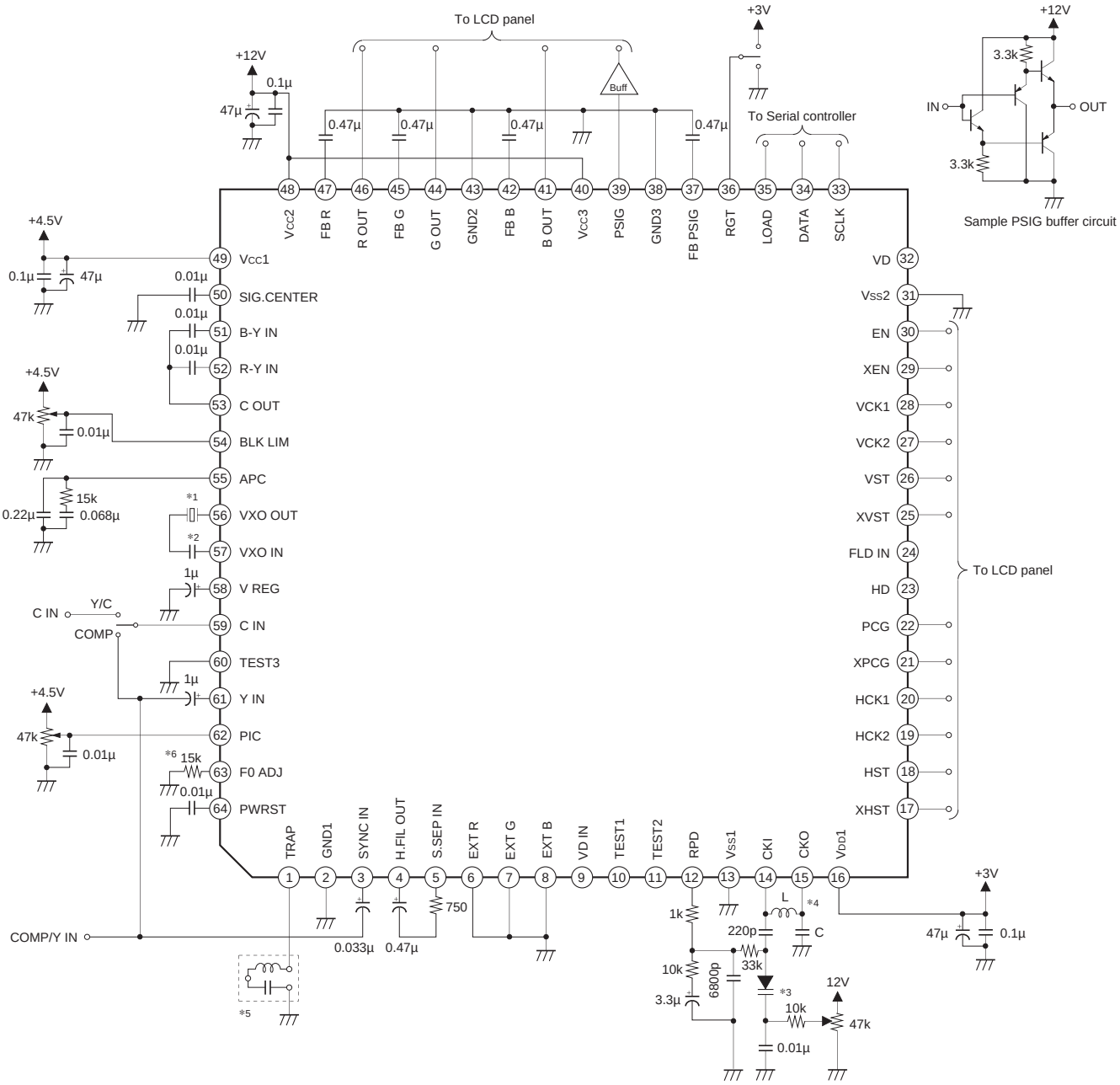
PAL Vertical Direction Timing Chart (UP)



EVEN FIELD

Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

Application Circuit (NTSC/PAL, COMP and Y/C input)



*1 Used crystal: KINSEKI CX-5F
Frequency deviation: within ±30ppm, frequency temperature characteristics: within ±30ppm, load capacity: 16pF
NTSC: 3.579545Hz
PAL: 4.433619Hz

*2 NTSC: shorted, PAL: 18pF

*3 Variable Capcitance Diode: 1T369 (SONY)

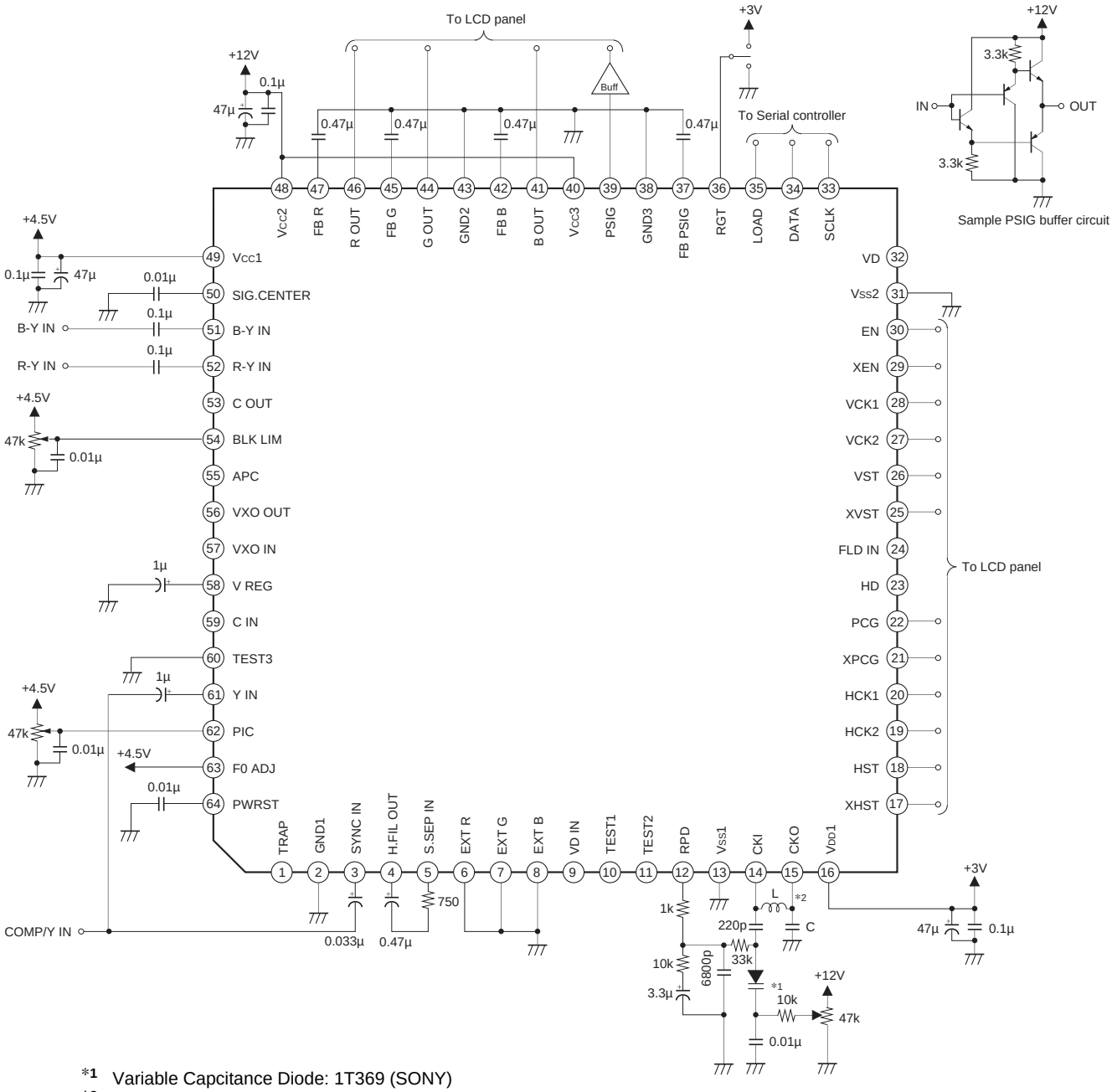
*4 DCX501 mode: L value: 4.7µH, C value: 22pF
LCX018 (4:3) mode: L value: 4.7µH, C value: 22pF
LCX018 (16:9) mode: L value: 2.2µH, C value: 33pF

*5 Trap (TDK)
NTSC: NLT4532-S3R6B
PAL: NLT4532-S4R4

*6 Resistance value variation: ±2%,
temperature coefficient: ±200ppm or less
Connect to +4.5V during Y/C input

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (NTSC/PAL, Y/color difference input)

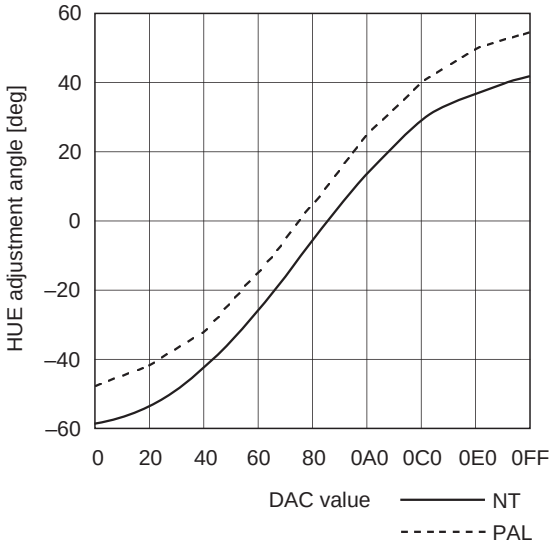


*1 Variable Capcitance Diode: 1T369 (SONY)
*2 DCX501 mode: L value: 4.7µH, C value: 22pF
LCX018 (4:3) mode: L value: 4.7µH, C value: 22pF
LCX018 (16:9) mode: L value: 2.2µH, C value: 33pF

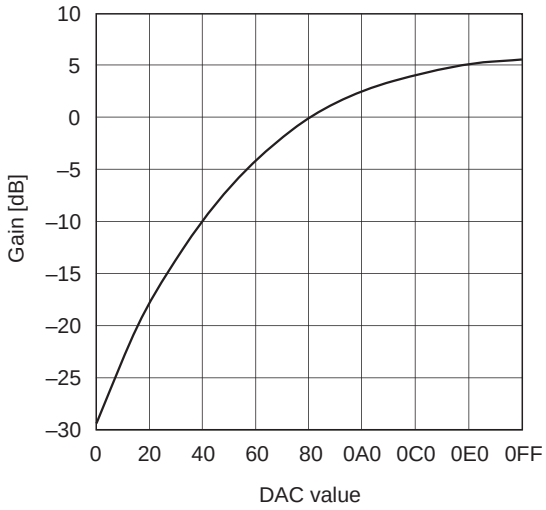
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

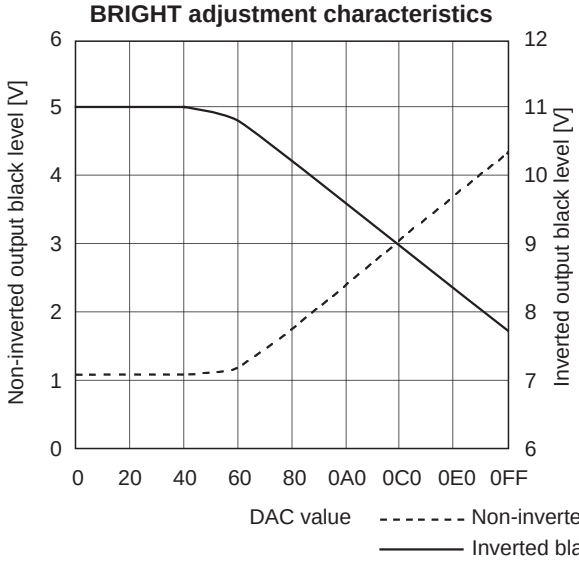
HUE adjustment characteristics



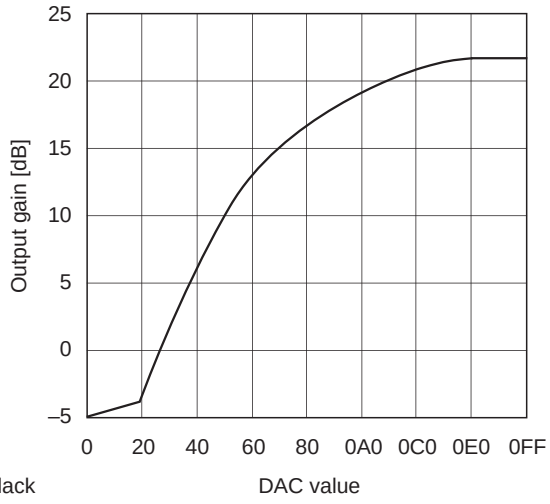
COLOR adjustment characteristics



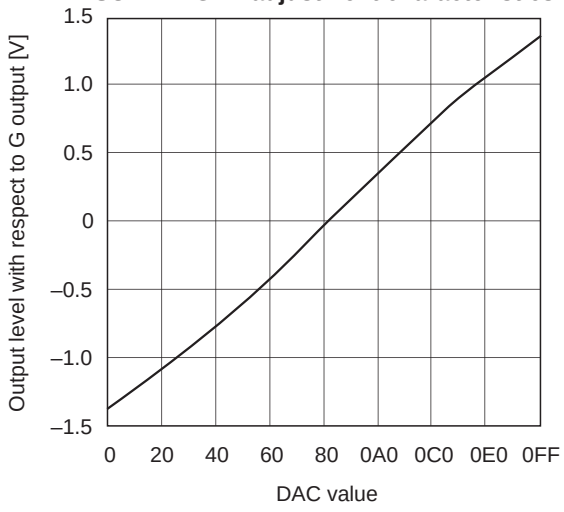
BRIGHT adjustment characteristics



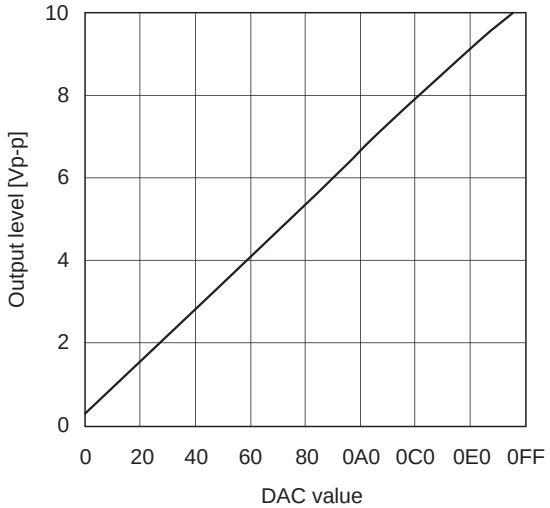
CONTRAST adjustment characteristics



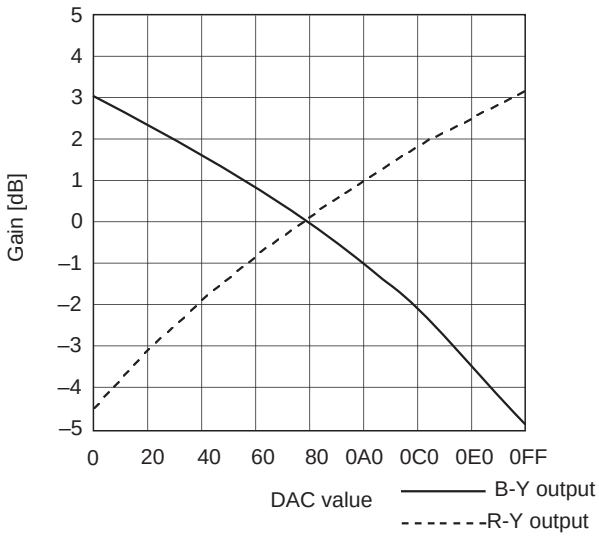
SUB-BRIGHT adjustment characteristics



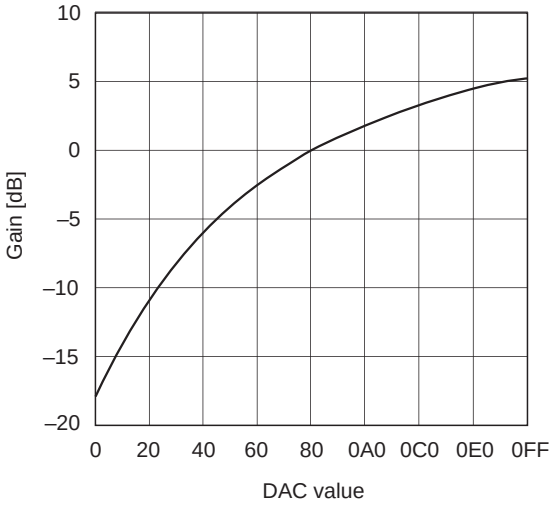
PSIG-BRIGHT adjustment characteristics



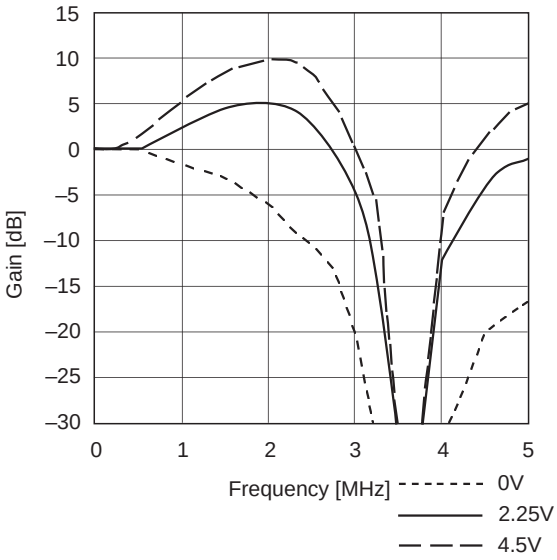
Color difference balance adjustment



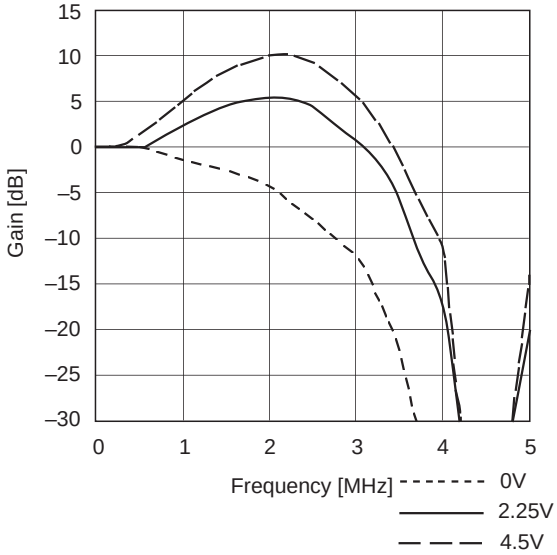
Color difference COLOR adjustment characteristics



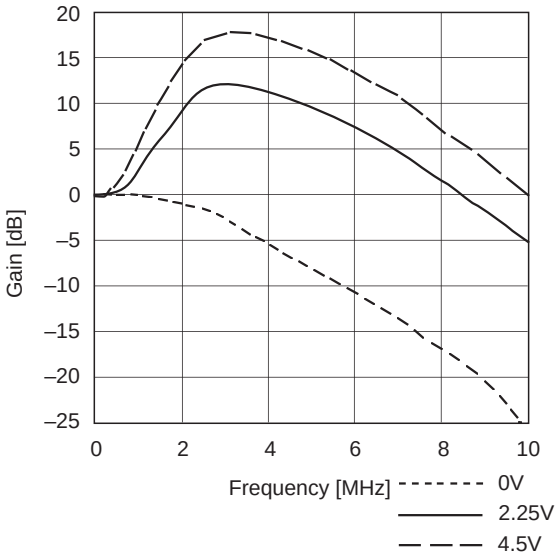
Sharpness characteristics (COMP, NTSC)



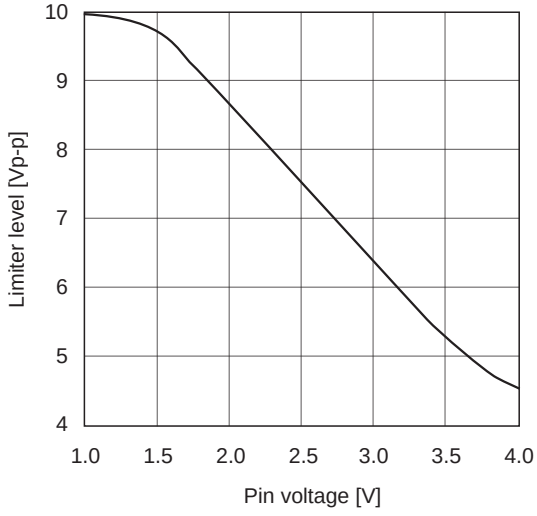
Sharpness characteristics (COMP, PAL)



Sharpness characteristics (Y/C)



Black level limiter adjustment characteristics



Notes on Operation

The CXA2543R contains digital circuits, so the set board pattern must be designed in consideration of undesired radiation, interference to analog circuits, etc. Care should also be taken for the following items when designing the pattern.

- Make the IC power supply and GND patterns as plain as possible. In particular, GND and V_{SS} should not be separated and should be connected to the same GND pattern as close to the pins as possible.
- Connect the by-pass capacitors between the power supplies and GND as close to the pins as possible.
- The trap connected to Pin 1 should be located as close to the pin as possible. Also, don't pass other signal lines close to this pin or the connected trap.
- The wiring for the crystal and capacitor connected to Pins 56 and 57 should be as short as possible in order to prevent floating capacitance. Don't pass other signal lines close to these pins in order to prevent interference such as color unevenness. In addition, the APC pull-in characteristics vary significantly according to the characteristics of the used crystal and the wiring pattern, so be sure to thoroughly investigate these items before using the set.
- The resistor connected to Pin 63 should be located as close to the pin as possible. Also, take care not to pass other signal lines close to this pin.

The composite/Y signal and the external R-Y and B-Y signals are clamped at the inputs using the capacitors connected to the input pins, so these signals should be input at sufficiently low impedance. The C signal is received by the internal capacitor, so this signal should be directly input at low impedance.

The smoothing capacitor of the DC level control feedback circuit in the output block should have a leak current with a small absolute value and variance.

A thorough study of the external buffer for PSIG output should be made before deciding on a circuit to ascertain that it sufficiently brings out the characteristics of the LCD panel.

If this IC is used in connection with a circuit other than an LCD, it may cause that circuit to malfunction depending on the order power is supplied to the circuits. Thoroughly study the consequences of using this IC with other circuits before deciding on its use.

Since this IC utilizes a C-MOS structure, it may latch up due to excessive noise or power surge greater than the maximum rating of the I/O pins, or due to interface with the power supply of another circuit, or due to the order in which power is supplied to circuits. Be sure to take measures against the possibility of latch up.

Do not apply a voltage higher than V_{DD} or lower than V_{SS} to I/O pins.

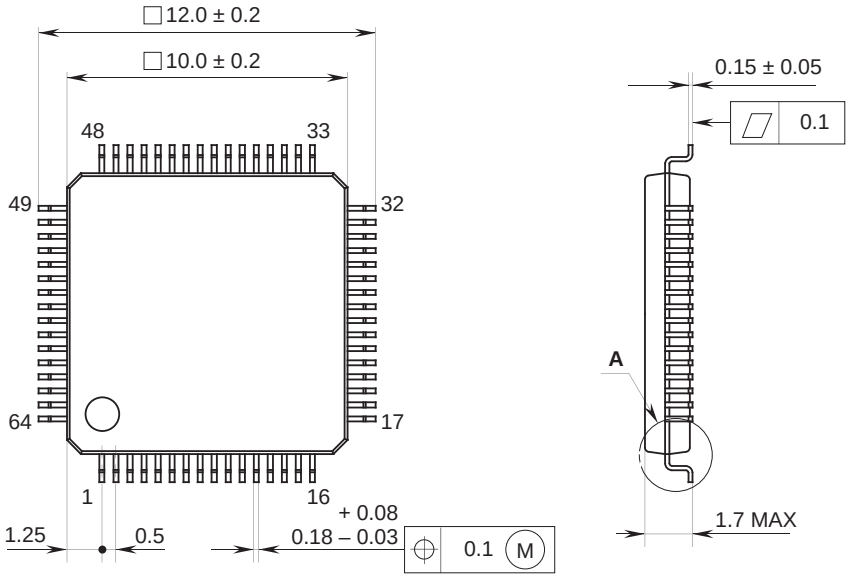
Do not use this IC under operating conditions other than those given.

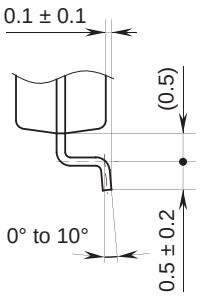
Absolute maximum rating values should not be exceeded even momentarily. Exceeding ratings may damage the device, leading to eventual breakdown.

This IC has a MOS structure which is easily damaged by static electricity, so thorough measures should be taken to prevent electrostatic discharge.

Package Outline Unit: mm

64PIN LQFP (PLASTIC)





DETAIL **A**

SONY CODE	LQFP-64P-L061
EIAJ CODE	LQFP064-P-1010-AY
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g