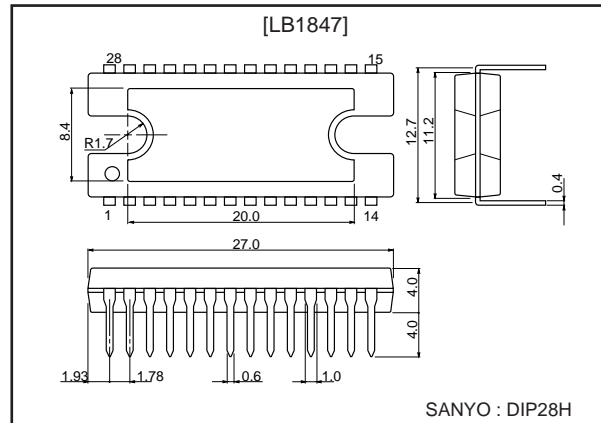


**LB1847****PWM Current Control Type Stepping Motor Driver****Overview**

The LB1847 is a driver IC for stepping motors with PWM current control bipolar drive (fixed OFF time). A special feature of this IC is that  $V_{REF}$  voltage is constant while the current can be set in 15 steps, allowing drive of motors ranging from 1-2 phase exciter types to 4W 1-2 phase exciter types. The current decay pattern can also be selected (SLOW DECAY, FAST DECAY, MIX DECAY) to increase the decay of regenerative current at chopping OFF, thereby improving response characteristics. This is especially useful for carriage and paper feed stepping motors in printers and similar applications where high-precision control and low vibrations are required.

**Package Dimensions**

unit: mm

**3147B-DIP28H****Features**

- PWM current control (fixed OFF time)
- Load current digital selector (1-2, W1-2, 2W1-2, 4W1-2 phase exciter drive possible)
- Selectable current decay pattern (SLOW DECAY, FAST DECAY, MIX DECAY)
- Simultaneous ON prevention function (feedthrough current prevention)
- Noise canceler
- Built-in thermal shutdown circuit
- Built-in logic low-voltage OFF circuit

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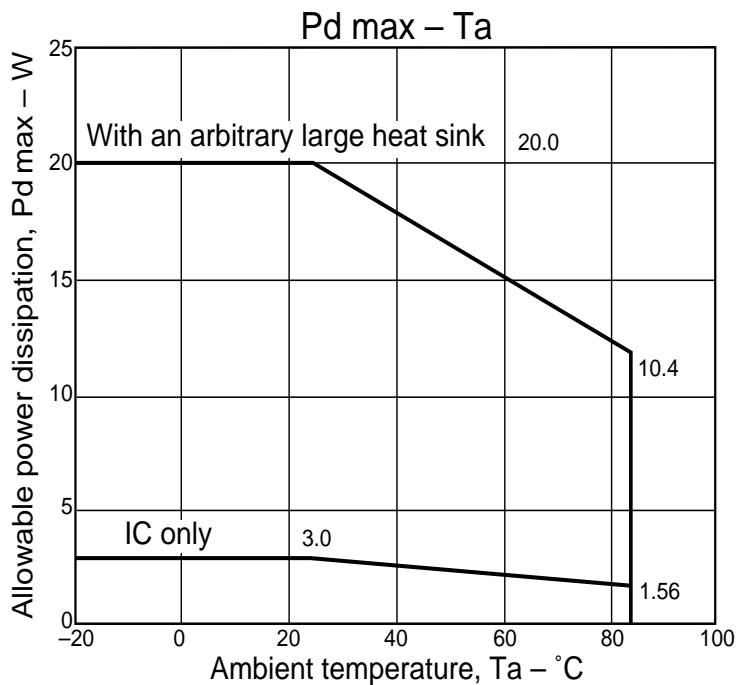
Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	$V_{BB}$		50	V
Output peak current	$I_{OPEAK}$	$t_W \leq 20 \mu\text{s}$	1.75	A
Output continuous current	$I_O \text{ max}$		1.5	A
Logic supply voltage	$V_{CC}$		7.0	V
Logic input voltage range	$V_{IN}$		-0.3 to $V_{CC}$	V
Emitter output voltage	$V_E$		1.0	V
Allowable power dissipation	Pd max	$T_a = 25^\circ\text{C}$	3.0	W
		With heat sink	20	W
Operating temperature range	$T_{opr}$		-20 to +85	$^\circ\text{C}$
Storage temperature range	$T_{stg}$		-55 to +150	$^\circ\text{C}$

Allowable Operating Ranges at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage range	$V_{BB}$		10 to 45	V
Logic supply voltage range	$V_{CC}$		4.75 to 5.25	V
Reference voltage range	$V_{REF}$		0.0 to 3.0	V



# LB1847

## Electrical Characteristics at Ta = 25°C, V<sub>BB</sub> = 45V, V<sub>CC</sub> = 5V, V<sub>REF</sub> = 1.52V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Output Block]						
Output stage supply voltage	I <sub>BB ON</sub>		2.3	3.5	5.0	mA
	I <sub>BB OFF</sub>		0.5	0.8	1.1	mA
Output saturation voltage	V <sub>O(sat)1</sub>	I <sub>O</sub> =+1.0A, sink		1.2	1.6	V
	V <sub>O(sat)2</sub>	I <sub>O</sub> =+1.5A, sink		1.5	1.9	V
	V <sub>O(sat)3</sub>	I <sub>O</sub> =-1.0A, source		1.9	2.2	V
	V <sub>O(sat)4</sub>	I <sub>O</sub> =-1.5A, source		2.2	2.4	V
Output leak current	I <sub>O(leak)1</sub>	V <sub>O</sub> =V <sub>BB</sub> , sink			50	μA
	I <sub>O(leak)2</sub>	V <sub>O</sub> =0V, source	-50			μA
Output sustain voltage	V <sub>SUS</sub>	L=15 mH, I <sub>O</sub> =1.5A, Guaranteed design value	45			V
[Logic Block]						
Logic supply voltage	I <sub>CC ON</sub>	I <sub>4</sub> =3.2V, I <sub>3</sub> =3.2V, I <sub>2</sub> =3.2V, I <sub>1</sub> =3.2V	19.5	26	36.5	mA
	I <sub>CC OFF</sub>	ENABLE=3.2V	10.5	15	19.5	mA
Input voltage	V <sub>IH</sub>		3.2			V
	V <sub>IL</sub>				0.8	V
Input current	I <sub>IH</sub>	V <sub>IH</sub> =3.2V			100	μA
	I <sub>IL</sub>	V <sub>IL</sub> =0.8V	-10			μA
Sensing voltage	V <sub>E</sub>	I <sub>4</sub> =3.2V, I <sub>3</sub> =3.2V, I <sub>2</sub> =3.2V, I <sub>1</sub> =3.2V	0.470	0.50	0.525	V
		I <sub>4</sub> =3.2V, I <sub>3</sub> =3.2V, I <sub>2</sub> =3.2V, I <sub>1</sub> =0.8V	0.445	0.48	0.505	V
		I <sub>4</sub> =3.2V, I <sub>3</sub> =3.2V, I <sub>2</sub> =0.8V, I <sub>1</sub> =3.2V	0.425	0.46	0.485	V
		I <sub>4</sub> =3.2V, I <sub>3</sub> =3.2V, I <sub>2</sub> =0.8V, I <sub>1</sub> =0.8V	0.410	0.43	0.465	V
		I <sub>4</sub> =3.2V, I <sub>3</sub> =0.8V, I <sub>2</sub> =3.2V, I <sub>1</sub> =3.2V	0.385	0.41	0.435	V
		I <sub>4</sub> =3.2V, I <sub>3</sub> =0.8V, I <sub>2</sub> =3.2V, I <sub>1</sub> =0.8V	0.365	0.39	0.415	V
		I <sub>4</sub> =3.2V, I <sub>3</sub> =0.8V, I <sub>2</sub> =0.8V, I <sub>1</sub> =3.2V	0.345	0.37	0.385	V
		I <sub>4</sub> =3.2V, I <sub>3</sub> =0.8V, I <sub>2</sub> =0.8V, I <sub>1</sub> =0.8V	0.325	0.35	0.365	V
		I <sub>4</sub> =0.8V, I <sub>3</sub> =3.2V, I <sub>2</sub> =3.2V, I <sub>1</sub> =3.2V	0.280	0.30	0.325	V
		I <sub>4</sub> =0.8V, I <sub>3</sub> =3.2V, I <sub>2</sub> =3.2V, I <sub>1</sub> =0.8V	0.240	0.26	0.285	V
		I <sub>4</sub> =0.8V, I <sub>3</sub> =3.2V, I <sub>2</sub> =0.8V, I <sub>1</sub> =3.2V	0.195	0.22	0.235	V
		I <sub>4</sub> =0.8V, I <sub>3</sub> =3.2V, I <sub>2</sub> =0.8V, I <sub>1</sub> =0.8V	0.155	0.17	0.190	V
		I <sub>4</sub> =0.8V, I <sub>3</sub> =0.8V, I <sub>2</sub> =3.2V, I <sub>1</sub> =3.2V	0.115	0.13	0.145	V
I <sub>4</sub> =0.8V, I <sub>3</sub> =0.8V, I <sub>2</sub> =3.2V, I <sub>1</sub> =0.8V	0.075	0.09	0.100	V		
Reference current	I <sub>REF</sub>	V <sub>REF</sub> =1.5V	-0.5			μA
CR pin current	I <sub>CR</sub>	CR=1.0V	-4.6		-1.0	mA
MD pin current	I <sub>MD</sub>	MD=1.0V, CR=4.0V	-5.0			μA
DECAY pin current Low	I <sub>DECL</sub>	V <sub>DEC</sub> =0.8V	-10			μA
DECAY pin current High	I <sub>DECH</sub>	V <sub>DEC</sub> =3.2V			5	μA
Thermal shutdown temperature	TSD			170		°C
Logic ON voltage	L <sub>VSD1</sub>		3.35	3.65	3.95	V
Logic OFF voltage	L <sub>VSD2</sub>		3.20	3.50	3.80	V
L <sub>VSD</sub> hysteresis width	ΔL <sub>VSD</sub>		0.065	0.15	0.23	V

**Truth table**

PHASE	ENABLE	OUT <sub>A</sub>	OUT <sub>A</sub> <sup>̄</sup>
H	L	H	L
L	L	L	H
—	H	OFF	OFF

**Set current truth table**

I <sub>A4</sub>	I <sub>A3</sub>	I <sub>A2</sub>	I <sub>A1</sub>	Set current I <sub>out</sub>	Current ratio (%)
1	1	1	1	11.5/11.5 X V <sub>REF</sub> /3.04RE=lout	100
1	1	1	0	11.0/11.5 X V <sub>REF</sub> /3.04RE=lout	95.65
1	1	0	1	10.5/11.5 X V <sub>REF</sub> /3.04RE=lout	91.30
1	1	0	0	10.0/11.5 X V <sub>REF</sub> /3.04RE=lout	86.95
1	0	1	1	9.5/11.5 X V <sub>REF</sub> /3.04RE=lout	82.61
1	0	1	0	9.0/11.5 X V <sub>REF</sub> /3.04RE=lout	78.26
1	0	0	1	8.5/11.5 X V <sub>REF</sub> /3.04RE=lout	73.91
1	0	0	0	8.0/11.5 X V <sub>REF</sub> /3.04RE=lout	69.56
0	1	1	1	7.0/11.5 X V <sub>REF</sub> /3.04RE=lout	60.87
0	1	1	0	6.0/11.5 X V <sub>REF</sub> /3.04RE=lout	52.17
0	1	0	1	5.0/11.5 X V <sub>REF</sub> /3.04RE=lout	43.48
0	1	0	0	4.0/11.5 X V <sub>REF</sub> /3.04RE=lout	34.78
0	0	1	1	3.0/11.5 X V <sub>REF</sub> /3.04RE=lout	26.08
0	0	1	0	2.0/11.5 X V <sub>REF</sub> /3.04RE=lout	17.39

\* Current ratio (%) is the calculated set current value.

**Current decay switching truth table**

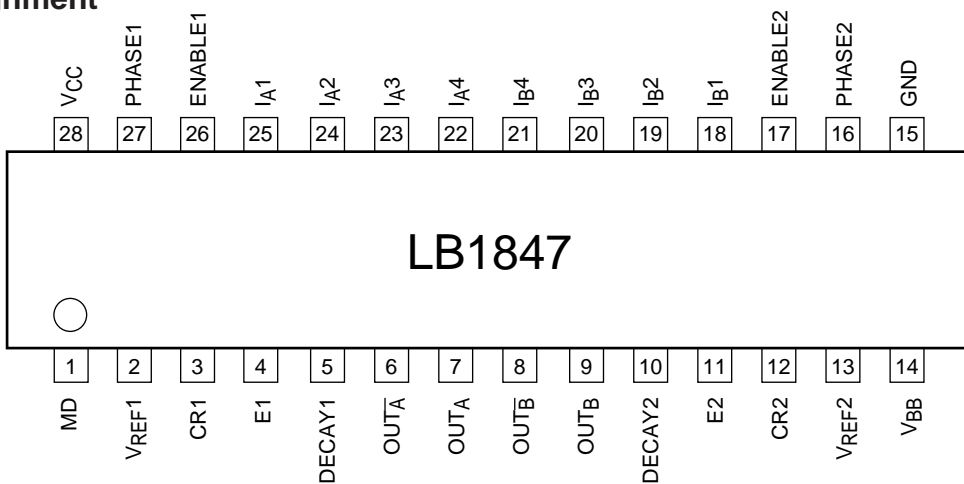
Current decay mode	DECAY pin	MD pin	Output chopping
SLOW DECAY	H	L	Top-side chopping
FAST DECAY	L	L	Dual-side chopping
MIX DECAY	L	4V to 1.5V input voltage setting	CR voltage > MD : dual-side chopping CR voltage < MD : top-side chopping

# LB1847

## Pin function

Pin number	Pin name	Function description
1	MD	Sets the OFF time for FAST mode and SLOW mode in MIX DECAY Setting input range: 4V to 1.5V
2	V <sub>REF1</sub>	Output set current reference supply pin
13	V <sub>REF2</sub>	Setting voltage range: 0V to 3V
3	CR1	Output OFF time setting pin for switching operation
12	CR2	
4	E1	Pin for controlling the set current with sensing resistor RE
11	E2	
5	DECAY1	SLOW mode/FAST mode selector pin
10	DECAY2	SLOW DECAY: H FAST DECAY: L
6	OUT <sub>A</sub>	Output pin
7	OUT <sub>A</sub>	
8	OUT <sub>B</sub>	
9	OUT <sub>B</sub>	
14	V <sub>BB</sub>	Output stage supply voltage pin
15	GND	Ground pin
27	PHASE1	Output phase selector input pin
16	PHASE2	
26	ENABLE1	Output ON/OFF setting input pin
17	ENABLE2	
22, 23	I <sub>A4</sub> , I <sub>A3</sub>	Output set current digital input pin 15-stage voltage setting
24, 25	I <sub>A2</sub> , I <sub>A1</sub>	
21, 20	I <sub>B4</sub> , I <sub>B3</sub>	
19, 18	I <sub>B2</sub> , I <sub>B1</sub>	
28	V <sub>CC</sub>	Logic block supply voltage pin

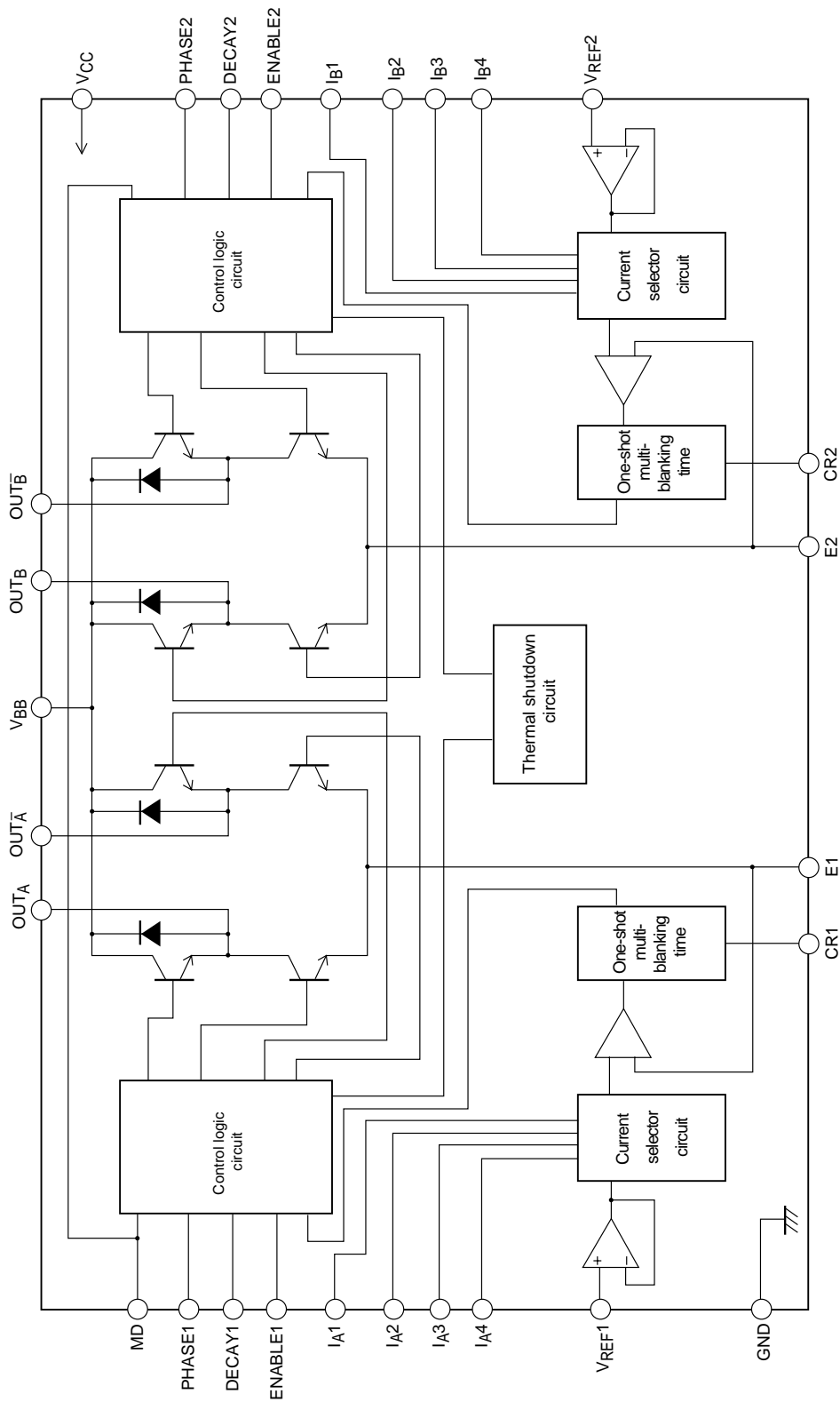
## Pin Assignment



Top view

A11312

Block diagram



A11311

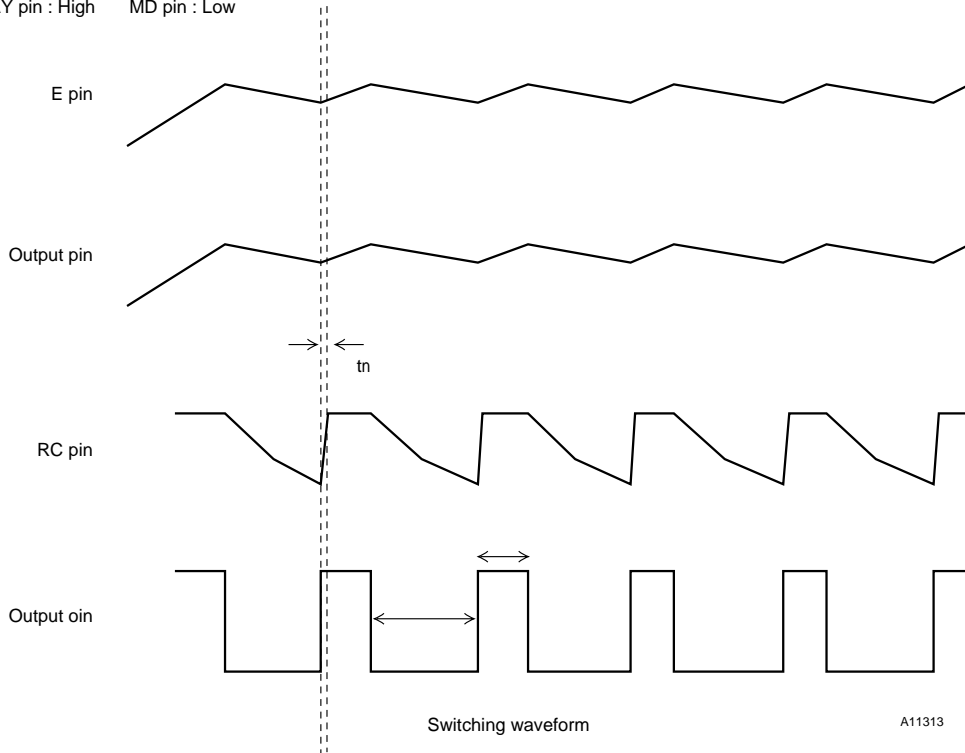
Sequence table

No.	Phase A							Phase B							Phase 1-2	Phase W1-2	Phase 2W1-2	Phase 4W1-2
	IA4	IA3	IA2	IA1	ENA1	PHA1	lout	IB4	IB3	IB2	IB1	ENA1	PHA1	lout				
0	1	1	1	1	0	0	100%	0	0	1	0	1	*	0%	√	√	√	√
1	1	1	1	1	0	0	100	0	0	1	0	0	0	17.39				√
2	1	1	1	1	0	0	100	0	0	1	1	0	0	26.08			√	√
3	1	1	1	0	0	0	96.65	0	1	0	0	0	0	34.78			√	√
4	1	1	0	1	0	0	91.30	0	1	0	1	0	0	43.48		√	√	√
5	1	1	0	0	0	0	86.95	0	1	1	0	0	0	52.17			√	√
6	1	0	1	1	0	0	82.61	0	1	1	1	0	0	60.87			√	√
7	1	0	1	0	0	0	78.26	1	0	0	0	0	0	69.56			√	√
8	1	0	0	1	0	0	73.91	1	0	0	1	0	0	73.91	√	√	√	√
9	1	0	0	0	0	0	69.56	1	0	1	0	0	0	78.26			√	√
10	0	1	1	1	0	0	60.87	1	0	1	1	0	0	82.61			√	√
11	0	1	1	0	0	0	52.17	1	1	0	0	0	0	86.95			√	√
12	0	1	0	1	0	0	43.48	1	1	0	1	0	0	91.30		√	√	√
13	0	1	0	0	0	0	34.78	1	1	1	0	0	0	96.65			√	√
14	0	0	1	1	0	0	26.08	1	1	1	1	0	0	100			√	√
15	0	0	1	0	0	0	17.39	1	1	1	1	0	0	100			√	√
16	0	0	0	1	1	*	0	1	1	1	1	0	0	100	√	√	√	√
17	0	0	1	0	0	1	17.39	1	1	1	1	0	0	100			√	√
18	0	0	1	1	0	1	26.08	1	1	1	1	0	0	100			√	√
19	0	1	0	0	0	1	34.78	1	1	1	0	0	0	95.65			√	√
20	0	1	0	1	0	1	43.48	1	1	0	1	0	0	91.30		√	√	√
21	0	1	1	0	0	1	52.17	1	1	0	0	0	0	86.95			√	√
22	0	1	1	1	0	1	60.87	1	0	1	1	0	0	82.61			√	√
23	1	0	0	0	0	1	69.56	1	0	1	0	0	0	78.26			√	√
24	1	0	0	1	0	1	73.91	1	0	0	1	0	0	73.91	√	√	√	√
25	1	0	1	0	0	1	78.26	1	0	0	0	0	0	69.56			√	√
26	1	0	1	1	0	1	82.61	0	1	1	1	0	0	60.87			√	√
27	1	1	0	0	0	1	86.95	0	1	1	0	0	0	52.17			√	√
28	1	1	0	1	0	1	91.30	0	1	0	1	0	0	43.48		√	√	√
29	1	1	1	0	0	1	95.65	0	1	0	0	0	0	34.78			√	√
30	1	1	1	1	0	1	100	0	0	1	1	0	0	26.08			√	√
31	1	1	1	1	0	1	100	0	0	1	0	0	0	17.39			√	√

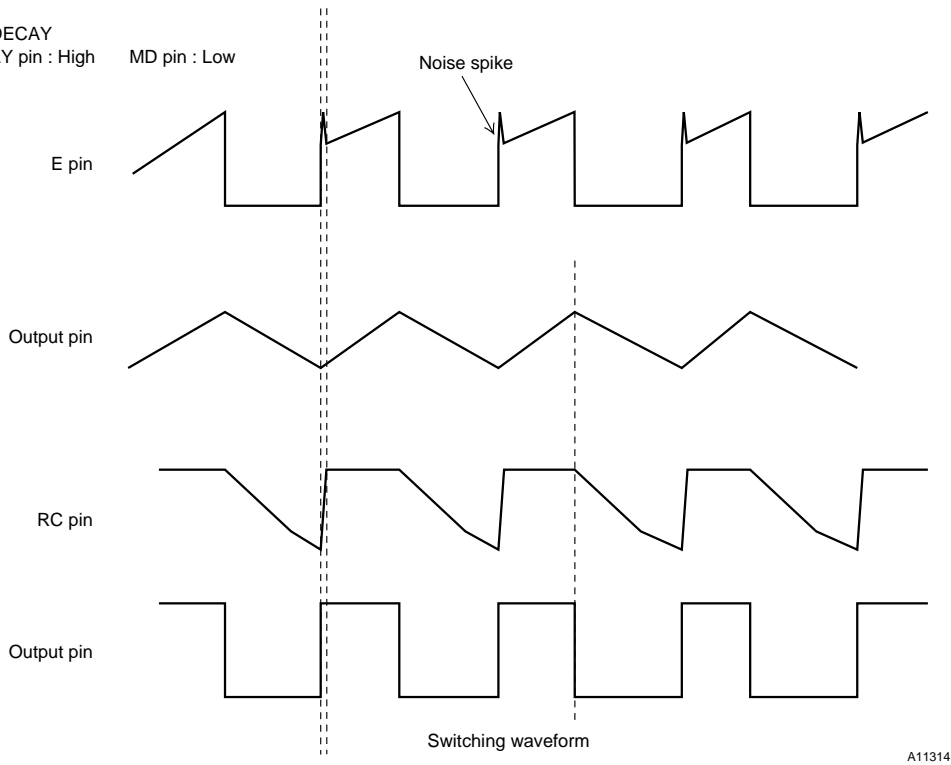
\* : lout percentage (%) is the calculated setting value.

### Switch timing chart during PWM drive

SLOW DECAY (top-side chopping)  
DECAY pin : High MD pin : Low

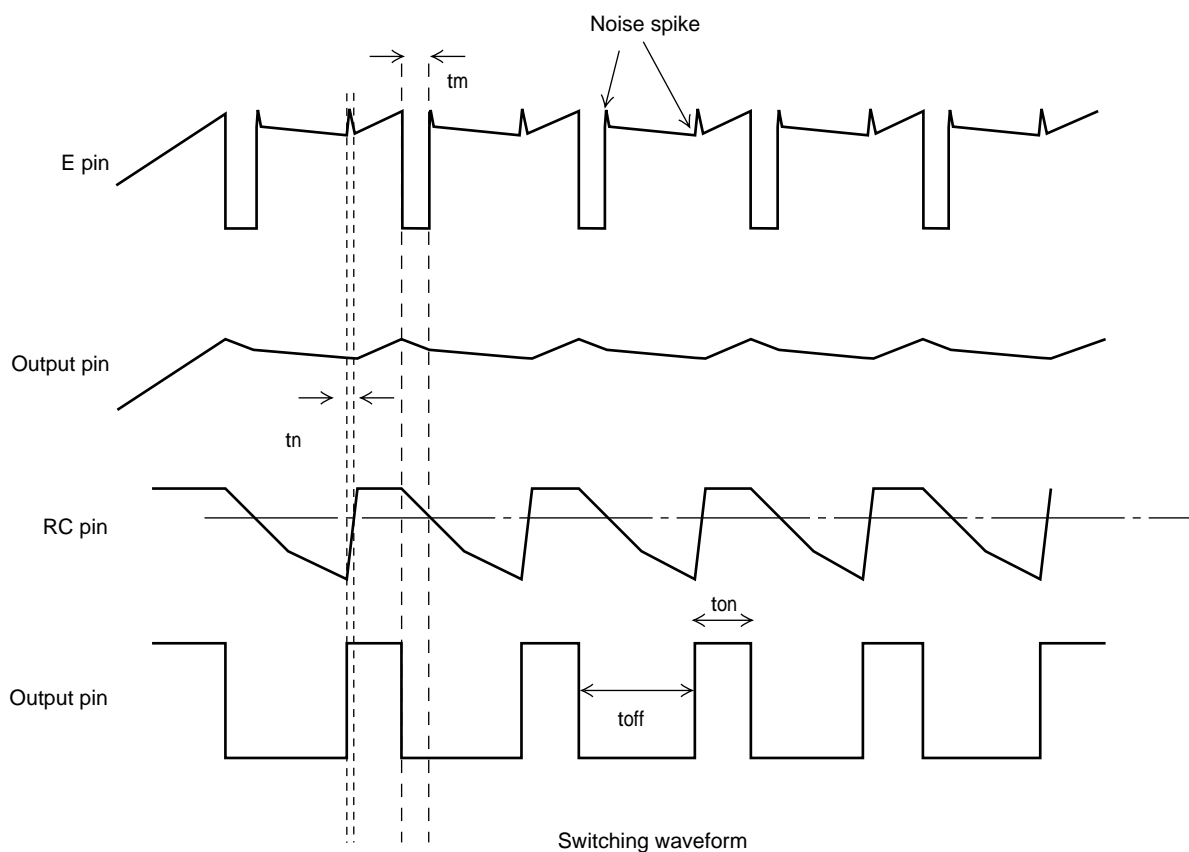


FAST DECAY  
DECAY pin : High MD pin : Low





MIX DECAY



A11315

- $t_{on}$  : Output ON time
- $t_{off}$  : Output OFF time
- $t_m$  : FAST DECAY time in MIX DECAY mode
- $t_n$  : Noise cancelling time

MIX DECAY logic setting

DECAY pin : L

MD pin : 1.5V to 4.0V voltage setting

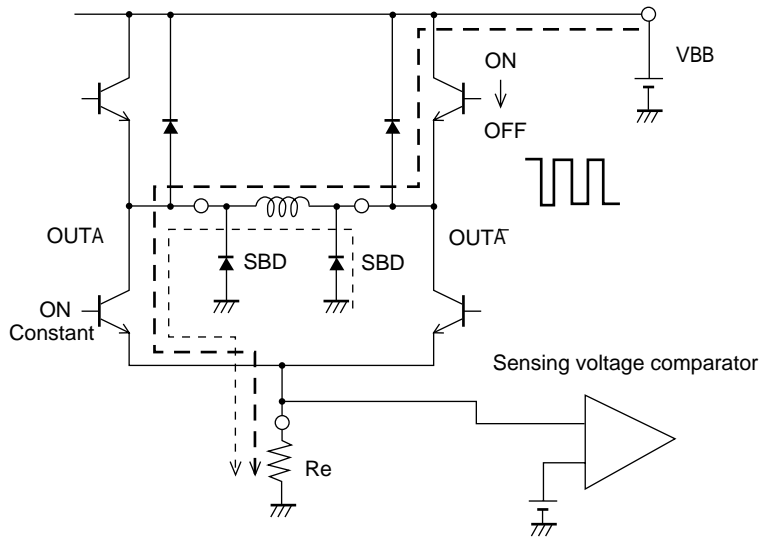
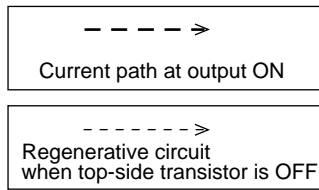
CR voltage and MD pin voltage are compared to select dual-side chopping or top-side chopping.

CR voltage > MD pin voltage: dual-side chopping

CR voltage < MD pin voltage: top-side choppi

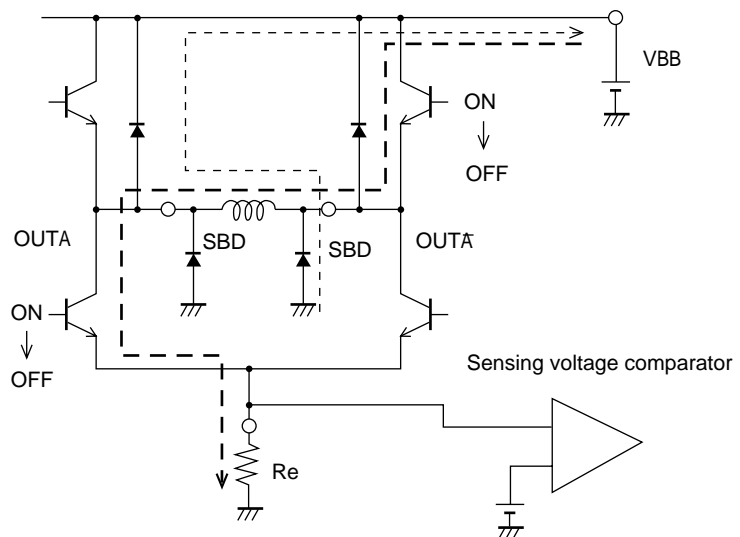
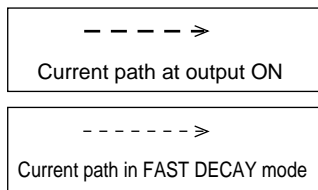
SLOW DECAY current path

Regenerative current during top-side transistor switching operation



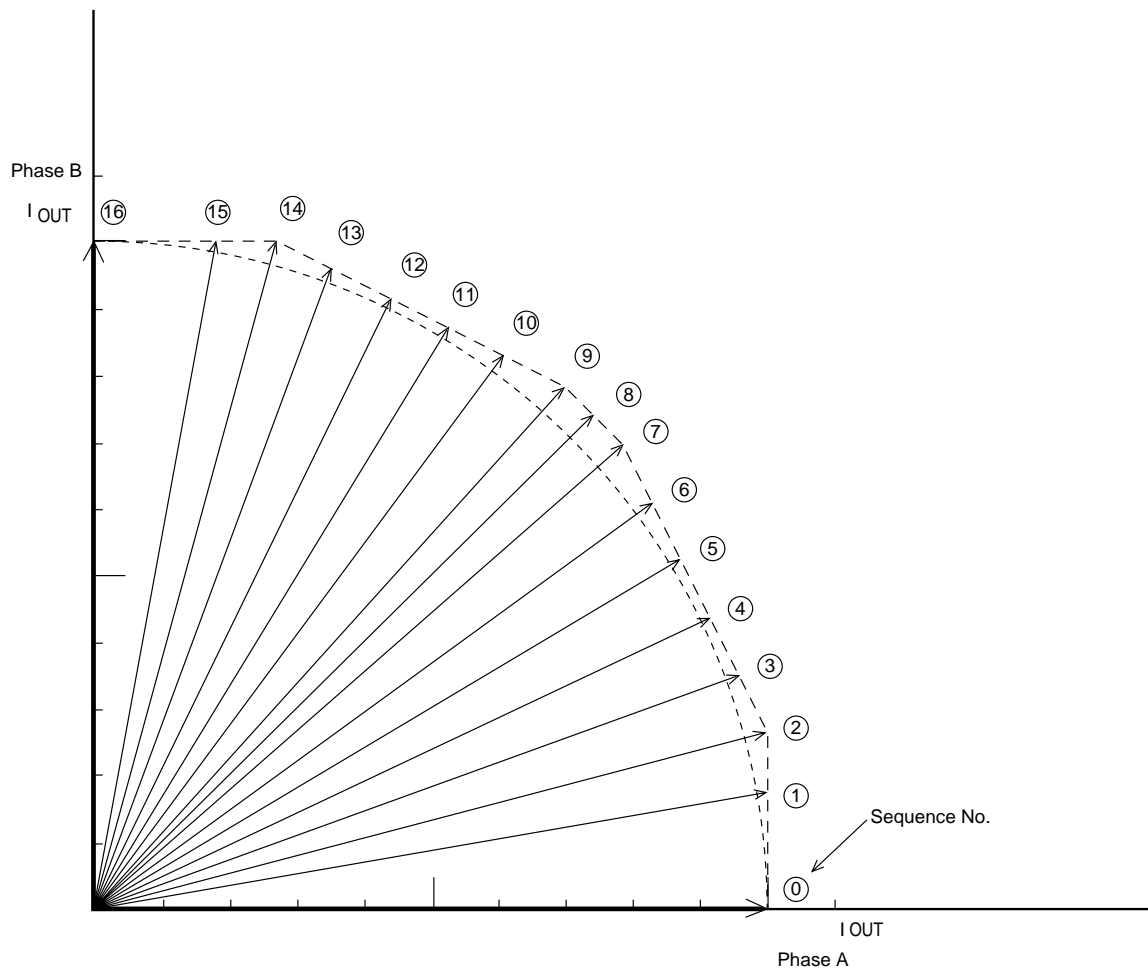
A11316

Current path in FAST DECAY mode



A11317

Composite spectrum of set current (1 step normalized to 90°)

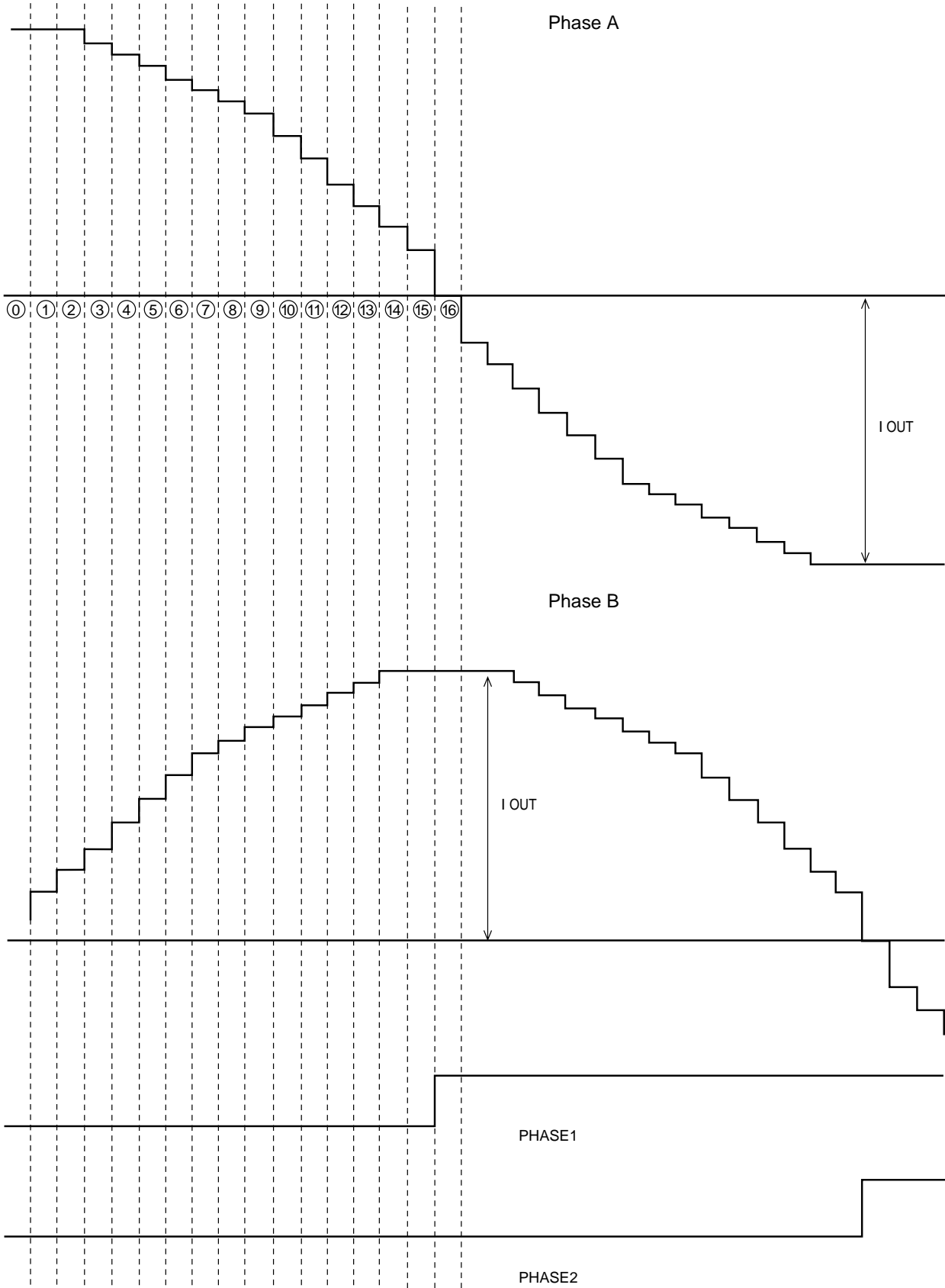


A11318

No.	$\theta$	Rotation angle	Composite spectrum
0	$\theta_0$	0°	100.0
1	$\theta_1$	9.87°	101.5
2	$\theta_2$	14.6°	103.35
3	$\theta_3$	20.0°	101.78
4	$\theta_4$	25.5°	101.12
5	$\theta_5$	30.96°	101.4
6	$\theta_6$	36.38°	102.61
7	$\theta_7$	41.63°	104.7
8	$\theta_8$	45.0°	104.5
9	$\theta_9$	48.37°	104.7
10	$\theta_{10}$	53.62°	102.61
11	$\theta_{11}$	59.04°	101.4
12	$\theta_{12}$	64.5°	101.12
13	$\theta_{13}$	70.0°	101.78
14	$\theta_{14}$	75.4°	103.35
15	$\theta_{15}$	80.13°	101.5
16	$\theta_{16}$	90.0°	100.0

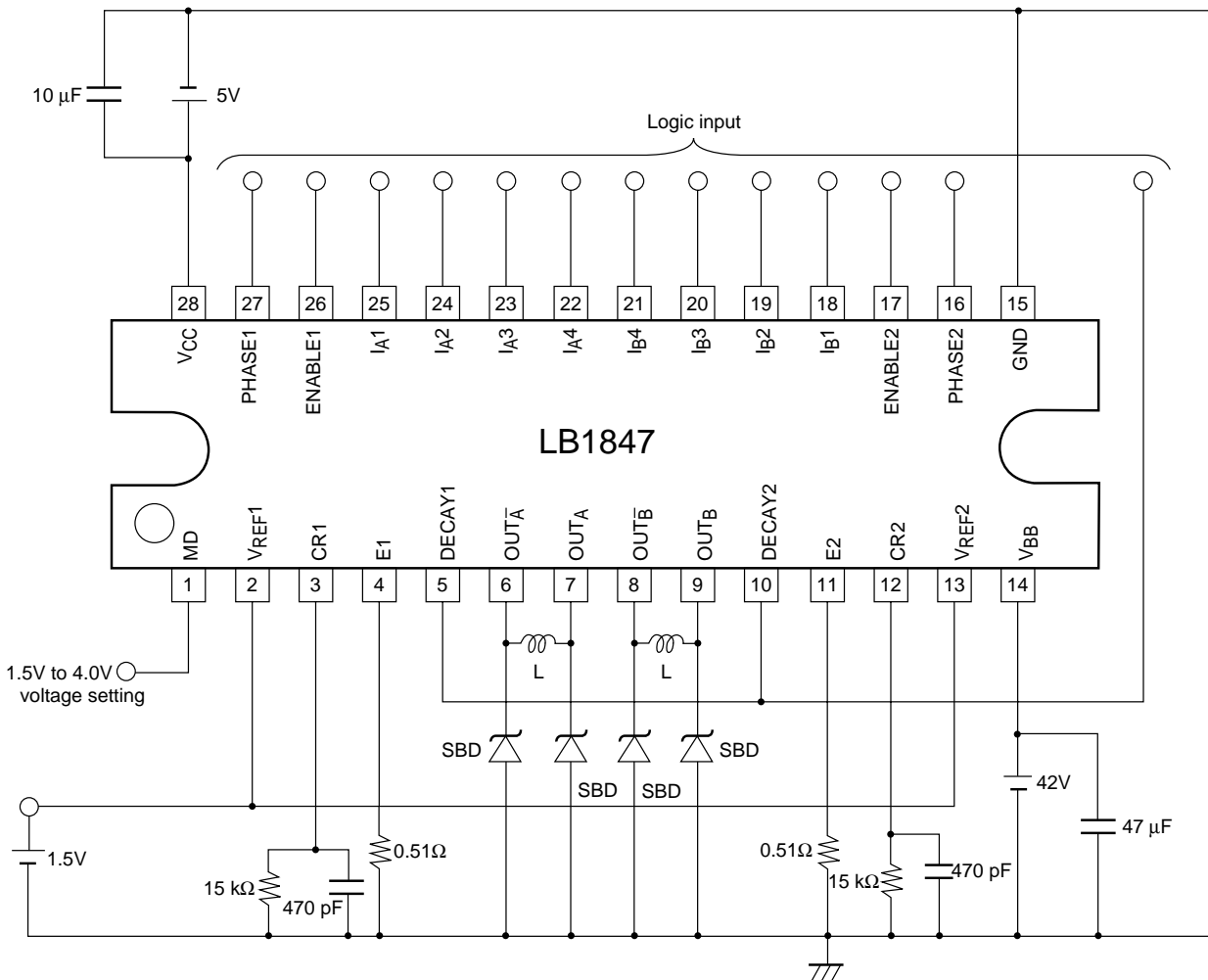
\* Rotation angle and composite spectrum are calculated values.

Set current waveform model



A11319

Sample Application Circuit



A11320

Notes on Usage

1. External diodes

Because this IC uses top-side transistor switching in SLOW DECAY mode and dual-side transistor switching in FAST DECAY mode, it requires external diodes between the OUT pins and ground, for the regenerative current during switching OFF. Use Schottky barrier diodes with low VF.

2. VREF pin

Because the VREF pin serves for input of the set current reference voltage, precautions against noise must be taken. The input voltage range is 0 to 3.0V.

3. GND pin

The ground circuit for this IC must be designed so as to allow for high-current switching. Blocks where high current flows must use low-impedance patterns and must be removed from small-signal lines. Especially the ground connection for the sensing resistor RE at pin E, and the ground connection for the Schottky barrier diodes should be in close proximity to the IC ground.

The capacitors between VCC and ground, and VBB and ground should be placed close to the VCC and VBB pins, respectively.

4. Simultaneous ON prevention function

This IC incorporates a circuit to prevent feedthrough current when phase switching. For reference, the output ON and OFF delay times at PHASE and ENABLE switching are given below.

Reference data \* typical value

		Sink side	Source side
PHASE switching (Low -> Hi)	ON delay time	1.9 μs	2.2 μs
	OFF delay time	0.8 μs	1.8 μs
PHASE switching (Hi -> Low)	ON delay time	1.4 μs	1.7 μs
	OFF delay time	0.9 μs	1.35 μs
ENABLE switching	ON delay time	2.15 μs	2.75 μs
	OFF delay time	1.2 μs	5.8 μs

5. Noise canceler

This IC has a noise canceling function to prevent malfunction due to noise spikes generated when switching ON. The noise cancel time  $t_n$  is determined by internal resistance of the CR pin and the constant of the externally connected CR components. The constant also determines the switching OFF time.

Figure 1 shows the internal configuration at the CR pin, and Figure 2 the CR pin constant setting range.

Equation when logic voltage  $V_{CC} = 5\text{ V}$

$$\text{CR pin voltage } E1 = V_{CC} \cdot R / (R1 + R2 + R) \quad [\text{V}]$$

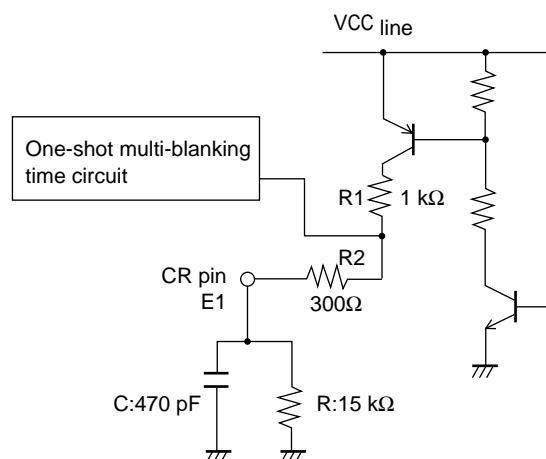
$$\text{Noise cancel time } t_n \cong (R1 + R2) \cdot C \cdot \ln \{ (E1 - 1.5) / (E1 - 4.0) \} \quad [\text{s}]$$

$$\text{Switching OFF time } t_{off} \cong -R \cdot C \cdot \ln (1.5 / E1) \quad [\text{s}]$$

Internal resistance at CR pin :  $R1 = 1\text{ k}\Omega$ ,  $R2 = 300\Omega$  (typ.)

\*The CR constant setting range in Figure 2 on page 15 is given for reference. It applies to a switching OFF time in the range from 8 to 100 μs. The switching time can also be made higher than 100 μs. However, a capacitor value of more than several thousand pF will result in longer noise canceling time, which can cause the output current to become higher than the set current. The longer switching OFF time results in higher output current ripple, causing a drop in average current and rotation efficiency. When keeping the switching OFF time within 100 μs, it is recommended to stay within the CR constant range shown in Figure 2.

Internal configuration at CR pin



A11321

Figure 1

Switching OFF time and CR setting range

( $t_{off}$  time : approx. 8 to 100  $\mu$ s)

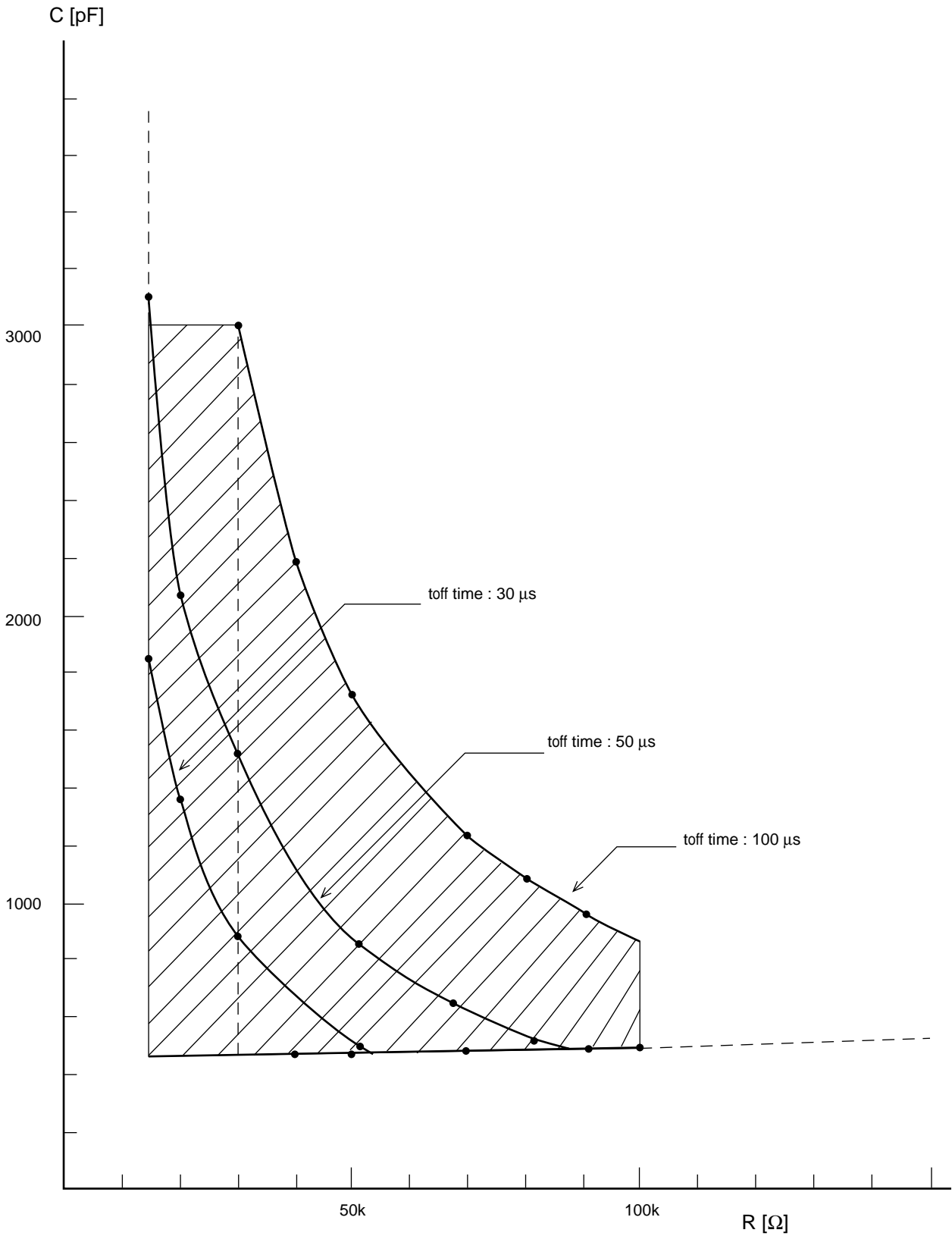
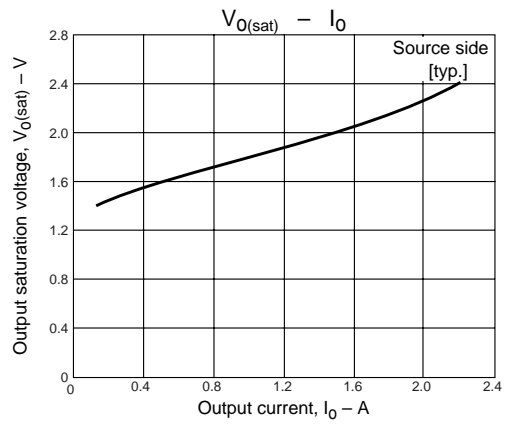
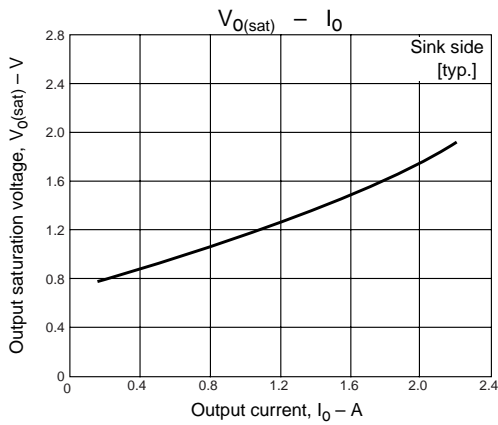
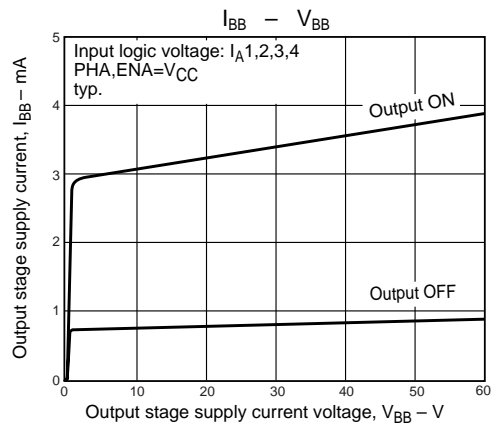
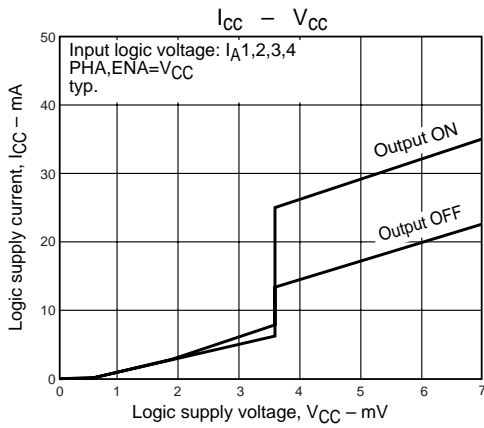


Figure 2

A11322



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