Ordering number : EN*5155

CMOS LSI

LC82102, LC82102W

Image-Processing LSI for Fax, Copier and OCR Products

Preliminary

Overview

The LC82102 and LC82102W convert analog video signals from CCD or contact image sensors to high-quality binary video data. The LC82102/W converts the input analog data to multi-valued data and uses two-dimensional filtering and an error diffusion technique that produces high-quality images to produce a two-valued image. Finally, the LC82102 reduces the image in the main and subsidiary scan directions. The LC82102 requires absolutely no external memory since it limits the number of pixels processed to 2040 per line. This LSI can implement the image processing used by FAX, copier and OCR products.

Features

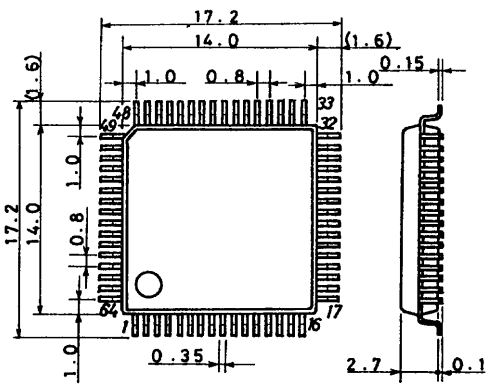
- Number of pixels processed: 2040 pixels/line
- Processing speed: 500 ns/pixel maximum (when the CLKIN input frequency is 32 MHz)
- Built-in 8-bit A/D converter (includes a sensor signal delay adjustment function)
- Built-in 6-bit D/A converter for setting the A/D converter high reference potential
- Sensor drive circuit (supports CCD and all CIS types)
- Digital clamp (single-point clamp, even/odd clamp)
- Distortion correction (white correction: 8-pixel averaging correction, black correction: black correction subtraction data setting)
- Gamma correction (supports user-defined curves)
- Simple binary-conversion processing (fixed threshold level, density-adaptive threshold level)
- Intermediate processing error diffusion (64 levels)
- Image reduction (thinning, fine black line retaining, fine white line retaining)
- Single-voltage 5 V supply and low power due to CMOS process fabrication

Package Dimensions

unit: mm

3159-QFP64E

[LC82102]

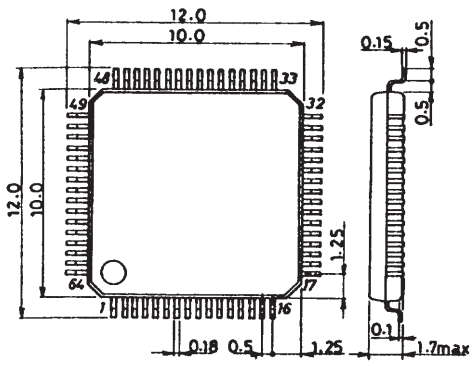


SANYO: QIP64E

unit: mm

3190-SQFP64

[LC82102W]



SANYO: SQFP64

Specifications

Absolute Maximum Ratings at Ta = 25°C, GND = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Maximum I/O voltages	V_I, V_O max		–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	350	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering conditions		Hand soldering: 3 seconds	350	°C
		Reflow soldering: 10 seconds	235	°C

Allowable Operating Ranges at Ta = –30 to +70°C, GND = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5		5.5	V
Input voltage	V_{IN}		0		V_{DD}	V

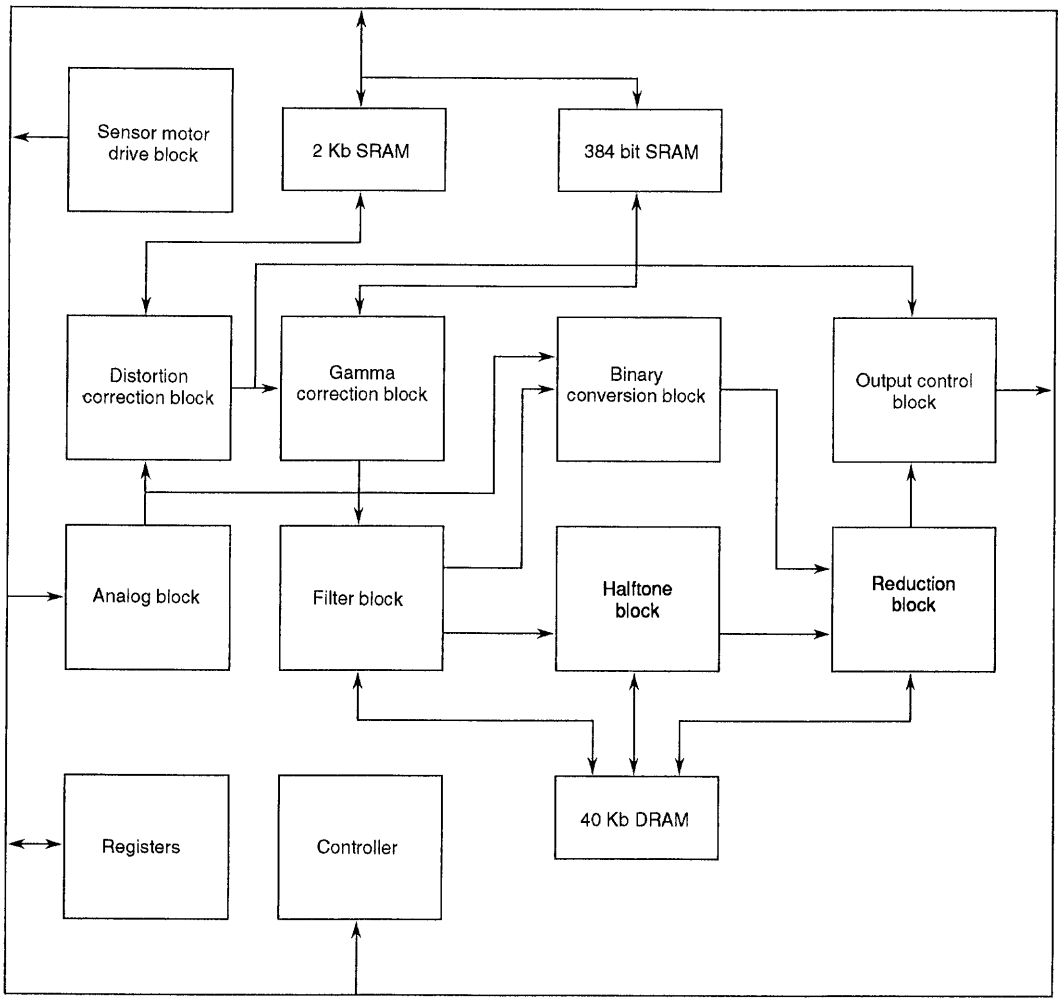
DC Characteristics at Ta = –30 to +70°C, GND = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	V_{IH}		2.2			V
Input low level voltage	V_{IL}				0.8	V
Input leakage current	I_L	V_{IN} = V_{DD}, V_{SS}	–25		+25	µA
Output high level voltage	V_{OH}	I_{OH} = –3 mA	2.4			V
Output low level voltage	V_{OL}	I_{OL} = 3 mA			0.4	V
Output leakage current	I_L	For high-impedance output	–100		+100	µA
Current drain	I_{DD}	CLKIN = 32 MHz		40	70	mA

Analog Characteristics

Parameter	Symbol	Conditions	min	typ	max	Unit
[D/A Converter]						
Resolution				6		bit
Internal resistance				5.0		kΩ
[A/D Converter] when ADREFL = 0 V, and the ATAP potential is 4.2 V						
Resolution				8		bit
Linearity error					±1	LSB
Differential linearity error					±1	LSB
Internal resistance				300		Ω

Block Diagram



Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection

Pin No.	Symbol	I/O	Function
1	D7	B	CPU interface data bus D7 is the MSB and D0 is the LSB.
2	D6	B	
3	D5	B	
4	D4	B	
5	D3	B	
6	D2	B	
7	D1	B	
8	D0	B	
9	DGND	P	Digital system ground
10	DV_{DD}	P	Digital system power supply
11	A8	I	CPU interface address bus A8 is the MSB and A0 is the LSB.
12	A7	I	
13	A6	I	
14	A5	I	
15	A4	I	
16	A3	I	
17	DGND	P	Digital system ground
18	A2	I	CPU interface address bus
19	A1	I	
20	A0	I	

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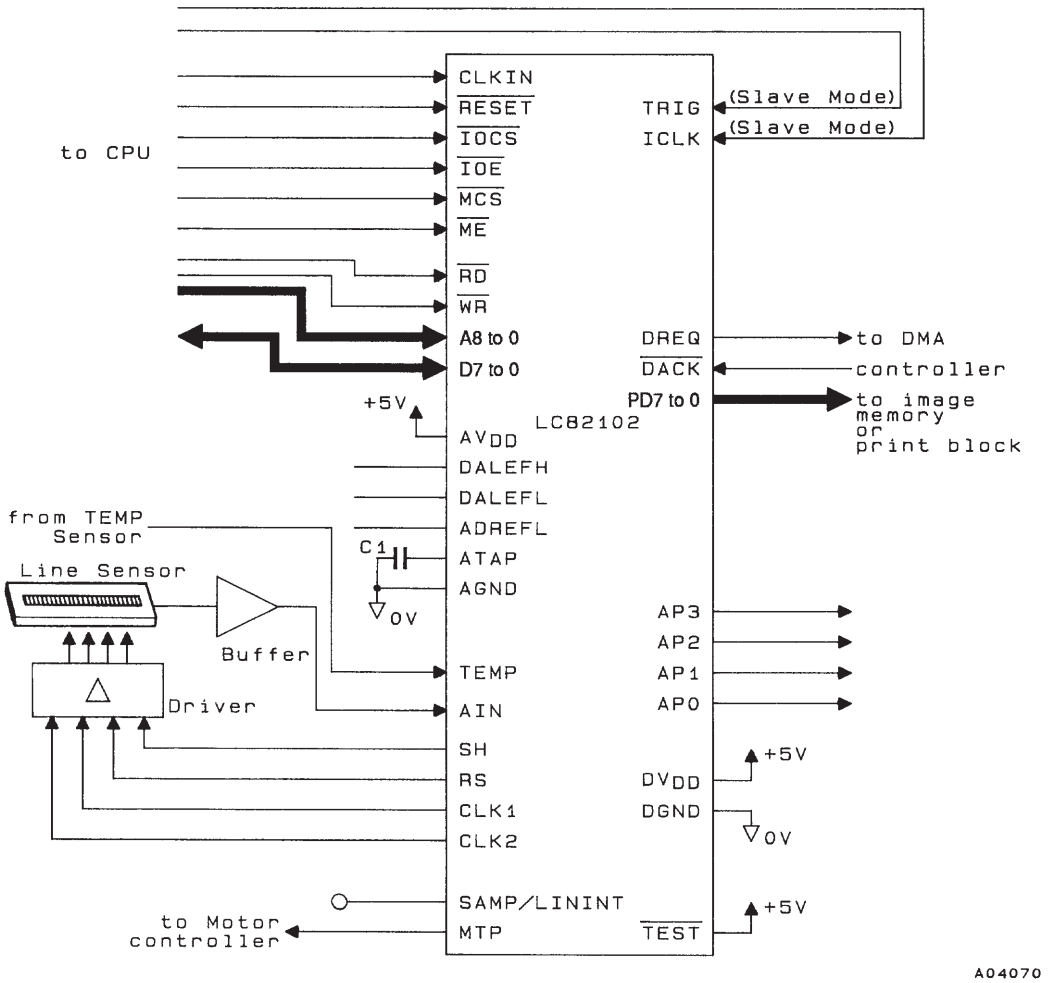
Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection

Pin No.	Symbol	I/O	Function
21	$\overline{WR}$	I	CPU interface write signal
22	$\overline{RD}$	I	CPU interface read signal
23	$\overline{ME}$	I	CPU interface memory enable signal
24	DV_{DD}	P	Digital system power supply
25	CLKIN	I	System clock input
26	$\overline{TEST}$	I	Test pin (Connect to ground in normal use.)
27	$\overline{IOE}$	I	CPU interface I/O enable signal
28	$\overline{MCS}$	I	CPU interface memory chip select signal
29	$\overline{IOCS}$	I	CPU interface I/O chip select signal
30	ICLK	I	External sampling point signal input
31	TRIG	I	External trigger signal input
32	$\overline{RESET}$	I	System reset
33	SAMP/LININT	O	A/D converter sampling point monitor signal output/LINE signal output
34	AP3	O	General-purpose analog ports
35	AP2	O	
36	AGND	P	Digital system ground
37	ADREFL	I	A/D converter low reference voltage
38	DAREFL	I	D/A converter low reference voltage
39	AIN	I	Sensor signal input
40	TEMP	I	Temperature signal input
41	ATAP	O	Intermediate analog connection
42	DAREFH	I	D/A converter high reference voltage
43	AV_{DD}	P	Analog system power supply
44	AP1	O	General-purpose analog ports
45	AP0	O	
46	AGND	P	Analog system ground
47	PD7/SD	B	DMA output/serial data output
48	PD6/SDCK	B	DMA output/serial data transfer clock
49	DGND	P	Digital system ground
50	PD5/SDE	B	DMA output/serial data output valid signal
51	PD4/PP4	B	DMA output/general-purpose I/O ports
52	PD3/PP3	B	
53	PD2/PP2	B	
54	PD1/PP1	B	
55	PD0/PP0	B	
56	DV_{DD}	P	Digital system power supply
57	$\overline{DACK}$/PP5	B	DMA data acknowledge signal input/general-purpose I/O port
58	DREQ/PP5	B	DMA data request signal output/general-purpose I/O port
59	MTP/PP7	B	Motor drive timing signal output/general-purpose I/O port
60	CLK2	O	Sensor drive signal output
61	CLK1	O	
62	RS	O	
63	SH	O	
64	DGND	P	Digital system ground

Sample Application



1. C1: Use a 0.01 µF laminated ceramic capacitor.
2. Set up the polarity of the image signal from the sensor so that white data is represented by the highest potential and black data by the lowest potential. A level conversion circuit can allow the whole dynamic range of the built-in A/D converter to be used effectively if the maximum output level of the peaks in the image signal from the sensor does not reach 4.2 V.
3. Although AGND and DGND are completely isolated internally in this LSI, AV_{DD} and DV_{DD} are connected through the substrate. Therefore, the power supply system must be designed so that no potential difference between AV_{DD} and DV_{DD} can occur. Also, when power is applied or removed, the time lag between the power supplies must be under 3 ms.