

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90520 Series

MB90522/523/F523/V520

■ DESCRIPTION

The MB90520 series is a general-purpose 16-bit microcontroller developed and designed by Fujitsu for process control applications in consumer products that require high-speed real-time processing.

The instruction set of the F²MC-16LX CPU core inherits AT architecture of the F²MC* family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data.

The MB90520 series has peripheral resources of 8/10-bit A/D converter, 8-bit D/A converter, UART (SCI), extended I/O serial interfaces 0 and 1, 8/16-bit up/down counter/timers 0 and 1, 8/16-bit PPG timers 0 and 1, I/O timer (16-bit free-run timers 1 and 2, input captures 0 and 1 (ICU), output compares 0 and 1 (OCU)), and an LCD controller/driver.

*:F²MC stands for FUJITSU Flexible Microcontroller, a registered trademark of FUJITSU LIMITED.

■ FEATURES

- Clock

Embedded PLL clock multiplication circuit

Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz, 4 MHz to 16 MHz).

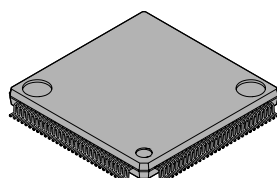
The system can be operated by a sub-clock (rated at 32.768 kHz).

Minimum instruction execution time: 62.5 ns (at oscillation of 4 MHz, four times the oscillation clock, operation at V_{CC} of 5.0 V)

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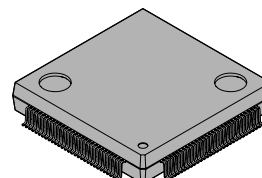
■ PACKAGES

120-pin Plastic LQFP



(FPT-120P-M05)

120-pin Plastic QFP



(FPT-120P-M13)

MB90520 Series

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- Maximum memory space
16 Mbytes
- Instruction set optimized for controller applications
Rich data types (bit, byte, word, long word)
Rich addressing mode (23 types)
Enhanced signed multiplication/division instruction and RETI instruction functions
Enhanced precision calculation realized by 32-bit accumulator
- Instruction set designed for high level language (C) and multi-task operations
Adoption of system stack pointer
Enhanced pointer indirect instructions
Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed
4-byte instruction queue
- Enhanced interrupt function
8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
Extended intelligent I/O service function (EI²OS): Up to 16 channels
- Embedded ROM size and types
Mask ROM: 64 kbytes/128 kbytes
Flash ROM: 128 kbytes
- Embedded RAM size
Mask ROM: 4 kbytes
Flash ROM: 4 kbytes
Evaluation product: 6 kbytes
- Low-power consumption (stand-by) mode
Sleep mode (mode in which CPU operating clock is stopped)
Stop mode (mode in which oscillation is stopped)
CPU intermittent operation mode
Hardware stand-by mode
Clock mode (mode in which other than sub-clock and timebase timer are stopped)
- Process
CMOS technology
- I/O port
General-purpose I/O ports (CMOS): 53 ports
General-purpose I/O ports (via pull-up resistors): 24 ports
General-purpose I/O ports (open-drain): 8 ports
Total: 85 ports
- Timer
Timebase timer/watchdog timer: 1 channel
8/16-bit PPG timers 0, 1: 8-bit × 2 channels or 16-bit × 1 channel
- 16-bit re-load timers 0, 1: 2 channels

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- 16-bit I/O timer
 - 16-bit free-run timers 1, 2: 2 channels
 - Input captures 0, 1 (ICU): Generates an interrupt request by latching a 16-bit free-run timer counter value upon detection of an edge input to the pin.
 - Output compares 0, 1 (OCU): Generates an interrupt request and reverses the output level upon detection of a match between the 16-bit free-run timer counter value and the compare setting value.
 - 8/16-bit up/down counter/timers 0, 1: 1 channel (8-bit × 2 channels)
- Extended I/O serial interfaces 0, 1: 1 channel
- UART (SCI)
 - With full-duplex double buffer
 - Clock asynchronous or clock synchronized transmission can be selectively used.
- DTP/external interrupt circuit (8 channels)
 - A module for starting extended intelligent I/O service (EI²OS) and generating an external interrupt triggered by an external input.
- Wake-up interrupt
 - Receives external interrupt requests and generates an interrupt request upon an “L” level input.
- Delayed interrupt generation module
 - Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
 - 8/10-bit resolution can be selectively used.
 - Starting by an external trigger input.
 - Conversion time: minimum 15.0 μs (at machine clock frequency of 16 MHz, including sampling time)
- 8-bit D/A converter (based on the R-2R system)
 - 8-bit resolution: 2 channels (independent)
 - Setup time: 12.5 μs
- Clock timer: 1 channel
- LCD controller/driver
 - A common driver and a segment driver that can directly drive the LCD (liquid crystal display) panel
- Clock output function

Note: Do not set external bus mode for the MB90520 series because it cannot be operated in this mode.

MB90520 Series

■ PRODUCT LINEUP

Part number		MB90522	MB90523	MB90F523	MB90V520
Item					
Classification		Mask ROM product		Flash ROM product	Evaluation product
ROM size		64 kbytes	128 kbytes		None
RAM size		4 kbytes			6 kbytes
CPU functions		Number of instructions: 351 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits			
		Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz)			
		Interrupt processing time: 1.5 μ s (at machine clock frequency of 16 MHz, minimum value)			
Ports		General-purpose I/O ports (CMOS output): 53 General-purpose I/O ports (via pull-up resistor): 24 General-purpose I/O ports (N-ch open-drain output): 8 Total: 85			
UART (SCI)		Clock synchronized transmission (62.5 kbps to 1 Mbps) Clock asynchronous transmission (1202 bps to 9615 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.			
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel only once) Scan conversion mode (converts two or more successive channels and can program up to 8 channels.) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)			
8/16-bit PPG timers 0, 1		Number of channels: 1 (8-bit \times 2 channels) PPG operation of 8-bit or 16-bit Pulse wave of given intervals and given duty ratios can be output. Pulse interval: 62.5 ns to 1 μ s (at machine clock frequency of 16 MHz)			
8/16-bit up/down counter/timers 0, 1		Number of channels: 1 (8-bit \times 2 channels) Event input: 6 channels 8-bit up/down counter/timer used: 2 channels 8-bit re-load/compare function supported: 1 channel			
16-bit I/O timer	16-bit free-run timers 1, 2	Number of channels: 2 Overflow interrupts			

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MB90520 Series

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Part number		MB90523	MB90523	MB90F523	MB90V520
Item					
16-bit I/O timer	Output compares 0, 1 (OCU)	Number of channels: 8 Pin input factor: Match signal of compare register			
	Input captures 0, 1 (ICU)	Number of channels: 2 Rewriting register value upon pin input (rising, falling, or both edges)			
DTP/external interrupt circuit		Number of inputs: 8 Started by rising edge, falling edge, "H" level input, or "L" level input. External interrupt circuit or extended intelligent I/O service (EI ² OS) can be used.			
Wake-up interrupt		Number of inputs: 8 Started by "L" level input.			
Delayed interrupt generation module		Interrupt generation module for switching tasks Used in real-time operating systems.			
Extended I/O serial interfaces 0, 1		Clock synchronized transmission (3125 bps to 1 Mbps) LSB first/MSB first			
Timebase timer		18-bit counter Interrupt interval: 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms (at oscillation of 4 MHz)			
8-bit D/A converter		8-bit resolution Number of channels: 2 channels Based on R-2R system			
LCD controller/driver		Number of common output pins: 4 Number of segment output pins: 32 Number of power supply pins for LCD drive: 4 RAM for LCD indication: 16 bytes Booster for LCD drive: Internal Split resistor for LCD drive: Internal			
Watchdog timer		Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)			
Low-power consumption (stand-by) mode		Sleep/stop/CPU intermittent operation/clock timer/hardware stand-by			
Process		CMOS			
Power supply voltage for operation*		3.0 V to 5.5 V		4.0 V to 5.5 V	3.0 V to 5.5 V

* : Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")
Assurance for the MB90V520 is given only for operation with a tool at a power voltage of 3.0 V to 5.5 V, an operating temperature of 0 to 55 degrees centigrade, and an operating frequency of 1 MHz to 16 MHz.

MB90520 Series

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90522	MB90523	MB90F523
FPT-120P-M05	○	○	○
FPT-120P-M13	○	○	○

○ : Available × : Not available

Note: For more information about each package, see section “■ Package Dimensions.”

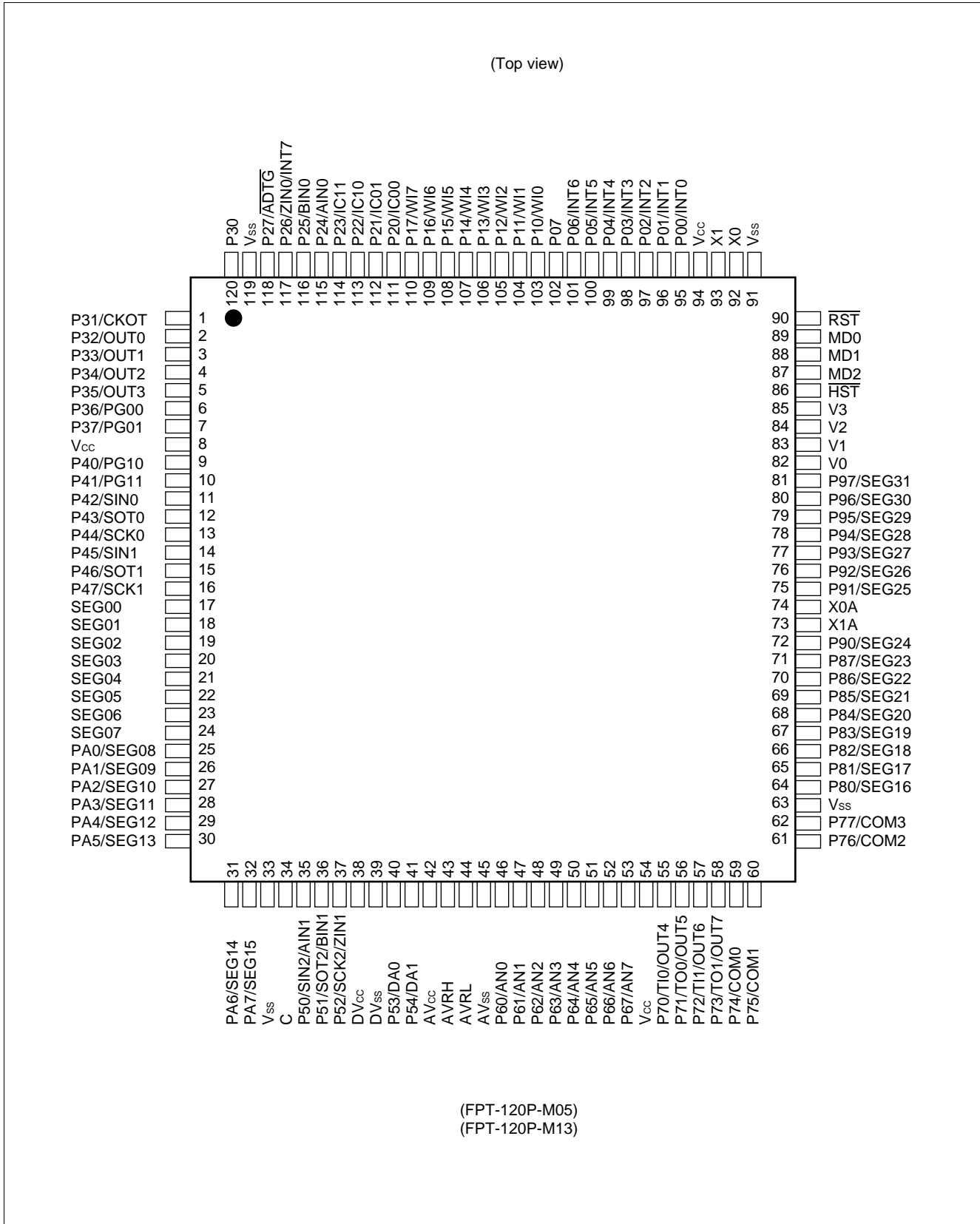
■ DIFFERENCES AMONG PRODUCTS

Memory Size

In evaluation with an evaluation chip, note the difference between the evaluation chip and the chip actually used. The following items must be taken into consideration.

- The MB90V520 does not have an internal ROM. However, operations equivalent to those performed by a chip with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by setting the development tool.
- In the MB90V520, images from FF4000_H to FFFFFFF_H are mapped to bank 00, and FE0000_H to FF3FFF_H are mapped to bank FE and FF only. (This setting can be changed by configuring the development tool.)
- In the MB90522, images from FF4000_H to FFFFFFF_H are mapped to bank 00, and FF0000_H to FF3FFF_H to bank FF only.
- In the MB90523/F523, images from FF4000_H to FFFFFFF_H are mapped to bank 00, and FE0000_H to FF3FFF_H to bank FE and bank FF.

■ PIN ASSIGNMENT



MB90520 Series

■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Function
LQFP-120*1 QFP-120*2			
92, 93	X0, X1	A	This is a high-speed crystal oscillator pin.
74, 73	X0A, X1A	B	This is a low-speed crystal oscillator pin.
89 to 87	MD0 to MD2	C	This is an input pin for selecting operation modes. Connect directly to V _{CC} or V _{SS} .
90	$\overline{\text{RST}}$	C	This is an external reset request signal input pin.
86	$\overline{\text{HST}}$	C	This is a hardware stand-by input pin.
95 to 101	P00 to P06	D	This is a general-purpose I/O port. This function can be set by the port 0 input pull-up resistor setup register (RDR0) for input. For output, however, this function is invalid.
	INT0 to INT6		This is a request input pin of the DTP/external interrupt circuit ch.0 to ch.6.
102	P07	D	This is a general-purpose I/O port. This function can be set by the port 0 input pull-up resistor setup register (RDR0) for input. For output, however, this function is invalid.
103 to 110	P10 to 17	D	This is a general-purpose I/O port. This function can be set by the port 1 input pull-up resistor setup register (RDR1) for input. For output, however, this function is invalid.
	WI0 to WI7		This is an I/O pin for wake-up interrupts.
111, 112, 113, 114	P20, P21, P22, P23	E	This is a general-purpose I/O port.
	IC00, IC01, IC10, IC11		This is a trigger input pin for input capture (ICU) 0 and 1. Since this input is used as required for input capture 0 and 1 (ICU) ch.0, ch.01, ch.10 and ch.11 input operation, output by other functions must be suspended except for intentional operation.
115	P24	E	This is a general-purpose I/O port.
	AIN0		This port can be used as count clock A input for 8/16-bit up/down counter/timer 0.
116	P25	E	This is a general-purpose I/O port.
	BIN0		This port can be used as count clock B input for 8/16-bit up/down counter/timer 0.

*1: FPT-120P-M05

*2: FPT-120P-M13

(Continued)

MB90520 Series

Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
117	P26	E	This is a general-purpose I/O port.
	ZIN0		This port can be used as count clock Z input for 8/16-bit up/down counter/timer 0.
	INT7		This is a request input pin of the DTP/external interrupt circuit ch.7.
118	P27	E	This is a general-purpose I/O port.
	$\overline{\text{ADTG}}$		This is an external trigger input pin of the 8/10-bit A/D converter. Since this input is used as required for 8/10-bit A/D converter input operation, output by other functions must be suspended except for intentional operation.
120	P30	E	This is a general-purpose I/O port.
1	P31	E	This is a general-purpose I/O port.
	CKOT		This is a clock monitor function output pin. This function is valid when clock monitor output is enabled.
2	P32	E	This is a general-purpose I/O port. This function becomes valid when waveform output from the OUT0 is disabled.
	OUT0		This is an event output pin for output compare 0 (OCU) ch.0. This function is valid when output for each channel is enabled.
3	P33	E	This is a general-purpose I/O port. This function becomes valid when waveform output from the OUT1 is disabled.
	OUT1		This is an event output pin for output compare 0 (OCU) ch.1. This function is valid when output for each channel is enabled.
4	P34	E	This is a general-purpose I/O port. This function becomes valid when waveform output from the OUT2 is disabled.
	OUT2		This is an event output pin for output compare 0 (OCU) ch.2. This function is valid when output for each channel is enabled.
5	P35	E	This is a general-purpose I/O port. This function becomes valid when waveform output from the OUT3 is disabled.
	OUT3		This is an event output pin for output compare 0 (OCU) ch.3. This function is valid when output for each channel is enabled.
6	P36	E	This is a general-purpose I/O port. This function becomes valid when waveform output from the PG00 is disabled.
	PG00		This is an output pin of 8/16-bit PPG timer 0. This function becomes valid when waveform output from PG00 is enabled.

*1: FPT-120P-M05

*2: FPT-120P-M13

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MB90520 Series

Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
7	P37	E	This is a general-purpose I/O port. This function becomes valid when waveform output from the PG01 is disabled.
	PG01		This is an output pin of 8/16-bit PPG timer 0. This function becomes valid when waveform output from PG01 is enabled.
9, 10	P40, P41	D	This is a general-purpose I/O port. This function becomes valid when waveform output from the PG10 and PG11 are disabled. This function can be set by the pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	PG10, PG11		This is an output pin of 8/16-bit PPG timer 1. This function becomes valid when waveform outputs from PG10 and PG11 are enabled.
11	P42	D	This is a general-purpose I/O port. This function can be set by the pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SIN0		This is a serial data input pin of UART (SCI). Because this input is used as required when UART (SCI) is performing input operations, it is necessary to stop outputs by other functions unless such outputs are made intentionally. When using other output functions as well, disable output during SIN operation.
12	P43	D	This is a general-purpose I/O port. This function can be set by the pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SOT0		This is a serial data output pin of UART (SCI). This function becomes valid when serial data output from UART (SCI) is enabled.
13	P44	D	This is a general-purpose I/O port. This function can be set by the pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SCK0		This is a serial clock I/O pin of UART (SCI). This function becomes valid when serial clock output from UART (SCI) is enabled.
14	P45	D	This is a general-purpose I/O port. This function can be set by the port 4 input pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SIN1		This is a data input pin for extended I/O serial interface 0. Since this input is used as required for serial data input operation, output by other functions must be suspended except for intentional operation. When using other output functions as well, disable output during SIN operation.

*1: FPT-120P-M05

*2: FPT-120P-M13

(Continued)

MB90520 Series

Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
15	P46	D	This is a general-purpose I/O port. This function can be set by the port 4 input pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SOT1		This is a data output pin for extended I/O serial interface 0. This function becomes valid when serial data output from SOT1 is enabled.
16	P47	D	This is a general-purpose I/O port. This function can be set by the port 4 input pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SCK1		This is a serial clock I/O pin for extended I/O serial interface 0. This function becomes valid when serial clock output from SCK1 is enabled.
35	P50	D	This is a general-purpose I/O port.
	SIN2		This is a data input pin for extended I/O serial interface 1. Since this input is used as required for serial data input operation, output by other functions must be suspended except for intentional operation.
	AIN1		This port can be used as count clock A input for 8/16-bit up/down counter/timer 1.
36	P51	D	This is a general-purpose I/O port.
	SOT2		This is a data output pin for extended I/O serial interface 1. This function becomes valid when serial data output from SOT2 is enabled.
	BIN1		This port can be used as count clock B input for 8/16-bit up/down counter/timer 1.
37	P52	D	This is a general-purpose I/O port.
	SCK2		This is a serial clock I/O pin for extended I/O serial interface 1. This function becomes valid when serial clock output from serial SCK2 is enabled.
	ZIN1		This port can be used as control clock Z input for 8/16-bit up/down counter/timer 1.
40, 41	P53, P54	I	This is a general-purpose I/O port.
	DA0, DA1		These are analog signal output pins for 8-bit D/A converter ch.0 and ch.1.
46 to 53	P60 to P67	K	This is a general-purpose I/O port. The input function become valid when the analog input enable register (ADER) is set to select a port.
	AN0 to AN7		These are analog input pins of the 8/10-bit A/D converter. This function is valid when the analog input enable register (ADER) is enabled.

*1: FPT-120P-M05

*2: FPT-120P-M13

(Continued)

MB90520 Series

Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
55, 57	P70, P72	E	This is a general-purpose I/O port.
	T10, T11		These are event input pins for 16-bit re-load timers 0 and 1. Since this input is used as required for 16-bit re-load timers 0 and 1 operation, output by other functions must be suspended except for intentional operation.
	OUT4, OUT6		These are event output pins for output compare 1 (OCU) ch.4 and ch.6. This function is valid when output for each channel is enabled.
56, 58	P71, P73	E	This is a general-purpose I/O port. This function is valid when TO0 and TO1 output are disabled.
	TO0, TO1		These are output pins for 16-bit re-load timers 0 and 1. This function is valid when TO0 and TO1 output are enabled.
	OUT5, OUT7		These are event output pins for output compare 1 (OCU) ch.5 and ch.7. This function is valid when output for each channel is enabled.
59 to 62	P74 to P77	L	This is a general-purpose I/O port. This function is valid with port output specified for the LCD controller/driver control register.
	COM0 to COM3		These are common pins for the LCD controller/driver. This function is valid with common output specified for the LCD controller/driver control register.
64 to 71	P80 to P87	L	This is a general-purpose I/O port. This function is valid with port output specified for the LCD controller/driver control register.
	SEG16 to SEG23		These are segment outputs for the LCD controller/driver. This function is valid with segment output specified for the LCD controller/driver control register.
72, 75 to 81	P90, P91 to P97	M	This is a general-purpose I/O port. The maximum I _{OL} can be 10mA. This function is valid with port output specified for the LCD controller/driver control register.
	SEG24, SEG25 to SEG31		These are segment outputs for the LCD controller/driver. This function is valid with port output specified for the LCD controller/driver control register.
17 to 24	SEG00 to SEG07	F	These are pins dedicated to LCD segments 00 to 07 for the LCD controller/driver.
25 to 32	PA0 to PA7	L	This is a general-purpose I/O port. This function is valid with port output specified for the LCD controller/driver control register.
	SEG08 to SEG15		These are pins for LCD segments 08 to 15 for the LCD controller/driver. Units of four ports or segments can be selected by the internal register in the LCD controller.

*1: FPT-120P-M05

*2: FPT-120P-M13

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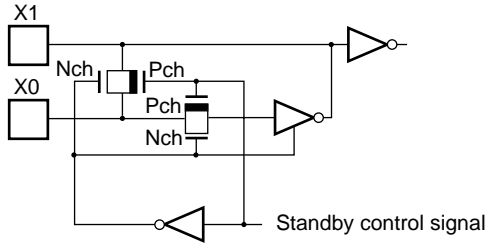
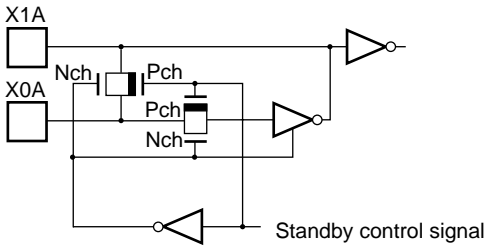
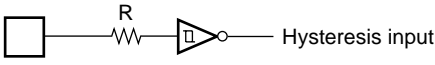
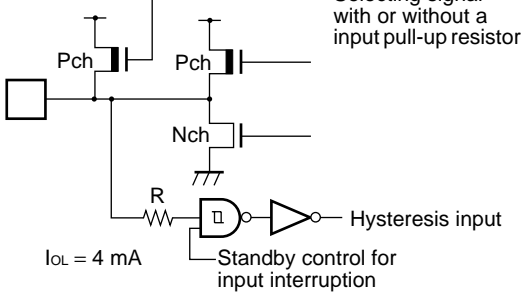
Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
34	C	G	This is a capacitance pin for power supply stabilization. Connect an external ceramic capacitor rated at about 0.1 μ F. This capacitor is not, however, required for the M90F523 (flash product).
82 to 85	V0 to V3	N	This is a pin for the reference power supply for the LCD controller/driver.
8, 54, 94	V _{cc}	Power supply	This is a power supply (5.0 V) input pin to the digital circuit.
33, 63, 91, 119	V _{ss}	Power supply	This provides the GND level (0.0 V) input pin for the digital circuit.
42	AV _{cc}	H	This is a power supply for the analog circuit. Make sure to turn on/turn off this power supply with a voltage exceeding AV _{cc} applied to V _{cc} .
43	AVRH	J	This is a reference voltage input to the analog circuit. Make sure to turn on/turn off this power supply with a voltage exceeding AVRH applied to AV _{cc} .
44	AVRL	H	This is a reference voltage input to the analog circuit.
45	AV _{ss}	H	This is a GND level of the analog circuit.
38	DV _{cc}	H	This is the Vref input pin for the D/A converter. The voltage to be applied must not exceed V _{cc} .
39	DV _{ss}	H	This is the GND level pin for the D/A converter. The potential must be the same as V _{ss} .

*1: FPT-120P-M05

*2: FPT-120P-M13

MB90520 Series

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> High-speed oscillation feedback resistor approx. $1M\Omega$
B		<ul style="list-style-type: none"> Low-speed oscillation feedback resistor approx. $1M\Omega$
C		<ul style="list-style-type: none"> Hysteresis input
D		<ul style="list-style-type: none"> Hysteresis input (can be set with the input pull-up resistor) CMOS level output Pull-up resistor approx. $50\text{ k}\Omega$ Provided with a standby control function for input interruption

(Continued)

Type	Circuit	Remarks
E	<p> $I_{OL} = 4 \text{ mA}$ Hysteresis input Standby control for input interruption </p>	<ul style="list-style-type: none"> • CMOS hysteresis input/output • CMOS level output • Provided with a standby control function for input interruption
F		<ul style="list-style-type: none"> • Pins dedicated to segment output
G		<ul style="list-style-type: none"> • C pin output (Pin for capacitor connection) N.C. pin for the MB90F523
H		<ul style="list-style-type: none"> • Analog power input protector
I	<p> $I_{OL} = 4 \text{ mA}$ Hysteresis input Standby control for input interruption DAO </p>	<ul style="list-style-type: none"> • CMOS hysteresis input/output • Pin for analog output/CMOS output (During analog output, CMOS output is not produced.) (Analog output has priority over CMOS output: DAE = 1) • Provided with a standby control function for input interruption

(Continued)

MB90520 Series

Type	Circuit	Remarks
J		<ul style="list-style-type: none"> • Input pin for ref+ power for the A/D converter • Provided with power protection
K		<ul style="list-style-type: none"> • Hysteresis input/analog input • CMOS output • Provided with a standby control for input interruption
L		<ul style="list-style-type: none"> • CMOS hysteresis input/output • Segment input • Standby control to cut off the input is available in segment input operation
M		<ul style="list-style-type: none"> • Hysteresis input • Nch open-drain output (High current for LCD drive) • Standby control to cut off the input is available in segment input operation
N		<ul style="list-style-type: none"> • Reference power supply pin for the LCD controller

■ HANDLING DEVICES

1. Ensuring that the Voltage does not exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when a voltage exceeding V_{CC} or below V_{SS} is applied to input or output pins or if a voltage exceeding the rating is applied across V_{CC} and V_{SS} .

When a latch-up is caused, the power supply current may be dramatically increased, resulting in thermal breakdown of devices. To avoid the latch-up, make sure that the voltage does not exceed the maximum rating. In turning on/turning off the analog power supply, make sure the analog power voltages (AV_{CC} , AV_{RH} , DV_{CC}) and analog input voltages do not exceed the digital voltage (V_{CC}).

And also make sure the voltages applied to the LCD power supply pins (V_3 to V_0) do not exceed the power supply voltage (V_{CC}).

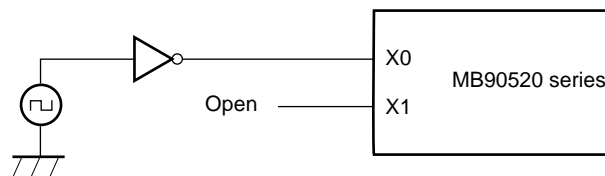
2. Handling Unused Pins

- Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled-up or pull-down through at least 2 k Ω resistance.
- Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

3. Notes on Using External Clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

• Using external clock



4. Unused Sub Clock Mode

If sub clock modes are not used, the oscillator should be connected to the X0A pin and X1A pin.

5. Power Supply Pins

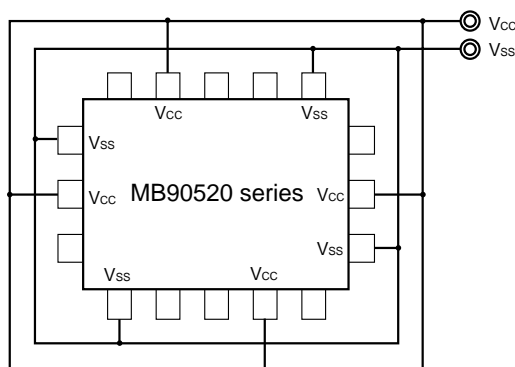
In products with multiple V_{CC} or V_{SS} pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-ups. However, the pins should be connected to external powers and ground lines to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.

It is recommended that a bypass capacitor of around 0.1 μF be placed between the V_{CC} and V_{SS} pins near the device.

MB90520 Series

• Using power supply pins



6. Crystal Oscillator Circuit

Noise around the X0 and X1 pins may cause abnormal operation in this device. In designing printed circuit boards, the X0 and X1 pins and crystal oscillator (or ceramic oscillator), as well as the bypass capacitor to the ground, should be placed as close as possible, and the related wiring should have as few crossings with other wiring as possible.

Circuit board artwork in which the area of the X0 and X1 pins is surrounded by grounding is recommended for stabilizing the operation.

7. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply, D/A converter power supply (AV_{CC} , AV_{RH} , AV_{RL} , DV_{CC} , DV_{SS}) and analog inputs (AN0 to AN7) after turning on the digital power supply (V_{CC}).

Turn off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that AV_{RH} and DV_{CC} do not exceed AV_{CC} (turning on/off the analog and digital supplies simultaneously is acceptable).

8. Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter and those of D/A converter to $AV_{CC} = DV_{CC} = V_{CC}$, $AV_{SS} = AV_{RH} = AV_{RL} = V_{SS}$.

9. N.C. Pin

The N.C. (internally connected) pin must be opened for use.

10. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μ s or more (0.2 V to 2.7 V).

11. Use of SEG/COM Pins for the LCD Controller/Driver as Ports

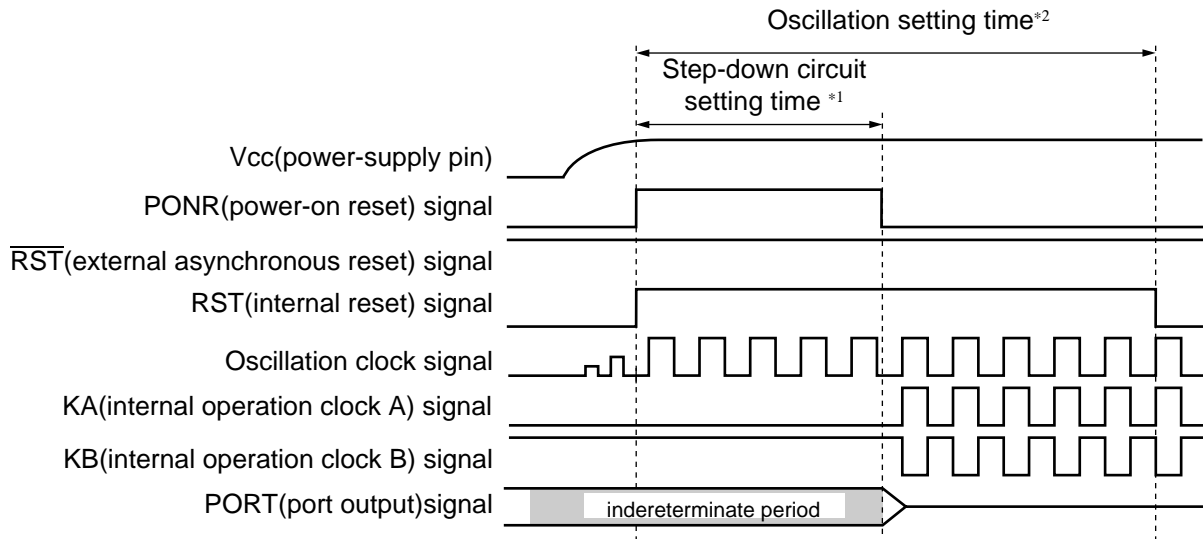
In MB90520 series, pins SEG08 to SEG31, and COM0 to COM3 can also be used as general-purpose ports. The electrical standard is such that pins SEG08 to SEG23, and COM0 to COM3 have the same ratings as the CMOS output port, while pins SEG24 to SEG31 have the same ratings as the open-drain type.

12. Indeterminate outputs from ports 0 and 1

The outputs from ports 0 and 1 become indeterminate during oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on.

Pay attention to the port output timing shown as follow

• Timing chart of indeterminate outputs from ports 0 and 1



* : 1: Step-down circuit setting time : $2^{17}/\text{oscillation clock frequency}$ (oscillation clock frequency of 16 MHz: 8.19 ms)

* : 2: Oscillation setting time: $2^{18}/\text{oscillation clock frequency}$ (oscillation clock frequency of 16 MHz: 16.38 ms)

13. Initialization

The device contains internal registers that can be initialized only by a power-on reset. To initialize the internal registers, restart the power supply.

14. Interrupt Recovery from Standby

If an external interrupt is used for recovery from standby, use an "H" level input request. An "L" level request causes abnormal operation.

15. Precautions for Use of "DIV A, Ri", and "DIVW A, Ri" Instructions

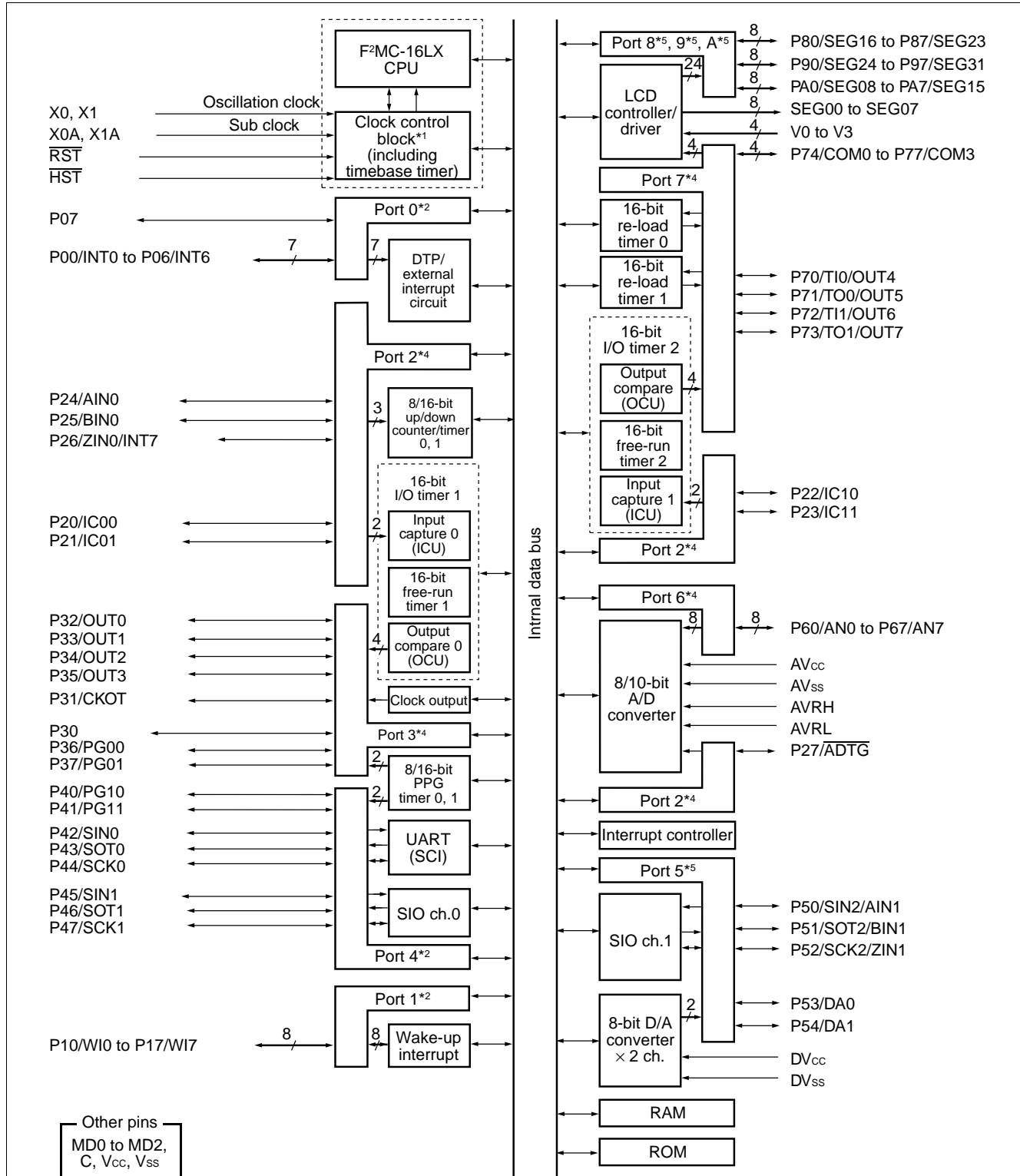
The signed multiplication-division instructions "DIV A, Ri", and "DIVW A, RWi" should be used when the corresponding bank registers (DTB, ADB, USB, SSB) are set to value "00h". If the corresponding bank registers (DTB, ADB, USB, SSB) are set to a value other than "00h," then the remainder obtained after the execution of the instruction will not be placed in the instruction operand register.

16. Precautions for Use of REALOS

Extended intelligent I/O service(EI²OS) cannot be used, when REALOS is used.

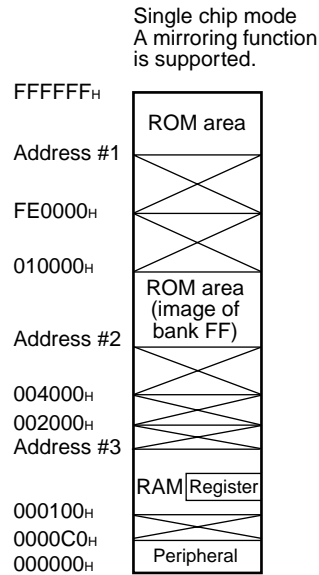
MB90520 Series

■ BLOCK DIAGRAM





Notes: Actually 16-bit free-run timer 1 is supported although two free-run timers are seemingly supported.
 *1: The clock control circuit comprises a watchdog timer, a timebase timer, and a power consumption controller.
 *2: A register for setting a pull-up resistor is supported.
 *3: This is a high-current port for an LCD drive.
 *4: A register for setting a pull-up resistor is supported. Signals in the CMOS level are input and output.
 *5: Also used for LCD output. With this port used as is, Nch open-drain output develops. A register for setting a pull-up resistor is supported.

■ MEMORY MAP



Part number	Address #1*	Address #2*	Address #3*
MB90522	FF0000H	004000H	001100H
MB90523	FE0000H	004000H	001100H
MB90F523	FE0000H	004000H	001100H

 : Internal access memory
 : Access prohibited

*: Addresses #1, #2 and #3 vary with product type.

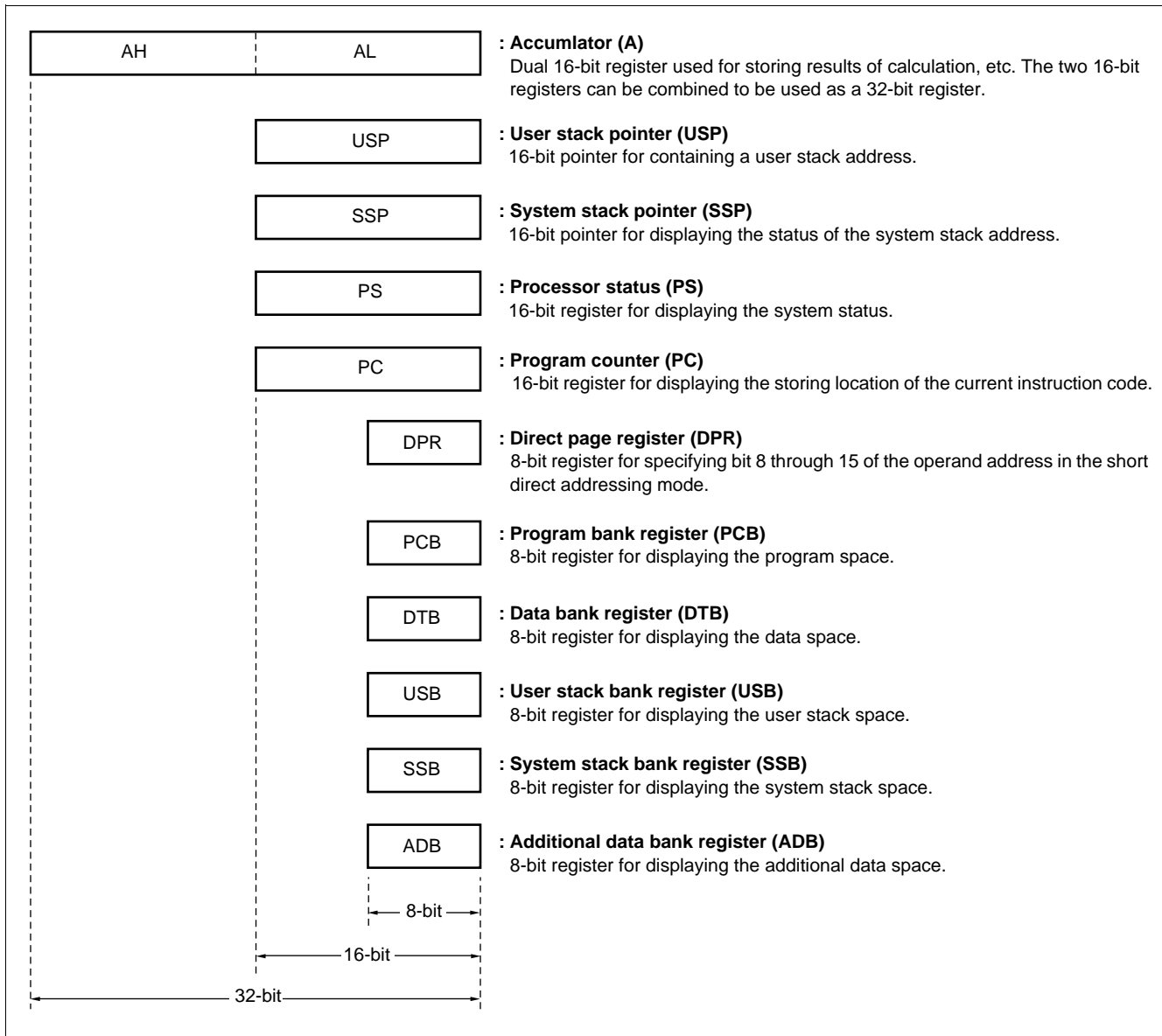
Note: The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating "far."

For example, if an attempt has been made to access 00C000H, the contents of the ROM at FFC000H are actually accessed. Since the ROM area of the FF bank exceeds 48k bytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFFH looks, therefore, as if it were the image for 00400H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFFH.

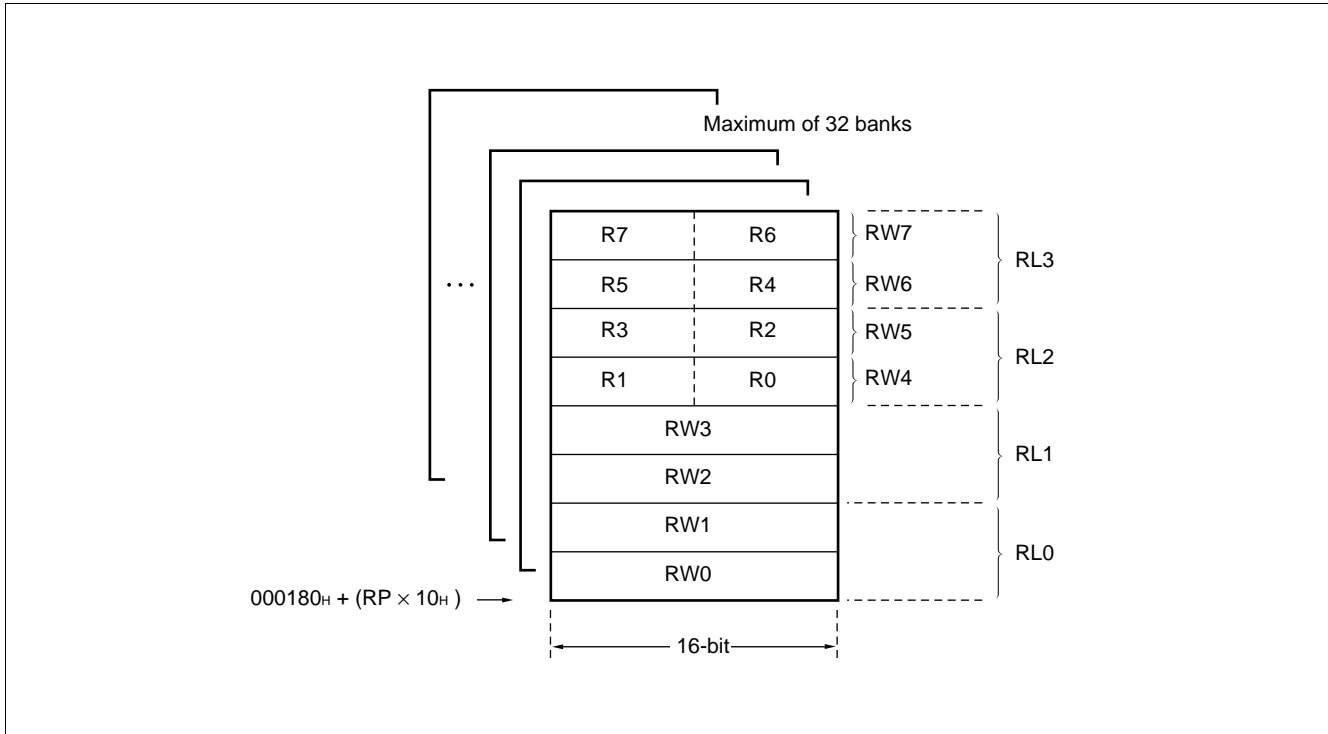
MB90520 Series

■ F²MC-16LX CPU PROGRAMMING MODEL

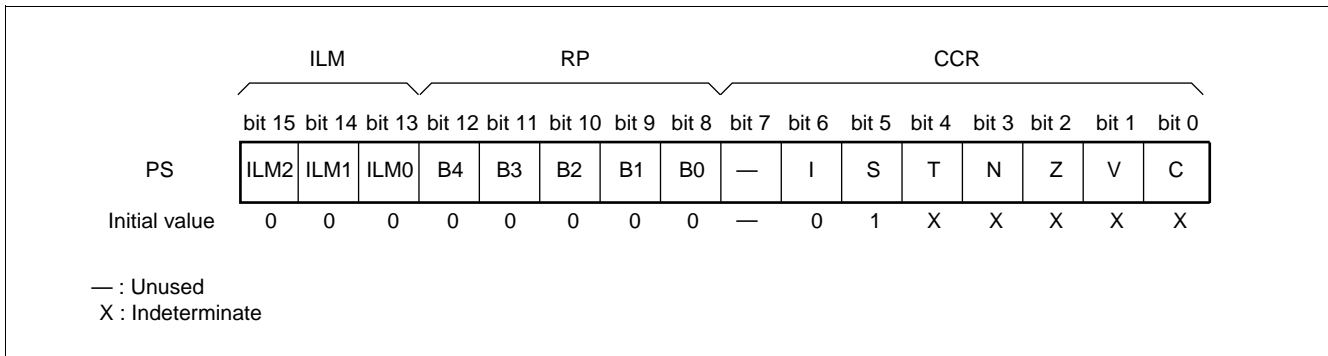
• Dedicated registers



- General-purpose registers



- Processor status (PS)



MB90520 Series

■ I/O MAP

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000000 _H	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXX _B
000001 _H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXX _B
000002 _H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXX _B
000003 _H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXX _B
000004 _H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXX _B
000005 _H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXX _B
000006 _H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXX _B
000007 _H	PDR7	Port 7 data register	R/W	Port 7	XXXXXXXX _B
000008 _H	PDR8	Port 8 data register	R/W	Port 8	XXXXXXXX _B
000009 _H	PDR9	Port 9 data register	R/W	Port 9	XXXXXXXX _B
00000A _H	PDRA	Port A data register	R/W	Port A	XXXXXXXX _B
00000B _H	LCDCMR	Port 7/COM pin selection register	R/W	Port 7, LCD controller/driver	XXXX0000 _B
00000C _H	OCP4	OCU compare register ch.4	R/W	16-bit I/O timer (output compare 1 (OCU) section)	XXXXXXXX _B
00000D _H					XXXXXXXX _B
00000E _H	(Disabled)				
00000F _H	EIFR	Wake-up interrupt flag register	R/W	Wake-up interrupt	XXXXXXXX0 _B
000010 _H	DDR0	Port 0 direction register	R/W	Port 0	00000000 _B
000011 _H	DDR1	Port 1 direction register	R/W	Port 1	00000000 _B
000012 _H	DDR2	Port 2 direction register	R/W	Port 2	00000000 _B
000013 _H	DDR3	Port 3 direction register	R/W	Port 3	00000000 _B
000014 _H	DDR4	Port 4 direction register	R/W	Port 4	00000000 _B
000015 _H	DDR5	Port 5 direction register	R/W	Port 5	XXX00000 _B
000016 _H	DDR6	Port 6 direction register	R/W	Port 6	00000000 _B
000017 _H	DDR7	Port 7 direction register	R/W	Port 7	00000000 _B
000018 _H	DDR8	Port 8 direction register	R/W	Port 8	00000000 _B
000019 _H	DDR9	Port 9 direction register	R/W	Port 9	00000000 _B
00001A _H	DDRA	Port A direction register	R/W	Port A	00000000 _B
00001B _H	ADER	Analog input enable register	R/W	Port 6, A/Dconverter	11111111 _B
00001C _H	OCP5	OCU compare register ch.5	R/W	16-bit I/O timer (output compare 1 (OCU) section)	XXXXXXXX _B
00001D _H					XXXXXXXX _B
00001E _H	(Disabled)				
00001F _H	EICR	Wake-up interrupt enable register	W	Wake-up interrupt	00000000 _B

(Continued)

MB90520 Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value	
000020H	SMR	Serial mode register	R/W	UART (SCI)	0 0 0 0 0 0 0 0 _B	
000021H	SCR	Serial control register	R/W or W		0 0 0 0 0 1 0 0 _B	
000022H	SIDR/SODR	Serial input data register/serial output data register	R/W		X X X X X X X X _B	
000023H	SSR	Serial status register	R/W or R		0 0 0 0 1 X 0 0 _B	
000024H	SMCSL0	Serial mode control lower status register 0	R/W	Extended I/O serial interface 0	X X X X 0 0 0 0 _B	
000025H	SMCSH0	Serial mode control upper status register 0	R/W		0 0 0 0 0 0 1 0 _B	
000026H	SDR0	Serial data register 0	R/W		X X X X X X X X _B	
000027H	CDCR	Communications prescaler control register	R/W	Communications prescaler control register	0 X X X 1 1 1 1 _B	
000028H	SMCSL1	Serial mode control lower status register 1	R/W	Extended I/O serial interface 1	X X X X 0 0 0 0 _B	
000029H	SMCSH1	Serial mode control upper status register 1	R/W		0 0 0 0 0 0 1 0 _B	
00002AH	SDR1	Serial data register 1	R/W		X X X X X X X X _B	
00002BH	(Disabled)					
00002CH	OCS45	OCU control status register ch.45	R/W	16-bit I/O timer (output compare 1 (OCU) section)	0 0 0 0 X X 0 0 _B	
00002DH					X X X 0 0 0 0 0 _B	
00002EH	OCS67	OCU control status register ch.67	R/W		0 0 0 0 X X 0 0 _B	
00002FH					X X X 0 0 0 0 0 _B	
000030H	ENIR	DTP/interrupt enable register	R/W		DTP/external interrupt circuit	0 0 0 0 0 0 0 0 _B
000031H	EIRR	DTP/interrupt factor register	R/W			X X X X X X X X _B
000032H	ELVR	Request level setting register	R/W	0 0 0 0 0 0 0 0 _B		
000033H				0 0 0 0 0 0 0 0 _B		
000034H	OCP6	OCU compare register ch.6	R/W	16-bit I/O timer (output compare 1 (OCU) section)	X X X X X X X X _B	
000035H					X X X X X X X X _B	
000036H	ADCS1	A/D control status register lower digits	R/W	8/10-bit A/D converter	0 0 0 0 0 0 0 0 _B	
000037H	ADCS2	A/D control status register upper digits	R/W		0 0 0 0 0 0 0 0 _B	
000038H	ADCR1	A/D data register lower digits	R		X X X X X X X X _B	
000039H	ADCR2	A/D data register upper digits	R or W		0 0 0 0 1 X X X _B	
00003AH	DADR0	D/A converter data register ch.0	R/W	8-bit D/A converter	X X X X X X X X _B	
00003BH	DADR1	D/A converter data register ch.1	R/W		X X X X X X X X _B	
00003CH	DACR0	D/A control register 0	R/W		X X X X X X X 0 _B	
00003DH	DACR1	D/A control register 1	R/W		X X X X X X X 0 _B	
00003EH	CLKR	Clock output enable register	R/W	Clock monitor function	X X X X 0 0 0 0 _B	

(Continued)

MB90520 Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
00003FH	(Disabled)				
000040H	PRLLO	PPG0 re-load register L	R/W	8/16-bit PPG timer 0, 1	XXXXXXXX _B
000041H	PRLHO	PPG0 re-load register H	R/W		XXXXXXXX _B
000042H	PRLLO	PPG1 re-load register L	R/W		XXXXXXXX _B
000043H	PRLHO	PPG1 re-load register H	R/W		XXXXXXXX _B
000044H	PPGC0	PPG0 operating mode control register	R/W		0X000XX1 _B
000045H	PPGC1	PPG1 operating mode control register	R/W		0X000001 _B
000046H	PPGOE0/ PPGOE1	PPG0 and 1 output control registers	R/W		00000000 _B
000047H	(Disabled)				
000048H	TMCSR0	Timer control status register lower ch.0	R/W	16-bit re-load timer 0	00000000 _B
000049H		Timer control status register upper ch.0			XXXXXXXX0000 _B
00004AH	TMR0/ TMRLR0	16-bit timer register upper, lower ch.0/ 16-bit re-load register upper, lower ch.0	R/W		XXXXXXXX _B
00004BH		XXXXXXXX _B			
00004CH	TMCSR1	Timer control status register lower ch.1	R/W	16-bit re-load timer 1	00000000 _B
00004DH		Timer control status register upper ch.1			XXXXXXXX0000 _B
00004EH	TMR1/ TMRLR1	16-bit timer register upper, lower ch.1/ 16-bit re-load register upper, lower ch.1	R/W		XXXXXXXX _B
00004FH		XXXXXXXX _B			
000050H	IPCP0	ICU data register ch.0	R	16-bit I/O timer (input compare 0, 1 (ICU) section)	XXXXXXXX _B
000051H					XXXXXXXX _B
000052H	IPCP1	ICU data register ch.1	R		XXXXXXXX _B
000053H					XXXXXXXX _B
000054H	ICS01	ICU control status register	R/W	00000000 _B	
000055H	(Disabled)				
000056H	TCDT1	Free-run timer data register 1	R/W	16-bit I/O timer (16-bit free-run timer 1 section)	00000000 _B
000057H					00000000 _B
000058H	TCCS1	Free-run timer control status register 1	R/W		00000000 _B
000059H	(Disabled)				
00005AH	OCP0	OCU compare register ch.0	R/W	16-bit I/O timer (output compare 0 (OCU) section)	XXXXXXXX _B
00005BH					XXXXXXXX _B
00005CH	OCP1	OCU compare register ch.1	R/W		XXXXXXXX _B
00005DH					XXXXXXXX _B
00005EH	OCP2	OCU compare register ch.2	R/W		XXXXXXXX _B
00005FH					XXXXXXXX _B
000060H	OCP3	OCU compare register ch.3	R/W		XXXXXXXX _B
000061H				XXXXXXXX _B	

(Continued)

MB90520 Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value	
000062 _H	OCS01	OCU control status register ch.01	R/W	16-bit I/O timer (output compare 0 (OCU) section)	0 0 0 0 X X 0 0 _B	
000063 _H					X X X 0 0 0 0 0 0 _B	
000064 _H	OCS23	OCU control status register ch.23	R/W		0 0 0 0 X X 0 0 _B	
000065 _H					X X X 0 0 0 0 0 0 _B	
000066 _H	TCDT2	Free-run timer data register 2	R/W		16-bit I/O timer (16-bit free-run timer 2 section)	0 0 0 0 0 0 0 0 _B
000067 _H						0 0 0 0 0 0 0 0 _B
000068 _H	TCCS2	Free-run timer control status register 2	R/W	0 0 0 0 0 0 0 0 _B		
000069 _H	(Disabled)					
00006A _H	LCR0	LCDC control registers 0 and 1	R/W	LCD controller/driver	0 0 0 1 0 0 0 0 _B	
00006B _H	LCR1		R/W		0 0 0 0 0 0 0 0 _B	
00006C _H	OCP7	OCU compare register ch.7	R/W	16-bit I/O timer (output compare 1 (OCU) section)	X X X X X X X X _B	
00006D _H					X X X X X X X X _B	
00006E _H	(Disabled)					
00006F _H	ROMM	ROM mirroring function selection register	W	ROM mirroring function selection module	X X X X X X X 1 _B	
000070 _H to 00007F _H	VRAM	RAM for LCD indication	R/W	LCD controller/driver	X X X X X X X X _B	
000080 _H	UDCR0	Up/down count register 0	R	8/16-bit up/down counter/timer 0, 1	0 0 0 0 0 0 0 0 _B	
000081 _H	UDCR1	Up/down count register 1	R		0 0 0 0 0 0 0 0 _B	
000082 _H	RCR0	Re-load compare register 0	W		0 0 0 0 0 0 0 0 _B	
000083 _H	RCR1	Re-load compare register 1	W		0 0 0 0 0 0 0 0 _B	
000084 _H	CSR0	Counter status register 0	R/W		0 0 0 0 0 0 0 0 _B	
000085 _H	(Reserved area)* ³					
000086 _H	CCRL0	Counter control register 0	R/W	8/16-bit up/down counter/timer 0, 1	X 0 0 0 0 0 0 0 _B	
000087 _H	CCRH0				0 0 0 0 0 0 0 0 _B	
000088 _H	CSR1	Counter status register 1	R/W		0 0 0 0 0 0 0 0 _B	
000089 _H	(Reserved area)* ³					
00008A _H	CCRL1	Counter control register 1	R/W	8/16-bit up/down counter/timer 0, 1	X 0 0 0 0 0 0 0 _B	
00008B _H	CCRH1				X 0 0 0 0 0 0 0 _B	
00008C _H	RDR0	Port 0 input pull-up resistor setup register	R/W	Port 0	0 0 0 0 0 0 0 0 _B	
00008D _H	RDR1	Port 1 input pull-up resistor setup register	R/W	Port 1	0 0 0 0 0 0 0 0 _B	
00008E _H	RDR4	Port 4 input pull-up resistor setup register	R/W	Port 4	0 0 0 0 0 0 0 0 _B	

(Continued)

MB90520 Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
00008F _H to 00009D _H	(Area used by the system)* ³				
00009E _H	PACSR	Program address detection control status register	R/W	Address match detection function	0 0 0 0 0 0 0 0 _B
00009F _H	DIRR	Delayed interrupt factor generation/cancellation register	R/W	Delayed interrupt generation module	X X X X X X X 0 _B
0000A0 _H	LPMCR	Low-power consumption mode control register	R/W or W	Low-power consumption (stand-by) mode	0 0 0 1 1 0 0 0 _B
0000A1 _H	CKSCR	Clock select register	R/W or R		1 1 1 1 1 1 0 0 _B
0000A2 _H to 0000A7 _H	(Disabled)				
0000A8 _H	WDTC	Watchdog timer control register	R or W	Watchdog timer	X X X X X X X X _B
0000A9 _H	TBTC	Timebase timer control register	R/W	Timebase timer	1 X X 0 0 0 0 0 _B
0000AA _H	WTC	Clock timer control register	R/W or R	Clock timer	1 X 0 0 1 0 0 0 _B
0000AB _H to 0000AD _H	(Disabled)				
0000AE _H	FMCS	Flash control register	R/W	Flash interface	1 X X 0 0 1 0 0 _B
0000AF _H	(Disabled)				
0000B0 _H	ICR00	Interrupt control register 00	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
0000B1 _H	ICR01	Interrupt control register 01	R/W		0 0 0 0 0 1 1 1 _B
0000B2 _H	ICR02	Interrupt control register 02	R/W		0 0 0 0 0 1 1 1 _B
0000B3 _H	ICR03	Interrupt control register 03	R/W		0 0 0 0 0 1 1 1 _B
0000B4 _H	ICR04	Interrupt control register 04	R/W		0 0 0 0 0 1 1 1 _B
0000B5 _H	ICR05	Interrupt control register 05	R/W		0 0 0 0 0 1 1 1 _B
0000B6 _H	ICR06	Interrupt control register 06	R/W		0 0 0 0 0 1 1 1 _B
0000B7 _H	ICR07	Interrupt control register 07	R/W		0 0 0 0 0 1 1 1 _B
0000B8 _H	ICR08	Interrupt control register 08	R/W		0 0 0 0 0 1 1 1 _B
0000B9 _H	ICR09	Interrupt control register 09	R/W		0 0 0 0 0 1 1 1 _B
0000BA _H	ICR10	Interrupt control register 10	R/W		0 0 0 0 0 1 1 1 _B
0000BB _H	ICR11	Interrupt control register 11	R/W		0 0 0 0 0 1 1 1 _B
0000BC _H	ICR12	Interrupt control register 12	R/W		0 0 0 0 0 1 1 1 _B
0000BD _H	ICR13	Interrupt control register 13	R/W		0 0 0 0 0 1 1 1 _B

(Continued)

(Continued)

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
0000BE _H	ICR14	Interrupt control register 14	R/W	Interrupt controller	0 0 0 0 1 1 1 1 _B
0000BF _H	ICR15	Interrupt control register 15	R/W		0 0 0 0 1 1 1 1 _B
0000C0 _H to 0000FF _H	(External area)* ¹				
000100 _H to 00#### _H	(RAM area)* ²				
00#### _H to 001FEF _H	(Reserved area)* ³				
001FF0 _H	PADR0	Program address detection register 0	R/W	Address match detection function	XXXXXXXX _B
001FF1 _H		Program address detection register 1	R/W		XXXXXXXX _B
001FF2 _H		Program address detection register 2	R/W		XXXXXXXX _B
001FF3 _H	PADR1	Program address detection register 3	R/W		XXXXXXXX _B
001FF4 _H		Program address detection register 4	R/W		XXXXXXXX _B
001FF5 _H		Program address detection register 5	R/W		XXXXXXXX _B
001FF6 _H to 001FFF _H	(Reserved area)* ³				

Descriptions for read/write

R/W: Readable and writable

R: Read only

W: Write only

Descriptions for initial value

0 : The initial value is "0."

1 : The initial value is "1."

X : The initial value is indeterminate.

*1: This area is the only external access area having an address of 0000FF_H or lower. An access operation to this area is handled as that to external I/O area.

*2: For details of the "RAM area", see the memory map.

*3: The "reserved area" is basically disabled because it is used in the system.

*4: "Area used by the system" is the area set by the resistor for evaluating tool.

Notes: • For bits initialized by reset operations, the initial value set by the reset operation is listed as an initial value. Note that the values are different from reading results.

For LPMCR/CKSCR/WDTIC, there are cases in which initialization is performed or not performed, depending on the types of the reset. The value listed is the initial value in cases where initialization is performed.

- The addresses following 0000FF_H are reserved. No external bus access signal is generated.
- Boundary ####_H between the "RAM area" and the "reserved area" varies with the product models.
- Channels 0 to 3 of the OCU compare register use 16-bit free-run timer 2, while channels 4 to 7 of the OCU compare register use 16-bit free-run timer 1. 16-bit free-run timer 1 is also used by input captures (ICU) 0 and 1.

MB90520 Series

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTERS

Interrupt source	EI ² OS support	Interrupt vector		Interrupt control register		Priority
		Number	Address	ICR	Address	
Reset	×	# 08	FFFFDC _H	—	—	High ↑
INT9 instruction	×	# 09	FFFFD8 _H	—	—	
Exception	×	# 10	FFFFD4 _H	—	—	
8/10-bit A/D converter	○	# 11	FFFFD0 _H	ICR00	0000B0 _H	↓ Low
Timebase timer	×	# 12	FFFFCC _H			
DTP0/DTP1 (external interrupt 0/ external interrupt 1)	○	# 13	FFFFC8 _H	ICR01	0000B1 _H	
16-bit free-run timer 1 overflow	×	# 14	FFFFC4 _H			
Extended I/O serial interface 0	○	# 15	FFFFC0 _H	ICR02	0000B2 _H	
Wake-up interrupt	×	# 16	FFFFBC _H			
Extended I/O serial interface 1	○	# 17	FFFFB8 _H	ICR03	0000B3 _H	
DTP2/DTP3 (external interrupt 2/ external interrupt 3)	○	# 18	FFFFB4 _H			
8/16-bit PPG timer 0 counter borrow	×	# 19	FFFFB0 _H	ICR04	0000B4 _H	
DTP4/DTP5 (external interrupt 4/ external interrupt 5)	○	# 20	FFFFAC _H			
8/16-bit up/down counter/timer 0 compare match	○	# 21	FFFFA0 _H	ICR05	0000B5 _H	
8/16-bit up/down counter/timer 0 overflow up/down inversion	○	# 22	FFFFA4 _H			
8/16-bit PPG timer 1 counter borrow	×	# 23	FFFFA0 _H	ICR06	0000B6 _H	
DTP6/DTP7 (external interrupt 6/ external interrupt 7)	○	# 24	FFFF9C _H			
Output compare 1 (OCU) ch.4/ch.5 match	○	# 25	FFFF98 _H	ICR07	0000B7 _H	
Clock prescaler	×	# 26	FFFF94 _H			
Output compare 1 (OCU) ch.6/ch.7 match	○	# 27	FFFF90 _H	ICR08	0000B8 _H	
16-bit free-run timer 2 overflow	×	# 28	FFFF8C _H			
8/16-bit up/down counter/timer 1 compare match	○	# 29	FFFF88 _H	ICR09	0000B9 _H	
8/16-bit up/down counter/timer 1 overflow, up/down inversion	○	# 30	FFFF84 _H			
Input capture 0 (ICU) include	○	# 31	FFFF80 _H	ICR10	0000BA _H	
Input capture 1 (ICU) include	○	# 32	FFFF7C _H			

(Continued)

(Continued)

Interrupt source	EI ² OS support	Interrupt vector		Interrupt control register		Priority
		Number	Address	ICR	Address	
Output compare 0 (OCU) ch.0 match	○	# 33	FFFF78 _H	ICR11	0000BB _H	
Output compare 0 (OCU) ch.1 match	○	# 34	FFFF74 _H			
Output compare 0 (OCU) ch.2 match	○	# 35	FFFF70 _H	ICR12	0000BC _H	
Output compare 0 (OCU) ch.3 match	○	# 36	FFFF6C _H			
UART (SCI) reception complete	◎	# 37	FFFF68 _H	ICR13	0000BD _H	
16-bit re-load timer 0	○	# 38	FFFF64 _H			
UART (SCI) transmission complete	◎	# 39	FFFF60 _H	ICR14	0000BE _H	
16-bit re-load timer 1	○	# 40	FFFF5C _H			
Reserved	×	# 41	FFFF58 _H	ICR15	0000BF _H	
Delayed interrupt generation module	×	# 42	FFFF54 _H			

○ : Can be used

× : Can not be used

◎ : Can be used with EI²OS stop function

■ PERIPHERALS

1. I/O Port

(1) Input/Output Port

Port 0 through A are general-purpose I/O ports having a combined function as a resource input. The I/O ports can be used as general-purpose I/O ports only in the single-chip mode.

- Operation as output port

The pin is configured as an output port by setting the corresponding bit of the DDR register to “1”.

Writing data to PDR register when the port is configured as output, the data is retained in the output latch in the PDR and directly output to the pin.

The value of the pin (the same value retained in the output latch of PDR) can be read out by reading the PDR register.

Note: When a read-modify-write type instruction (e.g. bit set instruction) is performed to the port data register, the destination bit of the operation is set to the specified value, not affecting the bits configured by the DDR register for output. However, values of bits configured as inputs by the DDR register are changed because input values to the pins are written into the output latch. To avoid this situation, configure the pins by the DDR register as output after writing output data to the PDR register when switching the bit used as input to output.

- Operation as input port

The pin is configured as input by setting the corresponding bit of the DDR register to “0.”

When the pin is configured as an input, the output buffer is turned off and the pin is put into a high-impedance status.

When data is written into the PDR register, the data is retained in the output latch of the PDR, but pin outputs are unaffected.

Reading the PDR register reads out the pin level (“0” or “1”).

(2) Register Configuration

- Port 0 data register (PDR0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000000 _H	P07	P06	P05	P04	P03	P02	P01	P00	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 1 data register (PDR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000001 _H	P17	P16	P15	P14	P13	P12	P11	P10	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 2 data register (PDR2)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000002 _H	P27	P26	P25	P24	P23	P22	P21	P20	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 3 data register (PDR3)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000003 _H	P37	P36	P35	P34	P33	P32	P31	P30	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 4 data register (PDR4)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000004 _H	P47	P46	P45	P44	P43	P42	P41	P40	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 5 data register (PDR5)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000005 _H	—	—	—	P54	P53	P52	P51	P50	XXXXXXXX _B
	—	—	—	R/W	R/W	R/W	R/W	R/W	

- Port 6 data register (PDR6)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000006 _H	P67	P66	P65	P64	P63	P62	P61	P60	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 7 data register (PDR7)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000007 _H	P77	P76	P75	P74	P73	P72	P71	P70	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 8 data register (PDR8)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000008 _H	P87	P86	P85	P84	P83	P82	P81	P80	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 9 data register (PDR9)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000009 _H	P97	P96	P95	P94	P93	P92	P91	P90	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

(Continued)

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- Port A data register (PDRA)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00000A _H	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 0 direction register (DDR0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000010 _H	D07	D06	D05	D04	D03	D02	D01	D00	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 1 direction register (DDR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000011 _H	D17	D16	D15	D14	D13	D12	D11	D10	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 2 direction register (DDR2)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000012 _H	D27	D26	D25	D24	D23	D22	D21	D20	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 3 direction register (DDR3)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000013 _H	D37	D36	D35	D34	D33	D32	D31	D30	00000000 _B
				R/W	R/W	R/W	R/W	R/W	

- Port 4 direction register (DDR4)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000014 _H	D47	D46	D45	D44	D43	D42	D41	D40	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 5 direction register (DDR5)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000015 _H	—	—	—	D54	D53	D52	D51	D50	XXX00000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 6 direction register (DDR6)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000016 _H	D67	D66	D65	D64	D63	D62	D61	D60	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 7 direction register (DDR7)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000017 _H	D77	D76	D75	D74	D73	D72	D71	D70	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 8 direction register (DDR8)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000018 _H	D87	D86	D85	D84	D83	D82	D81	D80	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

(Continued)

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- Port 9 direction register (DDR9)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000019 _H	D97	D96	D95	D94	D93	D92	D91	D90	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port A direction register (DDRA)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00001A _H	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 0 input pull-up resistor setup register (RDR0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00008C _H	RD07	RD06	RD05	RD04	RD03	RD02	RD01	RD00	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 1 input pull-up resistor setup register (RDR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00008D _H	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 4 input pull-up resistor setup register (RDR4)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00008E _H	RD47	RD46	RD45	RD44	RD43	RD42	RD41	RD40	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Analog input enable register (ADER)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00001B _H	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	11111111 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 7/COM pin selection register (LCDCMR)

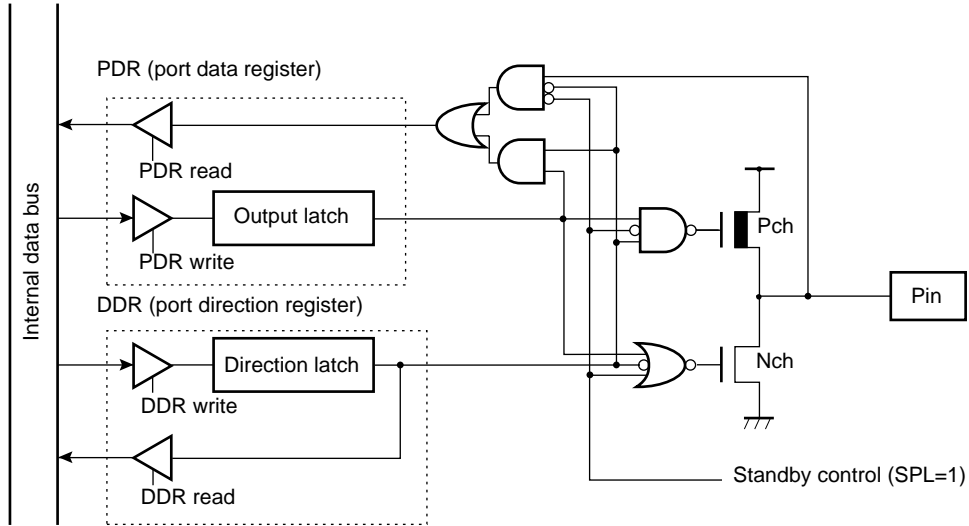
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00000B _H	—	—	—	—	COM3	COM2	COM1	COM0	XXXX0000 _B
	—	—	—	—	R/W	R/W	R/W	R/W	

R/W : Readable and writable
 X : Indeterminate
 — : Undefined bits (read value undefined)

MB90520 Series

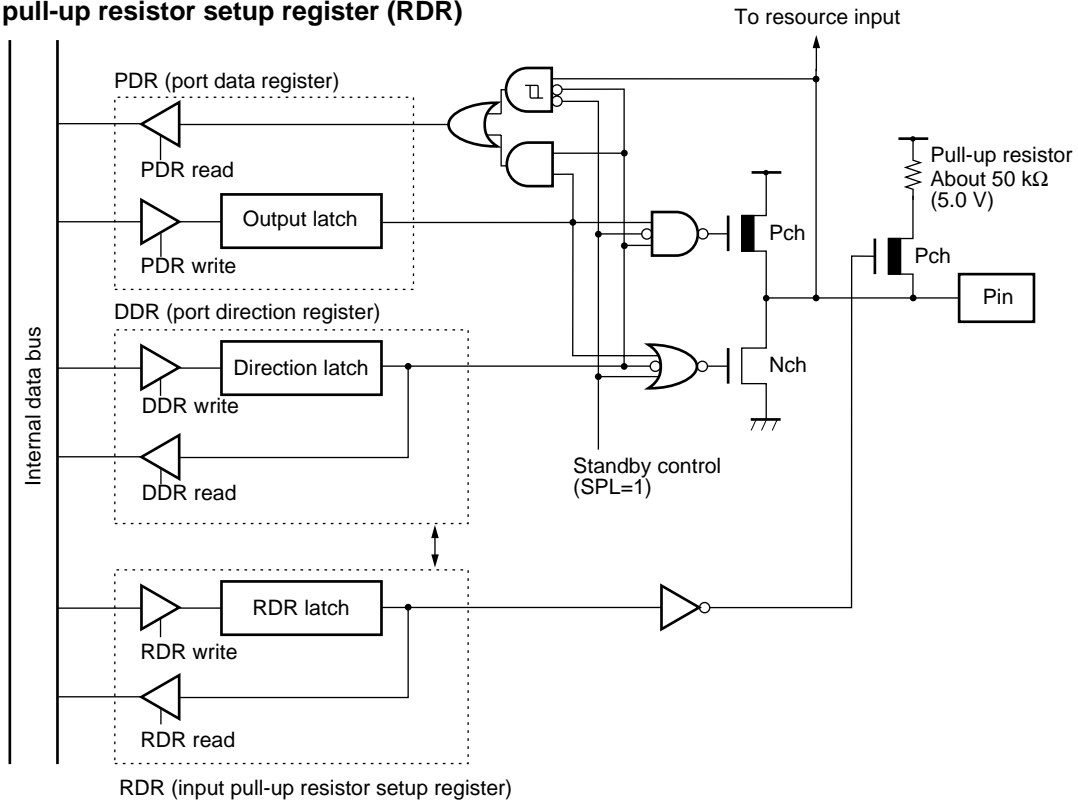
(3) Block Diagram

• Input/output port



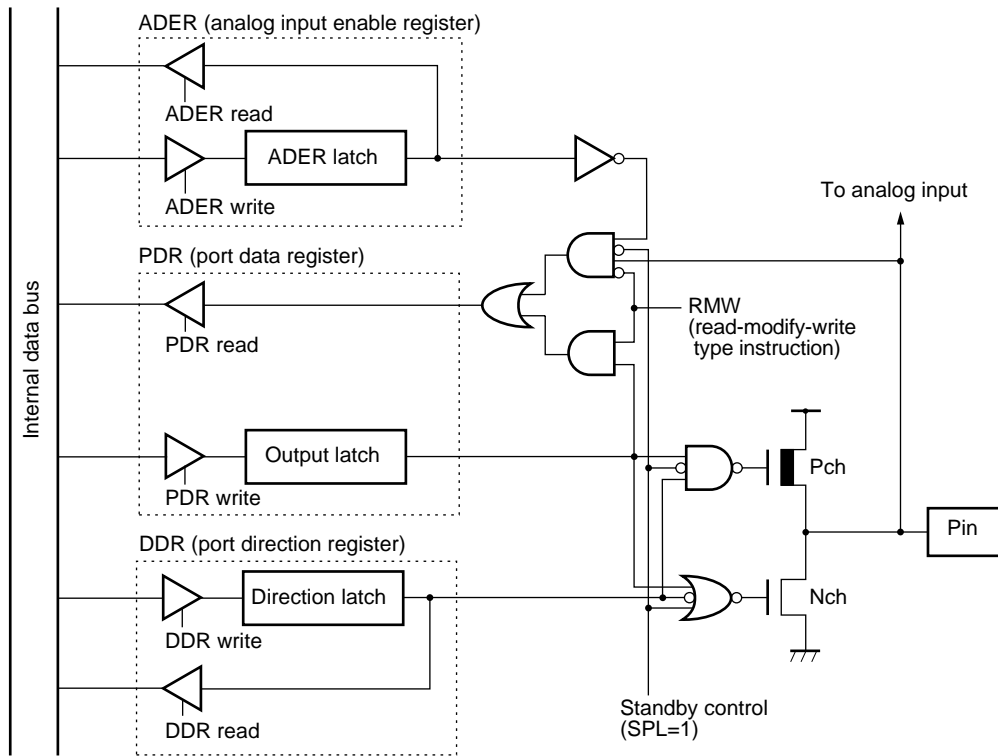
Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

• Input pull-up resistor setup register (RDR)



Standby control: Stop, timebase timer mode and SPL=1

• Analog input enable register (ADER)



Standby control: Stop, timebase timer mode and SPL=1

MB90520 Series

2. Timebase Timer

The timebase timer is a 18-bit free-run counter (timebase counter) for counting up in synchronization to the internal count clock (divided-by-2 of oscillation) with an interval timer function for selecting an interval time from four types : $2^{12}/HCLK$, $2^{14}/HCLK$, $2^{16}/HCLK$, and $2^{19}/HCLK$.

The timebase timer also has a function for supplying operating clocks for the timer output for the oscillation stabilization time or the watchdog timer, etc.

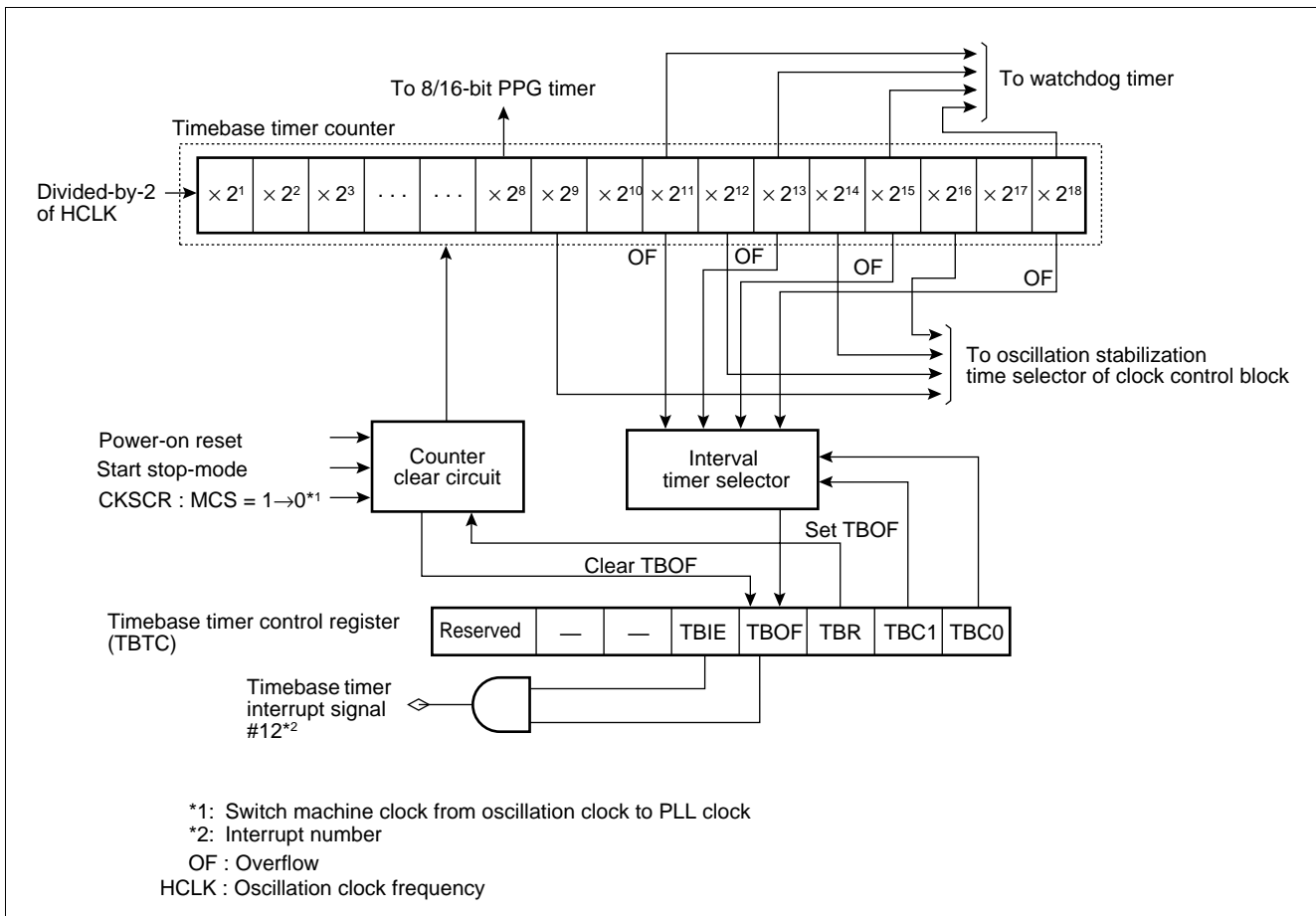
(1) Register Configuration

- Timebase timer control register (TBTC)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
0000A9 _H	Reserved	—	—	TBIE	TBOF	TBR	TBC1	TBC0	1XX0000 _B
	R/W	—	—	R/W	R/W	R/W	R/W	R/W	

R/W: Readable and writable
 — : Undefined bits (read value undefined)

(2) Block Diagram



3. Watchdog Timer

The watchdog timer is a 2-bit counter operating with an output of the timebase timer and resets the CPU when the counter is not cleared for a preset period of time.

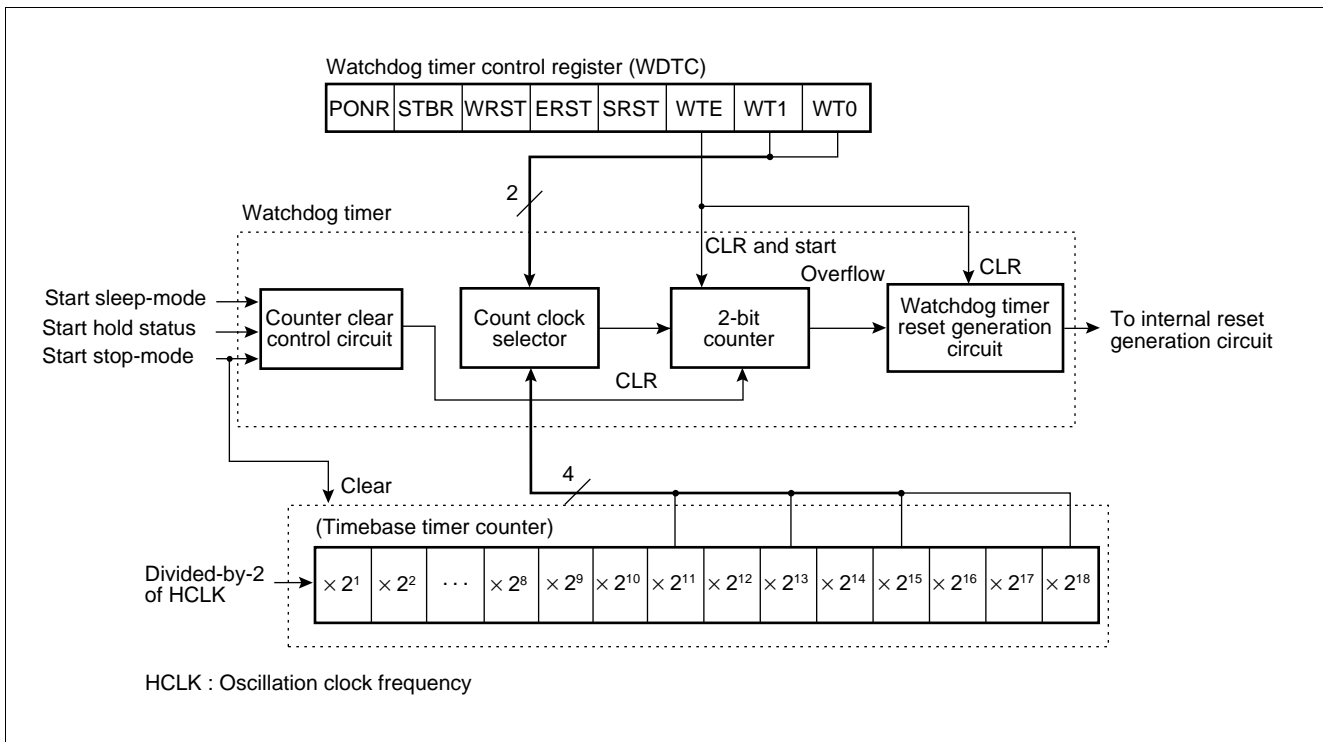
(1) Register Configuration

- Watchdog timer control register (WDTC)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000A8 _H	PONR	STBR	WRST	ERST	SRST	WTE	WT1	WT0	XXXXXXXX _B
	R	R	R	R	R	W	W	W	

R : Read only
W : Write only
X : Indeterminate

(2) Block Diagram



4. 8/16-bit PPG Timer 0, 1

The 8/16-bit PPG timer is a 2-CH re-load timer module for outputting pulse having given frequencies/duty ratios. The two modules perform the following operation by combining functions.

- 8-bit PPG timer output 2-CH independent output mode
This is a mode for operating independent 2-CH 8-bit PPG timers, in which PG00 and PG10 pins correspond to outputs from PPG0 and PPG1 respectively.
- 16-bit PPG timer output operation mode
In this mode, PPG0 and PPG1 are combined to be operated as a 1-CH 8/16-bit PPG timer 0 and 1 operating as a 16-bit timer. Because outputs during 16-bit PPG timer output operation mode are reversed by an underflow from PPG1, the same output pulses are output from PG10 and PG11 pins.
- 8 + 8-bit PPG timer output operation mode
In this mode, PPG0 is operated as an 8-bit prescaler register, in which an underflow output of PPG0 is used as a clock source for PPG1.
A prescaler output of PPG0 is output from PG00 and PG01 pins. PPG output of PPG1 is output from PG10 and PG11 pins.
- PPG output operation
A pulse wave with any period/duty ratio is output. The module can also be used as a D/A converter with an external add-on circuit.

(1) Register Configuration

- PPG0 operating mode control register (PPGC0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000044 _H	PEN0	—	PE00	PIE0	PUF0	—	—	Reserved	0X000XX1 _B
	R/W	—	R/W	R/W	R/W	—	—	—	

- PPG1 operating mode control register (PPGC1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000045 _H	PEN1	—	PE10	PIE1	PUF1	MD1	MD0	Reserved	0X000001 _B
	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	

- PPG0 output control register (PPGOE0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000046 _H	PCS2	PCS1	PCS0	PCM2	PCM1	PCM0	PE11	PE01	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- PPG1 output control register (PPGOE1)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000046 _H	PCS2	PCS1	PCS0	PCM2	PCM1	PCM0	PE11	PE01	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- PPG0 re-load register H (PRLH0)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000041 _H									XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- PPG1 re-load register H (PRLH1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000043 _H									XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- PPG0 re-load register L (PRL0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000040 _H									XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- PPG1 re-load register L (PRL1)

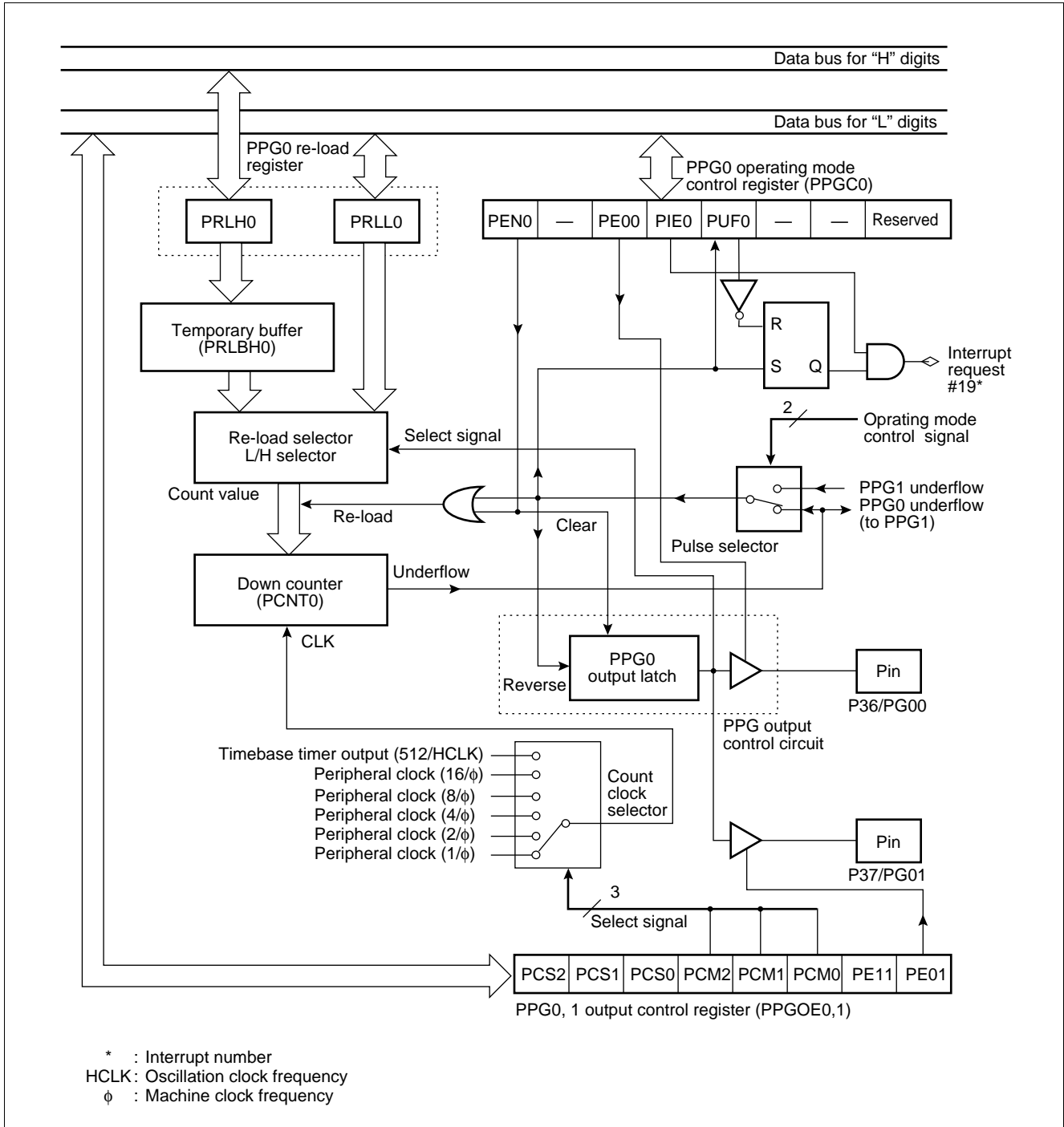
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000042 _H									XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W:Readable and writable
 X : Indeterminate
 — : Undefined bits (read value undefined)

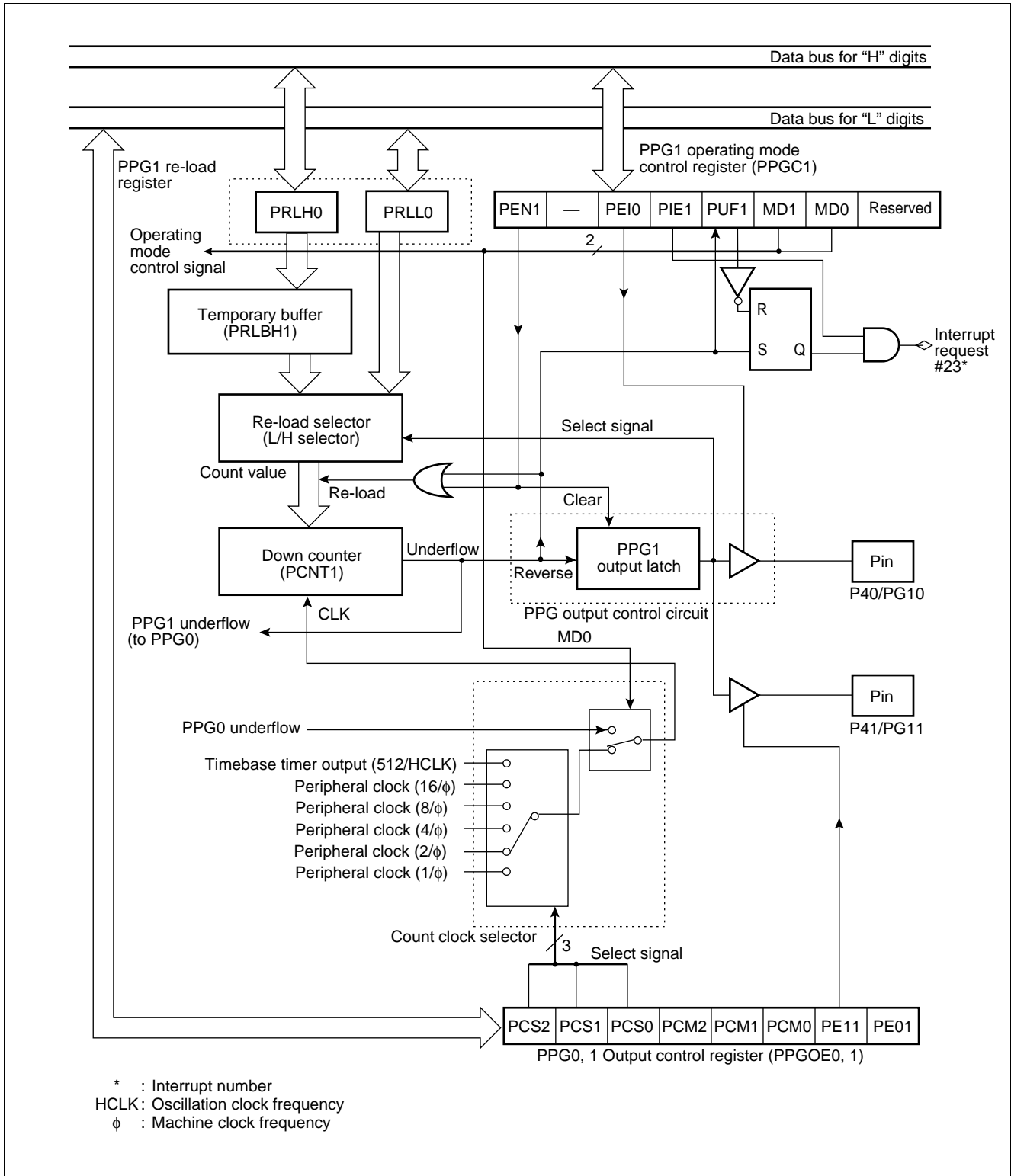
MB90520 Series

(2) Block Diagram

• Block diagram of 8/16-bit PPG timer 0



• Block diagram of 8/16-bit PPG timer 1



MB90520 Series

5. 16-bit Re-load Timer 0, 1 (With an Event Count Function)

The 16-bit re-load timer has an internal clock mode for counting down in synchronization to three types of internal clocks and an event count mode for counting down by detecting a given edge of the pulse input to the external bus pin. Either of the two functions can be selectively used.

For this timer, an “underflow” is defined as the timing of transition from the counter value of “0000H” to “FFFFH.” According to this definition, an underflow occurs after a counter value of [re-load register setting value + 1].

In operating the counter, the re-load mode for repeating counting operation after re-loading a counter value after an underflow or the one-shot mode for stopping the counting operation after an underflow can be selectively used.

Because the timer can generate an interrupt upon an underflow, the timer conforms to the extended intelligent I/O service (EI²OS).

The MB90520 series has 2 channels of 16-bit re-load timers.

(1) Register Configuration

- Timer control status register upper digits ch.0, ch.1 (TMCSR0, TMCSR1 : H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
TMCSR0 : 000049H	—	—	—	—	CSL1	CSL0	MOD2	MOD1	XXXX0000 _B
TMCSR1 : 00004DH	—	—	—	—	R/W	R/W	R/W	R/W	

- Timer control status register lower digits ch.0, ch.1 (TMCSR0, TMCSR1 : L)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
TMCSR0 : 000048H	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	00000000 _B
TMCSR1 : 00004CH	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- 16-bit timer register upper and lower digits ch.0, ch.1 (TMR0, TMR1)

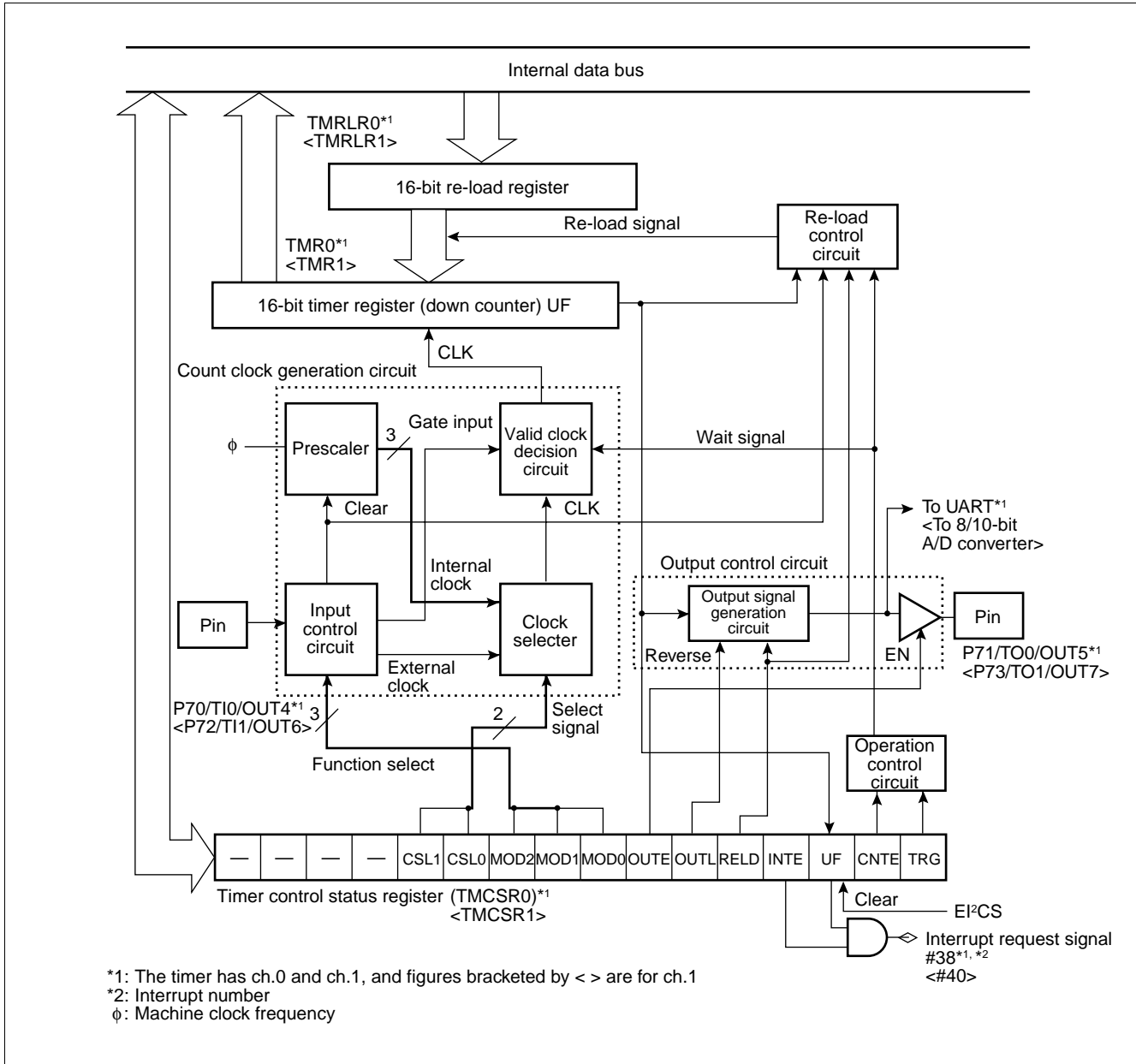
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
TMR0 : 00004BH																	XXXXXXXX _B
00004AH																	XXXXXXXX _B
TMR1 : 00004EH	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	XXXXXXXX _B
00004FH	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	XXXXXXXX _B

- 16-bit re-load register upper and lower digits ch.0, ch.1 (TMRLR0, TMRLR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
TMRLR0 : 00004BH																	XXXXXXXX _B
00004AH																	XXXXXXXX _B
TMRLR1 : 00004EH	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	XXXXXXXX _B
00004FH	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	XXXXXXXX _B

R/W : Readable and writable
 R : Read only
 W : Write only
 X : Indeterminate
 — : Undefined bits (read value undefined)

(2) Block Diagram

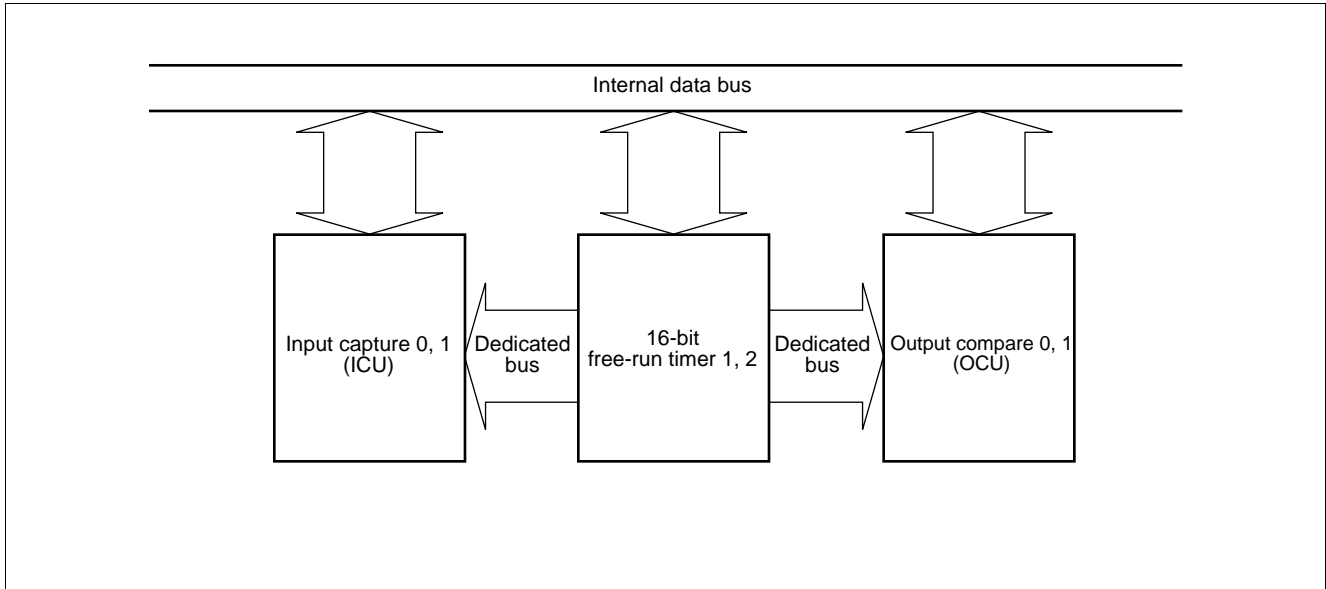


MB90520 Series

6. 16-bit I/O Timer

The 16-bit I/O timer module consists of two 16-bit free-run timers, two input capture circuits (ICU), and eight output comparators (OCU). This module allows two independent waveforms to be output on the basis of the 16-bit free-run timer. Input pulse width and external clock periods can, therefore, be measured.

- **Block diagram**



(1) 16-bit Free-run Timer 1, 2

The 16-bit free-run timer consists of a 16-bit up counter, a control register and a communications prescaler register. The value output from the timer counter is used as basic time (base timer) for input capture (ICU) and output compare (OCU).

- A counter operation clock can be selected from four internal clocks ($\phi/4$, $\phi/16$, $\phi/64$ and $\phi/256$).
- An interrupt can be generated by overflow of counter value or compare match with OCU compare register 0 and 4. (Compare match requires mode settings.)
- The counter value can be initialized to "0000H" by a reset, software clear or compare match with OCU compare register 0 and 4.

• Register configuration

- Free-run timer data register 1, 2 (TCDT1, TCDT2)

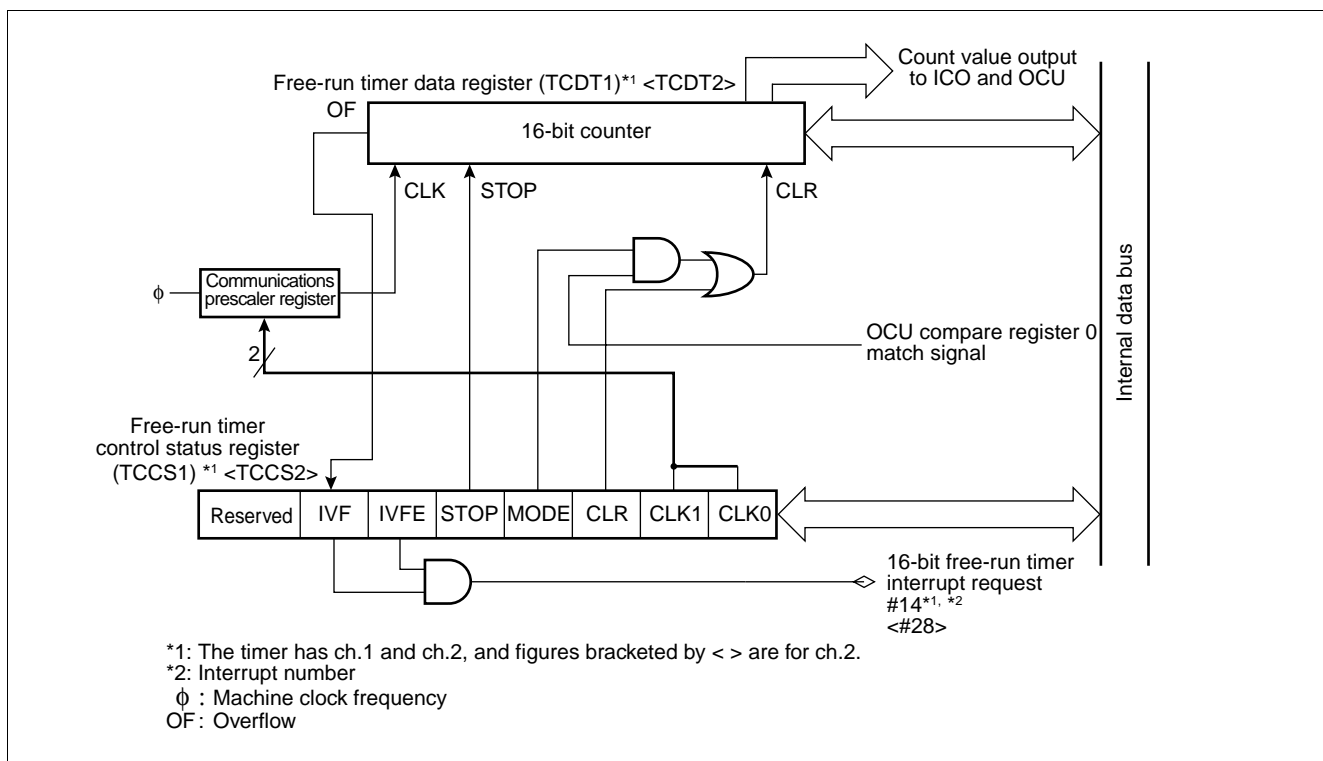
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
TCDT1 : 000057H	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	00000000B
000056H																	00000000B
TCDT2 : 000067H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	00000000B
000066H																	00000000B

- Free-run timer control status register 1, 2 (TCCS1, TCCS2)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
TCCS1 : 000058H	Reserved	IVF	IVFE	STOP	MODE	CLR	CLK1	CLK0	00000000B
TCCS2 : 000068H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	00000000B

R/W: Readable and writable

• Block diagram



MB90520 Series

(2) Input Capture 0, 1 (ICU)

The input capture (ICU) generates an interrupt request to the CPU while storing the current counter value of the 16-bit free-run timer to the ICU data register (IPCP) upon input of a trigger edge from the external pin.

There are two sets (two channels) of input capture external pins and ICU data registers, enabling measurements of a maximum of four events.

- The input capture has two sets of external input pins (IN0, IN1) and ICU registers (IPCP), enabling measurements of a maximum of four events.
- Trigger edge direction can be selected from rising/falling/both edges.
- The input capture can be set to generate an interrupt request at the storage timing of the counter value of the 16-bit free-run timer to the ICU data register (IPCP).
- The input compare conforms to the extended intelligent I/O service (EI²OS).
- The input capture (ICU) function is suited for measurements of intervals (frequencies) and pulse-widths.

• Register configuration

• ICU data register ch.0 ch.1 (IPCP0, IPCP1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
IPCP0(upper) : 000051 _H	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	XXXXXXXX _B
IPCP1(upper) : 000053 _H									
	R	R	R	R	R	R	R	R	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
IPCP0(lower) : 000050 _H	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	XXXXXXXX _B
IPCP1(lower) : 000052 _H									
	R	R	R	R	R	R	R	R	

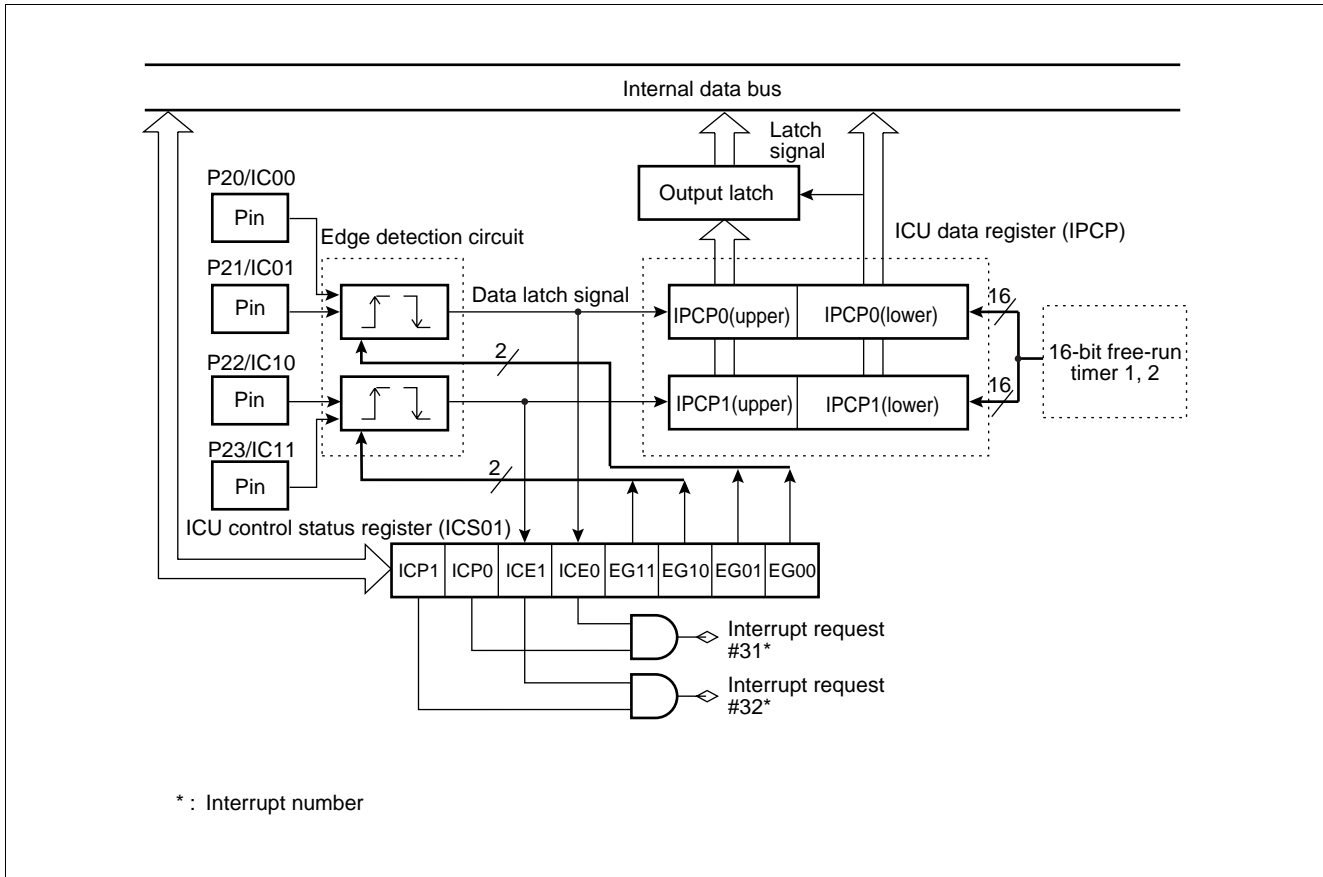
Note: This register holds a 16-bit free-run timer value when the valid edge of the corresponding external pin input waveform is detected. (This register can be word-accessed, but not programmed.)

• ICU control status register (ICS01)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000054 _H	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
 R : Read only
 X : Indeterminate

• Block diagram



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(3) Output Compare 0, 1 (OCU)

The output compare (OCU) is two sets of compare units each consisting of an eight-channel OCU compare register, a comparator and a control register.

An interrupt request can be generated for each channel upon a match detection by performing time-division comparison between the OCU compare data register setting value and the counter value of the 16-bit free-run timer.

The OUT pin can be used as a waveform output pin for reversing output upon a match detection or a general-purpose output port for directly outputting the setting value of the CMOD bit.

• Register Configuration

• OCU control status register ch.01, ch.23, ch.45, ch.67 (OCS01, OCS23, OCS45, OCS67)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
ch.01 : OCS01 (upper) : 0000063 _H	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	XXX00000 _B
ch.23 : OCS23 (upper) : 0000065 _H	—	—	—	R/W	R/W	R/W	R/W	R/W	
ch.45 : OCS45 (upper) : 000002D _H	—	—	—	R/W	R/W	R/W	R/W	R/W	
ch.67 : OCS67 (upper) : 000002F _H	—	—	—	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
ch.01 : OCS01 (lower) : 000062 _H	ICP1	ICP0	ICE1	ICE0	—	—	CST1	CST0	0000XX00 _B
ch.23 : OCS23 (lower) : 000064 _H	R/W	R/W	R/W	R/W	—	—	R/W	R/W	
ch.45 : OCS45 (lower) : 00002C _H	R/W	R/W	R/W	R/W	—	—	R/W	R/W	
ch.67 : OCS67 (lower) : 00002E _H	R/W	R/W	R/W	R/W	—	—	R/W	R/W	

• OCU control status register ch.0 to ch.7 (OCS0 to OCS7)

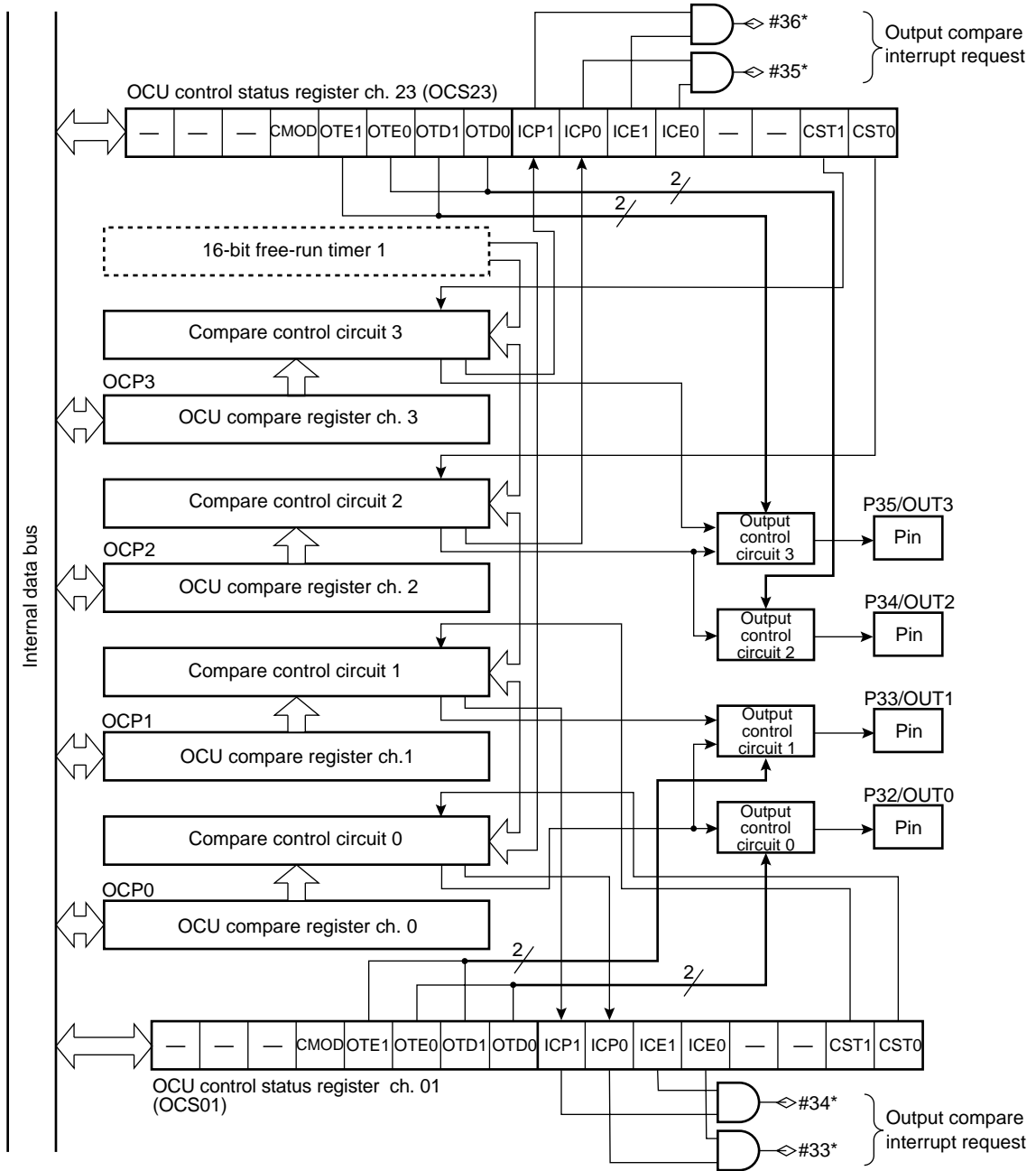
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
ch.0 : OCP0 (upper) : 00005B _H	C15	C14	C13	C12	C11	C10	C09	C08	XXXXXXXX _B
ch.1 : OCP1 (upper) : 00005D _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.2 : OCP2 (upper) : 00005F _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.3 : OCP3 (upper) : 000061 _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.4 : OCP4 (upper) : 00000D _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.5 : OCP5 (upper) : 00001D _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.6 : OCP6 (upper) : 000035 _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.7 : OCP7 (upper) : 00006D _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
ch.0 : OCP0 (lower) : 00005A _H	C07	C06	C05	C04	C03	C02	C01	C00	XXXXXXXX _B
ch.1 : OCP1 (lower) : 00005C _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.2 : OCP2 (lower) : 00005E _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.3 : OCP3 (lower) : 000060 _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.4 : OCP4 (lower) : 00000C _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.5 : OCP5 (lower) : 00001C _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.6 : OCP6 (lower) : 000034 _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ch.7 : OCP7 (lower) : 00006C _H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
 X : Indeterminate
 — : Undefined bits (read value undefined)

- Block diagram

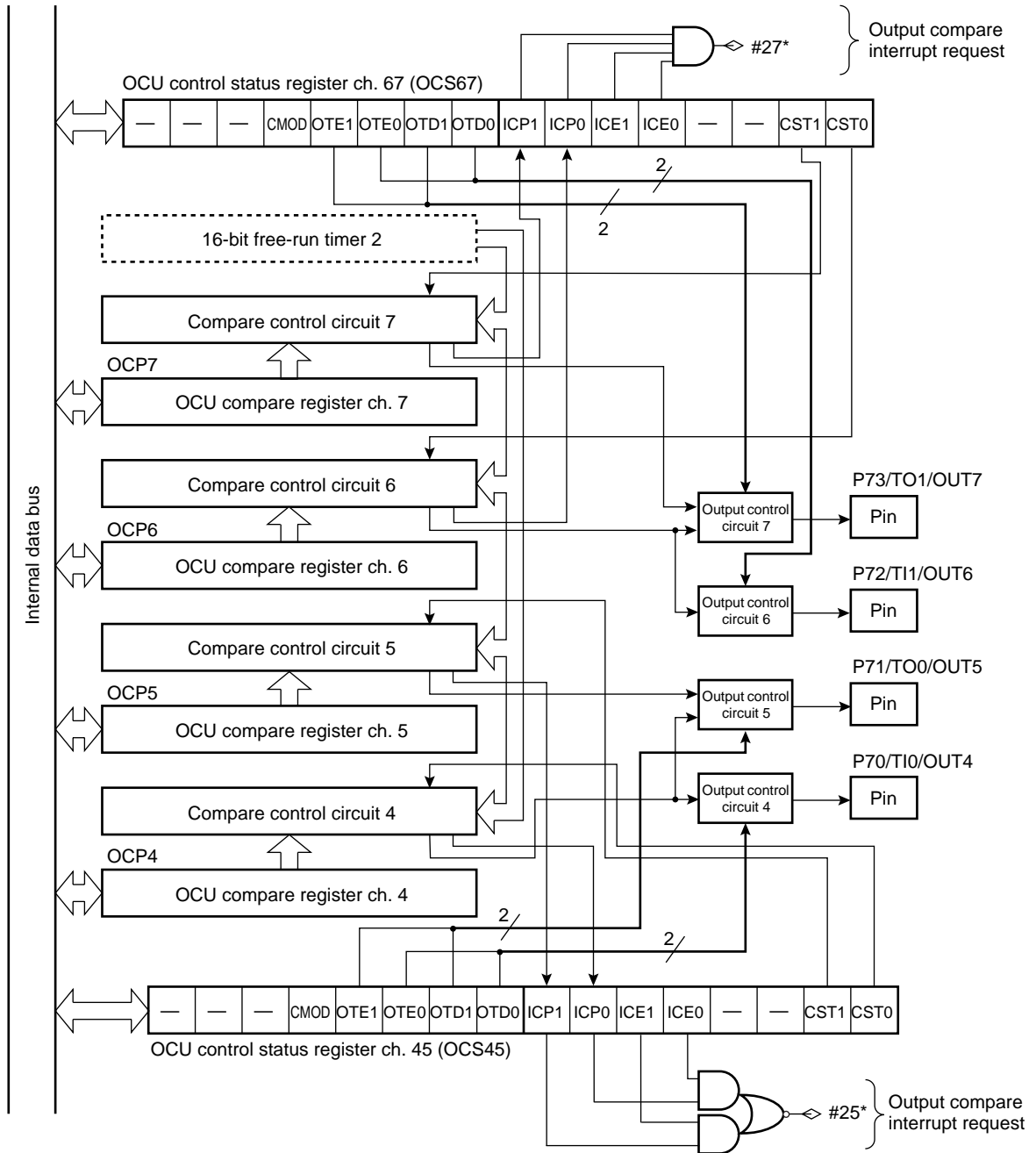
- Output compare 0 (OCU)



* : Interrupt number

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• Output compare 1(OCU)



* : Interrupt number

7. 8/16-bit Up/Down Counter/Timer 0, 1

The 8/16-bit up/down counter/timer consists of six event input pins, two 8-bit up/down counters, two 8-bit re-load compare registers, and their controllers.

(1) Register Configuration

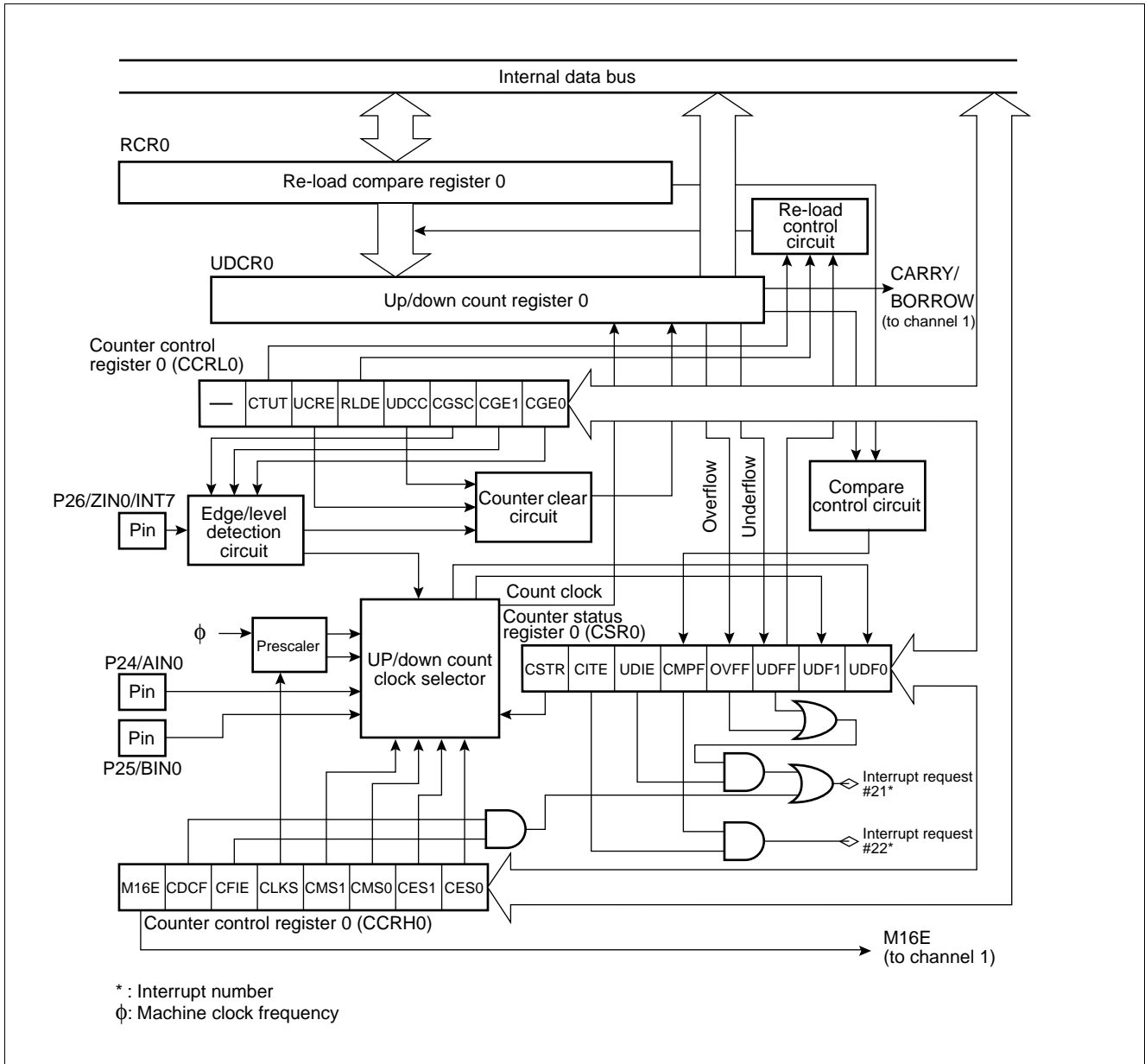
• Up/down count register 0 (UDCR0)										
Address	bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0	Initial value								
000080H	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td>D07</td><td>D06</td><td>D05</td><td>D04</td><td>D03</td><td>D02</td><td>D01</td><td>D00</td> </tr> </table>	D07	D06	D05	D04	D03	D02	D01	D00	00000000 _B
D07	D06	D05	D04	D03	D02	D01	D00			
	R R R R R R R R									
• Up/down count register 1 (UDCR1)										
Address	bit 15 bit 14 bit 13 bit 12 bit 11 bit 10 bit 9 bit 8	Initial value								
000081H	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td>D17</td><td>D16</td><td>D15</td><td>D14</td><td>D13</td><td>D12</td><td>D11</td><td>D10</td> </tr> </table>	D17	D16	D15	D14	D13	D12	D11	D10	00000000 _B
D17	D16	D15	D14	D13	D12	D11	D10			
	R R R R R R R R									
• Re-load compare register 0 (RCR0)										
Address	bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0	Initial value								
000082H	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td>D07</td><td>D06</td><td>D05</td><td>D04</td><td>D03</td><td>D02</td><td>D01</td><td>D00</td> </tr> </table>	D07	D06	D05	D04	D03	D02	D01	D00	00000000 _B
D07	D06	D05	D04	D03	D02	D01	D00			
	W W W W W W W W									
• Re-load compare register 1 (RCR1)										
Address	bit 15 bit 14 bit 13 bit 12 bit 11 bit 10 bit 9 bit 8	Initial value								
000083H	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td>D17</td><td>D16</td><td>D15</td><td>D14</td><td>D13</td><td>D12</td><td>D11</td><td>D10</td> </tr> </table>	D17	D16	D15	D14	D13	D12	D11	D10	00000000 _B
D17	D16	D15	D14	D13	D12	D11	D10			
	W W W W W W W W									
• Counter status register 0, 1 (CSR0, CSR1)										
Address	bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0	Initial value								
CSR0 : 000084H CSR1 : 000088H	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td>CSTR</td><td>CITE</td><td>UDIE</td><td>CMPF</td><td>OVFF</td><td>UDFF</td><td>UDF1</td><td>UDF0</td> </tr> </table>	CSTR	CITE	UDIE	CMPF	OVFF	UDFF	UDF1	UDF0	00000000 _B
CSTR	CITE	UDIE	CMPF	OVFF	UDFF	UDF1	UDF0			
	R/W R/W R/W R/W R/W R/W R R									
• Counter control register 0, 1 (CCRL0, CCRL1)										
Address	bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0	Initial value								
CCRL0 : 000086H CCRL1 : 00008AH	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td>—</td><td>CTUT</td><td>UCRE</td><td>RLDE</td><td>UDCC</td><td>CGSC</td><td>CGE1</td><td>CGE0</td> </tr> </table>	—	CTUT	UCRE	RLDE	UDCC	CGSC	CGE1	CGE0	X0000000 _B
—	CTUT	UCRE	RLDE	UDCC	CGSC	CGE1	CGE0			
	— R/W R/W R/W R/W R/W R/W R/W									
• Counter control register 0 (CCRH0)										
Address	bit 15 bit 14 bit 13 bit 12 bit 11 bit 10 bit 9 bit 8	Initial value								
000087H	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td>M16E</td><td>CDCF</td><td>CFIE</td><td>CLKS</td><td>CMS1</td><td>CMS0</td><td>CES1</td><td>CES0</td> </tr> </table>	M16E	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0	00000000 _B
M16E	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0			
	R/W R/W R/W R/W R/W R/W R/W R/W									
• Counter control register 1 (CCRH1)										
Address	bit 15 bit 14 bit 13 bit 12 bit 11 bit 10 bit 9 bit 8	Initial value								
00008BH	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td>—</td><td>CDCF</td><td>CFIE</td><td>CLKS</td><td>CMS1</td><td>CMS0</td><td>CES1</td><td>CES0</td> </tr> </table>	—	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0	X0000000 _B
—	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0			
	— R/W R/W R/W R/W R/W R/W R/W									

R/W : Readable and writable
R : Read only
W : Write only
— : Undefined bits (read value undefined)

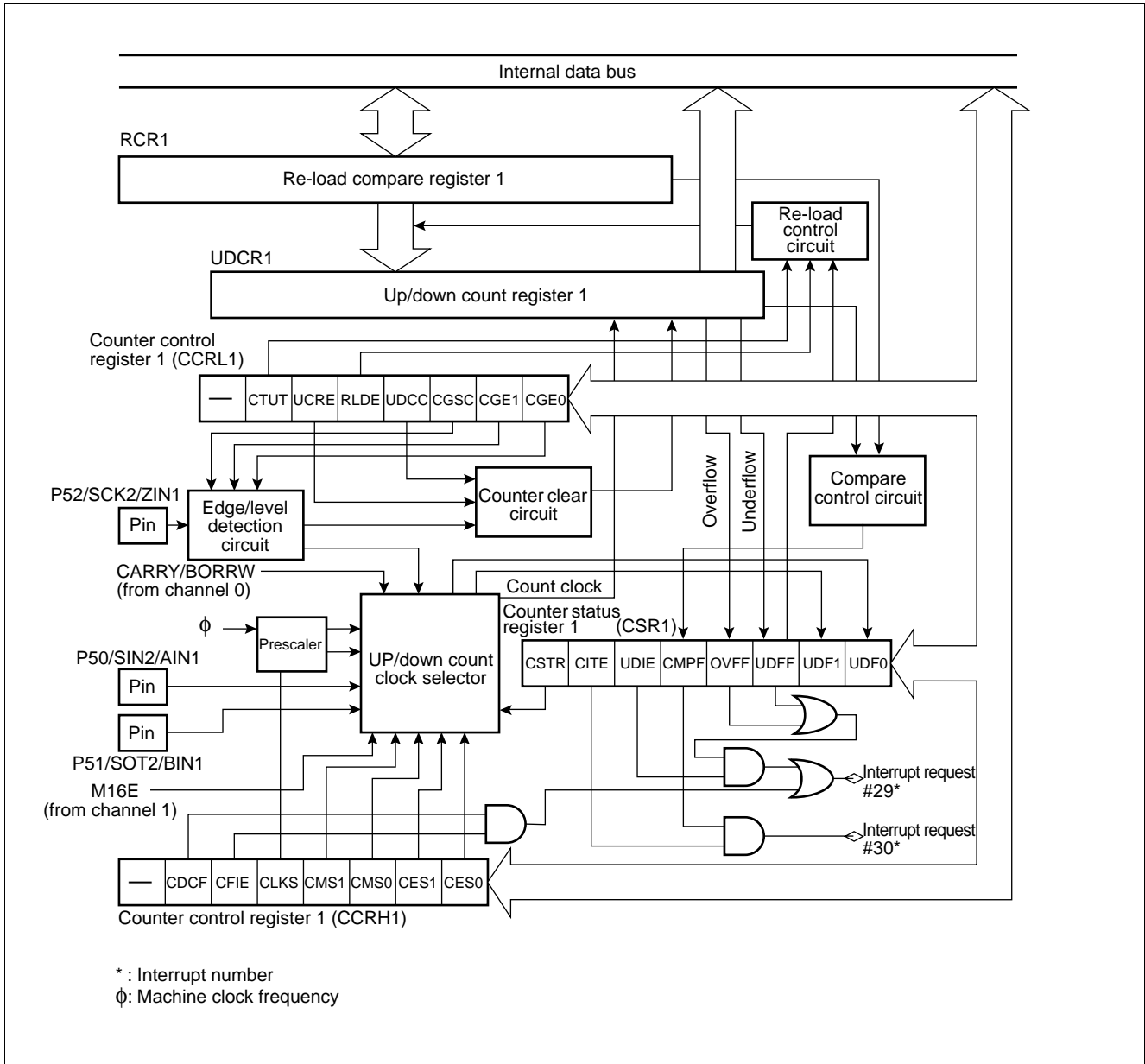
MB90520 Series

(2) Block Diagram

• Block diagram of 8/16-bit up/down counter/timer 0



• Block diagram of 8/16-bit up/down counter/timer 1



MB90520 Series

8. Extended I/O Serial Interface 0, 1

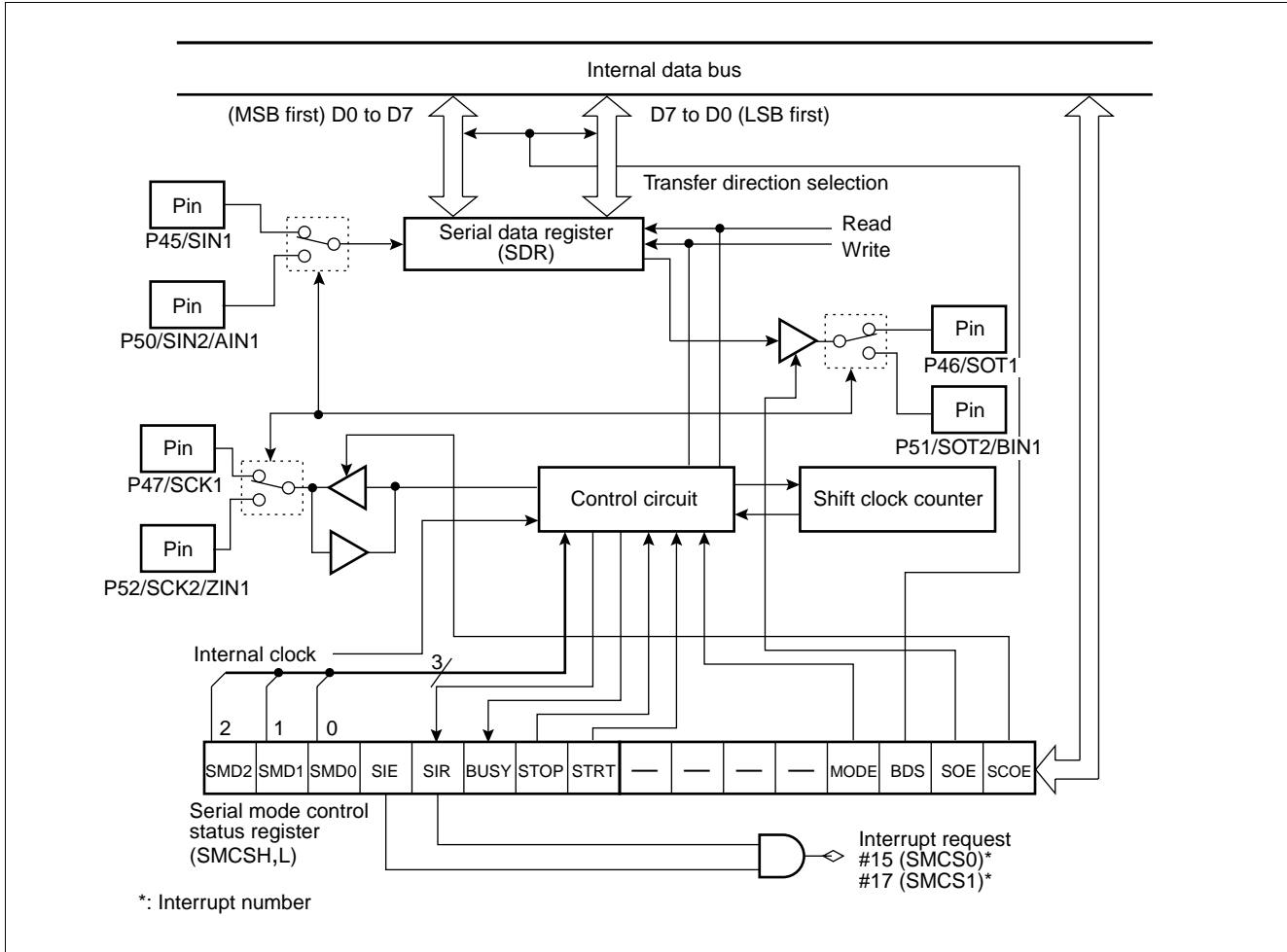
The extended I/O serial interface transfers data using a clock synchronization system having an 8-bit x 1 channel configuration.

For data transfer, you can select LSB first/MSB first.

(1) Register Configuration

<ul style="list-style-type: none"> Serial mode control upper status register 0, 1 (SMCSH0, SMCSH1) 									
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
SMCSH0 : 000025 _H SMCSH1 : 000029 _H	SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT	00000010 _B
	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	
<ul style="list-style-type: none"> Serial mode control lower status register 0, 1 (SMCSL0, SMCSL1) 									
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
SMCSL0 : 000024 _H SMCSL1 : 000028 _H	—	—	—	—	MODE	BDS	SOE	SCOE	XXXX0000 _B
	—	—	—	—	R/W	R/W	R/W	R/W	
<ul style="list-style-type: none"> Serial data register 0, 1 (SDR0, SDR1) 									
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
SDR0 : 000026 _H SDR1 : 00002A _H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
R/W : Readable and writable R : Read only X : Indeterminate — : Undefined bits (read value undefined)									

(2) Block Diagram



MB90520 Series

9. UART (SCI)

UART (SCI) is a general-purpose serial data communication interface for performing synchronous or asynchronous communication (start-stop synchronization system).

- Data buffer: Full-duplex double buffer
- Transfer mode: Clock synchronized (with start and stop bit)
Clock asynchronous (start-stop synchronization system)
- Baud rate: Embedded dedicated baud rate generator
External clock input possible
Internal clock (a clock supplied from 16-bit re-load timer 0 can be used.)
Asynchronization 9615 bps/31250 bps/4808 bps/2404 bps/1202 bps } Internal machine clock
CLK synchronization 1 Mbps/500 kbps/250 kbps/125 kbps/62.5 kbps } For 6 MHz, 8 MHz, 10 MHz,
12 MHz and 16 MHz
- Data length: 8 bit (without a parity bit)
7 bit (with a parity bit)
- Signal format: NRZ (Non Return to Zero) system
- Reception error detection: Framing error
Overrun error
Parity error (multi-processor mode is supported, enabling setup of any baud rate by an external clock.)
- Interrupt request: Receive interrupt (reception complete, receive error detection)
Transmit interrupt (transmission complete)
Transmit/receive conforms to extended intelligent I/O service (EI²OS)

(1) Register Configuration

- Serial control register (SCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000021 _H	PEN	P	SBL	CL	A/D	REC	RXE	TXE	0000100 _B
	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W	

- Serial mode register (SMR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000020 _H	MD1	MD0	CS2	CS1	CS0	Reserved	SCKE	SOE	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Serial status register (SSR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000023 _H	PE	ORE	FRE	RDRF	TRDE	—	RIE	TIE	00001X00 _B
	R	R	R	R	R	—	R/W	R/W	

- Serial input data register (SIDR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000022 _H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
	R	R	R	R	R	R	R	R	

- Serial output data register (SODR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000022 _H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
	W	W	W	W	W	W	W	W	

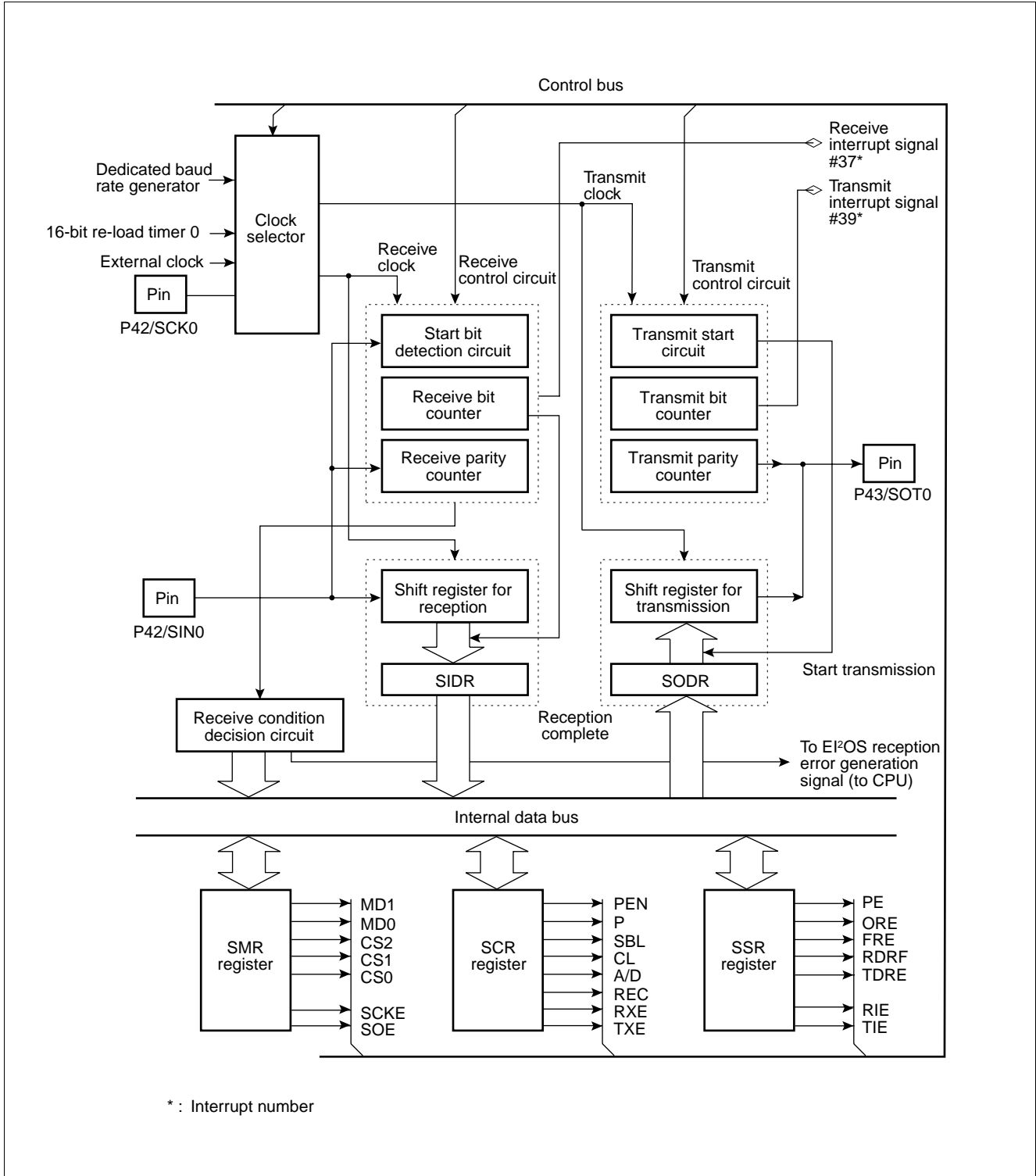
- Communications prescaler control register (CDCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000027 _H	MD	—	—	—	DIV3	DIV2	DIV1	DIV0	0XXX1111 _B
	R/W	—	—	—	R/W	R/W	R/W	R/W	

R/W:Readable and writable
 R : Read only
 W : Write only
 X : Indeterminate
 — : Undefined bits (read value undefined)

MB90520 Series

(2) Block Diagram



10. DTP/External Interrupt Circuit

The DTP (Data Transfer Peripheral), which is located between the peripheral circuit outside the device and the F²MC-16LX CPU, receives an interrupt request or DMA request generated by the external peripheral circuit* for transmission to the F²MC-16LX CPU. It is used to activate the intelligent I/O service or interrupt processing. As with request levels, two types of “H” and “L” can be selected for the intelligent I/O service. Rising and falling edges as well as “H” and “L” can be selected for an external interrupt request.

* : The external peripheral circuit is connected outside the MB90520 series device.

(1) Register Configuration

- DTP/interrupt factor register (EIRR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000031 _H	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- DTP/interrupt enable register (ENIR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000030 _H	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

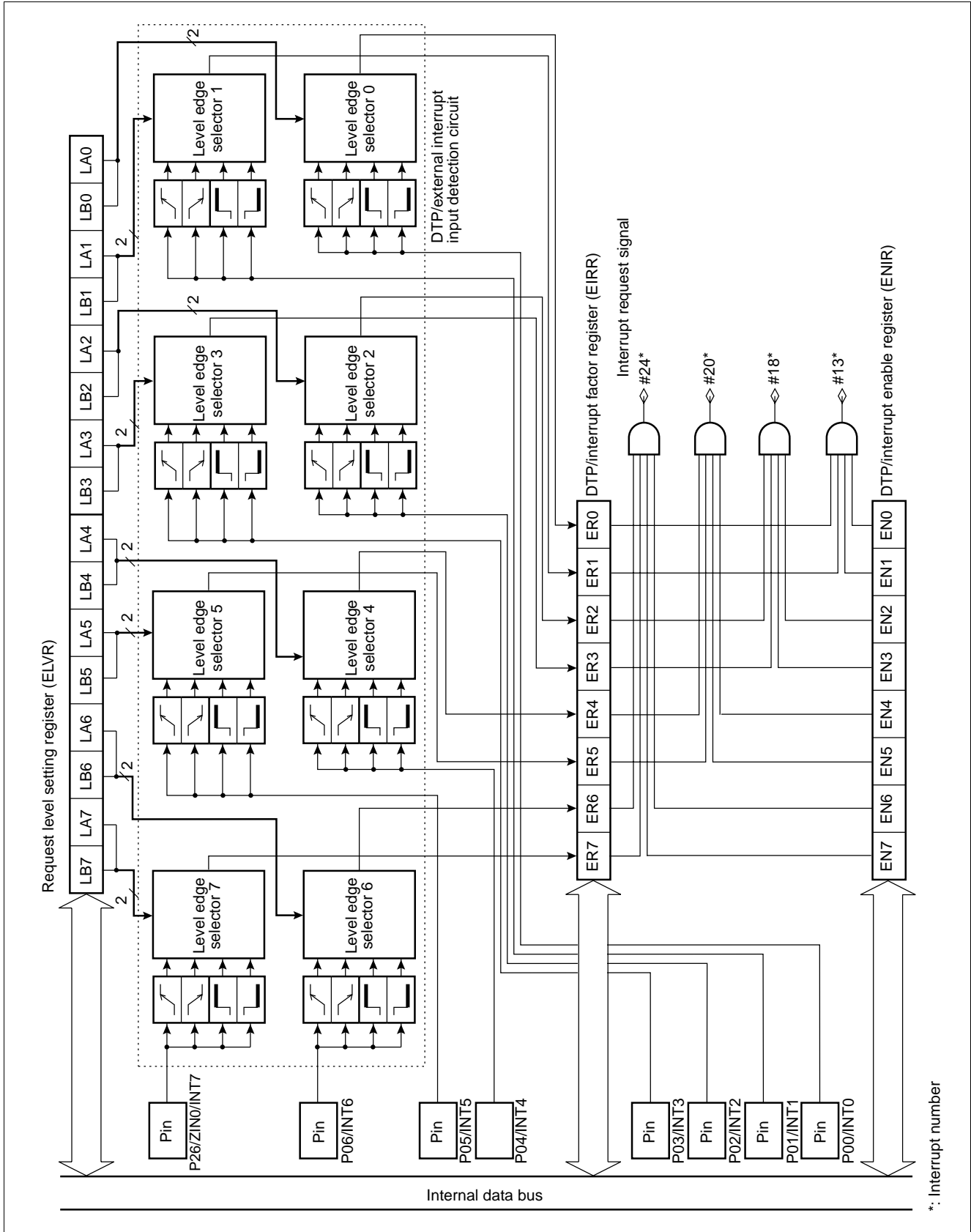
- Request level setting register (ELVR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
ELVR (lower) : 000032 _H	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
ELVR (upper) : 000033 _H	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W: Readable and writable
X : Indeterminate

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(2) Block Diagram



11. Wake-up Interrupt

Wake-up interrupts transmit interrupt request (“L” level) generated by peripheral equipment located between external peripheral devices and the F²MC-16LX CPU to the CPU and invoke interrupt processing.

The interrupt does not conform to the extended intelligent I/O service (EI²OS).

(1) Register Configuration

- Wake-up interrupt flag register (EIFR)

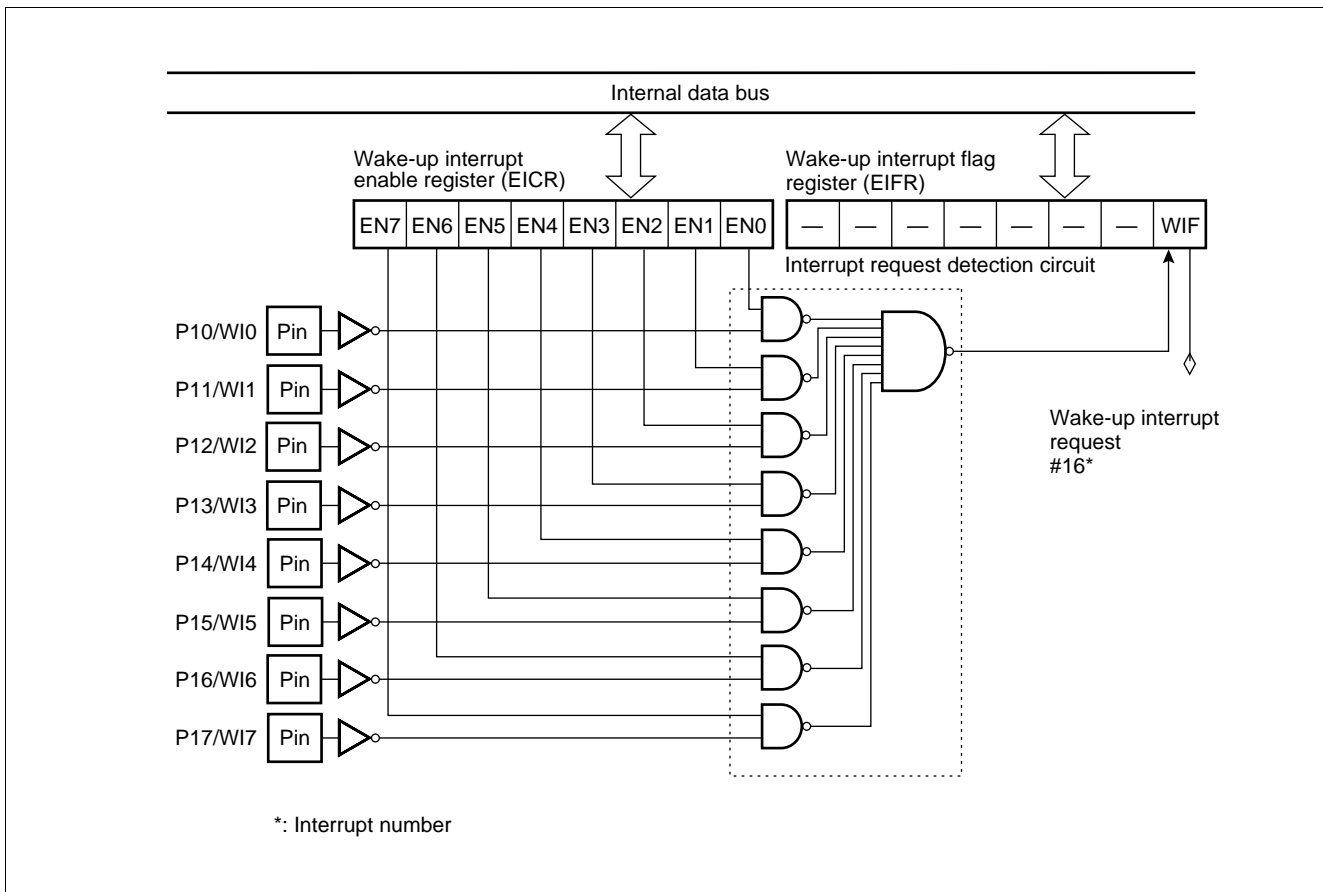
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00000F _H	—	—	—	—	—	—	—	WIF	XXXXXXXX0 _B
	—	—	—	—	—	—	—	R/W	

- Wake-up interrupt enable register (EICR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00001F _H	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000 _B
	W	W	W	W	W	W	W	W	

R/W: Readable and writable
 W : Write only
 — : Undefined bits (read value undefined)

(2) Block Diagram



12. Delayed Interrupt Generation Module

The delayed interrupt generation module generates interrupts for switching tasks. By using this module, hardware interrupt requests to the CPU can be generated and cancelled using software.

This module does not conform to the extended intelligent I/O service (EI²OS).

(1) Register Configuration

- Delayed interrupt factor generation/cancellation register (DIRR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00009F _H	—	—	—	—	—	—	—	R0	XXXXXXXX0 _B
	—	—	—	—	—	—	—	R/W	

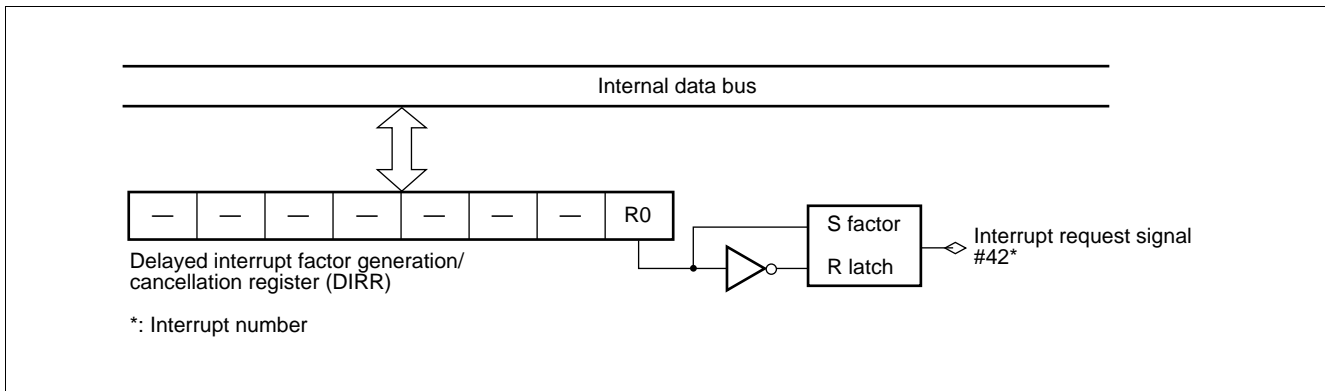
Note: Upon a reset, an interrupt is cancelled.

R/W: Readable and writable

— : Undefined bits (read value undefined)

The DIRR is the register used to control delay interrupt request generation/cancellation. Programming this register with “1” generates a delay interrupt request. Programming this register with “0” cancels a delay interrupt request. Upon a reset, an interrupt is canceled. The undefined bit area can be programmed with either “0” or “1.” For future extension, however, it is recommended that bit set and clear instructions be used to access this register.

(2) Block Diagram



13. 8/10-bit A/D Converter

The 8/10-bit A/D converter converts analog voltage input to the analog input pins (input voltage) to digital values (A/D conversion) and has the following features:

- Minimum conversion time: minimum 15.0 μs (at machine clock frequency of 16 MHz, including sampling time)
- Minimum sampling period: 4 μs /8 μs (at machine clock frequency of 16 MHz)
- Compare time: 99/176 machine cycles per channel
(99 machine cycles are used for a machine clock frequency below 10 MHz.)
- Conversion method: RC successive approximation method with a sample and hold circuit
- 8/10-bit resolution
- Analog input pins: Selectable from eight channels by software
 - Single conversion mode: Selects and converts one channel.
 - Scan conversion mode: Converts two or more successive channels. Up to eight channels can be programmed.
 - Continuous conversion mode: Repeatedly converts specified channels.
 - Stop conversion mode: Stops conversion after completing a conversion for one channel and wait for the next activation (conversion can be started synchronously).
- Interrupt requests can be generated and the extended intelligent I/O service (EI²OS) can be started after the end of A/D conversion. Furthermore, A/D conversion result data can be transferred to the memory, enabling efficient continuous processing.
- When interrupts are enabled, there is no loss of data even in continuous operations because the conversion data protection function is in effect.
- Starting factors for conversion: Selectable from software activation, external trigger (falling edge) and timer (rising edge).

MB90520 Series

(1) Register Configuration

- A/D control status register upper digits (ADCS2)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000037H	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Reserved	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	W	R/W	

- A/D control status register lower digits (ADCS1)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000036H	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- A/D data register upper digits (ADCR2)

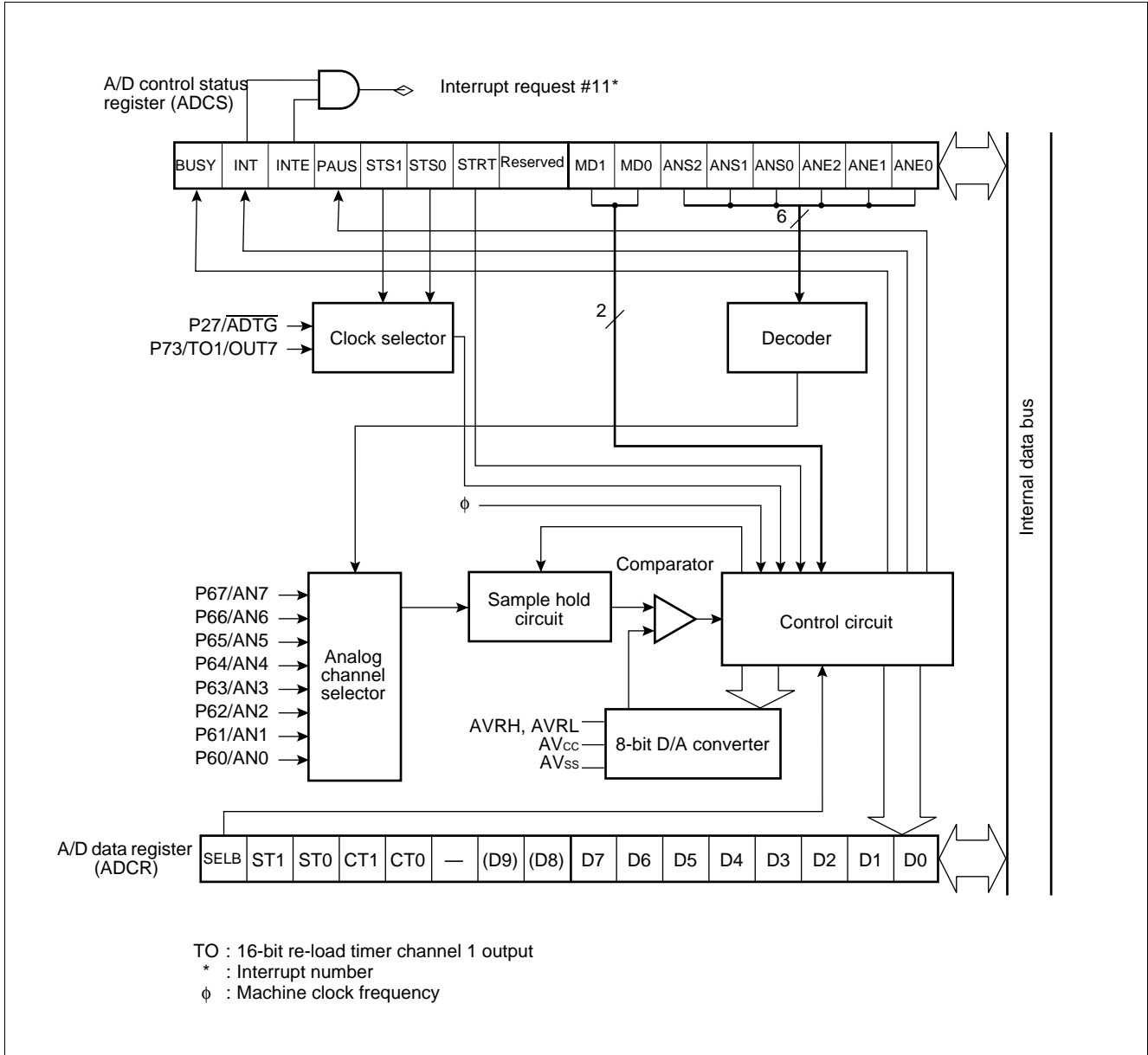
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000039H	SELB	ST1	ST0	CT1	CT0	—	(D9)	(D8)	00001XXX _B
	W	W	W	W	W	—	R	R	

- A/D data register lower digits (ADCR1)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000038H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
	R	R	R	R	R	R	R	R	

R/W: Readable and writable
 R : Read only
 W : Write only
 X : Indeterminate
 — : Undefined bits (read value undefined)

(2) Block Diagram



MB90520 Series

14. 8-bit D/A Converter

The 8-bit D/A converter, which is based on the R-2R system, supports 8-bit resolution mode. It contains two channels, each of which can be controlled in terms of output by the D/A control register.

(1) Register Configuration

- D/A converter data register ch.0 (DADR0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003A _H	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- D/A converter data register ch.1 (DADR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00003B _H	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- D/A control register 0 (DACR0)

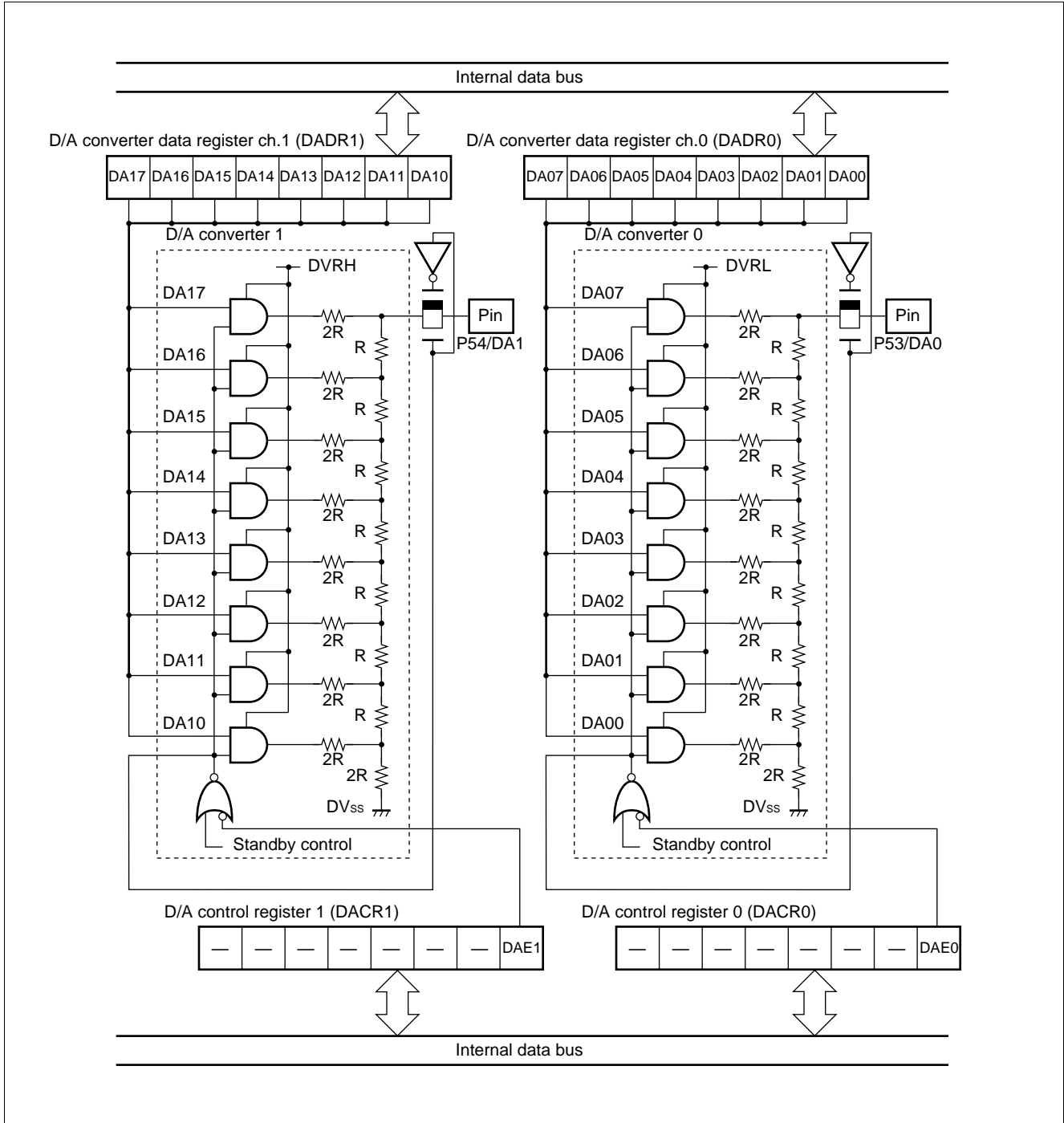
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003C _H	—	—	—	—	—	—	—	DAE0	XXXXXXXX0 _B
	—	—	—	—	—	—	—	R/W	

- D/A control register 1 (DACR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00003D _H	—	—	—	—	—	—	—	DAE1	XXXXXXXX0 _B
	—	—	—	—	—	—	—	R/W	

R/W: Readable and writable
 X : Indeterminate
 — : Undefined bits (read value undefined)

• Block Diagram



MB90520 Series

15. Clock Timer

The clock timer control register (WTC) controls operation of the clock timer, and time for an interval interrupt.

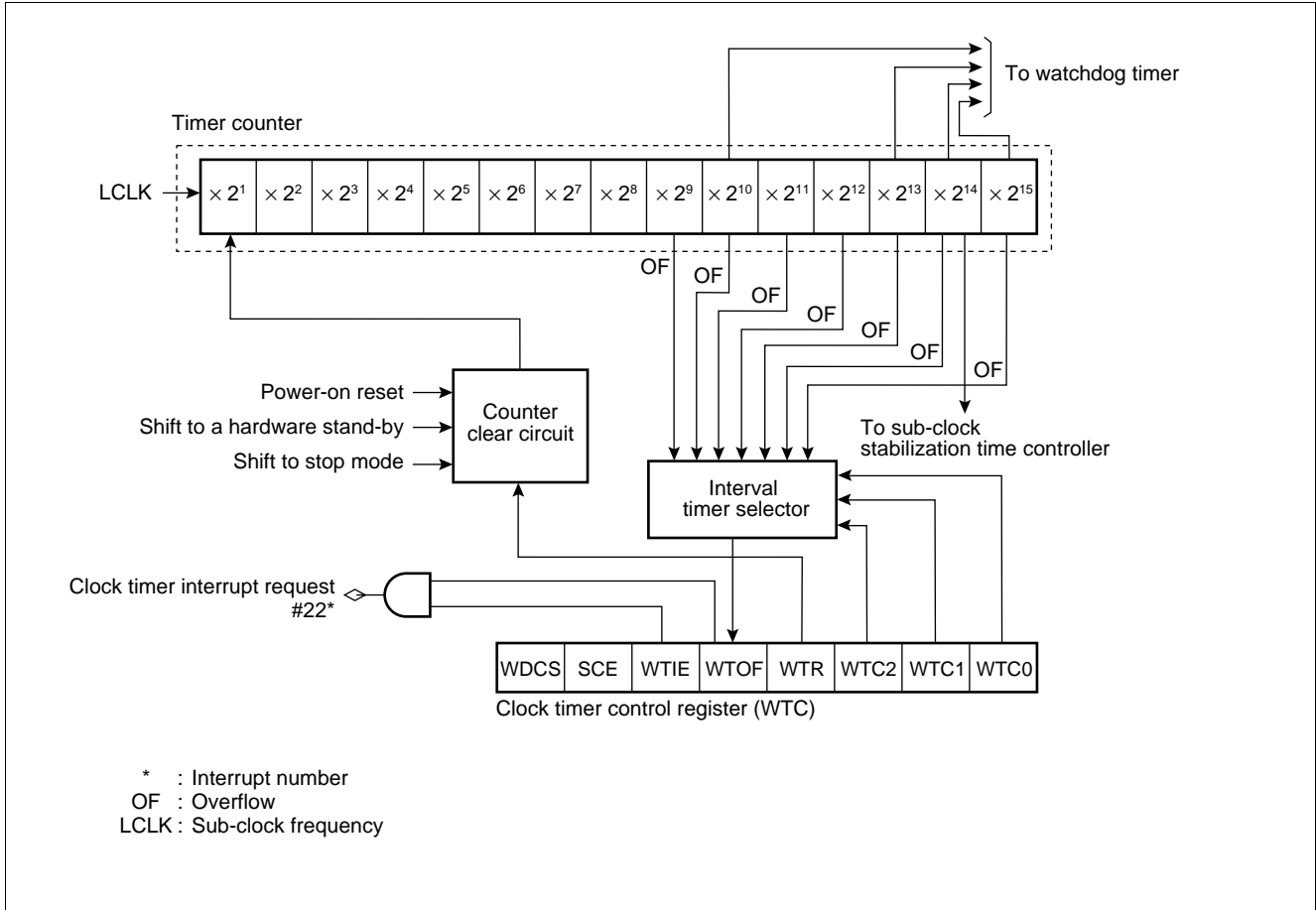
(1) Register Configuration

- Clock timer control register (WTC)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000AA _H	WDSCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0	1X001000 _B
	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	

R/W: Readable and writable
 R : Read only
 X : Indeterminate

(2) Block Diagram



16.LCD Controller/Driver

The LCD (liquid crystal display) controller/driver, which contains a 16-byte display data memory, controls LCD indication using four common output pins and 32 segment output pins. It can select three types of duty output and directly drive the LCD panel.

(1) Register Configuration

- LCDC control register 0 (LCR0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00006AH	CSS	LCEN	VSEL	BK	MS1	MS0	FP1	FP0	00010000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- LCDC control register 1 (LCR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00006BH	Reserved	SEG5	SEG4	Reserved	SEG3	SEG2	SEG1	SEG0	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 7/COM pin selection register (LCDCMR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00000BH	—	—	—	—	COM3	COM2	COM1	COM0	XXXX0000 _B
	—	—	—	—	R/W	R/W	R/W	R/W	

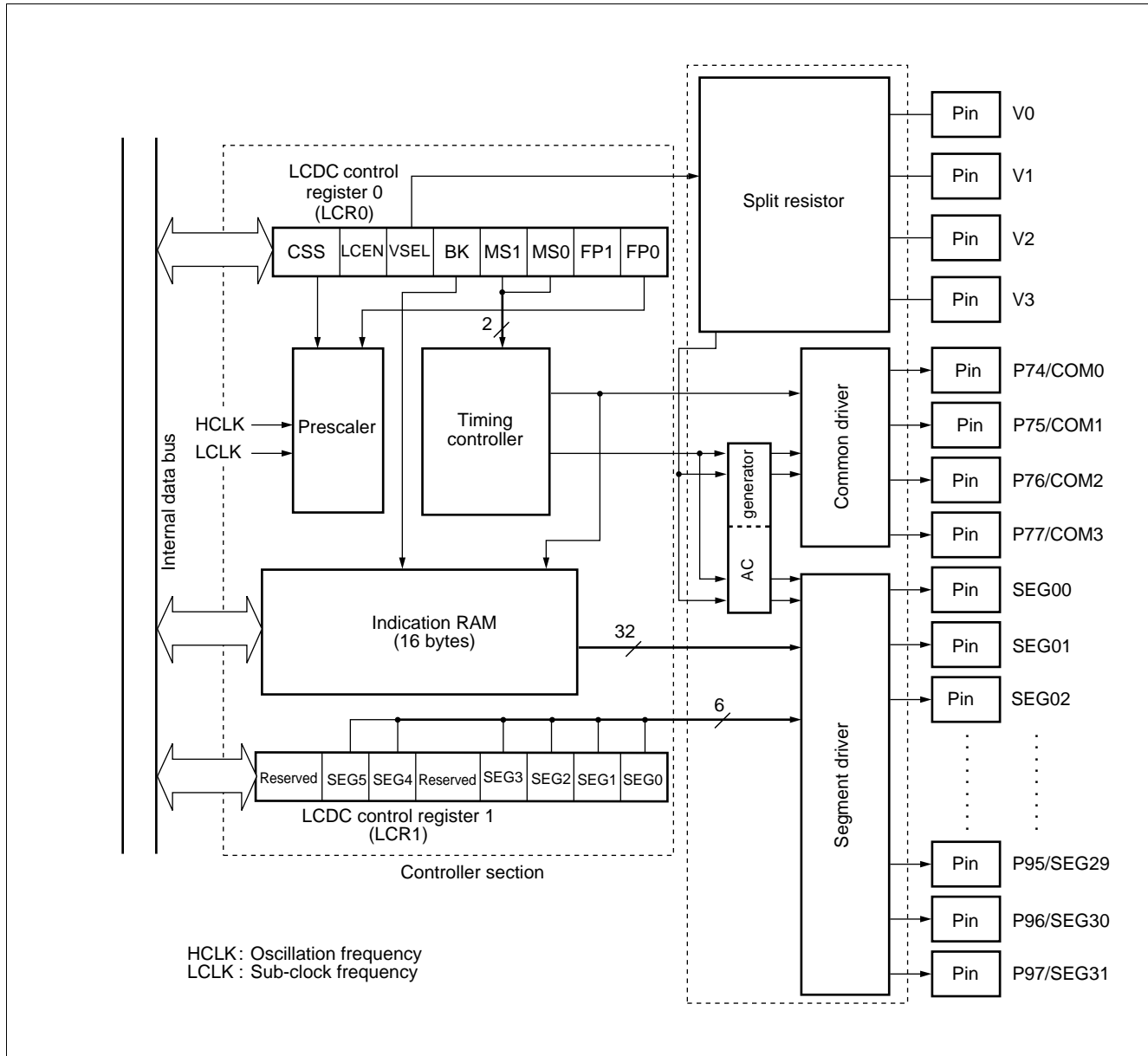
- RAM for LCD indication (VRAM)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000070H to 00007FH	b7	b6	b5	b4	b3	b2	b1	b0	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W: Readable and writable
 X : Indeterminate
 — : Undefined bits (read value undefined)

MB90520 Series

(2) Block Diagram



17. Communications Prescaler Register

This register controls machine clock division.

Output from the communications prescaler register is used for UART (SCI) and extended I/O serial interface.

The communications prescaler register is so designed that a constant baud rate may be acquired for various machine clocks.

(1) Register Configuration

- Communications prescaler control register (CDCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
000027 _H	MD	—	—	—	DIV3	DIV2	DIV1	DIV0	0XXX1111 _B
	R/W	—	—	—	R/W	R/W	R/W	R/W	

R/W: Readable and writable

— : Undefined bits (read value undefined)

18. Address Match Detection Function

When the address is equal to a value set in the address detection register, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code (01H). As a result, when the CPU executes a set instruction, the INT9 instruction is executed. Processing by the INT#9 interrupt routine allows the program patching function to be implemented.

Two address detection registers are supported. An interrupt enable bit is prepared for each register. If the value set in the address detection register matches an address and if the interrupt enable bit is set at "1," the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code.

(1) Register Configuration

- Program address detection register 0 to 2 (PADR0)

PADR0 (High order address) : 001FF2 _H	Address	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	Initial value XXXXXXXX _B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

PADR0 (Middle order address) : 001FF1 _H	Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value XXXXXXXX _B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

PADR0 (Low order address) : 001FF0 _H	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value XXXXXXXX _B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection register 3 to 5 (PADR1)

PADR1 (High order address) : 001FF5 _H	Address	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	Initial value XXXXXXXX _B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

PADR1 (Middle order address) : 001FF4 _H	Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value XXXXXXXX _B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

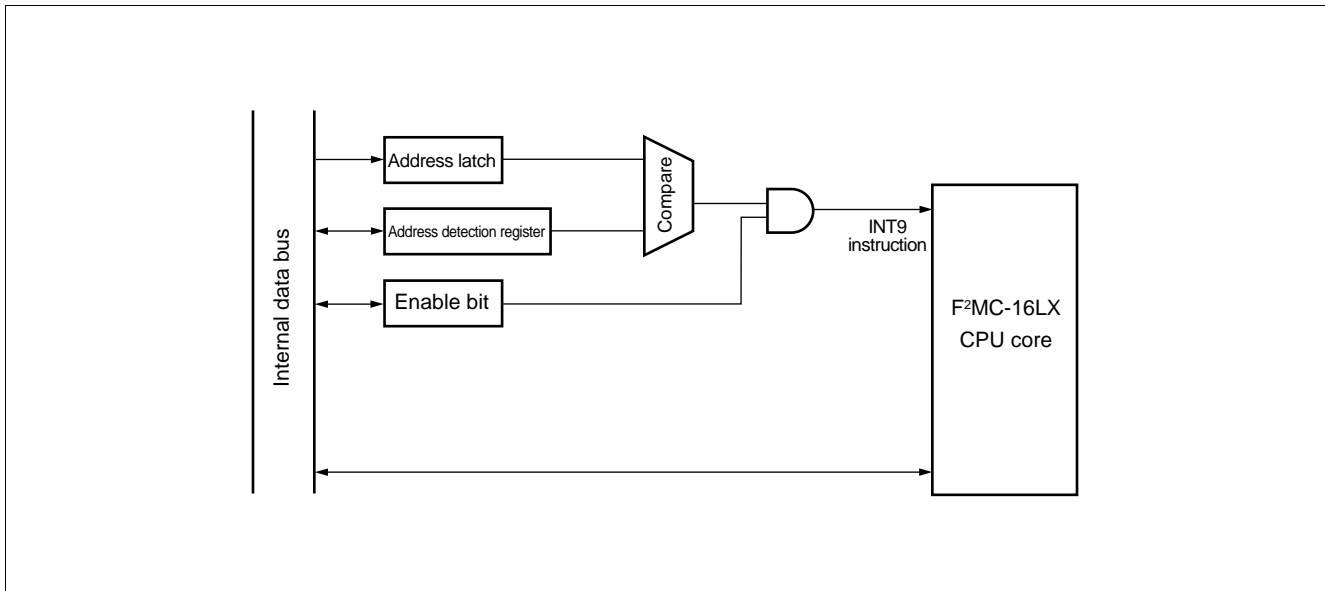
PADR1 (Low order address) : 001FF3 _H	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value XXXXXXXX _B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection control status register (PACSR)

00009E _H	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value 00000000 _B
		Reserved	Reserved	Reserved	Reserved	AD1E	Reserved	AD0E	Reserved	
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W: Readable and writable
 X : Indeterminate
 — : Undefined bits (read value undefined)

(2) Block Diagram



MB90520 Series

19. ROM Mirroring Function Selection Module

The ROM mirror function select module enables the ROM data from the FF bank to be read also from the 00 bank.

(1) Register Configuration

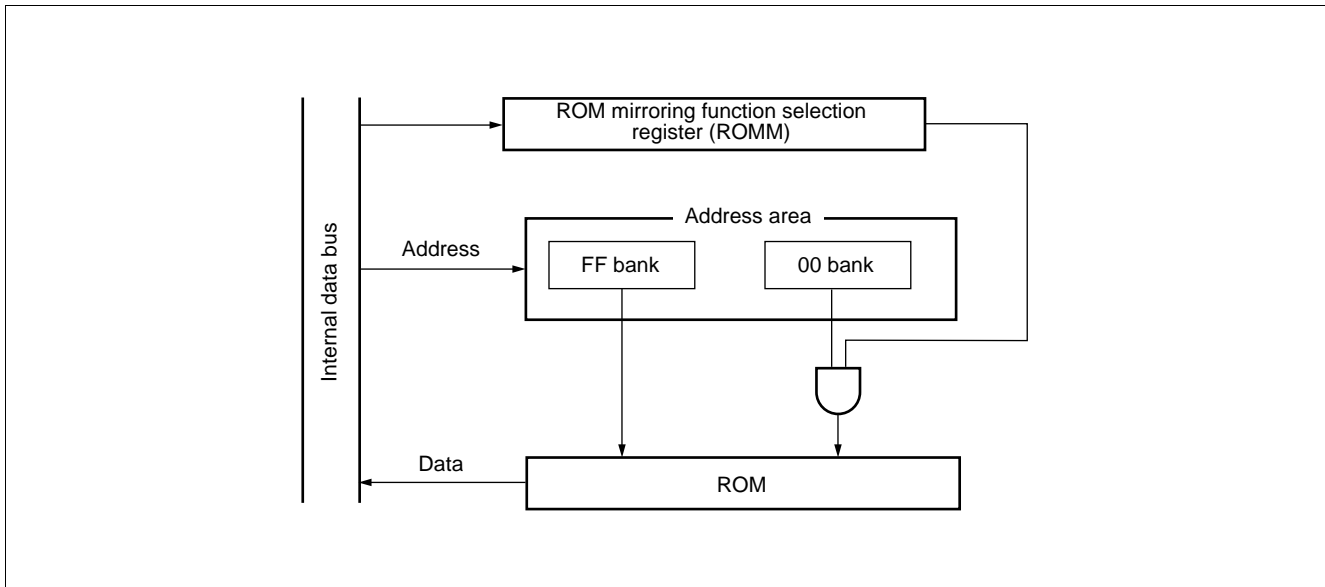
- ROM mirroring function selection register (ROMM)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
00006F _H	—	—	—	—	—	—	—	MI	XXXXXXXX _{1B}
	—	—	—	—	—	—	—	W	

W : Write only
— : Undefined bits (read value undefined)

Note: Do not access this register during operation at addresses 004000_H to 00FFFF_H.

(2) Block Diagram



20. Low-power Consumption (Stand-by) Mode

The F²MC-16LX has the following CPU operating modes configured by selection of an operating clock and clock operation control.

- **Clock mode**

PLL clock mode: A mode in which the CPU and peripheral equipment are driven by PLL-multiplied oscillation clock.

Main clock mode: A mode in which the CPU and peripheral equipment are driven by divided-by-2 of the oscillation clock. The PLL multiplication circuits stops in the main clock mode.

- **Sub-clock mode**

The sub-clock mode causes the CPU to operate only with the sub-clock. This mode uses the sub-clock frequency divided by four as the operating clock frequency while stopping the main clock and PLL clock.

- **CPU intermittent operation mode**

The CPU intermittent operation mode is a mode for reducing power consumption by operating the CPU intermittently while external bus and peripheral functions are operated at a high speed.

- **Hardware stand-by mode**

The hardware standby mode is a mode for reducing power consumption by stopping clock supply to the CPU by the low-power consumption control circuit (sleep mode), stopping clock supplies to the CPU and peripheral functions (timebase timer mode), and stopping oscillation clock (stop mode, hardware stand-by mode). Of these modes, modes other than the PLL clock mode are low power consumption modes.

(1) Register Configuration

- Clock select register (CKSCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
0000A1H	SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	11111100 _B
	R	R	R/W	R/W	R/W	R/W	R/W	R/W	

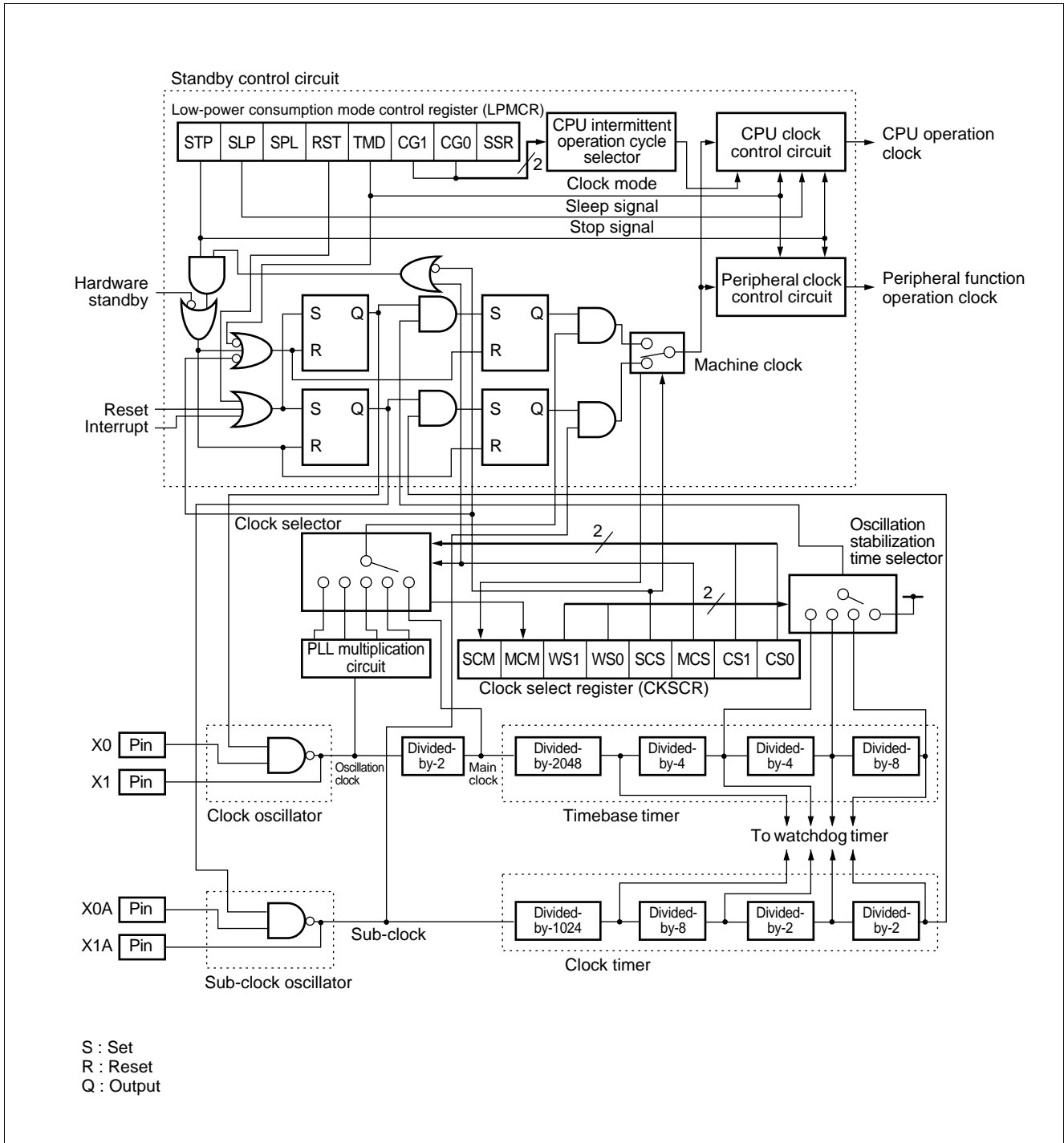
- Low-power consumption mode control register (LPMCR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000A0H	STP	SLP	SPL	RST	TMD	CG1	CG0	SSR	00011000 _B
	W	W	R/W	W	W	R/W	R/W	R/W	

R/W: Readable and writable
 R : Read only
 W : Write only

MB90520 Series

(2) Block Diagram



21. Clock Monitor Function

The clock monitor function outputs the frequency-divided machine clock signal (for monitoring purposes) from the CKOT pin.

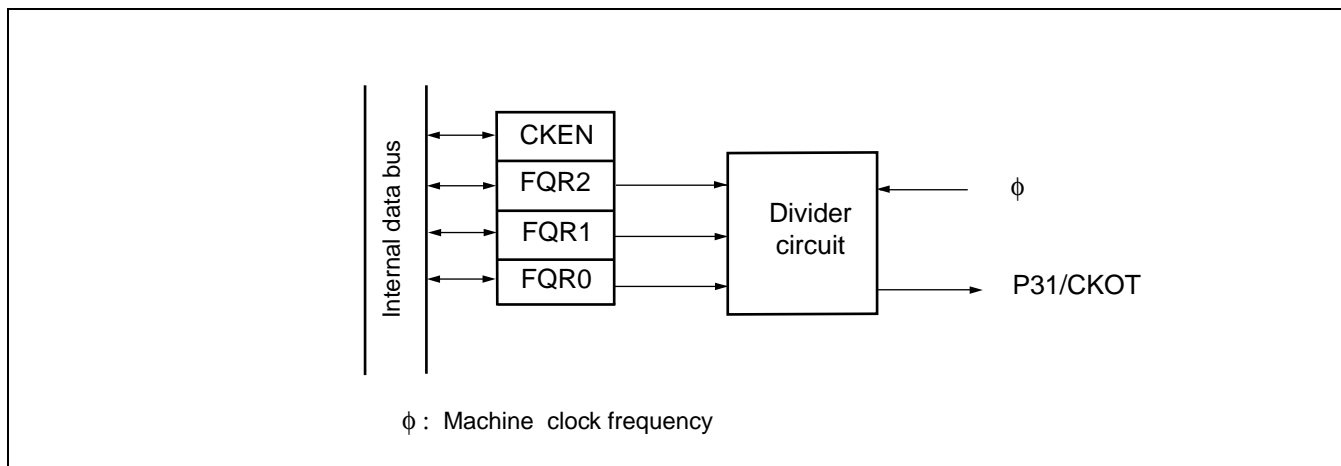
(1) Register configuration

- Clock output enable register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003EH	—	—	—	—	CKEN	FRQ2	FRQ1	FRQ0	XXXXXXXX1B
	—	—	—	—	R/W	R/W	R/W	R/W	

R/W:Readable and writable
 —:Undefined bits (read value undefined)

(2) Block Diagram



MB90520 Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V _{CC}	V _{SS} - 0.3	V _{SS} + 6.0	V	
	AV _{CC}	V _{SS} - 0.3	V _{SS} + 6.0	V	*1
	AVRH, AVRL	V _{SS} - 0.3	V _{SS} + 6.0	V	*1
	DV _{CC}	V _{SS} - 0.3	V _{SS} + 6.0	V	*2
Input voltage	V _I	V _{SS} - 0.3	V _{CC} + 6.0	V	*3
Output voltage	V _O	V _{SS} - 0.3	V _{CC} + 6.0	V	*3
"L" level maximum output current	I _{OL}	—	15	mA	*4
"L" level average output current	I _{OLAV}	—	4	mA	*5
"L" level total maximum output current	ΣI _{OL}	—	100	mA	
"L" level total average output current	ΣI _{OLAV}	—	50	mA	*6
"H" level maximum output current	I _{OH}	—	-15	mA	*4
"H" level average output current	I _{OHAV}	—	-4	mA	*5
"H" level total maximum output current	ΣI _{OH}	—	-100	mA	
"H" level total average output current	ΣI _{OHAV}	—	-50	mA	*6
Power consumption	P _D	—	300	mW	
Operating temperature	T _A	-40	+85	°C	
Storage temperature	T _{stg}	-55	+150	°C	

*1: AV_{CC}, AVRH, AVRL, and DV_{CC} shall never exceed V_{CC}. AVRL shall never exceed AVRH.

*2: V_{CC} ≥ AV_{CC} ≥ DV_{CC} ≥ 3.0V

*3: V_I and V_O shall never exceed V_{CC} + 0.3 V.

*4: The maximum output current is a peak value for a corresponding pin.

*5: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*6: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

Note: Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	5.5	V	Normal operation (MB90522, MB90523)
	V_{CC}	4.0	5.5	V	Normal operation (MB90F523) Guaranteed frequency = 10 MHz at 4.0 V to 4.5V
	V_{CC}	3.0	5.5	V	Retains status at the time operation stops
Smoothing capacitor	C_S	0.1	1.0	μF	*
Operating temperature	T_A	-40	+85	$^{\circ}\text{C}$	

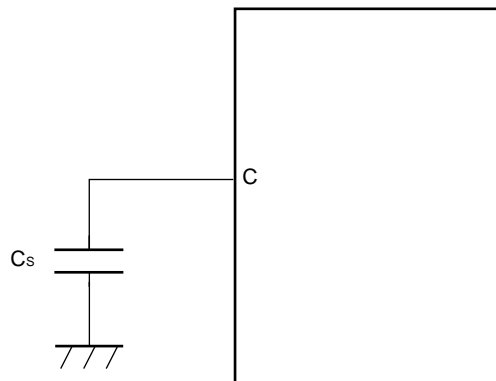
* : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S .

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

• C pin diagram



MB90520 Series

3. DC Characteristics

($V_{CC} = V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
“H” level input voltage	V_{IHS}	P20 to P27, P30 to P37, P53, P54, P70 to P77, P80 to P87, PA0 to PA7,	$V_{CC} = 3.0 \text{ V}$ to 5.5 V (MB90523)	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHM}	MD0 to MD2		$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
“L” level input voltage	V_{ILS}	P20 to P27, P30 to P37, P53, P54, P70 to P77, P80 to P87, PA0 to PA7,	$V_{CC} = 4.0 \text{ V}$ to 5.5 V (MB90F523)	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	
	V_{ILM}	MD0 to MD2		$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
“H” level output voltage	V_{OH}	Other than P90 to P97	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -2.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
“L” level output voltage	V_{OL}	All output pins	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 2.0 \text{ mA}$	—	—	0.4	V	
Open-drain output leakage current	I_{leak}	Output pin P90 to P97	—	—	0.1	5	μA	
Input leakage current	I_{IL}	Other than P90 to P97	$V_{CC} = 5.5 \text{ V}$, $V_{SS} < V_I < V_{CC}$	-5	—	5	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P40 to P47, \overline{RST} , MD0, MD1	—	15	30	100	$\text{k}\Omega$	
Pull-down resistance	R_{DOWN}	MD2	—	15	30	100	$\text{k}\Omega$	

(Continued)

MB90520 Series

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*	I_{CC}	V_{CC}	Internal operation at 16 MHz V_{CC} at 5.0 V	—	30	40	mA	MB90522, MB90523
	I_{CC}	V_{CC}	Normal operation	—	85	130	mA	MB90F523
	I_{CC}	V_{CC}	Internal operation at 16 MHz V_{CC} at 5.0 V	—	35	45	mA	MB90522, MB90523
	I_{CC}	V_{CC}	A/D converter operation	—	90	140	mA	MB90F523
	I_{CC}	V_{CC}	Internal operation at 16 MHz V_{CC} at 5.0 V	—	40	50	mA	MB90522, MB90523
	I_{CC}	V_{CC}	D/A converter operation	—	95	145	mA	MB90F523
	I_{CC}	V_{CC}	When data is written or erased in flash mode	—	95	140	mA	MB90F523
	I_{CCS}	V_{CC}	Internal operation at 16 MHz V_{CC} at 5.0 V	—	7	12	mA	MB90522, MB90523
	I_{CCS}	V_{CC}	In sleep mode	—	25	30	mA	MB90F523
	I_{CCL}	V_{CC}	Internal operation at 8 kHz V_{CC} at 5.0 V	—	0.1	1.0	mA	MB90522, MB90523
	I_{CCL}	V_{CC}	$T_A = +25^\circ\text{C}$ Subsystem operation	—	4	7	mA	MB90F523
	I_{CCLS}	V_{CC}	Internal operation at 8 kHz V_{CC} at 5.0 V	—	30	50	μA	MB90522, MB90523
	I_{CCLS}	V_{CC}	$T_A = +25^\circ\text{C}$ In subsleep mode	—	0.1	1	mA	MB90F523
	I_{CCT}	V_{CC}	Internal operation at 8 kHz V_{CC} at 5.0 V	—	15	30	μA	MB90522, MB90523
	I_{CCT}	V_{CC}	$T_A = +25^\circ\text{C}$ In clock mode	—	30	50	μA	MB90F523
	I_{CCH}	V_{CC}	$T_A = +25^\circ\text{C}$ In stop mode	—	5	20	μA	MB90522, MB90523
I_{CCH}	V_{CC}		—	0.1	10	μA	MB90F523	
Input capacitance	C_{IN}	Other than AV_{CC} , AV_{SS} , C, V_{CC} , V_{SS}	—	—	10	80	pF	

(Continued)

MB90520 Series

(Continued)

($A_{V_{CC}} = V_{CC} = 5.0 \text{ V} \pm 10\%$, $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
LCD split resistor	R_{LCD}	V0 to V1, V1 to V2, V2 to V3	—	50	100	200	$k\Omega$	
Output impedance for COM0 to COM3	R_{VCOM}	COM0 to COM3	V1 to V3 = 5.0 V	—	—	2.5	$k\Omega$	
Output impedance for SEG00 to SEG31	R_{VSEG}	SEG00 to SEG31		—	—	15	$k\Omega$	
LCDC leak current	I_{LCDC}	V0 to V3, COM1 to COM3, SEG00 to SEG31	—	—	—	± 5	μA	

* : The current value is preliminary and may be subject to change for enhanced characteristics without previous notice. The power supply current is measured with an external clock.

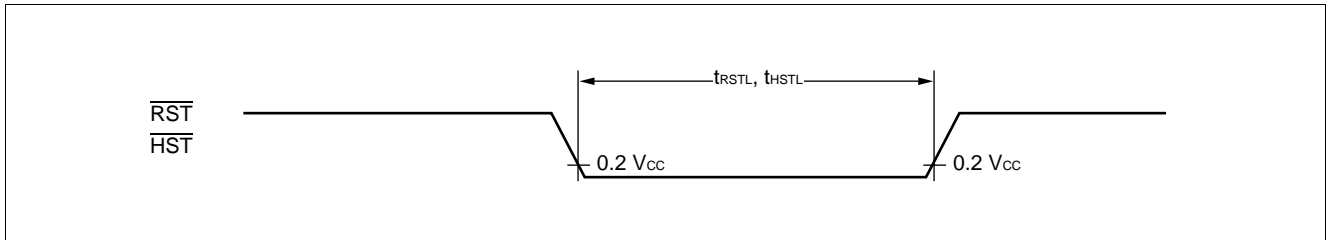
4. AC Characteristics

(1) Reset, Hardware Standby Input Timing

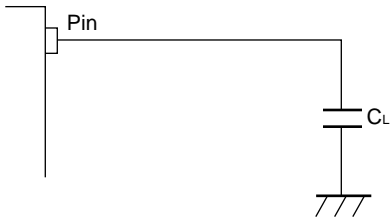
($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	\overline{RST}	—	$4 t_{CP}^*$	—	ns	
Hardware standby input time	t_{HSTL}	\overline{HST}	—	$4 t_{CP}^*$	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”



• Measurement conditions for AC ratings



C_L is a load capacitance connected to a pin under test.
 C_L of 80 pF must be connected to address data bus (AD15 to AD00).

MB90520 Series

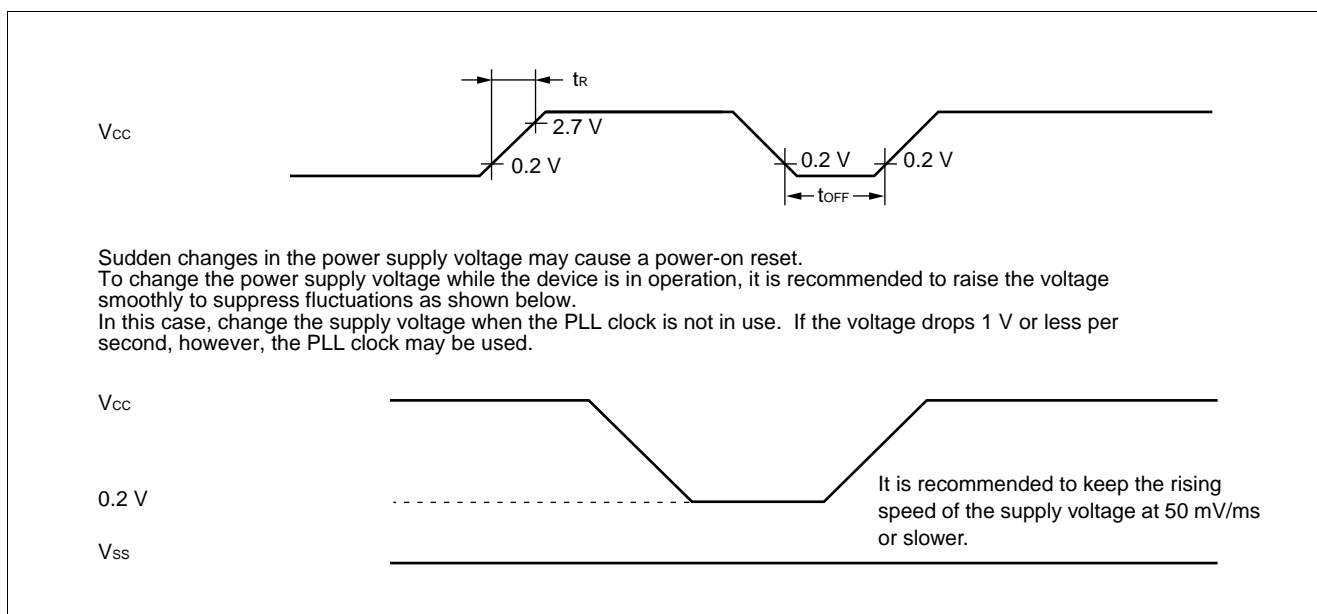
(2) Specification for Power-on Reset

($A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	—	0.05	30	ms	*
Power supply cut-off time	t_{OFF}	V_{CC}	—	4	—	ms	Due to repeated operations

* : V_{CC} must be kept lower than 0.2 V before power-on.

- Notes:
- The above ratings are values for causing a power-on reset.
 - There are internal registers which can be initialized only by a power-on reset. Apply power according to this rating to ensure initialization of the registers.

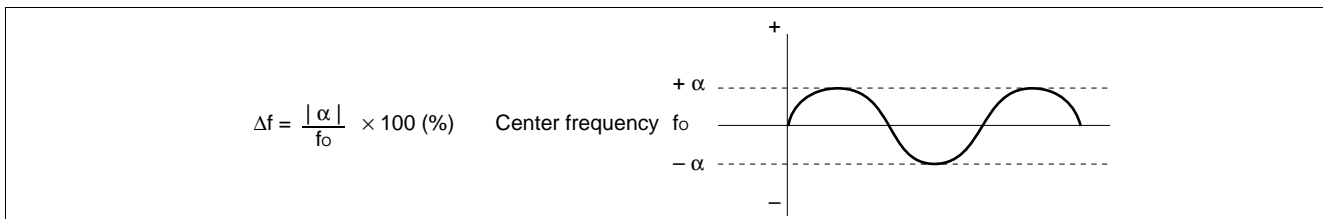


(3) Clock Timings

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F _C	X0, X1	—	3	—	16	MHz	
	F _C	X0, X1	4.0 V to 4.5 V	3	—	10	MHz	MB90F523
	F _{CL}	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	t _{H CYL}	X0, X1	—	62.5	—	333	ns	
	t _{H CYL}	X0, X1	4.0 V to 4.5 V	100	—	333	ns	MB90F523
	t _{L CYL}	X0A, X1A	—	—	30.5	—	μs	
Input clock pulse width	P _{WH} , P _{WL}	X0	—	10	—	—	ns	Recommended duty ratio of 30% to 70%
	P _{WLH} , P _{WLL}	X0A	—	—	15.2	—	μs	
Input clock rising/falling time	t _{CR} , t _{CF}	X0, X0A	—	—	—	5	ns	External clock operation
Internal operating clock frequency	f _{CP}	—	—	1.5	—	16	MHz	When the main clock is used
	f _{CP}	—	4.0 V to 4.5 V	1.5	—	10	MHz	When the main clock is used
	f _{LCP}	—	—	—	8.192	—	kHz	When the subclock is used
Internal operating clock cycle time	t _{CP}	—	—	62.5	—	333	ns	When the main clock is used
	t _{CP}	—	4.0 V to 4.5 V	100	—	333	ns	When the main clock is used
	t _{LCP}	—	—	—	122.1	—	μs	When the subclock is used
Frequency fluctuation rate locked	Δf	—	—	—	—	5	%	*

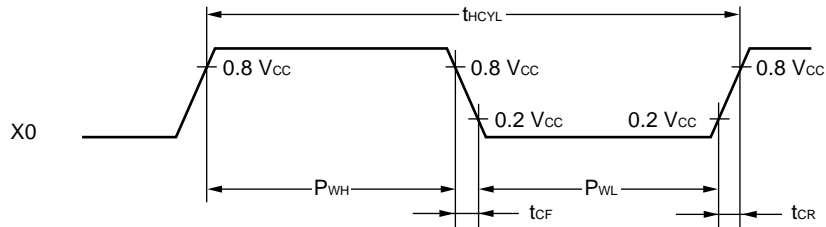
* : The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.



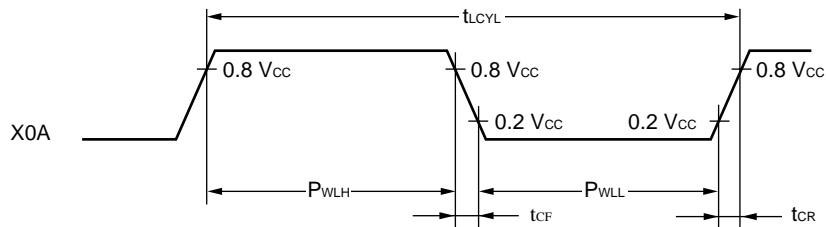
The PLL frequency deviation changes periodically from the preset frequency “(about CLK × (1CYC to 50 CYC),” thus minimizing the chance of worst values to be repeated (errors are minimal and negligible for pulses with long intervals).

MB90520 Series

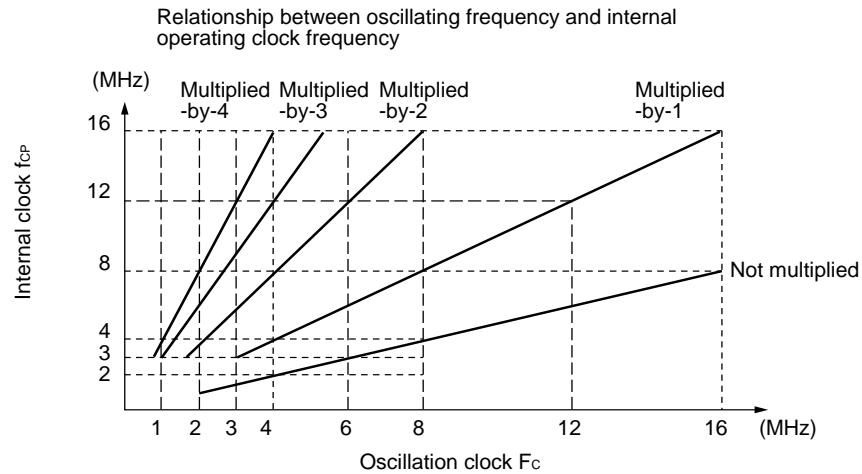
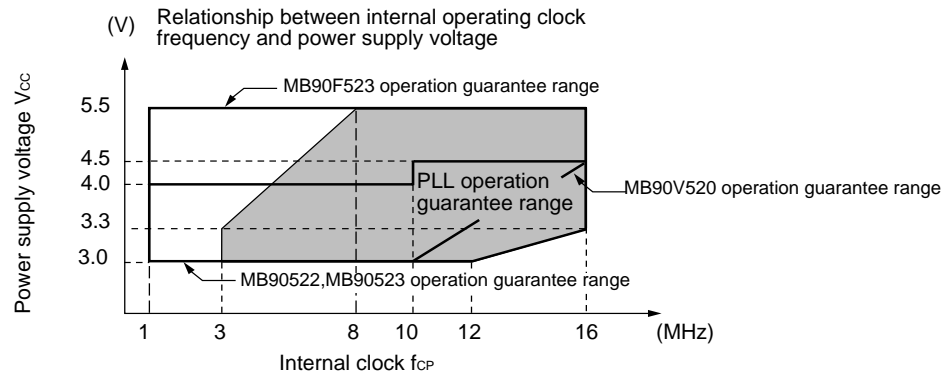
• X0, X1 clock timing



• X0A, X1A clock timing



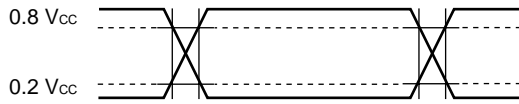
• PLL operation guarantee range



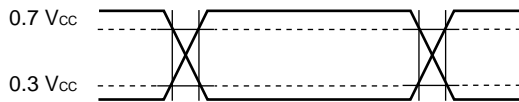
The AC ratings are measured for the following measurement reference voltages.

- **Input signal waveform**

Hysteresis input pin

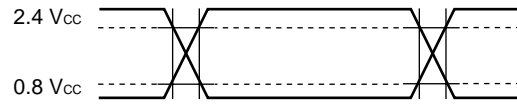


Pins other than hysteresis input/MD input



- **Output signal waveform**

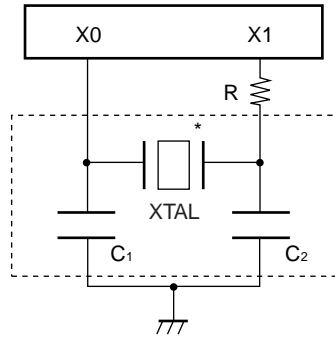
Hysteresis input pin



MB90520 Series

(4) Recommended Resonator Manufacturers

- Sample application of ceramic resonator



- Mask ROM product (MB90522, MB90523)

Resonator manufacturer	Resonator	Frequency (MHz)	C ₁ (pF)	C ₂ (pF)	R
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	Not required
	CSA4.00MG040	4.00	100	100	Not required
	CSA8.00MTZ	8.00	30	30	Not required
	CSA16.00MXZ040	16.00	15	15	Not required
	CSA32.00MXZ040	32.00	5	5	Not required
TDK Corporation	CCR3.52MC3 to CCR6.96MC3	3.52 to 6.96	Built-in	Built-in	Not required
	CCR7.0MC5 to CCR12.0MC5	7.00 to 12.00	Built-in	Built-in	Not required
	CCR20.0MSC6 to CCR32.0MSC6	20.00 to 32.00	Built-in	Built-in	Not required

(Continued)

MB90520 Series

(Continued)

• Flash ROM product (MB90F523)

Resonator manufacturer	Resonator	Frequency (MHz)	C ₁ (pF)	C ₂ (pF)	R
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	Not required
	CSA4.00MG040	4.00	100	100	Not required
	CSA8.00MTZ	8.00	30	30	Not required
	CSA16.00MXZ040	16.00	15	15	Not required
	CSA32.00MXZ040	32.00	5	5	Not required
TDK Corporation	CCR3.52MC3 to CCR6.96MC3	3.52 to 6.96	Built-in	Built-in	Not required
	CCR7.0MC5 to CCR12.0MC5	7.0 to 12.0	Built-in	Built-in	Not required
	CCR20.0MSC6 to CCR32.0MSC6	20.0 to 32.0	Built-in	Built-in	Not required

Inquiry: Murata Mfg. Co., Ltd..

- Murata Electronics North America, Inc.: TEL 1-404-436-1300
- Murata Europe Management GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.): TEL 65-758-4233

TDK Corporation

- TDK Corporation of America
Chicago Regional Office: TEL 1-708-803-6100
- TDK Electronics Europe GmbH
Components Division: TEL 49-2102-9450
- TDK Singapore (PTE) Ltd.: TEL 65-273-5022
- TDK Hong Kong Co., Ltd.: TEL 852-736-2238
- Korea Branch, TDK Corporation: TEL 82-2-554-6636

MB90520 Series

(5) UART (SCI) Timing

($V_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

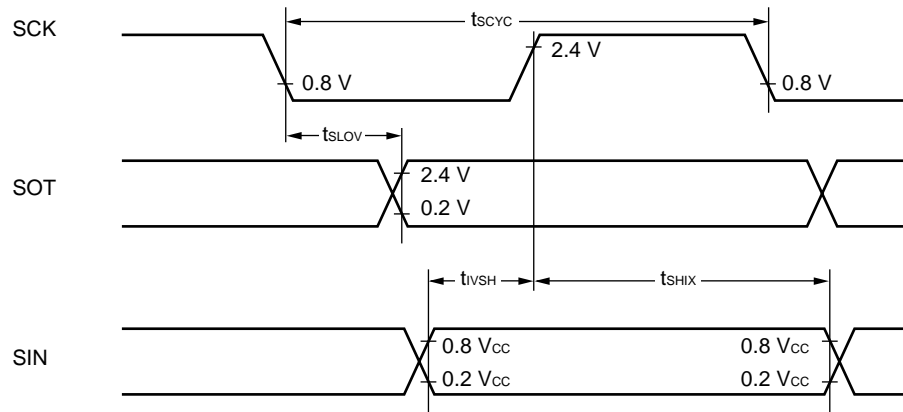
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t _{SCYC}	SCK0 to SCK2	Internal shift clock mode C _L = 80 pF + 1 TTL for an output pin	8 t _{CP} *	—	ns	
SCK ↓ → SOT delay time	t _{SLOV}	SCK0 to SCK2, SOT0 to SOT2		- 80	80	ns	
Valid SIN → SCK ↑	t _{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK ↑ → valid SIN hold time	t _{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0 to SCK2	External shift clock mode C _L = 80 pF + 1 TTL for an output pin	4 t _{CP} *	—	ns	
Serial clock "L" pulse width	t _{SLSH}	SCK0 to SCK2		4 t _{CP} *	—	ns	
SCK ↓ → SOT delay time	t _{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN → SCK ↑	t _{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK ↑ → valid SIN hold time	t _{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to "(3) Clock Timings."

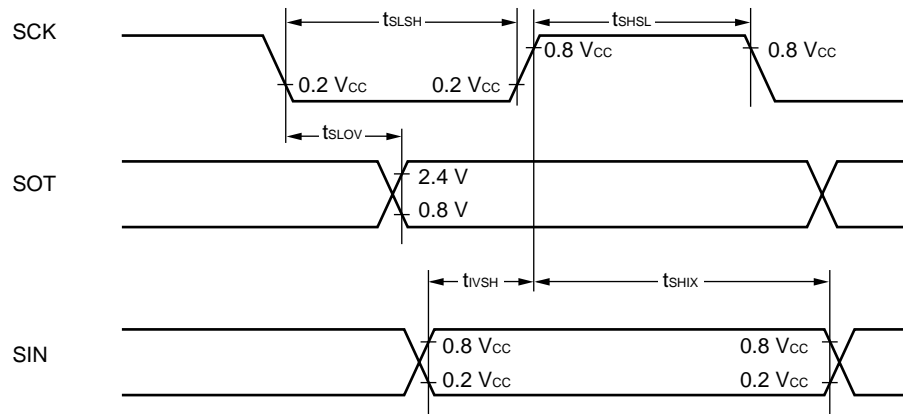
Notes: • These are AC ratings in the CLK synchronous mode.

- C_L is the load capacitor value connected to pins while testing.

- Internal shift clock mode



- External shift clock mode



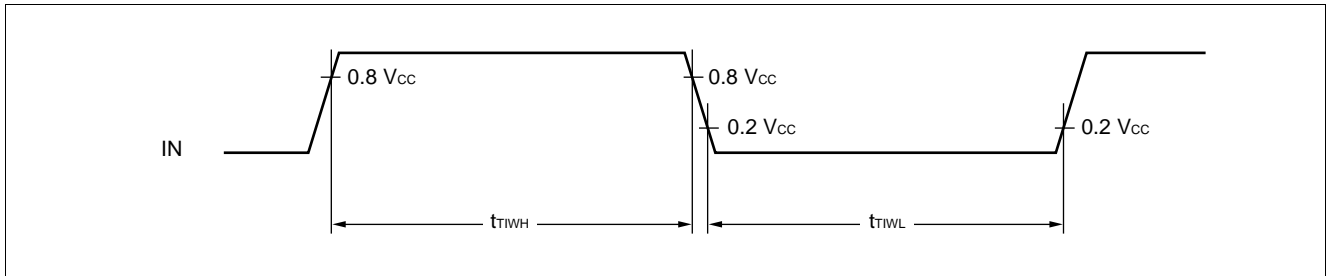
MB90520 Series

(6) Timer Input Timing

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH} , t_{TIWL}	IC00,IC01,IC10, IC11,TI0, TI1	—	$4 t_{CP}^*$	—	ns	

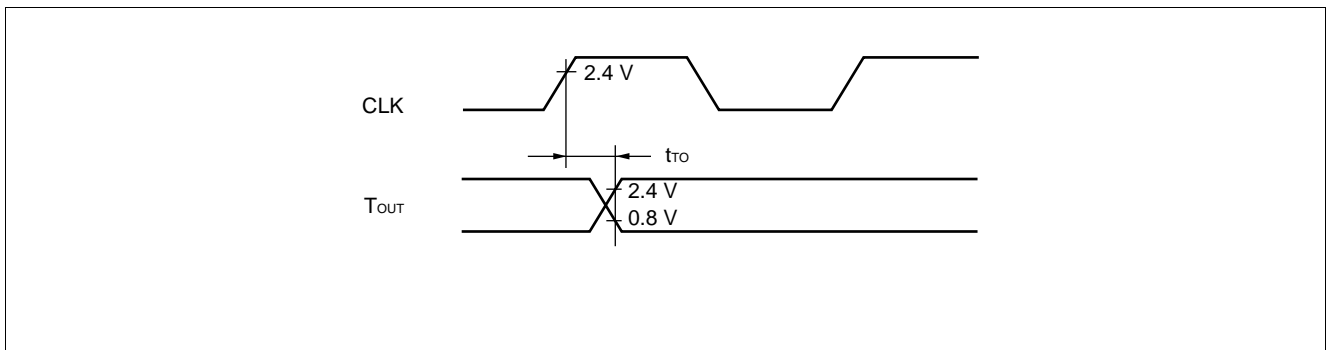
* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”



(7) Timer Output Timing

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK \uparrow \rightarrow T_{OUT} transition time	t_{TO}	OUT0 to OUT3, PG00, PG01,PG10, PG11	—	30	—	ns	



5. A/D Converter

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $3.0\text{ V} \leq AVR_H - AVR_L$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution	—	—	—	—	8/10	—	bit
Total error	—	—		—	—	± 5.0	LSB
Non-linear error	—	—		—	—	± 2.5	LSB
Differential linearity error	—	—		—	—	± 1.9	LSB
Zero transition voltage	V_{OT}	AN0 to AN7		AV_{SS} -3.5 LSB	+0.5 LSB	AV_{SS} +4.5 LSB	mV
Full-scale transition voltage	V_{FST}	AN0 to AN7		$AVRH$ -6.5 LSB	$AVRH$ -1.5 LSB	$AVRH$ +1.5 LSB	mV
Conversion time	—	—	$V_{CC} = 5.0\text{ V} \pm 10\%$ at machine clock of 16 MHz	240 t_{CP}^*	—	—	ns
Sampling time	—	—	$V_{CC} = 5.0\text{ V} \pm 10\%$ at machine clock of 16 MHz	64 t_{CP}^*	—	—	ns
Analog port input current	I_{AIN}	AN0 to AN7	—	—	—	10	μA
Analog input voltage	V_{AIN}	AN0 to AN7		$AVRL$	—	$AVRH$	V
Reference voltage	—	$AVRH$		$AVRL$ + 2.7	—	AV_{CC}	V
	—	$AVRL$		0	—	$AVRH$ -2.7	V
Power supply current	I_A	AV_{CC}		—	5	—	mA
	I_{AH}	AV_{CC}		Supply current when CPU stopped and 8/10-bit A/D converter not in operation ($V_{CC} = AV_{CC} = AVR_H = 5.0\text{ V}$)	—	—	5
Reference voltage supply current	I_R	$AVRH$	—	—	400	—	μA
	I_{RH}	$AVRH$	Supply current when CPU stopped and 8/10-bit A/D converter not in operation ($V_{CC} = AV_{CC} = AVR_H = 5.0\text{ V}$)	—	—	5	μA
Offset between channels	—	AN0 to AN7	—	—	—	4	LSB

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”

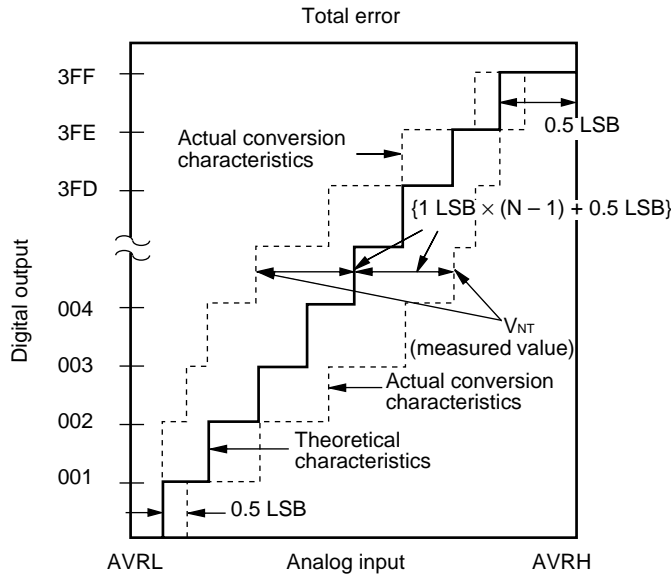
6. A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error, full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{AVRH - AVRL}{1024} \text{ [V]}$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

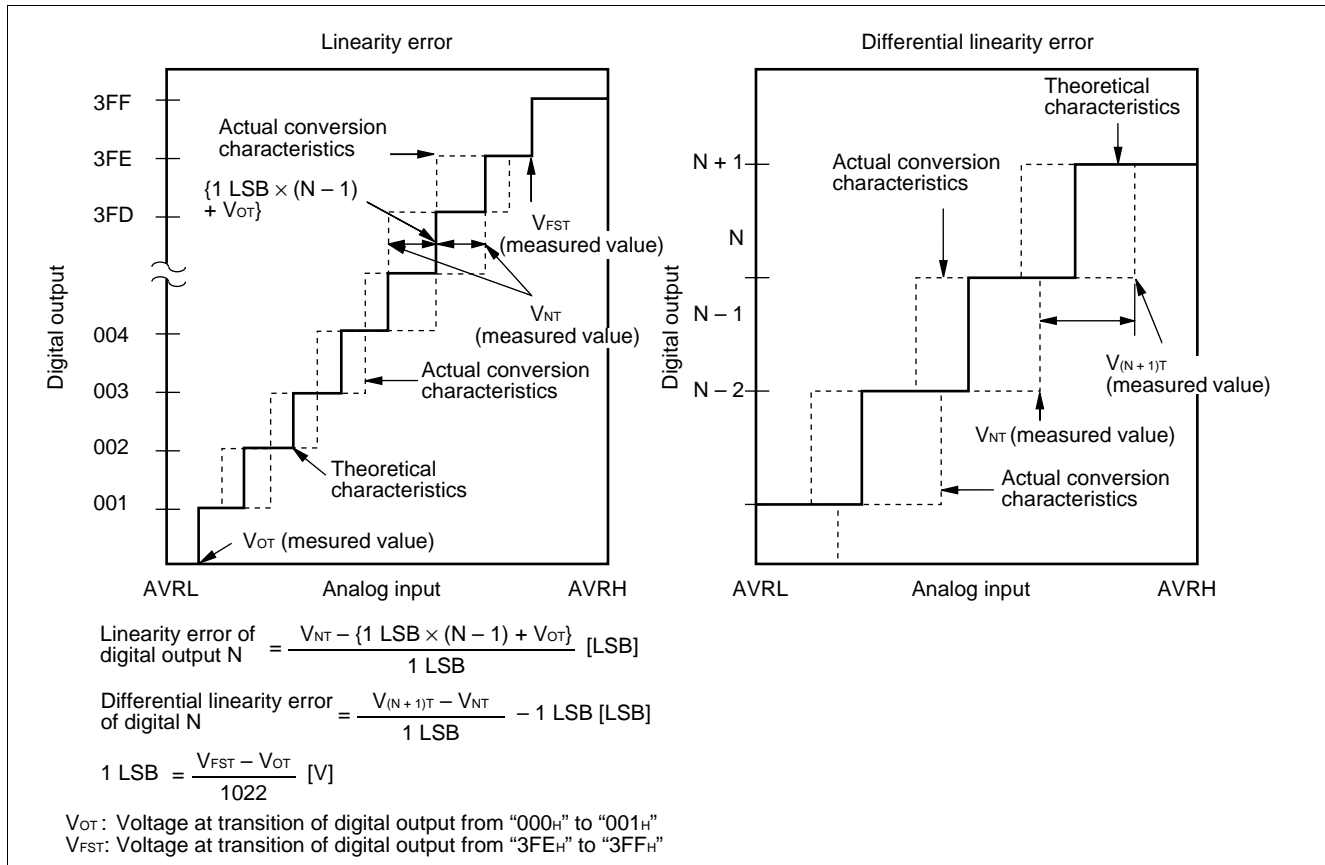
$$V_{OT} (\text{Theoretical value}) = AVRL + 0.5 \text{ LSB [V]}$$

V_{NT} : Voltage at a transition of digital output from (N - 1) to N

$$V_{FST} (\text{Theoretical value}) = AVRH - 1.5 \text{ LSB [V]}$$

(Continued)

(Continued)



7. Notes for A/D Conversion

Analog inputs should have external circuit impedance of approximately 5 kΩ or less.

External capacitance, if used, should be several thousand times the level of the chip's internal capacitance in consideration of the effects of partial potential between the external and internal capacitance.

If the impedance of the external circuit is too high, the analog voltage sampling interval may be insufficient (using a sampling interval of 4.00 μs and a machine clock frequency of 16 MHz).

• Block diagram of analog input circuit model



MB90522, MB90523
 R_{ON} : Approx. 1.5 kΩ
 C: Approx. 30 pF
 MB90F523
 R_{ON} : Approx. 3.0 kΩ
 C: Approx. 65 pF

Note: Listed values must be considered standards.

• Error

The smaller $|AVRH - AVRL|$ is, the greater the error is.

MB90520 Series

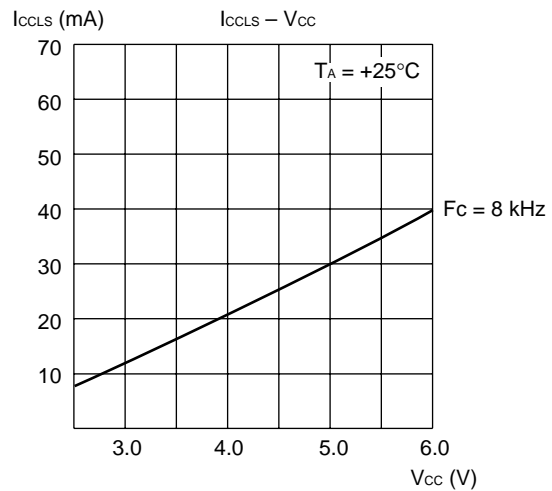
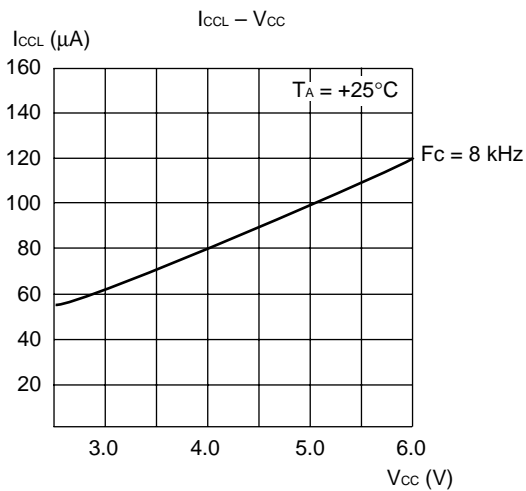
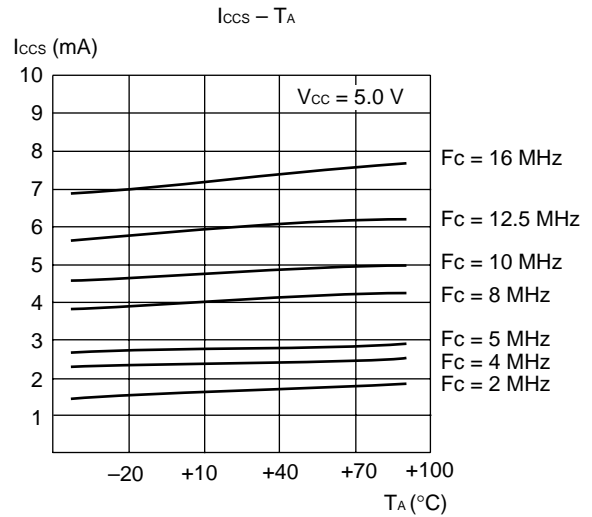
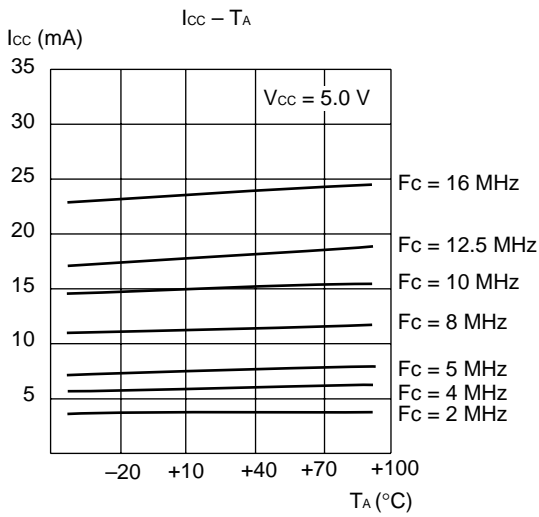
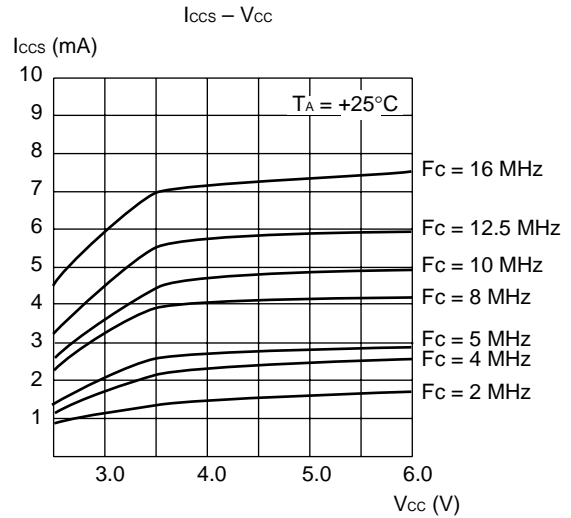
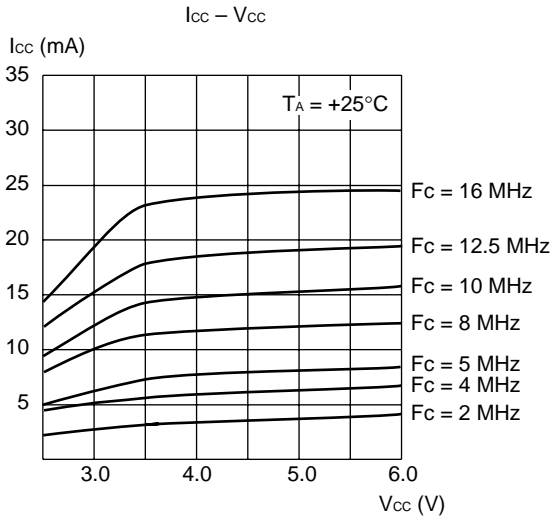
8. D/A Converter

($A_{V_{CC}} = V_{CC} = 5.0 \text{ V} \pm 10\%$, $A_{V_{SS}} = V_{SS} = DV_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

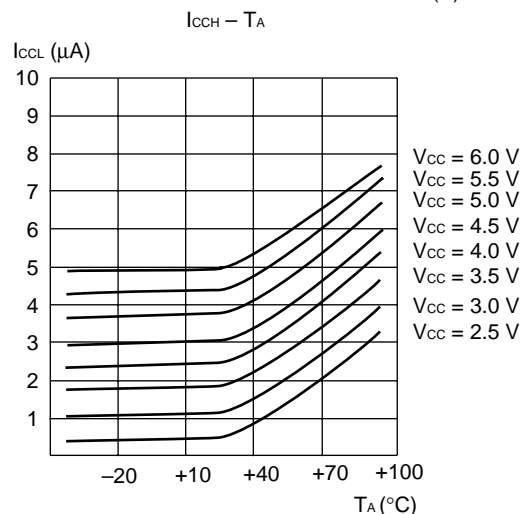
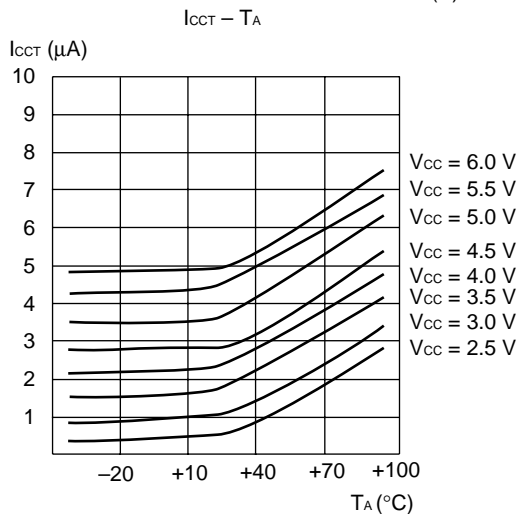
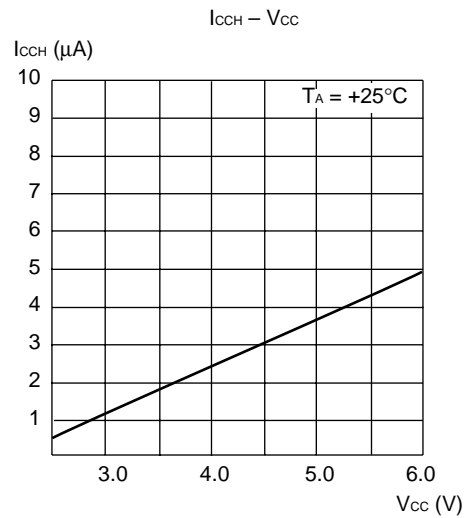
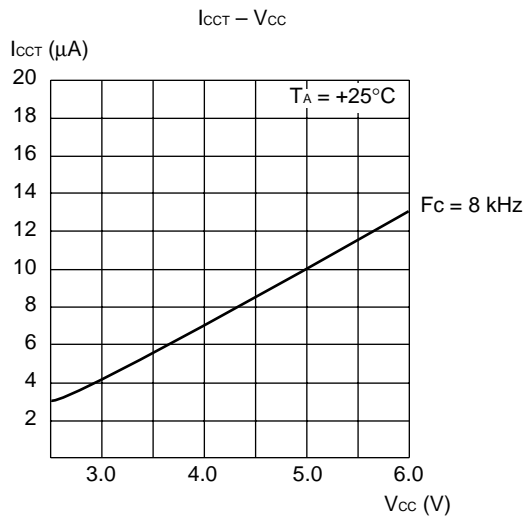
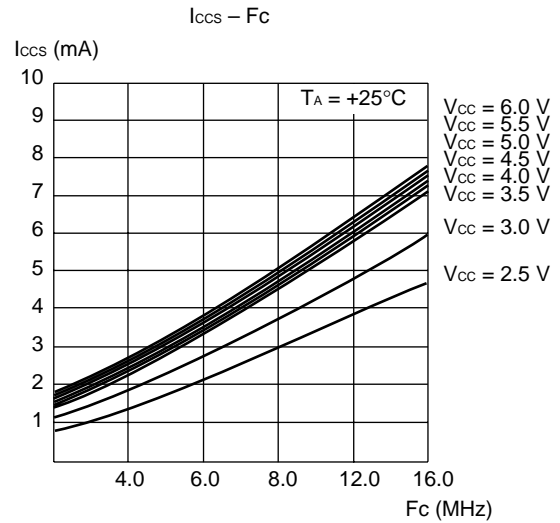
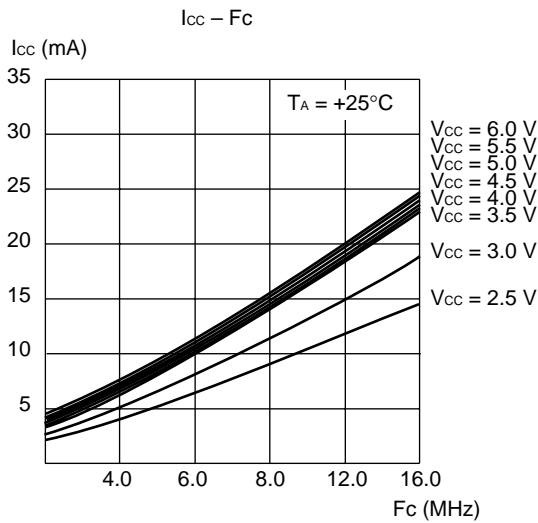
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	8	—	bit	
Differential linearity error	—	—	—	—	± 0.9	LSB	
Absolute accuracy	—	—	—	—	± 1.2	%	
Linearity error	—	—	—	—	± 1.5	LSB	
Conversion time	—	—	—	10	20	μs	Load capacitance: 20 pF
Analog reference voltage	—	DV _{CC}	$V_{SS} + 3.0$	—	$A_{V_{CC}}$	V	
Reference voltage supply current	I _{DVR}	DV _{CC}	—	—	300	μA	
	I _{DVRS}	DV _{CC}	—	—	10	μA	In sleep mode
Analog output impedance	—	—	—	20	—	k Ω	

EXAMPLE CHARACTERISTICS

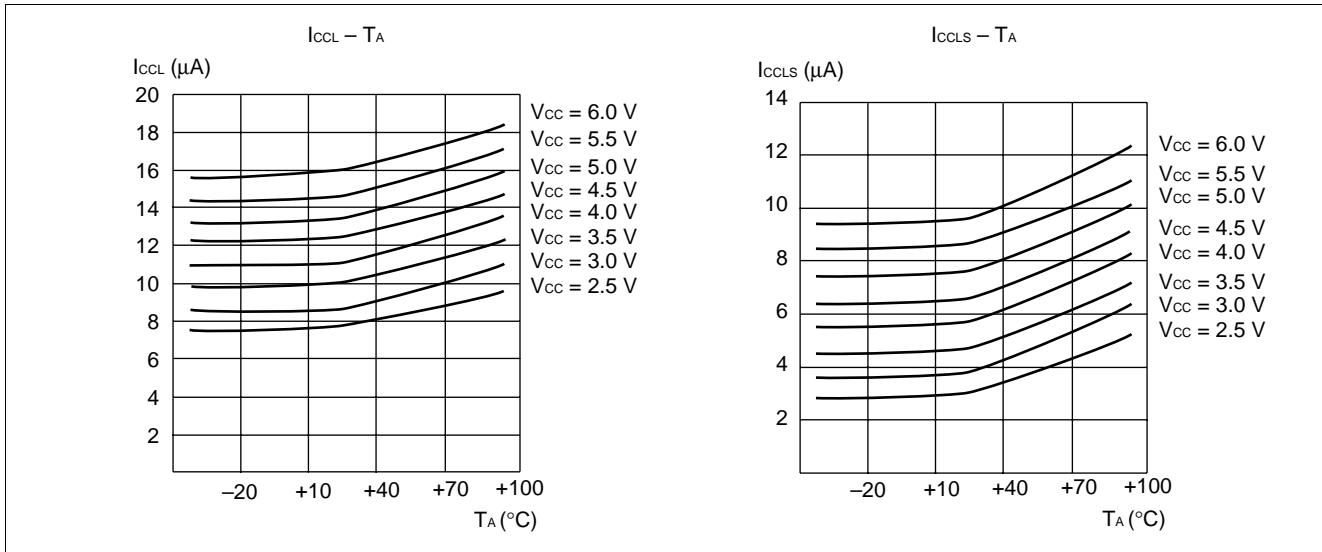
(1) Power Supply Current (MB90523)



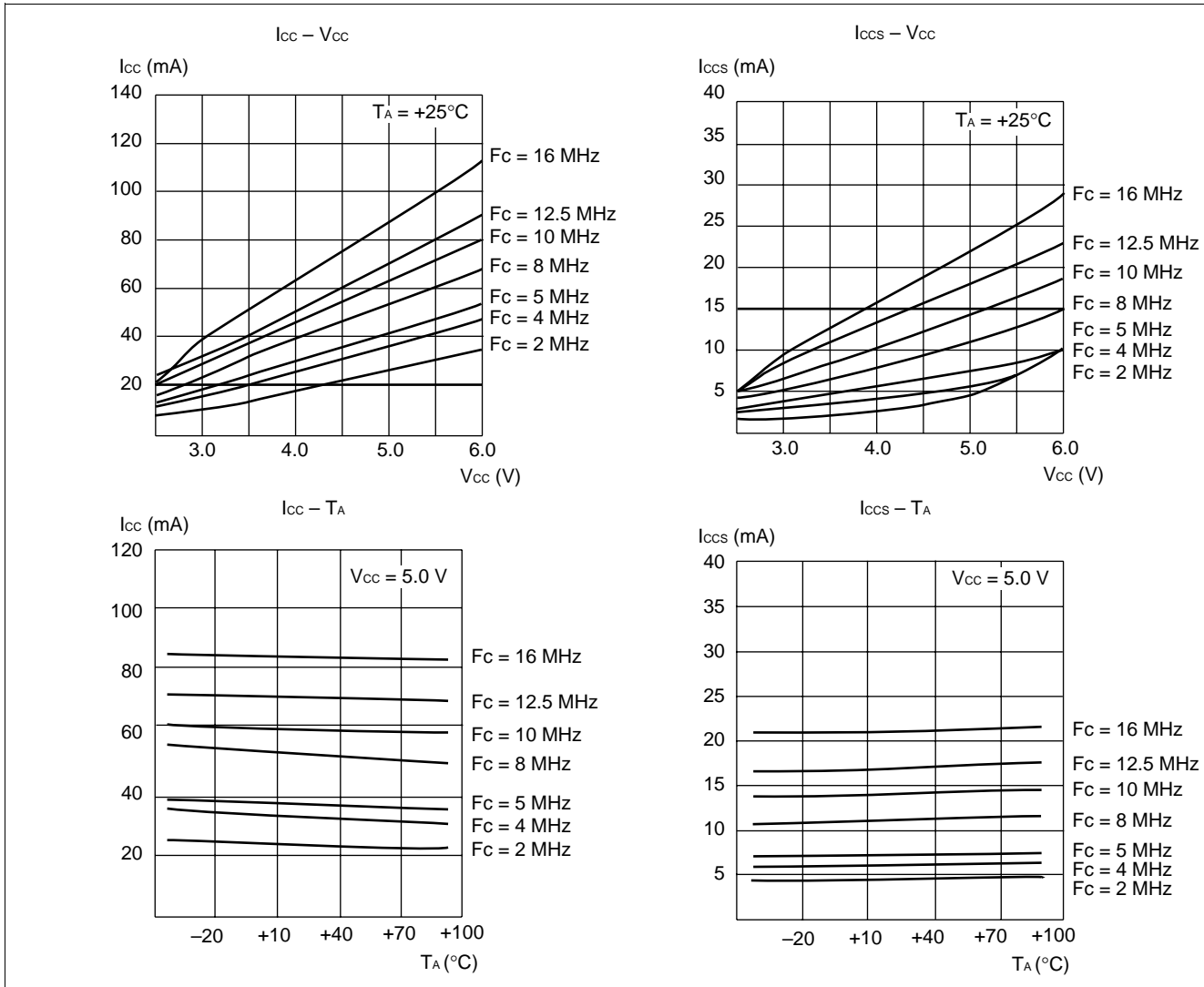
MB90520 Series



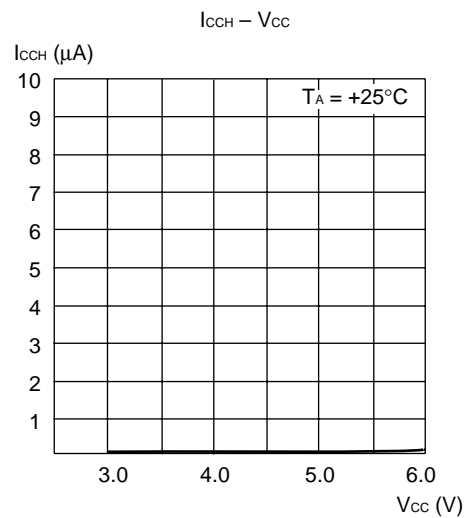
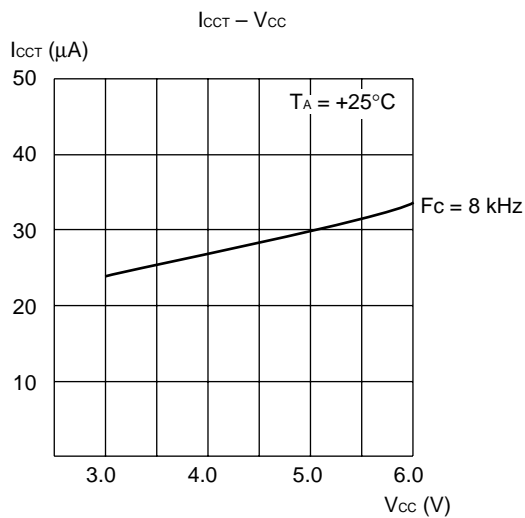
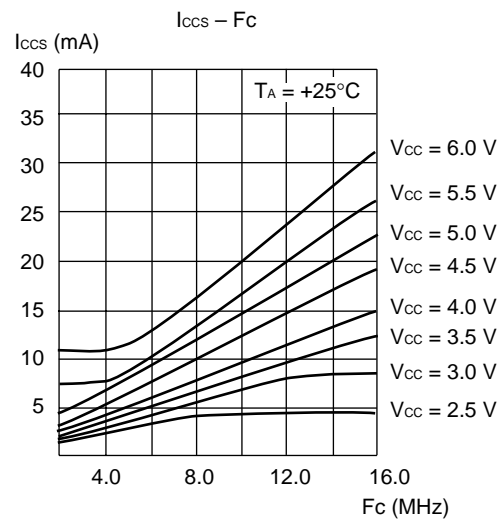
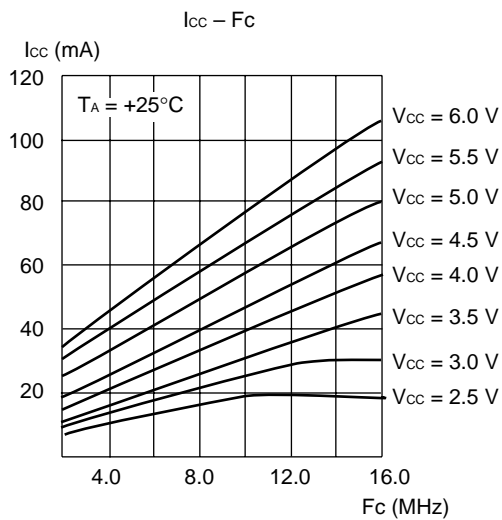
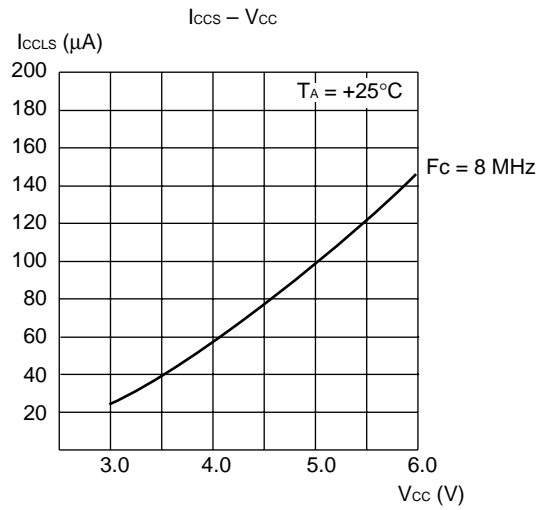
MB90520 Series



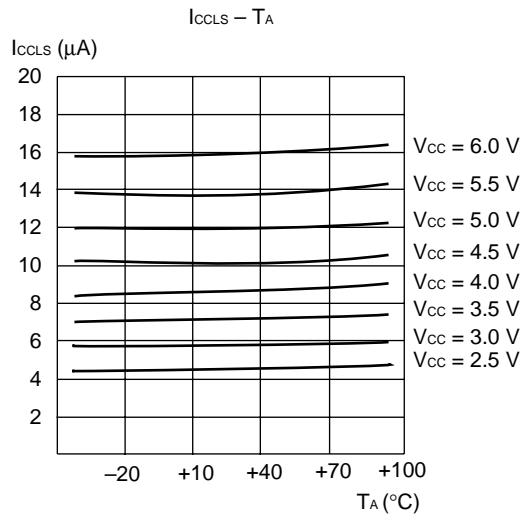
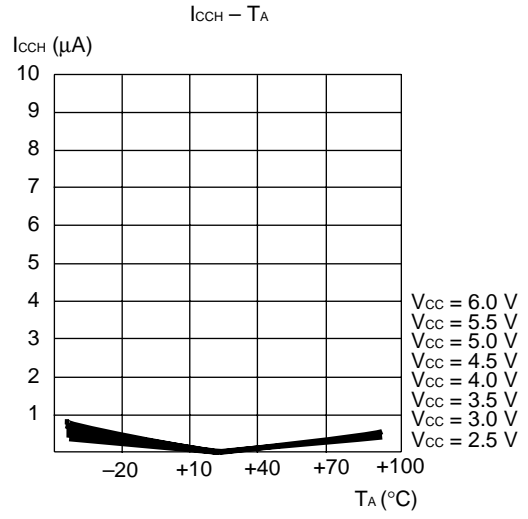
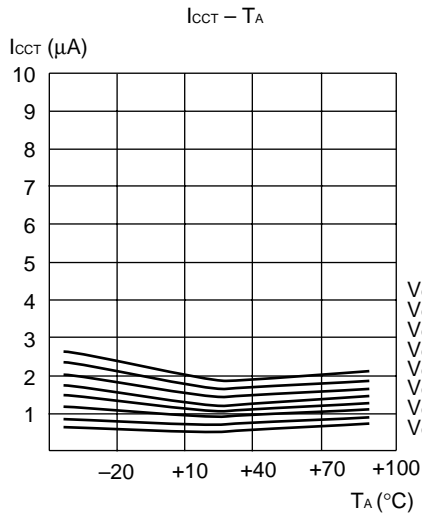
(2) Power Supply Current (MB90F523)



MB90520 Series



MB90520 Series



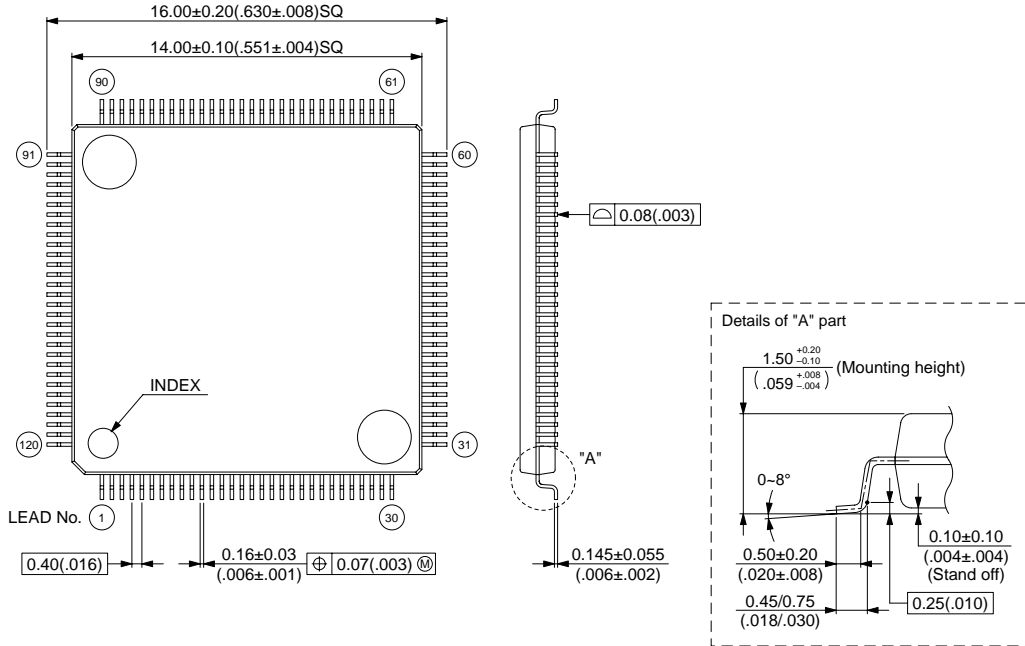
MB90520 Series

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90523PFF MB90522PFF MB90F523PFF	120-pin Plastic LQFP (FPT-120P-M05)	
MB90523PFV MB90522PFV MB90F523PFV	120-pin Plastic QFP (FPT-120P-M13)	

PACKAGE DIMENSIONS

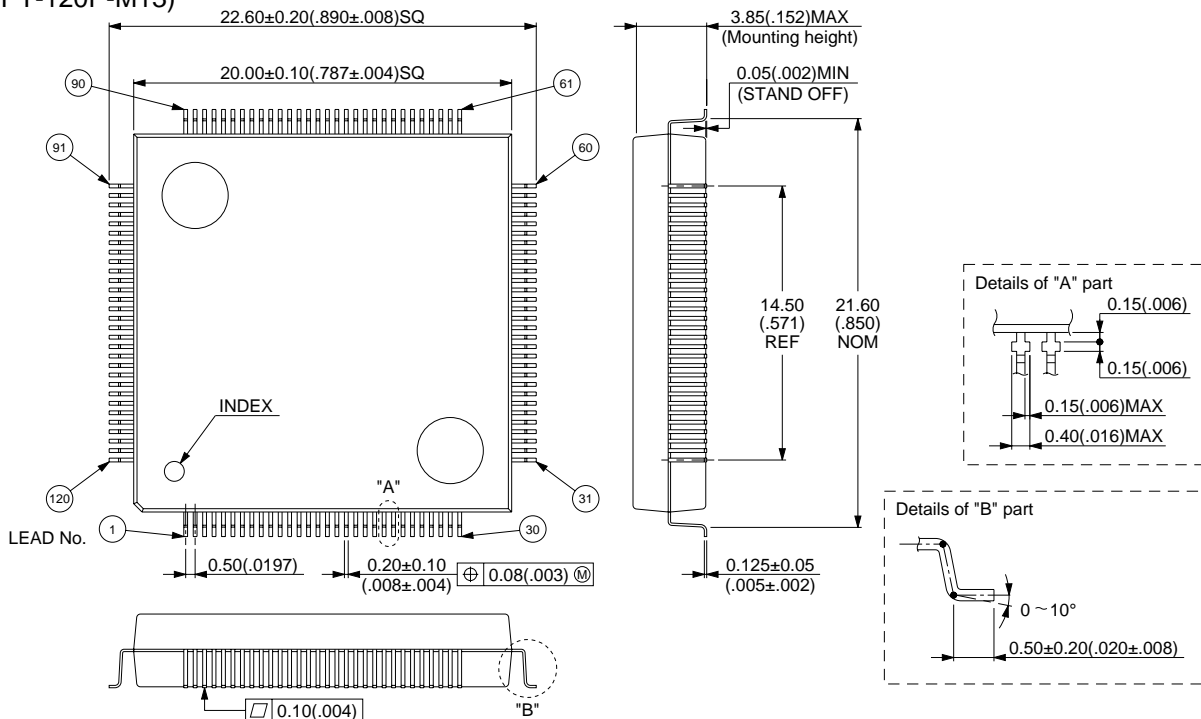
120-pin Plastic LQFP
(FPT-120P-M05)



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Dimensions in mm (inches)

120-pin Plastic QFP
(FPT-120P-M13)



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Dimensions in mm (inches)

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