

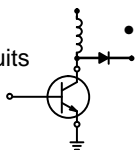
Designer's™ Data Sheet

SWITCHMODE Series

NPN Silicon Power Transistors

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16012 and MJW16012 are selected high gain versions of the MJ16010 and MJW16010 for applications where drive current is limited.

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times — $T_C = 100^\circ\text{C}$
 - 50 ns Inductive Fall Time (Typ)
 - 90 ns Inductive Crossover Time (Typ)
 - 800 ns Inductive Storage Time (Typ)
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



MAXIMUM RATINGS

Rating	Symbol	MJ16010 MJ16012	MJW16010 MJW16012	Unit
Collector-Emitter Voltage	V_{CEO}	450		Vdc
Collector-Emitter Voltage	V_{CEV}	850		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	15		Adc
— Peak (1)	I_{CM}	20		
Base Current — Continuous	I_B	10		Adc
— Peak (1)	I_{BM}	15		
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$ Derate above 25°C	P_D	1.75 100 1.0	135 53.8 1.11	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	0.93	$^\circ\text{C}/\text{W}$
Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	T_L	275		$^\circ\text{C}$

(1) Pulse Test: Pulse Width $\leq 50 \mu\text{s}$, Duty Cycle $\geq 10\%$

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

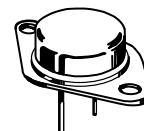
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REV 2

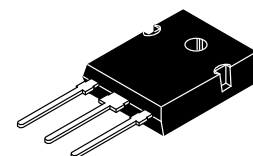
MJ16010
MJW16010
MJ16012*
MJW16012*

*Motorola Preferred Device

15 AMPERE
NPN SILICON
POWER TRANSISTORS
450 VOLTS
135 AND 175 WATTS



CASE 1-07
TO-204AA
(TO-3)
MJ16010
MJ16012



CASE 340F-03
TO-247AE
MJW16010
MJW16012

MJ16010 MJW16010 MJ16012 MJW16012

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 2) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	450	—	—	Vdc
Collector Cutoff Current (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current (V _{CE} = 850 Vdc, R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)	I _{EBO}	—	—	10	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector–Emitter Saturation Voltage (I _C = 5.0 Adc, I _B = 0.7 Adc) (I _C = 10 Adc, I _B = 1.3 Adc) (I _C = 10 Adc, I _B = 1.3 Adc, T _C = 100°C)	V _{CE(sat)}	—	—	2.5 3.0 3.0	Vdc
Base–Emitter Saturation Voltage (I _C = 10 Adc, I _B = 1.3 Adc) (I _C = 10 Adc, I _B = 1.3 Adc, T _C = 100°C)	V _{BE(sat)}	—	—	1.5 1.5	Vdc
DC Current Gain (I _C = 15 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	5.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	—	—	400	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	(I _C = 10 Adc, V _{CC} = 250 Vdc, I _{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I _{B2} = 2.6 Adc, R _{B2} = 1.6 Ω)	t _d	—	20	—	ns
Rise Time			t _r	—	200	—	
Storage Time			t _s	—	1200	—	
Fall Time		t _f	—	200	—		
Storage Time		t _s	—	650	—		
Fall Time		t _f	—	80	—		
Inductive Load (Table 2)							
Storage Time	(I _C = 10 Adc, I _{B1} = 1.3 Adc, V _{BE(off)} = 5.0 Vdc, V _{CE(pk)} = 400 Vdc)	(T _C = 100°C)	t _{sv}	—	800	1800	ns
Fall Time			t _{fi}	—	50	200	
Crossover Time			t _c	—	90	250	
Storage Time		t _{sv}	—	1050	—		
Fall Time		t _{fi}	—	70	—		
Crossover Time		t _c	—	120	—		

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	10	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector–Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.7\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	2.5 3.0 3.0	Vdc
Base–Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5 1.5	Vdc
DC Current Gain ($I_C = 15\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	400	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	$(I_C = 10\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 1.0\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 2.0\text{ Adc}$, $R_{B2} = 1.6\ \Omega)$	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	900	—	
Fall Time		t_f	—	150	—		
Storage Time		$(V_{BE(off)} = 5.0\text{ Vdc})$	t_s	—	500	—	
Fall Time			t_f	—	40	—	
Inductive Load (Table 2)							
Storage Time	$(I_C = 10\text{ Adc}$, $I_{B1} = 1.0\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_C = 100^\circ\text{C})$	t_{sv}	—	650	1500	ns
Fall Time			t_{fi}	—	30	150	
Crossover Time			t_c	—	50	200	
Storage Time		$(T_C = 150^\circ\text{C})$	t_{sv}	—	850	—	
Fall Time			t_{fi}	—	30	—	
Crossover Time			t_c	—	70	—	

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$

TYPICAL STATIC CHARACTERISTICS

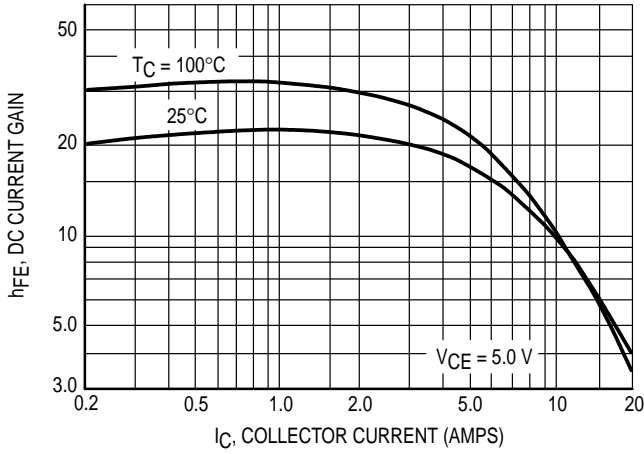


Figure 1. DC Current Gain

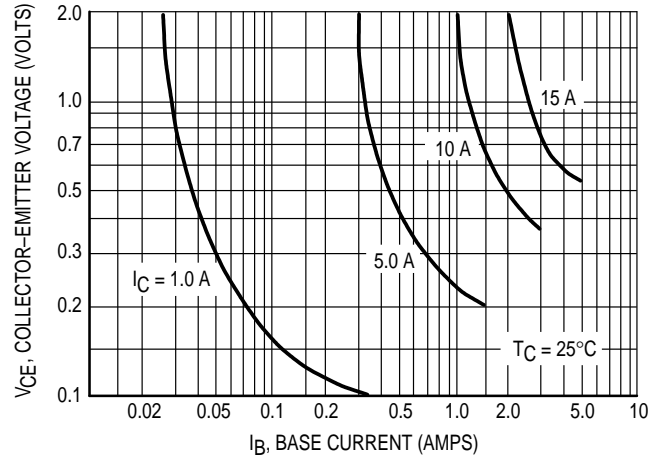


Figure 2. Collector Saturation Region

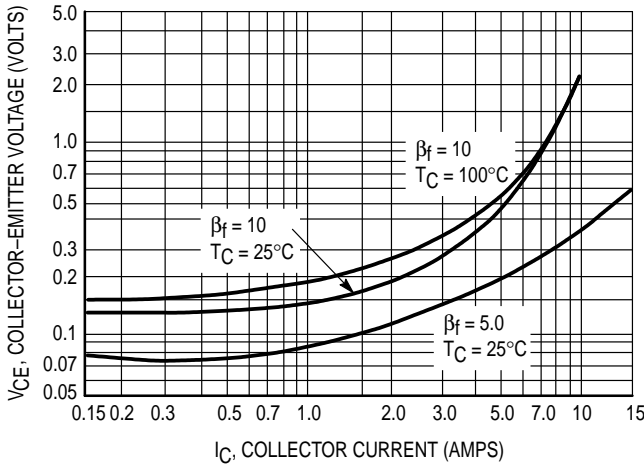


Figure 3. Collector-Emitter Saturation Voltage

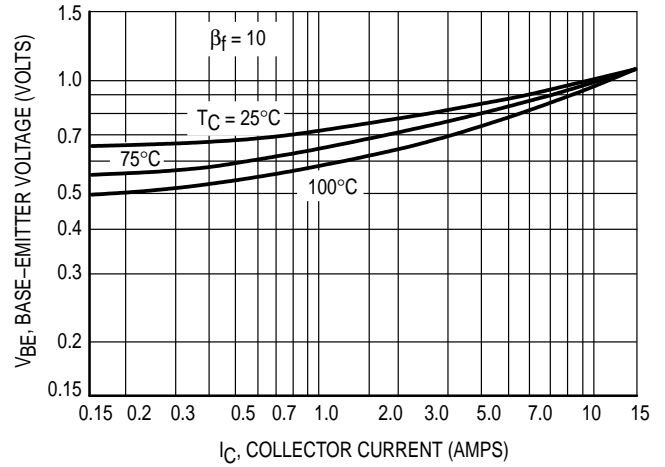


Figure 4. Base-Emitter Voltage

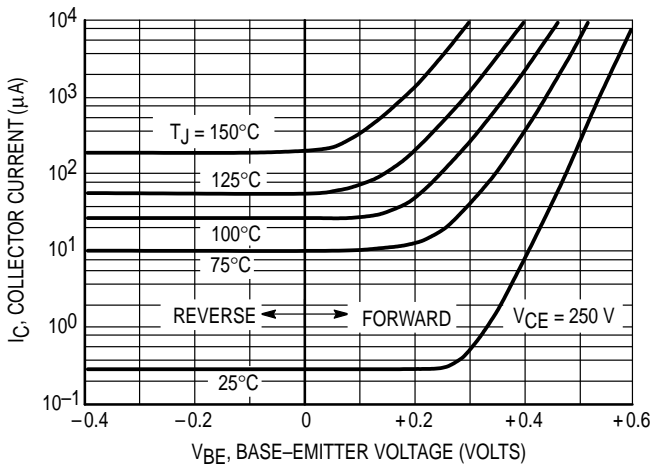


Figure 5. Collector Cutoff Region

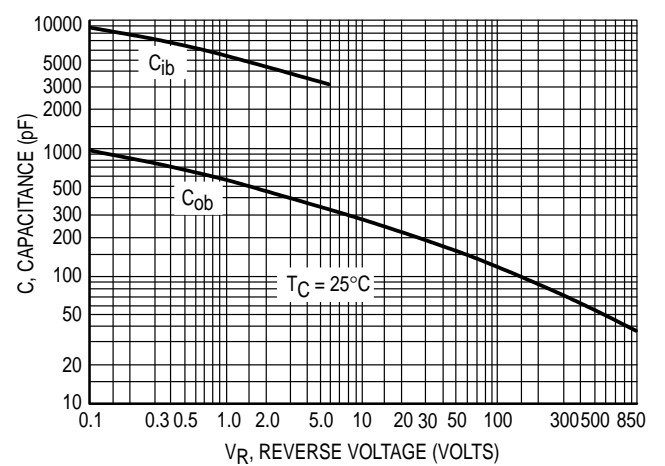


Figure 6. Capacitance

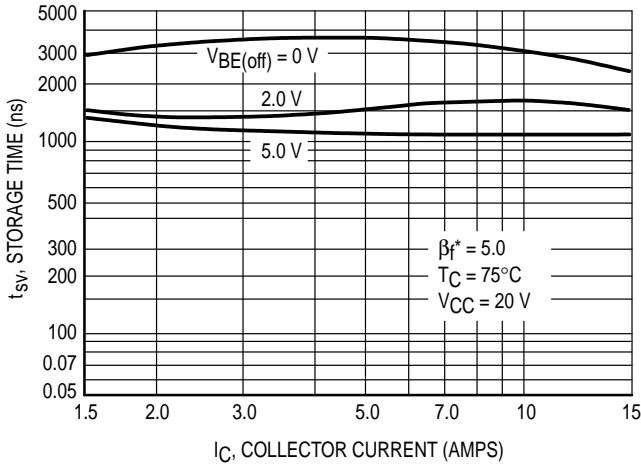


Figure 7. Storage Time

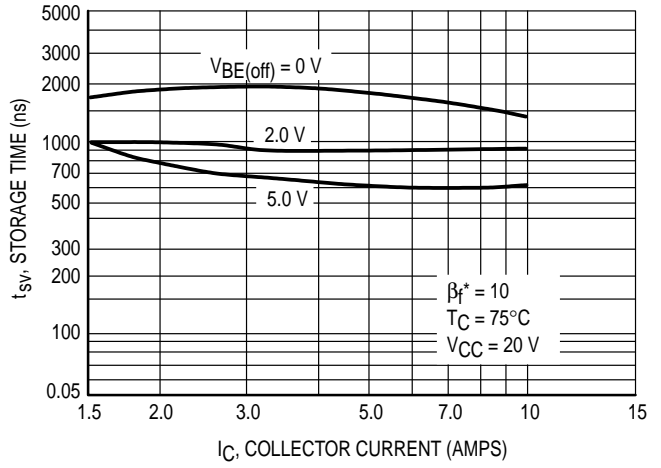


Figure 8. Storage Time

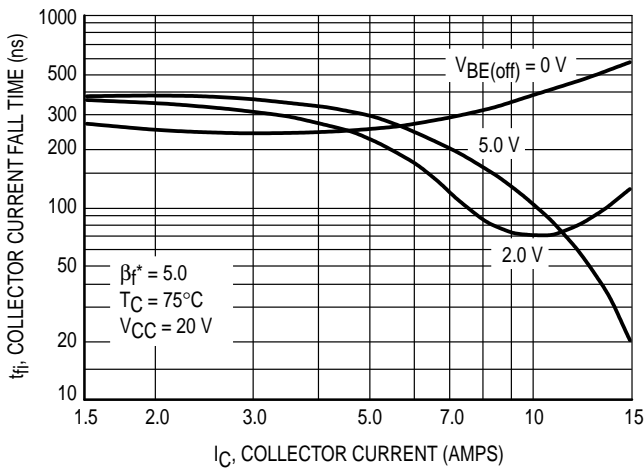


Figure 9. Collector Current Fall Time

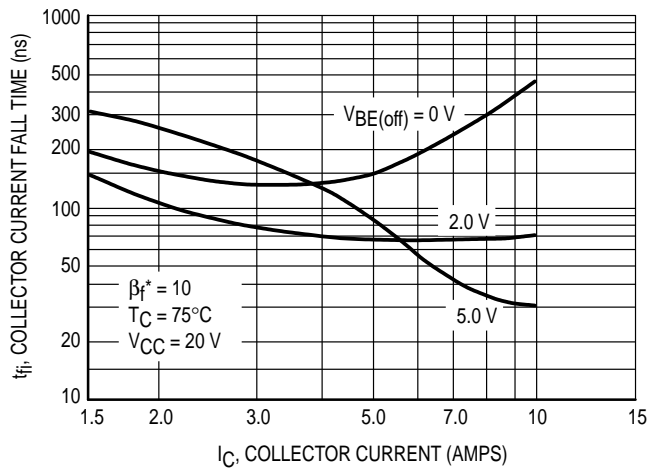


Figure 10. Collector Current Fall Time

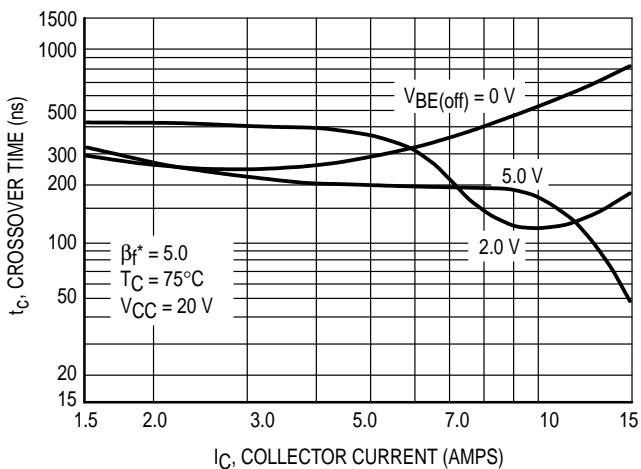


Figure 11. Crossover Time

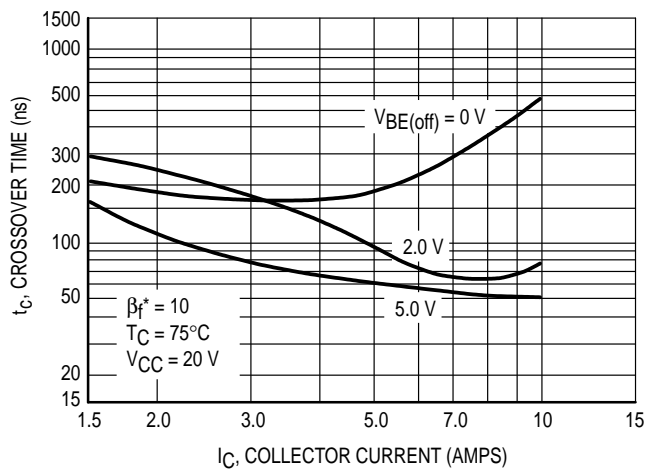


Figure 12. Crossover Time

$$*\beta_f = \frac{I_C}{I_{B1}}$$

GUARANTEED SAFE OPERATING AREA LIMITS

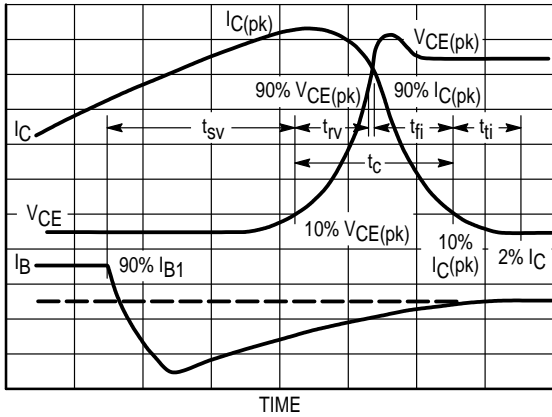


Figure 13. Inductive Switching Measurements

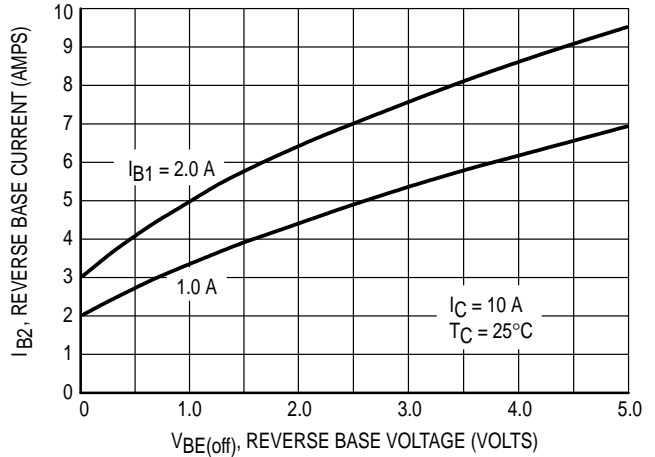


Figure 14. Peak Reverse Base Current

SAFE OPERATING AREA INFORMATION

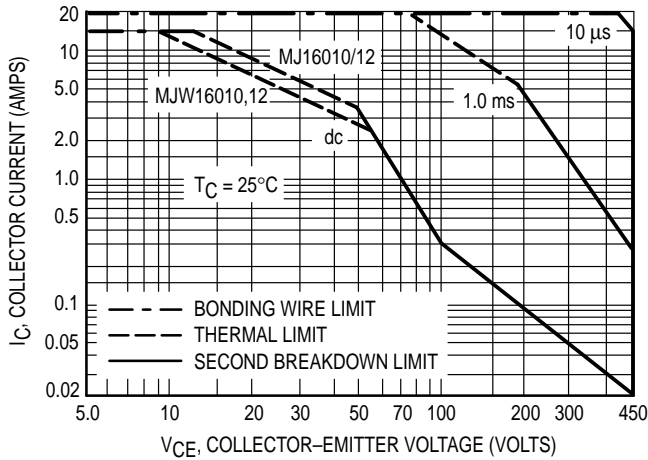


Figure 15. Maximum Forward Bias Safe Operating Area

$$\beta_f = \frac{I_C}{I_{B1}}$$

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_J(\text{pk})$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the

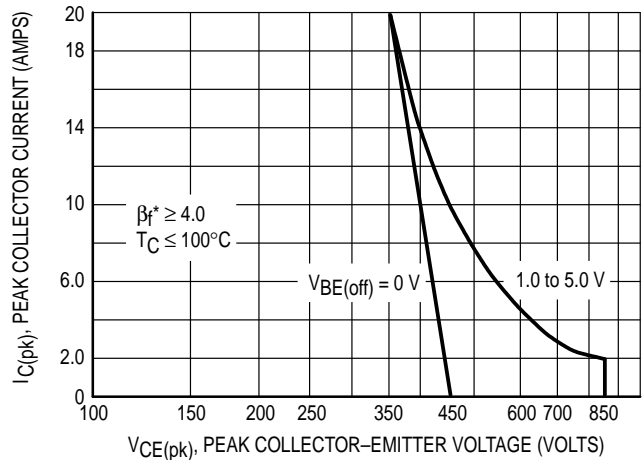


Figure 16. Maximum Reverse Bias Safe Operating Area

power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

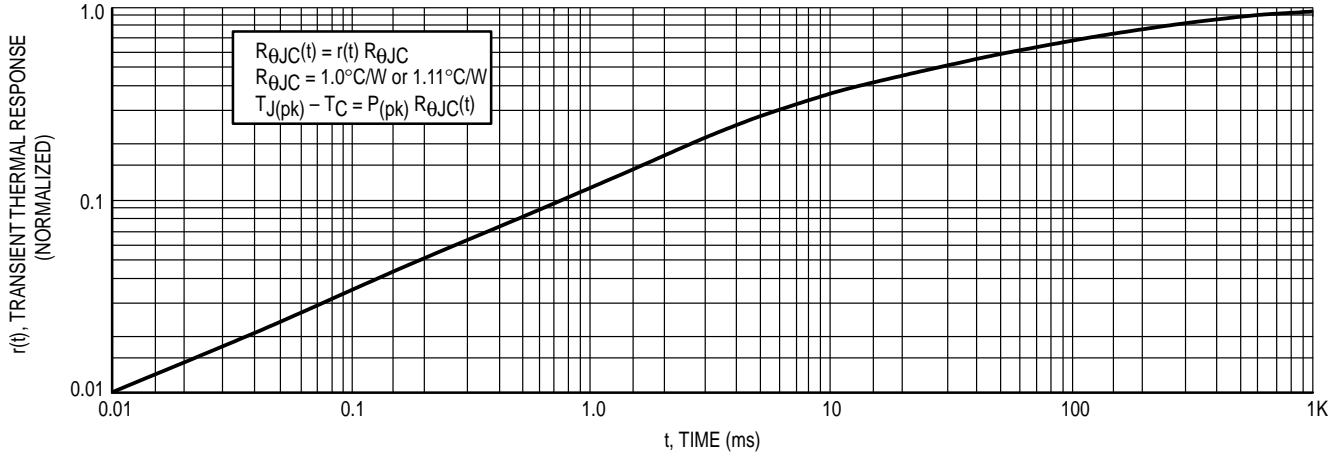


Figure 17. Thermal Response

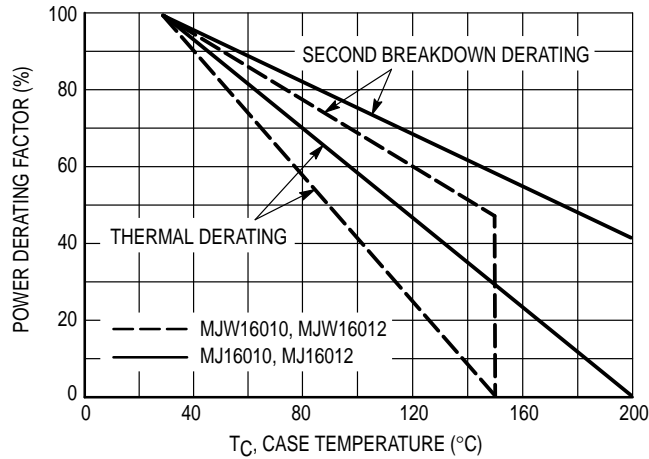
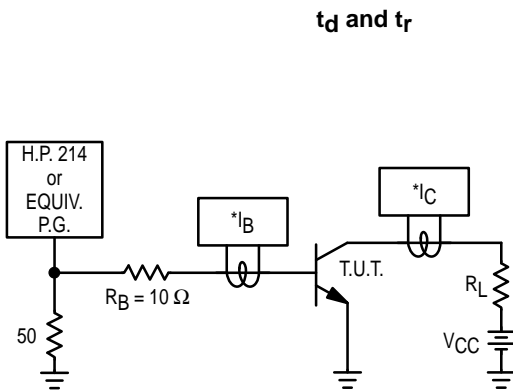
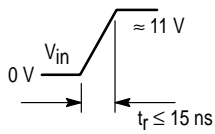


Figure 18. Power Derating

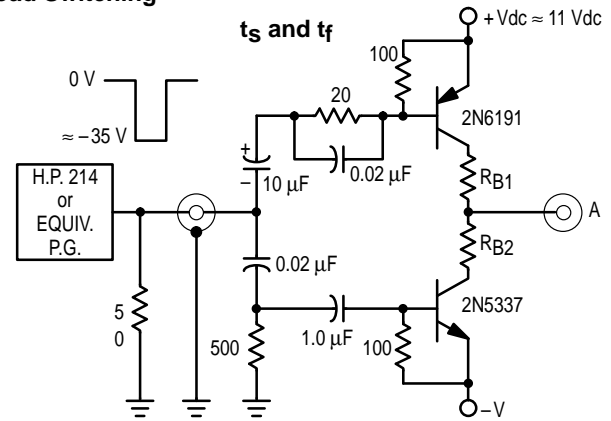
Table 1. Resistive Load Switching



$V_{CC} = 250 \text{ Vdc}$
 $R_L = 25 \Omega$
 $I_C = 10 \text{ Adc}$
 $I_B = 1.0 \text{ Adc}$



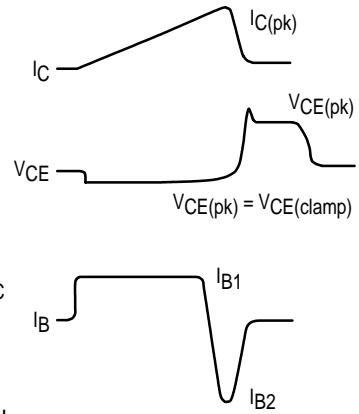
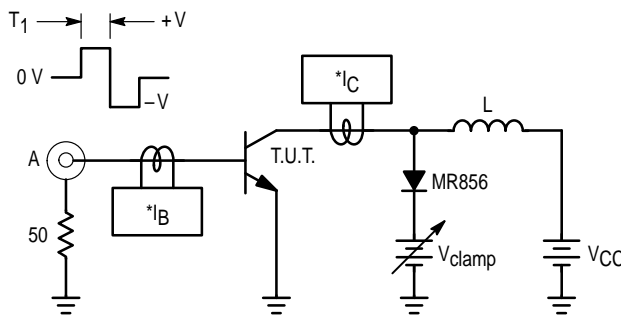
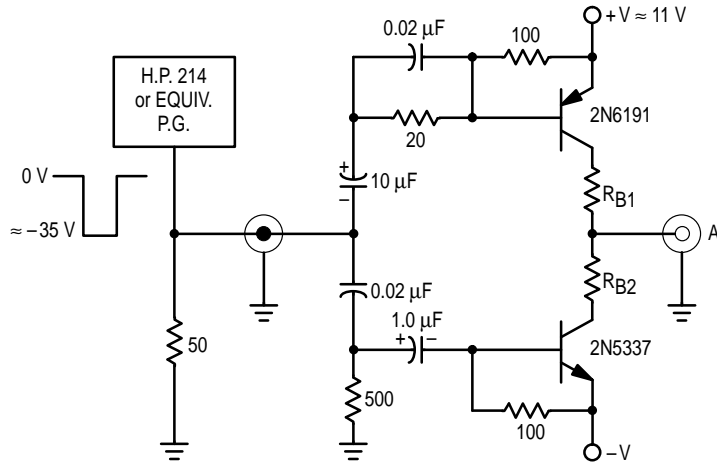
*Tektronix AM503
 P6302 or Equivalent



$V_{CC} = 250 \text{ Vdc}$
 $R_L = 25 \Omega$
 $I_C = 10 \text{ Adc}$
 $I_{B1} = 1.0 \text{ Adc}$
 $I_{B2} = 2.0 \text{ Adc}$
 For $V_{BE(off)} = 5.0 \text{ V}$, $R_{B2} = 0 \Omega$

Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at Point A.

Table 2. Inductive Load Switching



$$t_1 \approx \frac{L_{\text{coil}} (I_{Cpk})}{V_{CC}}$$

T₁ adjusted to obtain I_{C(pk)}

V_{CEO(sus)}

L = 10 mH
R_{B2} = ∞
V_{CC} = 20 V Its

*Tektronix AM503
P6302 or Equivalent

Inductive Switching

L = 200 μH
R_{B2} = 0
V_{CC} = 20 V
R_{B1} selected for desired I_{B1}

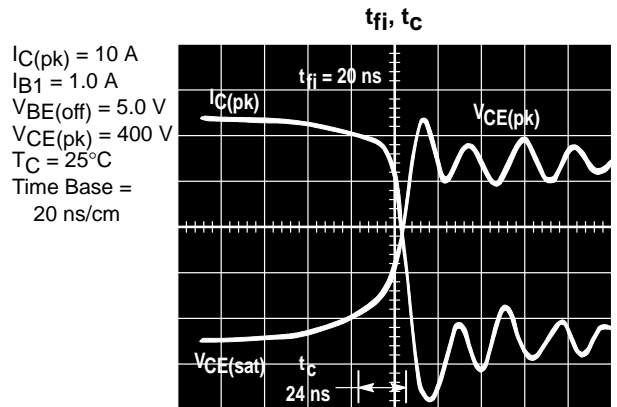
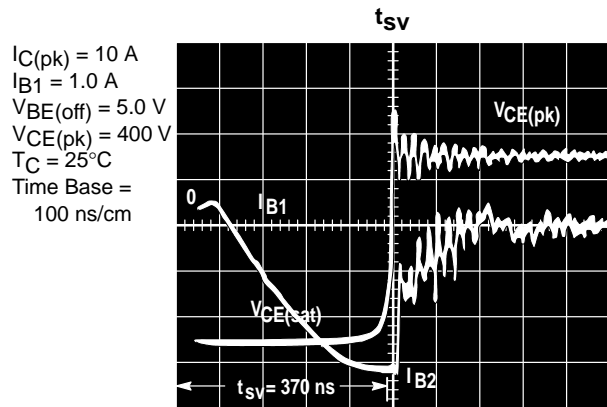
Scope — Tektronix
7403 or Equivalent

RBSOA

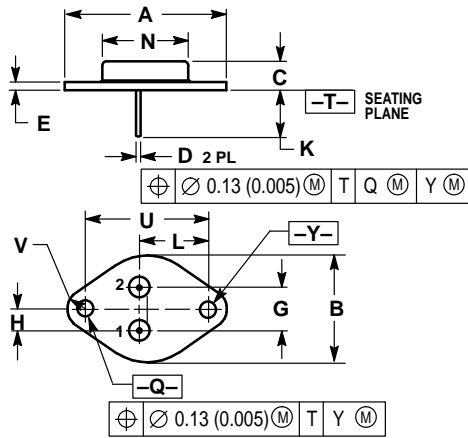
L = 200 μH
R_{B2} = 0
V_{CC} = 20 V
R_{B1} selected for desired I_{B1}

Note: Adjust -V to obtain desired V_{BE(off)} at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS



PACKAGE DIMENSIONS

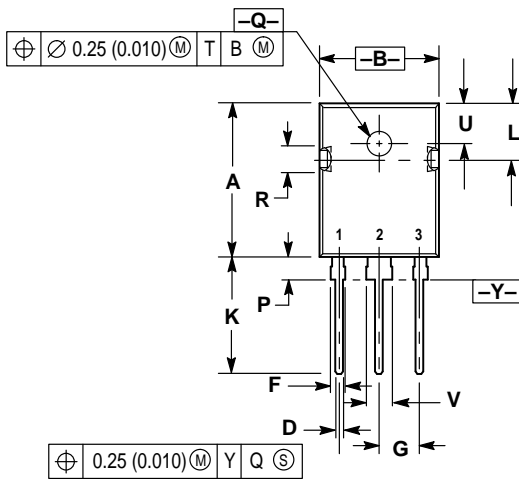


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF	—	39.37 REF	—
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC	—	10.92 BSC	—
H	0.215 BSC	—	5.46 BSC	—
K	0.440	0.480	11.18	12.19
L	0.665 BSC	—	16.89 BSC	—
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC	—	30.15 BSC	—
V	0.131	0.188	3.33	4.77

STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

CASE 1-07
 TO-204AA (TO-3)
 ISSUE Z




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC	—	0.215 BSC	—
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC	—	0.209 BSC	—
V	3.05	3.40	0.120	0.134

STYLE 3:
 PIN 1: BASE
 2: COLLECTOR
 3: EMITTER
 4: COLLECTOR

CASE 340F-03
 TO-247AE
 ISSUE E

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