## **Product Preview**

# TMOS VTM

# **SOT-223 for Surface Mount**

### N-Channel Enhancement-Mode Silicon Gate

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

#### **New Features of TMOS V**

- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low RDS(on) Technology
- Faster Switching than E–FET Predecessors

### Features Common to TMOS V and TMOS E-FETS

- · Avalanche Energy Specified
- IDSS and VDS(on) Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E-FET
- Available in 12 mm Tape & Reel
   Use MMFT3055VT1 to order the 7 inch/1000 unit reel
   Use MMFT3055VT3 to order the 13 inch/4000 unit reel

### MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

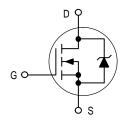
Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	60	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	VDGR	60	Vdc
Gate–to–Source Voltage – Continuous – Non–repetitive ( $t_p \le 10 \text{ ms}$ )	V <sub>G</sub> S V <sub>G</sub> SM	± 20 ± 25	Vdc Vpk
Drain Current – Continuous – Continuous @ $100^{\circ}$ C – Single Pulse ( $t_p \le 10 \ \mu s$ )	I <sub>D</sub> I <sub>DM</sub>	1.7 1.4 6.0	Adc Apk
Total PD @ T <sub>A</sub> = 25°C mounted on 1" sq. Drain pad on FR–4 bd material Total PD @ T <sub>A</sub> = 25°C mounted on 0.70" sq. Drain pad on FR–4 bd material Total PD @ T <sub>A</sub> = 25°C mounted on min. Drain pad on FR–4 bd material Derate above 25°C	PD	2.0 1.7 0.9 6.3	Watts mW/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ( $V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 3.4 Apk, L = 10 mH, $R_G$ = 25 $\Omega$ )	EAS	58	mJ
Thermal Resistance  – Junction to Ambient on 1" sq. Drain pad on FR–4 bd material  – Junction to Ambient on 0.70" sq. Drain pad on FR–4 bd material  – Junction to Ambient on min. Drain pad on FR–4 bd material	R <sub>θ</sub> JA R <sub>θ</sub> JA R <sub>θ</sub> JA	70 88 159	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

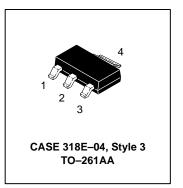
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## **MMFT3055V**

TMOS POWER FET
1.7 AMPERES
60 VOLTS
RDS(on) = 0.130 OHM







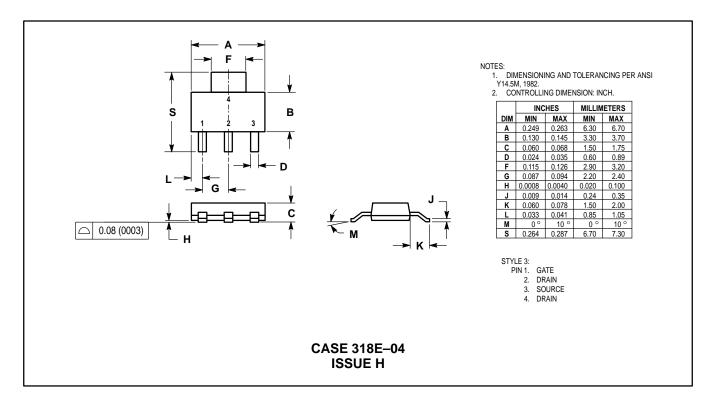
### **MMFT3055V**

## **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Cha	aracteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
$\begin{aligned} &\text{Drain-to-Source Breakdown Volta}\\ &(\text{V}_{GS} = 0 \text{ Vdc}, \text{I}_{D} = 0.25 \text{ mAdc})\\ &\text{Temperature Coefficient (Positive)} \end{aligned}$		V(BR)DSS	60 —	— 63	<u> </u>	Vdc mV/°C
Zero Gate Voltage Drain Current (VDS = 60 Vdc, VGS = 0 Vdc) (VDS = 60 Vdc, VGS = 0 Vdc, TJ = 150°C)		IDSS	_	_	10 100	μAdc
Gate–Body Leakage Current ( $V_{GS} = \pm 20 \text{ Vdc}$ , $V_{DS} = 0 \text{ Vdc}$ )		I <sub>GSS</sub>	_	_	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficie	ent (Negative)	V <sub>GS(th)</sub>	2.0 —	2.8 5.6	4.0 —	Vdc mV/°C
Static Drain-to-Source On-Resistance (VGS = 10 Vdc, ID = 0.85 Adc)		R <sub>DS(on)</sub>	_	0.115	0.13	Ohm
Drain-to-Source On-Voltage (VGS = 10 Vdc, $I_D$ = 1.7 Adc) (VGS = 10 Vdc, $I_D$ = 0.85 Adc, 7	「J = 150°C)	VDS(on)	_ _	_ _	0.27 0.25	Vdc
Forward Transconductance (V <sub>DS</sub> :	= 8.0 Vdc, I <sub>D</sub> = 1.7 Adc)	9FS	1.0	2.7	_	mhos
DYNAMIC CHARACTERISTICS						•
Input Capacitance		C <sub>iss</sub>	_	360	500	pF
Output Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	Coss	_	110	150	
Transfer Capacitance	1 = 1.02,	C <sub>rss</sub>	_	25	50	
SWITCHING CHARACTERISTICS (	2)					
Turn-On Delay Time		<sup>t</sup> d(on)	1	8.0	20	ns
Rise Time	$(V_{DD} = 30 \text{ Vdc}, I_{D} = 1.7 \text{ Adc}, \\ V_{GS} = 10 \text{ Vdc}, \\ R_{G} = 9.1 \Omega)$	t <sub>r</sub>	1	9.0	20	
Turn-Off Delay Time		td(off)	_	32	60	
Fall Time		t <sub>f</sub>	_	18	40	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 1.7 Adc, V <sub>GS</sub> = 10 Vdc)	QT	1	13	20	nC
		Q <sub>1</sub>	1	2.0	1	
		Q <sub>2</sub>	_	5.0	_	
		Q <sub>3</sub>	1	4.0		
SOURCE-DRAIN DIODE CHARAC	TERISTICS					
Forward On–Voltage (1)	$(I_S = 1.7 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$ $(I_S = 1.7 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 150^{\circ}\text{C})$	VSD	_ _	0.85 0.7	1.6 —	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 1.7 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	_	40	_	ns
		t <sub>a</sub>	_	34	_	
		t <sub>b</sub>	_	6.0	_	
Reverse Recovery Stored Charge	]	Q <sub>RR</sub>	1	0.089	1	μС
NTERNAL PACKAGE INDUCTANO	CE CONTRACTOR OF THE CONTRACTO					
Internal Drain Inductance (Measured from the drain lead 0	.25" from package to center of die)	LD	_	4.5		nH
Internal Source Inductance (Measured from the source lead	0.25" from package to source bond pad)	LS	_	7.5	_	nH

<sup>(1)</sup> Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

### **PACKAGE DIMENSIONS**



#### **MMFT3055V**

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