# SEROCCO-M 2 Channel Serial Optimized Communication Controller PEB 20532 Version 1.2 PEF 20532 Version 1.2

# Datacom



Never stop thinking.

Edition 2000-09-14

Published by Infineon Technologies AG, St.-Martin-Strasse 53, D-81541 München, Germany © Infineon Technologies AG 9/14/00. All Rights Reserved.

#### Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

#### Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

#### Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

# SEROCCO-M 2 Channel Serial Optimized Communication Controller PEB 20532 Version 1.2 PEF 20532 Version 1.2

# Datacom



Never stop thinking.

#### PEB 20532

Revision History:		2000-09-14	DS 1
Previous Version:		SEROCCO V1.1 Preliminary Data Sheet, 08.99, I	DS1
Page (previous Version)	Page (current Version)	Subjects (major changes since last revision)	
32-34	35-37	Correction: signal 'OSR' is multiplexed with signal ' 'OST' is multiplexed with 'CTS' (was vice versa)	CD', signal
80	83	corrected HDLC receive address recognition table	
214, 222	218, 226	Corrected location of TCD interrupt (async/bisync m in registers ISR0 and IMR0 from bit 7 to bit 2.	nodes only)
n.a.	263, 266	Added timing diagram for external DMA support sig	gnals
n.a.	263	Added address timing diagram for Intel multiplexed (signal ALE)	mode
253	257	Chapter "Electrical Characteristics" updated with fir characterization results.	nal

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com



**Table of Contents** 

Page

<b>1</b> 1.1 1.2 1.3 1.3.1 1.3.2 1.4 1.4.1 1.4.2	Introduction17Features18Logic Symbol21Typical Applications22System Integration Example22Serial Configuration Examples24Differences between SEROCCO-M and the ESCC Family26Enhancements to the ESCC Serial Core26Simplifications to the ESCC Serial Core26
<b>2</b> 2.1 2.2	Pin Descriptions       27         Pin Diagram P-TQFP-100-3       27         Pin Definitions and Functions       28
3	Functional Overview
3.1	Block Diagram
3.2	Serial Communication Controller (SCC) 42
3.2.1	Protocol Modes Overview
3.2.2	SCC FIFOs
3.2.2.1	SCC Transmit FIFO 43
3.2.2.2	SCC Receive FIFO 43
3.2.2.3	SCC FIFO Access 45
3.2.3	Clocking System
3.2.3.1	Clock Mode 0 (0a/0b) 50
3.2.3.2	Clock Mode 1
3.2.3.3	Clock Mode 2 (2a/2b) 52
3.2.3.4	Clock Mode 3 (3a/3b) 53
3.2.3.5	Clock Mode 4
3.2.3.6	Clock Mode 5a (Time Slot Mode) 55
3.2.3.7	Clock Mode 5b (Octet Sync Mode) 62
3.2.3.8	Clock Mode 6 (6a/6b) 65
3.2.3.9	Clock Mode 7 (7a/7b) 66
3.2.4	Baud Rate Generator (BRG) 67
3.2.5	Clock Recovery (DPLL) 67
3.2.6	SCC Timer Operation
3.2.7	SCC Serial Bus Configuration Mode 71
3.2.8	Serial Bus Access Procedure 71
3.2.9	Serial Bus Collisions and Recovery 71
3.2.10	Serial Bus Access Priority Scheme
3.2.11	Serial Bus Configuration Timing Modes

#### 



# **Table of Contents**

		•
3.2.13.2 3.2.13.3 3.2.14 3.2.14.1 3.2.14.2 3.2.15 3.3 3.4 3.5 3.6 3.6.1 3.6.2	FM0 and FM1 Encoding Manchester EncodingModem Control Signals (RTS, CTS, CD) RTS/CTS Handshaking Carrier Detect (CD) Receiver Control Local Loop Test ModeMicroprocessor Interface External DMA Controller Support Interrupt ArchitectureGeneral Purpose Port Pins GPP Functional Description GPP Interrupt Indication	74 75 76 76 77 77 78 79 80 81 81 81
4	Detailed Protocol Description	82
4.1	HDI C/SDI C Protocol Modes	83
4.1.1	HDLC Submodes Overview	83
4.1.1.1	Automode	83
4.1.1.2	Address Mode 2	84
4.1.1.3	Address Mode 1	84
4.1.1.4	Address Mode 0	85
4.1.2	HDLC Receive Data Processing	85
4.1.3	Receive Address Handling	87
4.1.4	HDLC Transmit Data Processing	87
4.1.5	Shared Flags	89
4.1.6	One Bit Insertion	89
4.1.7	Preamble Transmission	89
4.1.8	CRC Generation and Checking	90
4.1.9	Receive Length Check Feature	90
4.2	Point-to-Point Protocol (PPP) Modes	91
4.2.1	Bit Synchronous PPP	91
4.2.2	Octet Synchronous PPP	91
4.2.3	Asynchronous PPP	92
4.2.4	Data Transparency in PPP Mode	92
4.3	Extended Transparent Mode	95
4.4	Asynchronous (ASYNC) Protocol Mode	95
4.4.1	Character Framing	95
4.4.2	Data Reception	96
4.4.2.1	Asynchronous Mode	96
4.4.2.2	Isochronous Mode	96
4.4.2.3	Storage of Receive Data	97
4.4.3		97
4.4.4		98
4.4.4.1	Break Detection/Generation	98



Table of	Contents F	Page
4.4.4.2 4.4.4.3 4.5 4.5.1 4.5.2 4.5.3 4.5.4 4.5.4.1 4.6 4.6.1 4.6.2 4.6.3	In-band Flow Control by XON/XOFF Characters Out-of-band Flow Control BISYNC Protocol Mode Character Framing Data Reception Data Transmission Special Functions Preamble Transmission Procedural Support (Layer-2 Functions) Full-Duplex LAPB/LAPD Operation Half-Duplex SDLC-NRM Operation Signaling System #7 (SS7) Operation	. 98 100 102 102 103 104 105 105 105 111 113
<b>5</b> 5.1 5.2 5.2.1 5.2.2 5.2.3 5.2.3	Register Description         Register Overview         Detailed Register Description         Global Registers         Channel Specific SCC Registers         Channel Specific DMA Registers         Miscellaneous Registers	116 116 121 121 138 235 242
6 6.1 6.2 6.2.1 6.2.2 6.3 6.3.1 6.3.2	Programming         Initialization         Interrupt Mode         Data Transmission (Interrupt Driven)         Data Reception (Interrupt Driven)         External DMA Supported Mode         Data Transmission (With External DMA Support)         Data Reception (With External DMA Support)	245 245 245 247 250 250 253
<b>7</b> 7.1 7.2 7.3 7.4 7.5 7.6 7.7 7.7.1 7.7.1.1 7.7.1.2 7.7.1.3 7.7.2 7.7.2	Electrical Characteristics Absolute Maximum Ratings Operating Range DC Characteristics AC Characteristics Capacitances Thermal Package Characteristics Timing Diagrams Microprocessor Interface Timing Microprocessor Interface Clock Timing Infineon/Intel Bus Interface Timing Motorola Bus Interface Timing PCM Serial Interface Timing Clock Input Timing	257 257 258 259 259 260 261 261 261 261 262 265 268 268



#### **Table of Contents**

9	Package Outlines	282
<b>8</b> 8.1	Test Modes	277 277
7.7.3 7.7.4	JTAG-Boundary Scan Timing	275 276
7.7.2.6	Clock Mode 5 Frame Synchronisation Timing	274
7.7.2.5	Clock Mode 4 Gating Timing	273
7.7.2.4	Clock Mode 1 Strobe Timing	272
7.7.2.3	Transmit Cycle Timing	270
7.7.2.2	Receive Cycle Timing	269



#### List of Figures

# PEB 20532 PEF 20532

List of Figure	es Pa	ige
Figure 1	Logic Symbol	21
Figure 2	System Integration	22
Figure 3	System Integration With External DMA Controller	23
Figure 4	Point-to-Point Configuration.	24
Figure 5	Point-to-Multipoint Bus Configuration	25
Figure 6	Multimaster Bus Configuration	25
Figure 7	Pin Configuration P-TQFP-100-3 Package	27
Figure 8	Block Diagram	41
Figure 9	SCC Transmit FIFO	43
Figure 10	SCC Receive FIFO	44
Figure 11	XFIFO/RFIFO Word Access (Intel Mode)	45
Figure 12	XFIFO/RFIFO Word Access (Motorola Mode)	45
Figure 13	Clock Supply Overview	49
Figure 14	Clock Mode 0a/0b Configuration	50
Figure 15	Clock Mode 1 Configuration.	51
Figure 16	Clock Mode 2a/2b Configuration	52
Figure 17	Clock Mode 3a/3b Configuration	53
Figure 18	Clock Mode 4 Configuration.	54
Figure 19	Selecting one time-slot of programmable delay and width	56
Figure 20	Selecting one or more time-slots of 8-bit width	58
Figure 21	Clock Mode 5a Configuration	59
Figure 22	Clock Mode 5a "Continuous Mode"	60
Figure 23	Clock Mode 5a "Non Continuous Mode"	61
Figure 24	Selecting one or more octet wide time-slots	63
Figure 25	Clock Mode 5b Configuration	64
Figure 26	Clock Mode 6a/6b Configuration	65
Figure 27	Clock Mode 7a/7b Configuration	66
Figure 28	DPLL Algorithm (NRZ and NRZI Encoding, Phase Shift Enabled)	69
Figure 29	DPLL Algorithm (NRZ and NRZI Encoding, Phase Shift Disabled)	69
Figure 30	DPLL Algorithm for FM0, FM1 and Manchester Encoding	70
Figure 31	Request-to-Send in Bus Operation	73
Figure 32	NRZ and NRZI Data Encoding	74
Figure 33	FM0 and FM1 Data Encoding	75
Figure 34	Manchester Data Encoding	75
Figure 35	RTS/CTS Handshaking	77
Figure 36	SCC Test Loop	78
Figure 37	Interrupt Status Registers	80
Figure 38	HDLC Receive Data Processing in 16 bit Automode	85
Figure 39	HDLC Receive Data Processing in 8 bit Automode	85
Figure 40	HDLC Receive Data Processing in Address Mode 2 (16 bit)	86
Figure 41	HDLC Receive Data Processing in Address Mode 2 (8 bit)	86
Figure 42	HDLC Receive Data Processing in Address Mode 1	86



# PEB 20532 PEF 20532

# List of Figures

Figure 43	HDLC Receive Data Processing in Address Mode 0	. 87
Figure 44	SCC Transmit Data Flow (HDLC Modes)	. 88
Figure 45	PPP Mapping/Unmapping Example	. 94
Figure 46	Asynchronous Character Frame	. 96
Figure 47	Out-of-Band DTE-DTE Bi-directional Flow Control	101
Figure 48	Out-of-Band DTE-DCE Bi-directional Flow Control	102
Figure 49	BISYNC Message Format	103
Figure 50	Processing of Received Frames in Auto Mode	107
Figure 51	Timer Procedure/Poll Cycle	109
Figure 52	Transmission/Reception of I-Frames and Flow Control	110
Figure 53	Flow Control: Reception of S-Commands and Protocol Errors	110
Figure 54	No Data to Send: Data Reception/Transmission	113
Figure 55	Data Transmission (without error), Data Transmission (with error)	113
Figure 56	Interrupt Driven Data Transmission (Flow Diagram)	247
Figure 57	Interrupt Driven Data Reception (Flow Diagram)	249
Figure 58	DMA Transmit (Single Buffer per Packet)	251
Figure 59	Fragmented DMA Transmission (Multiple Buffers per Packet)	252
Figure 60	DMA Receive (Single Buffer per Packet)	254
Figure 61	Fragmented Reception per DMA (Example)	255
Figure 62	Fragmented Reception Sequence (Example)	256
Figure 63	Input/Output Waveform for AC Tests	259
Figure 64	Microprocessor Interface Clock Timing	261
Figure 65	Infineon/Intel Read Cycle Timing	262
Figure 66	Infineon/Intel Write Cycle Timing	262
Figure 67	Infineon/Intel DMA Read Cycle Timing	263
Figure 68	Infineon/Intel DMA Write Cycle Timing	263
Figure 69	Infineon/Intel Multiplexed Address Timing	263
Figure 70	Motorola Read Cycle Timing	265
Figure 71	Motorola Write Cycle Timing	265
Figure 72	Motorola DMA Read Cycle Timing.	266
Figure 73	Motorola DMA Write Cycle Timing	266
Figure 74	Clock Input Timing	268
Figure 75	Receive Cycle Timing	269
Figure 76	Transmit Cycle Timing	270
Figure 77	Clock Mode 1 Strobe Timing	272
Figure 78	Clock Mode 4 Receive Gating Timing	273
Figure 79	Clock Mode 4 Transmit Gating Timing.	273
Figure 80	Clock Mode 5 Frame Synchronisation Timing	274
Figure 81	Reset Timing	275
Figure 82	JTAG-Boundary Scan Timing	276
Figure 83	Block Diagram of Test Access Port and Boundary Scan Unit	277



# PEB 20532 PEF 20532

#### List of Tables

Table 1 Table 2 Table 3 Table 4 Table 5	Microprocessor Bus Interface	28 32 34 38 39
Table 6	Power Pins.	40
Table 7	Overview of Clock Modes	46
Table 8	Clock Modes of the SCCs	47
Table 9	BRRL/BRRH Register and Bit-Fields	67
Table 10	Data Bus Access 16-bit Intel Mode	78
Table 11	Data Bus Access 16-bit Motorola Mode	79
Table 12	Protocol Mode Overview	82
Table 13	Address Comparison Overview	83
Table 14	Error Handling	11
Table 15	Register Overview	16
Table 16	Status Information after RME interupt 24	48
Table 17	DMA Terminology 28	50
Table 18	Capacitances	
	TA = $25 \times C$ ; VDD3 = $3.3 \times V \pm 0.3 \times V$ , VSS = $0 \times 28$	59
Table 19	Thermal Package Characteristics P-TQFP-100-3 20	60
Table 20	Microprocessor Interface Clock Timing 20	61
Table 21	Infineon/Intel Bus Interface Timing 20	64
Table 22	Motorola Bus Interface Timing 20	66
Table 23	Clock Input Timing 20	68
Table 24	Receive Cycle Timing 20	69
Table 25	Transmit Cycle Timing 2	71
Table 26	Clock Mode 1 Strobe Timing 2	72
Table 27	Clock Mode 4 Gating Timing 2	73
Table 28	Clock Mode 5 Frame Synchronisation Timing 2	74
Table 29	Reset Timing	75
Table 30	JTAG-Boundary Scan Timing 2	76
Table 31	Boundary Scan Sequence of SEROCCO-M 2	78
Table 32	Boundary Scan Test Modes. 22	81



# List of Registers

Register 1	GCMDR	121
Register 2	GMODE	122
Register 3	GSTAR	124
Register 4	GPDIRL	126
Register 5	GPDIRH	126
Register 6	GPDATL	128
Register 7	GPDATH	128
Register 8	GPIML	130
Register 9	GPIMH	130
Register 10	GPISL	132
Register 11	GPISH	132
Register 12	DCMDR	134
Register 13	DISR	135
Register 14	DIMR	137
Register 15	FIFOL	138
Register 16	FIFOH	138
Register 17	STARL	141
Register 18	STARH	141
Register 19	CMDRL	146
Register 20	CMDRH	146
Register 21	CCR0L	151
Register 22	CCR0H	151
Register 23	CCR1L	155
Register 24	CCR1H	155
Register 25	CCR2L	160
Register 26	CCR2H	160
Register 27	CCR3L	167
Register 28	CCR3H	167
Register 29	PREAMB	175
Register 30	TOLEN	176
Register 31	АССМО	177
Register 32	ACCM1	177
Register 33	ACCM2	178
Register 34	ACCM3	178
Register 35	UDAC0	180
Register 36	UDAC1	180
Register 37	UDAC2	181
Register 38	UDAC3	181
Register 39	TTSA0	183
Register 40	TTSA1	183
Register 41	TTSA2	184
Register 42	TTSA3	184



#### **List of Registers**

_		_
Register 43	RTSA0	186
Register 44	RTSA1	186
Register 45	RTSA2	187
Register 46	RTSA3	187
Register 47	PCMTX0	189
Register 48	PCMTX1	189
Register 49	PCMTX2	190
Register 50	PCMTX3	190
Register 51	PCMRX0	192
Register 52	PCMRX1	192
Register 53	PCMRX2	193
Register 54	PCMRX3	193
Register 55	BRRL	195
Register 56	BRRH	195
Register 57	TIMR0	197
Register 58	TIMR1	197
Register 59	TIMR2	198
Register 60	TIMR3	198
Register 61	XAD1	201
Register 62	XAD2	201
Register 63	RAL1	203
Register 64	RAH1	203
Register 65	RAL2	204
Register 66	RAH2	204
Register 67	AMRAL1	206
Register 68	AMRAH1	206
Register 69	AMRAL2	207
Register 70	AMRAH2	207
Register 71	RLCRL	209
Register 72	RLCRH	209
Register 73	XON	211
Register 74	XOFF	211
Register 75	MXON	213
Register 76	MXOFF	213
Register 77	TCR	215
Register 78	TICR	216
Register 79	ISR0	218
Register 80	ISR1	218
Register 81	ISR2	219
Register 82	IMR0	226
Register 83	IMR1	226
Register 84	IMR2	227
<b>J</b>		



# List of Registers

Register 85	RSTA	9
Register 86	SYNCL	3
Register 87	SYNCH	3
Register 88	XBCL	6
Register 89	XBCH	6
Register 90	RMBSL	8
Register 91	RMBSH 23	8
Register 92	RBCL	0
Register 93	RBCH	0
Register 94	VER0 24	2
Register 95	VER1 24	2
Register 96	VER2	3
Register 97	VER3	3



# Preface

The 2 Channel Serial Optimized Communication Controller PEB 20532 (SEROCCO-M) is a Protocol Controller for a wide range of data communication and telecommunication applications. This document provides complete reference information on hardware and software related issues as well as on general operation.

#### **Organization of this Document**

This Data Sheet is divided into 9 chapters. It is organized as follows:

- Chapter 1, Introduction Gives a general description of the product, lists the key features, and presents some typical applications.
- Chapter 2, Pin Descriptions

Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

• Chapter 3, Functional Overview

This chapter provides detailed descriptions of all SEROCCO-M internal functional blocks.

• Chapter 4, Detailed Protocol Description

Gives a detailed description of all protocols supported by the serial communication controllers SCCs.

- Chapter 5, Register Description Gives a detailed description of all SEROCCO-M on chip registers.
- Chapter 6, Programming Provides programming help for SEROCCO-M initialization procedure and operation.
- Chapter 7, Electrical Characteristics Gives a detailed description of all electrical DC and AC characteristics and provides timing diagrams and values for all interfaces.
- Chapter 8, Test Modes Gives a detailed description of the JTAG boundary scan unit.
- Chapter 9, Package Outlines



#### **Your Comments**

We welcome your comments on this document. We are continuously trying improving our documentation. Please send your remarks and suggestions by e-mail to

sc.docu\_comments@infineon.com

Please provide in the *subject* of your e-mail:

device name (SEROCCO-M), device number (PEB 20532, PEF 20532), device version (Version 1.2),

and in the *body* of your e-mail:

document type (Data Sheet), issue date (2000-09-14) and document revision number (DS 1).



# 1 Introduction

The SEROCCO-M is a Serial Communication Controller with two independent serial channels<sup>1)</sup>. The serial channels are derived from updated protocol logic of the ESCC and DSCC4 device family providing a large set of protocol support and variety in serial interface configuration. This allows easy integration to different environments and applications.

A generic 8- or 16-bit multiplexed/demultiplexed slave interface provides fast device access with low bus utilization and easy software handshaking. DMA handshake control signals allow connection to an external DMA controller.

Large on-chip FIFOs of 64 byte capacity per port and direction in combination with enhanced threshold control mechanisms allow decoupling of traffic requirements on host bus and serial interfaces with little exception probabilities such as data underruns or overflows.

Each of the two Serial Communication Controllers (SCC) contains an independent Baud Rate Generator, DPLL and programmable protocol processing (HDLC, PPP, ASYNC and BISYNC). Data rates of up to 16 Mbit/s (HDLC, PPP, bit transparent) and 2 Mbit/s (DPLL assisted modes) are supported. The channels can also handle a large set of layer-2 protocol functions (LAPD, SS7) reducing bus and host CPU load. Two channel specific timers are provided to support protocol functions.

<sup>&</sup>lt;sup>1)</sup> The serial channels are also called 'ports' or 'cores' depending on the context.



# 2 Channel Serial Optimized Communication Controller SEROCCO-M

# Version 1.2

# 1.1 Features

# Serial communication controllers (SCCs)

- Two independent channels
- Full duplex data rates on each channel of up to 16 Mbit/s sync 2 Mbit/s with DPLL
- 64 Bytes deep receive FIFO per SCC
- 64 Bytes deep transmit FIFO per SCC

# Serial Interface

- On-chip clock generation or external clock sources
- On-chip DPLLs for clock recovery
- Baud rate generator
- Clock gating signals
- Clock gapping capability
- Programmable time-slot capability for connection to TDM interfaces (e.g. T1, E1)
- NRZ, NRZI, FM and Manchester data encoding
- Optional data flow control using modem control lines (RTS, CTS, CD)
- Support of bus configuration by collision detection and resolution

# **Bit Processor Functions**

- HDLC/SDLC Protocol Modes
  - Automatic flag detection and transmission
  - Shared opening and closing flag
  - Generation of interframe-time fill '1's or flags
  - Detection of receive line status
  - Zero bit insertion and deletion

Туре	Package
PEB 20532, PEF 20532	P-TQFP-100-3



CMOS

PEB 20532 PEF 20532



- CRC generation and checking (CRC-CCITT or CRC-32)
- Transparent CRC option per channel and/or per frame
- Programmable Preamble (8 bit) with selectable repetition rate
- Error detection (abort, long frame, CRC error, short frames)
- Bit Synchronous PPP Mode
  - Bit oriented transmission of HDLC frame (flag, data, CRC, flag)
  - Zero bit insertion/deletion
  - 15 consecutive '1' bits abort sequence
- Octet Synchronous PPP Mode
  - Octet oriented transmission of HDLC frame (flag, data, CRC, flag)
  - Programmable character map of 32 hard-wired characters (00<sub>H</sub>-1F<sub>H</sub>)
  - Four programmable characters for additional mapping
  - Insertion/deletion of control-escape character  $(7D_H)$  for mapped characters
- Asynchronous PPP Mode
  - Character oriented transmission of HDLC frame (flag, data, CRC, flag)
  - Start/stop bit framing of single character
  - Programmable character map of 32 hard-wired characters (00<sub>H</sub>-1F<sub>H</sub>)
  - Four programmable characters for additional mapping
  - Insertion/deletion of control-escape character (7D<sub>H</sub>) for mapped characters
- Asynchronous (ASYNC) Protocol Mode
  - Selectable character length (5 to 8 bits)
  - Even, odd, forced or no parity generation/checking
  - 1 or 2 stop bits
  - Break detection/generation
  - In-band flow control by XON/XOFF
  - Immediate character insertion
  - Termination character detection for end of block identification
  - Time out detection
  - Error detection (parity error, framing error)
- BISYNC Protocol Mode
  - Programmable 6/8 bit SYN pattern (MONOSYNC)
  - Programmable 12/16 bit SYN pattern (BISYNC)
  - Selectable character length (5 to 8 bits)
  - Even, odd, forced or no parity generation/checking
  - Generation of interframe-time fill '1's or SYN characters
  - CRC generation (CRC-16 or CRC-CCITT)
  - Transparent CRC option per channel and/or per frame
  - Programmable Preamble (8 bit) with selectable repetition rate
  - Termination character detection for end of block identification
  - Error detection (parity error, framing error)
- Extended Transparent Mode
  - Fully bit transparent (no framing, no bit manipulation)
  - Octet-aligned transmission and reception



- Protocol and Mode Independent
  - Data bit inversion
  - Data overflow and underrun detection
  - Timer

#### **Protocol Support**

- Address Recognition Modes
  - No address recognition (Address Mode 0)
  - 8-bit (high byte) address recognition (Address Mode 1)
  - 8-bit (low byte) or 16-bit (high and low byte) address recognition (Address Mode 2)
- HDLC Automode
  - 8-bit or 16-bit address generation/recognition
  - Support of LAPB/LAPD
  - Automatic handling of S- and I-frames
  - Automatic processing of control byte(s)
  - Modulo-8 or modulo-128 operation
  - Programmable time-out and retry conditions
  - SDLC Normal Response Mode (NRM) operation for slave
- Signaling System #7 (SS7) support
  - Detection of FISUs, MSUs and LSSUs
  - Unchanged Fill-In Signaling Units (FISUs) not forwarded
  - Automatic generation of FISUs in transmit direction (incl. sequence number)
  - Counting of errored signaling units
- Optional DTACK/READY controlled cycles

#### **Microprocessor Interface**

- 8/16-bit bus interface
- Multiplexed and De-multiplexed address/data bus
- Intel/Motorola style
- Asynchronous interface
- Maskable interrupts for each channel

### General Purpose Port (GPP) Pins (up to 7)

#### General

- 3.3V power supply with 5V tolerant inputs
- Low power consumption
- Power safe features
- P-TQFP-100-3 Package (Thermal Resistance: R<sub>JA</sub> = 42 K/W)



# 1.2 Logic Symbol



Figure 1 Logic Symbol



# **1.3** Typical Applications

SEROCCO-M devices can be used in LAN-WAN inter-networking applications such as Routers, Switches and Trunk cards and support the common V.35, ISDN BRI (S/T) and RFC1662 standards. Its new features provide powerful hardware and software interfaces to develop high performance systems.

# 1.3.1 System Integration Example



Figure 2 System Integration





Figure 3 System Integration With External DMA Controller



# 1.3.2 Serial Configuration Examples

SEROCCO-M supports a variety of serial configurations at Layer-1 and Layer-2 level. The outstanding variety of clock modes supporting a large number of combinations of external and internal clock sources allows easy integration in application environments.



Figure 4 Point-to-Point Configuration



PEB 20532 PEF 20532

#### Introduction



Figure 5 Point-to-Multipoint Bus Configuration



Figure 6 Multimaster Bus Configuration



# 1.4 Differences between SEROCCO-M and the ESCC Family

This chapter is useful for all being familiar with the ESCC family.

# **1.4.1** Enhancements to the ESCC Serial Core

The SEROCCO-M SCC cores contain the core logic of the ESCC as the heart of the device. Some enhancements are incorporated in the SCCs. These are:

- Octet-, Bit Synchronous and Asynchronous PPP protocol support as in RFC-1662
- Signaling System #7 (SS7) support
- 4-kByte packet length byte counter
- Enhanced address filtering (16-bit maskable)
- Enhanced time slot assigner
- Support of high data rates (16 Mbit/s)

# **1.4.2** Simplifications to the ESCC Serial Core

The following features of the ESCC core have been removed:

- Extended transparent mode 0

   (this mode provided octet buffered data reception without usage of FIFOs;
   SEROCCO-M supports octet buffered reception via appropriate threshold configurations for the SCC receive FIFOs)
- Support of interrupt acknowledge cycles
- Master clock mode





(top view)







# 2.2 Pin Definitions and Functions

Pin No.		Symbol	In (I)	Function
	P-TQFP- 100-3		Out (O)	
	81 80 79 78 75 74 73 72 67 66 65 64 61 60 59	D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	I/O	Data Bus The data bus lines are bi-directional tri-state lines which interface with the system's data bus.
	29 30 31 32 36 37 38	A7 A6 A5 A4 A3 A2 A1		Address Bus These pins connect to the system's address bus to select one of the internal registers for read or write.



Pin No.		Symbol	In (I)	Function
	P-TQFP- 100-3		Out (O)	
	39	A0	I	Address Line A0 (8-bit modes) In Motorola and in Intel 8-bit mode this signal represents the least significant address line.
		BLE	1	<b>Byte Low Enable (16-bit Intel bus mode)</b> This signal indicates a data transfer on the lower byte of the data bus (D7D0). Together with signal BHE the type of bus access is determined (byte or word access at even or odd address).
		UDS	I	<b>Upper Data Strobe (16-bit Motorola bus mode)</b> This active low strobe signal serves to control read/write operations. Together with signal LDS the type of bus access is determined.
	42	BM	1	<ul> <li>Bus Mode <ul> <li>BM = static '1' for operation in Motorola bus mode (de-multiplexed).</li> <li>BM = static '0' for operation in Intel bus mode with de-multiplexed address and data buses.</li> <li>Pin BM/ALE has the function of an Address Latch Enable (ALE) for operation in Intel bus mode with a multiplexed address/data bus. A falling edge on this pin selects Intel multiplexed bus mode.</li> </ul> </li> </ul>
		ALE		Address Latch Enable (mux'ed Intel bus) The address is latched by the SEROCCO-M with the falling edge of ALE. The address input pins A(7:0) pins A(15:0) must be externally connected to the data bus pins D(7:0)D(15:0). For operation of the 8-bit SEROCCO-M ( package) in a 16-bit environment, A(7:0) should be connected to address/data lines AD(8:1) of the external bus. D(7:0) interface to AD(7:0) of the external bus.



Pin No.		Symbol	In (I)	Function
	P-TQFP- 100-3		Out (O)	
	44	DS	I	<b>Data Strobe (8-bit Motorola bus mode only)</b> This active low strobe signal serves to control read/write operations.
		BHE	I	<b>Bus High Enable (16-bit Intel bus mode only)</b> This signal indicates a data transfer on the upper byte of the data bus (D15D8). In 8-bit Intel bus mode this signal has no function.
		LDS	1	Lower Data Strobe (16-bit Motorola bus mode) This active low strobe signal serves to control read/write operations. Together with signal UDS the type of bus access is determined (byte or word access at even or odd address).
				In 8-bit Intel bus mode, a pull-up resistor to $V_{DD3}$ is recommended on this pin.
	52	RD	1	<b>Read Strobe (Intel bus mode only)</b> This signal indicates a read operation. The current bus master is able to accept data on lines D(7:0) / D(15:0) during an active RD signal. In Motorola bus mode, a pull-up resistor to V <sub>DD3</sub> is recommended on this pin.
	45	R/W	1	<b>Read/Write Enable (Motorola bus mode)</b> This signal distinguishes between read and write operation. As an input it must be valid during data strobe ( $\overline{DS}$ ). In Intel bus mode, a pull-up resistor to $V_{DD3}$ is recommended on this pin.
	43	CS	1	Chip Select A low signal selects SEROCCO-M for read/write operations.



Pin No.		Symbol	In (I)	Function
	P-TQFP- 100-3		Out (O)	
	53	WR	1	Write Strobe (Intel bus mode only) This signal indicates a write operation. The current bus master presents valid data on lines D(7:0) / D(15:0) during an active WR signal. In Motorola bus mode, a pull-up resistor to $V_{DD3}$ is recommended on this pin.
	33	WIDTH	1	Width Of Bus Interface A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using BLE and BHE (Intel bus mode) or LDS and UDS (Motorola bus mode)
	55	CLK	1	<b>Clock</b> The system clock for SEROCCO-M is provided through this pin.
	20	INT/INT	O o/d	Interrupt Request The INT/INT goes active when one or more of the bits in registers ISR0ISR2 are set to '1'. A read to these registers clears the interrupt. The INT/ INT line is inactive when all interrupt status bits are reset. Interrupt sources can be unmasked in registers IMR0IMR2 by setting the corresponding bits to '0'.
	54	READY DTACK	0	<b>Ready (Intel bus mode)</b> <b>Data Transfer Acknowledge (Motorola mode)</b> During a slave access (register read/write) this signal (output) indicates, that the SEROCCO-M is ready for data transfer. The signal remains active until the data strobe ( $\overline{DS}$ in Motorola bus mode, $\overline{RD}/WR$ in Intel bus mode) and/or the chip select ( $\overline{CS}$ ) go inactive. <i>This line is tri-state when unused.</i> <i>A pull-up resistor to</i> V <sub>DD3</sub> <i>is recommended if this</i> <i>function is not used.</i>



#### Table 1 Microprocessor Bus Interface

Pin No.		Symbol	In (I) Out (O)	Function
	P-TQFP- 100-3			
	19	RESET	1	<b>Reset</b> With this active low signal the on-chip registers and state machines are forced to reset state. During Reset all pins are in a high impedance state.

#### Table 2External DMA Interface

Pin No.		Symbol	In (I)	Function
	P-TQFP- 100-3		Out (O)	
	84	DRTA	0	<b>DMA Request Transmitter Channel A</b> The transmitter on a this channel requests a DMA transfer by activating the DRTA line. The request remains active as long as the Transmit FIFO requires data transfers. The amount of data bytes to be transferred from the system memory to the serial channel (= Byte Count) must be written first to the XBCL, XBCH registers. Always blocks of data (n x 32 bytes + rest ; n=0,1,) are transferred till the Byte Count is reached. DRTA is deactivated with the beginning of the last write cycle.
	86	DRRA	0	<b>DMA Request Receiver Channel A</b> The receiver on this serial channel requests a DMA transfer by activating the DRRA line. The request remains active as long as the Receive FIFO requires data transfers, thus always blocks of data are transferred. DRRA is deactivated immediately following the falling edge of the last read cycle.



Pin No.		Symbol	In (I)	Function
	P-TQFP- 100-3		Out (O)	
	85	DACKA	1	<b>DMA Acknowledge Channel A</b> A low signal on this pin informs the SEROCCO-M that the requested DMA cycle controlled via DRTA or DRRA of this channel is in progress, i.e. the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either write or read). In conjunction with a read or write operation this input serves as Access Enable (similar to $\overline{CS}$ ) to the respective FIFOs. If DACKA is active, the input to pins A(7:0) and $\overline{CS}$ is ignored and the FIFOs are implicitly selected. <i>If not used, a pull-up resistor to</i> $V_{DD}$ <i>is required for</i> <i>this pin.</i>
	88	DRTB	0	DMA Request Transmitter Channel B (corresponding to channel A)
		GP0	I/O	<b>General Purpose Pin #0</b> If DMA support is not enabled, this pin serves as a general pupose input/output pin. <i>After reset this pin serves as a general purpose</i> <i>input. A pull-up resistor to</i> V <sub>DD3</sub> <i>is recommended.</i>
	87	DRRB	0	DMA Request Receiver Channel B (corresponding to channel A)
		GP1	I/O	<b>General Purpose Pin #1</b> If DMA support is not enabled, this pin serves as a general pupose input/output pin. <i>After reset this pin serves as a general purpose</i> <i>input. A pull-up resistor to</i> V <sub>DD3</sub> <i>is recommended.</i>
	89	DACKB	1	DMA Acknowledge Channel B (corresponding to channel A)
		GP2	I/O	<b>General Purpose Pin #2</b> If DMA support is not enabled, this pin serves as a general pupose input/output pin. A pull-up resistor to V <sub>DD3</sub> is recommended if this pin is not used.

#### Table 2 External DMA Interface



Table 5 Se		liai Fuit Filis					
Pin No.		Symbol	In (I)	Function			
	P-TQFP- 100-3		Out (O)				
	17	TxCLK A	I/O	Transmit Clock Channel A The function of this pin depends on the selected clock mode and the value of bit 'TOE' (CCR0L register, refer to Table 8 "Clock Modes of the SCCs" on Page 47).			
				<ul> <li>If programmed as Input (CCR0L.TOE='0'), either</li> <li>the transmit clock for the channel (clock mode 0a, 2a, 4, 5b, 6a), or</li> <li>a transmit strobe signal for the channel (clock mode 1)</li> <li>can be provided to this pin.</li> <li>If programmed as Output (CCR0L.TOE='1'), this pin supplies either</li> <li>the transmit clock from the baud rate generator (clock mode 0b, 2b, 3b, 6b, 7b), or</li> <li>the transmit clock from the DPLL circuit (clock mode 3a, 7a), or</li> <li>an active-low control signal marking the programmed transmit time-slot in clock mode</li> </ul>			
	13	RxCLK A	1	<ul> <li>5a.</li> <li>Receive Clock Channel A The function of this pin depends on the selected clock mode (refer to Table 8 "Clock Modes of the SCCs" on Page 47). </li> <li>A signal provided on pin RxCLKA may supply <ul> <li>the receive clock (clock mode 0, 4, 5b), or</li> <li>the receive and transmit clock (clock mode 1, 5a), or</li> <li>the clock input for the baud rate generator (clock mode 2, 3).</li> </ul> </li> </ul>			



Pin No.		Symbol	In (I)	Function
	P-TQFP- 100-3		Out (O)	
	11	CDA	1	<ul> <li>Carrier Detect Channel A</li> <li>The function of this pin depends on the selected clock mode.</li> <li>It can supply <ul> <li>either a modem control or a general purpose input (clock modes 0, 2, 3, 6, 7). If auto-start is programmed, it functions as a receiver enable</li> </ul> </li> </ul>
				<ul> <li>signal.</li> <li>or a receive strobe signal (clock mode 1).</li> <li>Polarity of CDA can be set to 'active low' with bit ICD in register CCR1H.</li> </ul>
				Additionally, an interrupt may be issued if a state transition occurs at the CDA pin (programmable feature).
		FSCA	1	Frame Sync Clock Channel A (cm 5a) When the SCC is in the time-slot oriented clock mode 5a, this pin functions as the Frame Synchronization Clock input.
		RCGA	1	<b>Receive Clock Gating Channel A (cm 4)</b> In clock mode 4 this pin is used as Receive Clock Gating signal. If no clock gating function is required, a pull-up resistor to $V_{DD3}$ is recommended.
		OSRA	1	Octet Sync Receive Channel A (cm 5b) (clock mode 5b) When the SCC is in the time-slot oriented clock mode with octet-alignment (clock mode 5b), received octets are aligned to this synchronization pulse input.

# Table 3Serial Port Pins (cont'd)



Pin No.		Symbol	In (I)	Function
	P-TQFP- 100-3		Out (O)	
	18	RTSA	0	<ul> <li>Request to Send Channel A The function of this pin depends on the settings of bits RTS, FRTS in register CCR1H. In bus configuration, RTS can be programmed to:  <ul> <li>go low during the actual transmission of a frame shifted by one clock period, excluding  collision bits. </li> <li>go low during reception of a data frame.</li> <li>stay always high (RTS disabled).</li> </ul></li></ul>
	10	CTSA	T	<b>Clear to Send Channel A</b> A low on the CTSA input enables the transmitter. Additionally, an interrupt may be issued if a state transition occurs at the CTSA pin (programmable feature). If no 'Clear To Send' function is required, a pull- down resistor to $V_{SS}$ is recommended.
		CxDA	ł	<b>Collision Data Channel A</b> In a bus configuration, the external serial bus must be connected to the corresponding CxDA pin for collision detection. A collision is detected whenever a logical '1' is driven on the open drain TxDA output but a logical '0' is detected via CxDA input.
		TCGA	1	<b>Transmit Clock Gating Channel A (cm 4)</b> In clock mode 4 these pins are used as Transmit Clock Gating signals. If no clock gating function is required, a pull-up resistor to $V_{DD3}$ is recommended.
		OSTA	I	Octet Sync Transmit Channel A (cm 5b) When the SCC is in the time-slot oriented clock mode with octet-alignment (clock mode 5b), a synchronization pulse on this input pin aligns transmit octets.

# Table 3Serial Port Pins (cont'd)


Pin No.		Symbol	In (I)	Function			
	P-TQFP- 100-3		Out (O)				
	14	TxDA	O o/d	<b>Transmit Data Channel A</b> Transmit data is shifted out via this pin. It can be configured as push/pull or open drain output characteristic via bit 'ODS' in register CCR1L.			
	12	RxDA	I	Receive Data Channel A Serial data is received on this pin.			
	96	TxCLK B	I/O	Transmit Clock Channel B (corresponding to channel A)			
	94	RxCLK B	I	Receive Clock Channel B (corresponding to channel A)			
	97	CDB FSCB RCGB OSRB	     	Carrier Detect Channel B Frame Sync Clock Channel B (cm 5a) Receive Clock Gating Channel B (cm 4) Octet Sync Receive Channel B (cm 5b) (corresponding to channel A)			
	90	RTSB	0	Request to Send Channel B (corresponding to channel A)			
	5	CTSB CxDB TCGB OSTB	     	Clear to Send Channel B Collision Data Channel B Transmit Clock Gating Channel B (cm 4) Octet Sync Transmit Channel B (cm 5b) (corresponding to channel A)			
	95	TxDB	O o/d	Transmit Data Channel B (corresponding to channel A)			



Table 3	able 3     Serial Port Pins (cont'd)						
Pin No.		Symbol	In (I)	Function			
	P-TQFP- 100-3		Out (O)				
91		RxDB I		Receive Data Channel B (corresponding to channel A)			
	87	XTAL1 XTAL2	I O	<b>Crystal Connection</b> If the internal oscillator is used for clock generation (clock modes 0b, 6, 7) the external crystal has to be connected to these pins. The internal oscillator should be powered up (GMODE:OSCPD = '0') and the signal shaper may be activated (GMODE:DSHP = '0'). Moreover, XTAL1 may be used as input for a common clock source to both SCCs, provided by an external clock generator (oscillator). In this case the oscillator unit may be powered down and it is recommended to bypass the shaper of the internal oscillator unit by setting bit 'DSHP' to '1'. <i>A pull-down resistor to</i> V <sub>SS</sub> <i>is recommended for</i> <i>pin XTAL1 if not used.</i>			

## Table 4General Purpose Pins

Pin No.		Symbol	In (I)	Function
	P-TQFP- 100-3		Out (O)	
	23 24 25 26	GP10 GP9 GP8 GP6	I/O	<b>General Purpose Pins</b> These pins serve as general purpose input/output pins.



	10	Stintena		
Pin No.		Symbol	In (I)	Function
P-TQFP- 100-3			Out (O)	
	99	TRST		<b>JTAG Reset Pin (internal pull-up)</b> For proper device operation, a reset for the boundary scan controller must be supplied to this active low pin. If the boundary scan of the SEROCCO-M is not used, this pin can be connected to V <sub>SS</sub> to keep it in reset state.
	2	ТСК	I	<b>JTAG Test Clock (internal pull-up)</b> If the boundary scan of the SEROCCO-M is not used, this pin may remain unconnected.
	100	TDI	I	JTAG Test Data Input (internal pull-up) If the boundary scan of the SEROCCO-M is not used, this pin may remain unconnected.
	1	TDO	0	JTAG Test Data Output
	46	TMS	I	JTAG Test Mode Select (internal pull-up) If the boundary scan of the SEROCCO-M is not used, this pin may remain unconnected.
	68	TEST1	I	<b>Test Input 1</b> When connected to $V_{DD3}$ the SEROCCO-M works in a vendor specific test mode. <i>This pin must be connected to</i> $V_{SS}$ .
	69	TEST2	1	<b>Test Input 2</b> When connected to $V_{DD3}$ the SEROCCO-M works in a vendor specific test mode. <i>This pin must be connected to</i> $V_{SS}$ .



Table 6   Power Pins					
Pin No.		Symbol	In (I) Out (O)	Function	
	P-TQFP- 100-3				
	3, 15, 21, 27, 35, 40, 47, 49, 56, 62, 70, 76, 82, 92, 98	V <sub>DD3</sub>	-	<b>Digital Supply Voltage</b> $3.3 \vee \pm 0.3 \vee$ All pins must be connected to the same voltage potential.	
	4, 16, 22, 28, 34, 41, 48, 50, 51, 57, 63, 71, 77, 83, 93	V <sub>SS</sub>	-	<b>Digital Ground</b> (0 V) All pins must be connected to the same voltage potential.	
	9	V <sub>DDA</sub>	-	Analog Supply Voltage $3.3 V \pm 0.3 V$ This pin supplies the on-chip oscillator of the SEROCCO-M. If no separate analog power supply is available, this pin can be directly connected to V <sub>DD3</sub> .	
	6	V <sub>SSA</sub>	-	Analog Ground (0 V) This pin supplies the ground level to the on-chip oscillator of the SEROCCO-M. If no separate analog power supply is available, this pin can be directly connected to $V_{SS}$ .	
	-	N.C.	-	Not Connected	



# 3 Functional Overview

The functional blocks of SEROCCO-M can be divided into two major domains:

- the microprocessor interface of SEROCCO-M provides access to on-chip registers and to the "user" portion of the receive and transmit FIFOs (RFIFO/XFIFO). Optionally these FIFOs can be accessed by an external 4-channel DMA controller.
- the Serial Communication Controller (SCC) is capable of processing bit-synchronous (HDLC/SDLC/bitsync PPP) and octet-synchronous (octet-sync PPP) as well as fully transparent data traffic.

Data exchange between the serial communication controller and the microprocessor interface is performed using FIFOs, decoupling these two domains.

## 3.1 Block Diagram

### Figure 8 Block Diagram





## 3.2 Serial Communication Controller (SCC)

## 3.2.1 Protocol Modes Overview

The SCC is a multi-protocol communication controller. The core logic provides different protocol modes which are listed below:

- HDLC Modes
  - HDLC Transparent Operation (Address Mode 0)
  - HDLC Address Recognition (Address Mode 1, Address Mode 2 8/16-bit)
  - Full-Duplex LAPB/LAPD Operation (Automode 8/16-bit)
  - Half-Duplex SDLC-NRM Operation (Automode 8-bit)
  - Signaling System #7 (SS7) Operation
- Point-to-Point Protocol (PPP) Modes
  - Bit Synchronous PPP
  - Octet Synchronous PPP
  - Asynchronous PPP
- ASYNC Modes
  - Asynchronous Mode
  - Isochronous Mode
- BISYNC Modes
  - Bisynchronous Mode
  - Monosynchronous Mode
- Extended Transparent Mode

A detailed description of these protocol modes is given in **Chapter 4**, starting on **Page 82**.

## 3.2.2 SCC FIFOs

Each SCC provides its own transmit and receive FIFOs to handle internal arbitration and microcontroller latencies.



# 3.2.2.1 SCC Transmit FIFO

The SCC transmit FIFO is divided into two parts of 32 bytes each ('transmit pools'). The interface between the two parts provides synchronization between the microprocessor accesses and the protocol logic working with the serial transmit clock.



## Figure 9 SCC Transmit FIFO

A 32 bytes FIFO part is accessable by the CPU/DMA controller; it accepts transmit data even if the SCC is in power-down condition (register CCR0H bit PU='0').

The only exception is a transmit data underrun (XDU) event. In case of an XDU event (e.g. after excessive bus latency), the FIFO will neither accept more data nor transfer another byte to the protocol logic. This XDU blocking mechanism prevents unexpected serial data. The blocking condition must be cleared by reading the interrupt status register ISR1 after the XDU interrupt was generated. Thus, the XDU interrupt indication should not be masked in register IMR1.

Transfer of data to the 32 byte shadow part only takes place if the SCC is in power-up condition and an appropriate transmit clock is provided depending on the selected clock mode.

Serial data transmission will start as soon as at least one byte is transferred into the shadow FIFO and transmission is enabled depending on the selected clock mode ( $\overline{CTS}$  signal active, clock strobe signal active, timeslot valid or clock gapping signal inactive).

# 3.2.2.2 SCC Receive FIFO

The SCC receive FIFO is divided into two parts of 32 bytes each. The interface between the two parts provides synchronization between the microprocessor accesses and the protocol logic working with the serial receive clock.





### Figure 10 SCC Receive FIFO

New receive data is announced to the CPU with an interrupt latest when the FIFO fill level reaches a chosen threshold level (selected with bitfield 'RFTH(1..0)' in register "CCR3H" on Page 167). Default value for this threshold level is 32 bytes in HDLC/PPP modes and 1 byte in ASYNC or BISYNC mode.

If the SCC receive FIFO is completely filled, further incoming data is ignored and a receive data overflow condition ('RDO') is detected. As soon as the receive FIFO provides empty space, receive data is accepted again after a frame end or frame abort sequence. The automatically generated receive status byte (RSTA) will contain an 'RDO' indication in this case and the next incoming frame will be received in a normal way.

Therefore no further CPU intervention is necessary to recover the SCC from an 'RDO' condition.

A "frame" with 'RDO' status might be a mixture of a frame partly received before the 'RDO' event occured and the rest of <u>this</u> frame received after the receive FIFO again accepted data and the frame was still incoming. A quite arbitrary series of data or complete frames might get lost in case of an 'RDO' event. Every frame which is completely discarded because of an 'RDO' condition generates an 'RFO' interrupt.

The SCC receive FIFO can be cleared by command 'RRES' in register CMDRH. Note that clearing the receive FIFO during operation might delete a frame end / block end indication. A frame which was already partly transferred cannot be "closed" in this case. A new frame received after receiver reset command will be appended to this "open" frame.



## 3.2.2.3 SCC FIFO Access

Figure 11 and Figure 12 illustrate byte interpretation for Intel and Motorola 16-bit accesses to the transmit and receive FIFOs.



Figure 11 XFIFO/RFIFO Word Access (Intel Mode)



Figure 12 XFIFO/RFIFO Word Access (Motorola Mode)



## 3.2.3 Clocking System

The SEROCCO-M includes an internal Oscillator (OSC) as well as two independent Baud Rate Generators (BRG) and two Digital Phase Locked Loop (DPLL) circuits.

The transmit and receive clock can be generated either

- externally, and supplied directly via the RxCLK and/or TxCLK pins (called external clock modes)
- internally, by selecting
  - the internal oscillator (OSC) and/or the channel specific baud rate generator (BRG)
  - the internal DPLL, recovering the receive (and optionally transmit) clock from the receive data stream.

(called internal clock modes)

There are a total of 14 different clocking modes programmable via bit field 'CM' in register CCR0L, providing a wide variety of clock generation and clock pin functions, as shown in **Table 8**.

The transmit clock pins (TxCLK) may also be configured as output clock and control signals in certain clock modes if enabled via bit 'TOE' in register CCR0L.

The clocking source for the DPLL's is always the internal channel specific BRG; the scaling factor (divider) of the BRG can be programmed through BRRL and BRRH registers.

There are two channel specific internal operational clocks in the SCC:

One operational clock (= transmit clock) for the transmitter part and one operational clock (= receive clock) for the receiver part of the protocol logic.

Note: The internal timers always run using the internal transmit clock.

Clock						
Туре	Source	Generation	Clock Mode			
	RxCLK Pins	Externally	0, 1, 4, 5			
Receive Clock	OSC, DPLL, BRG,	Internally	2, 3a, 6, 7a 3b, 7b			
Transmit Clock	TxCLK Pins, RxCLK Pins	Externally	0a, 2a, 4, 6a 1,5			
	OSC, DPLL, BRG/BCR, BRG	Internally	3a, 7a 2b, 6b 0b, 3b, 7b			

#### Table 7 Overview of Clock Modes



The internal structure of each SCC channel consists of a transmit protocol machine clocked with the transmit frequency  $f_{TRM}$  and a receive protocol machine clocked with the receive frequency  $f_{REC}$ .

The clocks  $f_{TRM}$  and  $f_{REC}$  are internal clocks only and need not be identical to external clock inputs e.g.  $f_{TRM}$  and TxCLK input pin.

The features of the different clock modes are summarized in Table 8.

Channel Configuration		Clock Sources				Control Sources					
Clock Mode CCR0L: CM(20)	CCR0L: SSEL	to BRG	to DPLL	to REC	to TRM	CD	R- Strobe	X- Strobe	Fram Sync Tx	e- Rx	Output via TxCLK (if CCR0L: TOE = '1')
0a 0b 1 2a 2b 3a 3b 4 5a	0 1 X 0 1 0 1 X 0	- OSC - RxCLK RxCLK RxCLK - -	- - BRG BRG BRG - -	RXCLK RXCLK DPLL DPLL BRG RXCLK RXCLK	TxCLK BRG RxCLK TxCLK BRG/16 DPLL BRG TxCLK RxCLK	CD CD CD CD CD CD CD - -	- CD - - RCG (TSAR/ PCMRX) (TSAR/	- TxCLK - - TCG (TSAX/ PCMTX) (TSAX/	- - - - - FSC	- - - - - FSC	- BRG - BRG/16 DPLL BRG - TS-Control
6a 6b 7a 7b	0 1 0 1	OSC OSC OSC OSC	- BRG BRG BRG -	DPLL DPLL DPLL BRG	TxCLK BRG/16 DPLL BRG	CD CD CD CD CD	– – – –	PCMTX) - - -	- - -	- - -	– BRG/16 DPLL BRG

### Table 8 Clock Modes of the SCCs

Note: If asynchronous operation is selected (asynchronous PPP, ASYNC mode), some clock mode frequencies can or must be divided by 16 as selected by the Bit Clock Rate bit CCR0L:BCR:

Clock Mode	f <sub>REC</sub>	f <sub>TRM</sub>
0a	f <sub>RxCLK</sub> /BCR	f <sub>TxCLK</sub>
0b	f <sub>RxCLK</sub> /BCR	f <sub>BRG</sub>
1	f <sub>RxCLK</sub> /BCR	f <sub>RxCLK</sub> /BCR
3b, 7b	f <sub>BRG</sub> /BCR	f <sub>BRG</sub> /BCR

When bit clock rate is '16' (bit BCR = '1'), oversampling (3 samples) in conjunction with majority decision is performed. BCR has no effect when using clock mode 2, 3a, 4, 5, 6, or 7a.



Note: If one of the clock modes 0b, 6 or 7 is selected, the internal oscillator (OSC) should be enabled by clearing bit GMODE:OSCPD. This allows connection of an external crystal to pins XTAL1-XTAL2. The output signal of the OSC can be used for one serial channel, or for both serial channels (independent baud rate generators and DPLLs). Moreover, XTAL1 alone can be used as input for an externally generated clock.

The first two columns of **Table 8** list all possible clock modes configured via bit field 'CM' and bit 'SSEL' in register CCR0L.

For example, clock mode 6b is choosen by writing a '6' to register CCR0L.CM(2:0) and by setting bit CCR0L.SSEL equal to '1'. The following 4 columns (grouped as 'Clock Sources') specify the source of the internal clocks. Columns REC and TRM correspond to the domain clock frequencies  $f_{REC}$  and  $f_{TRM}$ .

The columns grouped as 'Control Sources' cover additional clock mode dependent control signals like strobe signals (clock mode 1), clock gating signals (clock mode 4) or synchronization signals (clock mode 5). The last column describes the function of signal TxCLK which in some clock modes can be enabled as output signal monitoring the effective transmit clock or providing a time slot control signal (clock mode 5).

The following is an example of how to read **Table 8**:

For clock mode 6b (row '6b') the TRM clock (column 'TRM') is supplied by the baudrate generator (BRG) output divided by 16 (source BRG/16). The BRG (column 'BRG') is derived from the internal oscillator which is supplied by pin XTAL1 and XTAL2.

The REC clock (column 'REC') is supplied by the internal DPLL which itself is supplied by the baud rate generator (column 'DPLL') again.

Note: The REC clock is DPLL clock divided by 16.

If enabled by bit 'TOE' in register CCR0L the resulting transmit clock can be monitored via pin TxCLK (last column, row '6b').



The clocking concept is illustrated in a block diagram manner in the following figure: Additional control signals are not illustrated (please refer to the detailed clock mode descriptions below).



Figure 13 Clock Supply Overview



## **Clock Modes**

## 3.2.3.1 Clock Mode 0 (0a/0b)

Separate, externally generated receive and transmit clocks are supplied to the SCC via their respective pins. The transmit clock may be directly supplied by pin TxCLK (clock mode 0a) or generated by the internal baud rate generator from the clock supplied at pin XTAL1 (clock mode 0b).

In clock mode 0b the resulting transmit clock can be driven out to pin TxCLK if enabled via bit 'TOE' in register CCR0L.



Figure 14 Clock Mode 0a/0b Configuration



## 3.2.3.2 Clock Mode 1

Externally generated RxCLK is supplied to both the receiver and transmitter. In addition, a receive strobe can be connected via CD and a transmit strobe via TxCLK pin. These strobe signals work on a per bit basis. This operating mode can be used in time division multiplex applications or for adjusting disparate transmit and receive data rates.

Note: In Extended Transparent Mode, the above mentioned strobe signals provide byte synchronization (byte alignment).

This means that the strobe signal needs to be detected once only to transmit or receive a complete byte.



Figure 15 Clock Mode 1 Configuration



# 3.2.3.3 Clock Mode 2 (2a/2b)

The BRG is driven by an external clock (RxCLK pin) and delivers a reference clock for the DPLL which is 16 times of the resulting DPLL output frequency which in turn supplies the internal receive clock. Depending on the programming of register CCR0L bit 'SSEL', the transmit clock will be either an external input clock signal provided at pin TxCLK in clock mode 2a or the clock delivered by the BRG divided by 16 in clock mode 2b. In the latter case, the transmit clock can be driven out to pin TxCLK if enabled via bit 'TOE' in register CCR0L.



Figure 16 Clock Mode 2a/2b Configuration



## 3.2.3.4 Clock Mode 3 (3a/3b)

The BRG is fed with an externally generated clock via pin RxCLK. Depending on the value of bit 'SSEL' in register CCR0L the BRG delivers either a reference clock for the DPLL which is 16 times of the resulting DPLL output frequency (clock mode 3a) or delivers directly the receive and transmit clock (clock mode 3b). In the first case the DPLL output clock is used as receive and transmit clock.







## 3.2.3.5 Clock Mode 4

Separate, externally generated receive and transmit clocks are supplied via pins RxCLK and TxCLK. In addition separate receive and transmit clock gating signals are supplied via pins RCG and TCG. These gating signals work on a per bit basis.



Figure 18 Clock Mode 4 Configuration



## 3.2.3.6 Clock Mode 5a (Time Slot Mode)

This operation mode has been designed for application in time-slot oriented PCM systems.

Note: For correct operation NRZ data coding/encoding should be used.

The receive and transmit clock are common for each channel and must be supplied externally via pin RxCLK. The SCC receives and transmits only during fixed time-slots. Either one time-slot

- of programmable width (1 ... 512 bit, via TTSA and RTSA registers), and
- of programmable location with respect to the frame synchronization signal (via pin FSC)

or up to 32 time-slots

- of constant width (8 bits), and
- of programmable location with respect to the frame synchronization signal (via pin FSC)

can be selected.

The time-slot locations can be programmed independently for receive and transmit direction via TTSA/RTSA and PCMTX/PCMRX registers.

Depending on the value programmed via those registers, the receive/transmit time-slot starts with a delay of 1 (minimum delay) up to 1024 clock periods following the frame synchronization signal.

**Figure 19** shows how to select a time-slot of programmable width and location and **Figure 20** shows how to select one or more time-slots of 8-bit width.

If bit 'TOE' in register CCR0L is set, the selected transmit time-slot(s) is(are) indicated at an output status signal via pin TxCLK, which is driven to 'low' during the active transmit window.

Bit 'TSCM' in register CCR1H determines whether the internal offset counters are continuously running even if no synchronization pulse is detected at FSC signal or stopping at their maximum value.

In the continuous case the repetition rate of offset counter operation is 1024 transmit or receive clocks respectively. An FSC pulse detected earlier resets the counters and starts operation again.

In the non-continuous case the time slot assigner offset counter is stopped after the counter reached its maximum value and is started again if an FSC pulse is detected.





Figure 19 Selecting one time-slot of programmable delay and width



Note: If time-slot 0 is to be selected, the DELAY has to be as long as the PCM frame itself to achieve synchronization (at least for the 2nd and subsequent PCM frames): DELAY = PCM frame length = 1 + xTSN\*8 + xCS. xTSN and xCS have to be set appropriately.

Example: Time-slot 0 in E1 (2.048 Mbit/s) system has to be selected. PCM frame length is 256 clocks. 256 = 1 + xTSN\*8 + xCS. => xTSN = 31, xCS = 7.

Note: In extended transparent mode the width xCC of the selected time-slot has to be  $n \times 8$  bit because of character synchronization (byte alignment). In all other modes the width can be used to define windows down to a minimum length of one bit.





### Figure 20 Selecting one or more time-slots of 8-bit width

The common transmit and receive clock is supplied at pin RxCLK and the common frame synchronisation signal at pin FSC. The "strobe signals" for active time slots are generated internally by the time slot assigner block (TSA) independent in transmit and receive direction.

When the transmit and receive PCM masks are enabled, bit fields 'TCC' and 'RCC' are ignored because of the constant 8-bit time slot width.





Figure 21 Clock Mode 5a Configuration

Note: The transmit time slot delay and width is programmable via bit fields 'TTSN', 'TCS' and 'TCC' in registers TTSA0..TTSA3. The receive time slot delay and width is programmable via bit fields 'RTSN', 'RCS' and 'RCC' in registers RTSA0..RTSA3.



The following figures provide a more detailed description of the TSA internal counter operation and exceptional cases:



Figure 22 Clock Mode 5a "Continuous Mode"

60



Each frame sync pulse starts the internal offset counter with (1024 - TSdelay) whereas *TSdelay* is the configured value defining the start position. Whenever the offset counter reaches its maximum value 1024, it triggers the duration counter to start operation.

If continuous mode is selected (bit CCR1H.TSCM='0') the offset counter continues starting with value 0 until another frame sync puls is detected or again the maximum value 1024 is reached.

Once the duration counter is triggered it runs out independently from the offset counter, i.e. an active time slot period may overlap with the next frame beginning (frame sync event, refer to exception b) in Figure 22).



#### Figure 23 Clock Mode 5a "Non Continuous Mode"

If non-continuous mode is selected (bit CCR1H.TSCM='1') the offset counter is stopped on its maximum value 1024 until another frame sync puls is detected. This allows frame sync periods greater than 1024 clock cycles, but the accesible part is limited by the range of TSdelay value (1..1024) plus TSwidth (1..512) or plus 256 clock cycles if the PCM mask is selected.



## 3.2.3.7 Clock Mode 5b (Octet Sync Mode)

This operation mode has been designed for applications using Octet Synchronous PPP.

It is based on clock mode 5a, but only 8-bit (octet) wide time slot operation is supported, i.e. bits TTSA1.TEPCM and RTSA1.REPCM must be set to '1'. Clock mode 5b provides octet alignment to time slots if Octet Synchronous PPP protocol mode or extended transparent mode is selected.

Note: For correct operation NRZ data coding/encoding should be used.

The receive and transmit clocks are separate and must be supplied at pins RxCLK and TxCLK. The SCC receives and transmits only during fixed octet wide time-slots of programmable location with respect to the octet synchronization signals (via pins OSR and OST)

The time-slot locations can be programmed independently for receive and transmit direction via registers TTSA0..TTSA3 / RTSA0..RTSA3 and PCMTX0..PCMTX3 / PCMRX0..PCMRX3.

Figure 24 shows how to select one or more octet wide time-slots.

Bit 'TSCM' in register CCR1H determines whether the internal counters are continuously running even if no synchronization pulse is detected at OST/OSR signals or stopping at their maximum value.

In the continuous case the repetition rate of operation is 1024 transmit or receive clocks respectively. An OST/OSR pulse detected earlier resets the corresponding offset counter and starts operation again.

In the non-continuous case the transmit/receive time slot assigner offset counter is stopped after the counter reached its maximum value and is started again if an OST/ OSR pulse is detected.





#### Figure 24 Selecting one or more octet wide time-slots

The transmit and receive clocks are supplied at pins RxCLK and TxCLK. The Octet synchronisation signals are supplied at pins OSR and OST. The "strobe signals" for active time slots are generated internally by the time slot assigner blocks (TSA) independent in transmit and receive direction.

Bit fields 'TCC' and 'RCC' are ignored because of the constant 8-bit time slot width.





#### Figure 25 Clock Mode 5b Configuration

Note: The transmit time slot delay and width is programmable via bit fields 'TTSN', 'TCS' and 'TCC' in registers TTSA0..TTSA3. The receive time slot delay and width is programmable via bit fields 'RTSN', 'RCS' and 'RCC' in registers RTSA0..RTSA3.



# 3.2.3.8 Clock Mode 6 (6a/6b)

This clock mode is identical to clock mode 2a/2b except that the clock source of the BRG is supplied at pin XTAL1.

The BRG is driven by the internal oscillator and delivers a reference clock for the DPLL which is 16 times the resulting DPLL output frequency which in turn supplies the internal receive clock. Depending on the programming of register CCR0L bit 'SSEL', the transmit clock will be either an external input clock signal provided at pin TxCLK in clock mode 6a or the clock delivered by the BRG divided by 16 in clock mode 6b. In the latter case, the transmit clock can be driven out to pin TxCLK if enabled via bit 'TOE' in register CCR0L.



Figure 26 Clock Mode 6a/6b Configuration



# 3.2.3.9 Clock Mode 7 (7a/7b)

This clock mode is identical to clock mode 3a/3b except that the clock source of the BRG is supplied at pin XTAL1.

The BRG is driven by the internal oscillator. Depending on the value of bit 'SSEL' in register CCR0L the BRG delivers either a reference clock for the DPLL which is 16 times the resulting DPLL output frequency (clock mode 7a) or delivers directly the receive and transmit clock (clock mode 7b). In clock mode 7a the DPLL output clocks receive and transmit data.



Figure 27Clock Mode 7a/7b Configuration



## 3.2.4 Baud Rate Generator (BRG)

Each serial channel provides a baud rate generator (BRG) whose division factor is controlled by registers BRRL and BRRH. Whether the BRG is in the clocking path or not depends on the selected clock mode.

## Table 9 BRRL/BRRH Register and Bit-Fields

Register	Bit-Fields							
Offset	Pos. Name		Default	Description				
BRRL 38 <sub>H</sub> /88 <sub>H</sub>	50	BRN	0	Baud Rate Factor N range N = 063				
<mark>BRRH</mark> 39 <sub>H</sub> /89 <sub>H</sub>	118	BRM	0	Baud Rate Factor M, range M = 015				

The clock division factor k is calculated by:

 $\mathbf{k} = (\mathbf{N} + 1) \times \mathbf{2}^{\mathbf{M}}$ 

 $f_{BRG} = f_{in}/k$ 

# 3.2.5 Clock Recovery (DPLL)

The SCC offers the advantage of recovering the received clock from the received data by means of internal DPLL circuitry, thus eliminating the need to transfer additional clock information via a separate serial clock line. For this purpose, the DPLL is supplied with a 'reference clock' from the BRG which is 16 times the expected data clock rate (clock mode 2, 3a, 6, 7a). The transmit clock may be obtained by dividing the output of the BRG by a constant factor of 16 (clock mode 2b, 6b; bit 'SSEL' in register CCR0L set) or also directly from the DPLL (clock mode 3a, 7a).

The main task of the DPLL is to derive a receive clock and to adjust its phase to the incoming data stream in order to enable optimal bit sampling.

The mechanism for clock recovery depends on the selected data encoding (see "Data Encoding" on Page 73).

The following functions have been implemented to facilitate a fast and reliable synchronization:



### Interference Rejection and Spike Filtering

Two or more edges in the same directional data stream within a time period of 16 reference clocks are considered to be interference and consequently no additional clock adjustment is performed.

#### Phase Adjustment (PA)

Referring to Figure 28, Figure 29 and Figure 30, in the case where an edge appears in the data stream within the PA fields of the time window, the phase will be adjusted by 1/ 16 of the data.

### Phase Shift (PS) (NRZ, NRZI only)

Referring to **Figure 28** in the case where an edge appears in the data stream within the PS field of the time window, a second sampling of the bit is forced and the phase is shifted by 180 degrees.

Note: Edges in all other parts of the time window will be ignored.

This operation facilitates a **fast** and reliable synchronization for most common applications. Above all, it implies a very fast synchronization because of the phase shift feature: one edge on the received data stream is enough for the DPLL to synchronize, thereby eliminating the need for synchronization patterns, sometimes called preambles. However, in case of **extremely** high jitter of the incoming data stream the reliability of the clock recovery cannot be guaranteed.

The SCC offers the option to disable the Phase Shift function for NRZ and NRZI encodings by setting bit 'PSD' in register CCR0L to '1'. In this case, the PA fields are extended as shown in Figure 29.

Now, the DPLL is more insensitive to high jitter amplitudes but needs **more time** to reach the optimal sampling position. To ensure correct data sampling, preambles should precede the data information.

Figure 28, Figure 29 and Figure 30 explain the DPLL algorithms used for the different data encodings.



		Bit Cell	
DPLL Count	0 1 2 3 4	5 6 7 8 9 10	11 12 13 14 15
Correction	0 +PA	PS	-PA 0
DPLL Output			ITD01806

Figure 28 DPLL Algorithm (NRZ and NRZI Encoding, Phase Shift Enabled)



## Figure 29 DPLL Algorithm (NRZ and NRZI Encoding, Phase Shift Disabled)



	Bit Cell (FM Coding) Bit Cell (Manchester Coding)							
DPLL Count	0 1 2 3 4	5 6 7 8 9 101	1 12 13 14	15 0	1 2 3	4 5 6 7		
Correction	0 +PA	- ignore -	-PA	0	+PA	- ignore -		
Transmit Clock								
Receive Clock			]			ITD01807		

Figure 30 DPLL Algorithm for FM0, FM1 and Manchester Encoding

To supervise correct function when using bi-phase encoding, a status flag and a maskable interrupt inform about synchronous/asynchronous state of the DPLL.

## 3.2.6 SCC Timer Operation

Each SCC provides a general purpose timer e.g. to support protocol functions. In all operating modes the timer is clocked by the effective transmit clock. In clock mode 5 (time-slot oriented mode) the clock source for the timer can be optionally switched to the frame sync clock (input pin FSC) by setting bit 'SRC' in register TIMR3.

The timer is controlled by the CPU via access to registers CMDRL and TIMR0..TIMR3. The timer can be started any time by setting bit 'STI' in register CMDRL. After the timer has expired it generates a timer interrupt ('TIN').

With bit field 'CNT(2..0)' in register TIMR3 the number of automatic timer restarts can be programmed. If the maximum value '111' is entered, a timer interrupt is generated periodically, with the time period determined by bit field 'TVALUE' (registers TIMR0..TIMR3).

The timer can be stopped any time by setting bit 'TRES' in register CMDRL to '1'.

In HDLC Automode the timer is used internally for autonomous protocol functions (refer to the chapter "Automode" on Page 83). If this operating mode is selected, bit 'TMD' in register TIMR3 must be set to '1'.



# 3.2.7 SCC Serial Bus Configuration Mode

Beside the point-to-point configuration, the SCC effectively supports point-to-multipoint (pt-mpt, or bus) configurations by means of internal idle and collision detection/collision resolution methods.

In a pt-mpt configuration, comprising a central station (master) and several peripheral stations (slaves), or in a multimaster configuration, data transmission can be initiated by each station over a common transmit line (bus). In case more than one station attempts to transmit data simultaneously (collision), the bus has to be assigned to only one station. A collision-resolution procedure is implemented in the SCC. Bus assignment is based on a priority mechanism with rotating priorities. This allows each station a bus access within a predetermined maximum time delay (deterministic CSMA/CD), no matter how many transmitters are connected to the serial bus.

Prerequisites for bus operation are:

- NRZ encoding
- 'OR'ing of data from every transmitter on the bus (this can be realized as a wired-OR, using the TxD open drain capability)
- Feedback of bus information (CxD input).

The bus configuration is selected via bitfield SC(2:0) in register CCR0H.

Note: Central clock supply for each station is not necessary if both the receive and transmit clock is recovered by the DPLL (clock modes 3a, 7a). This minimizes the phase shift between the individual transmit clocks.

The bus configuration mode operates independently of the clock mode, e.g. also together with clock mode 1 (receive and transmit strobe operation).

### 3.2.8 Serial Bus Access Procedure

The idle state of the bus is identified by eight or more consecutive '1's. When a device starts transmission of a frame, the bus is recognized to be busy by the other devices at the moment the first 'zero' is transmitted (e.g. first 'zero' of the opening flag in HDLC mode).

After the frame has been transmitted, the bus becomes available again (idle).

Note: If the bus is occupied by other transmitters and/or there is no transmit request in the SCC, logical '1' will be continuously transmitted on TxD.

## 3.2.9 Serial Bus Collisions and Recovery

During the transmission, the data transmitted on TxD is compared with the data on CxD. In case of a mismatch ('1' sent and '0' detected, or vice versa) data transmission is immediately aborted, and idle (logical '1') is transmitted.



**HDLC/SDLC:** Transmission will be initiated again by the SCC as soon as possible if the first part of the frame is still present in the SCC transmit FIFO. If not, an XMR interrupt is generated.

Since a 'zero' ('low') on the bus prevails over a '1' (high impedance) if a wired-OR connection is implemented, and since the address fields of the HDLC frames sent by different stations normally differ from one another, the fact that a collision has occurred will be detected prior to or at the latest within the address field. The frame of the transmitter with the highest temporary priority (determined by the address field) is not affected and is transmitted successfully. All other stations cease transmission immediately and return to bus monitoring state.

Note: If a wired-OR connection has been realized by an external pull-up resistor without decoupling, the data output (TxD) can be used as an open drain output and connected directly to the CxD input.

For correct identification as to which frame is aborted and thus has to be repeated after an XMR interrupt has occurred, the contents of SCC transmit FIFO have to be unique, i.e. SCC transmit FIFO should not contain data of more than one frame. For this purpose new data may be provided to the transmit FIFO only after 'ALLS' interrupt status is detected.

## 3.2.10 Serial Bus Access Priority Scheme

To ensure that all competing stations are given a fair access to the transmission medium, a two-stage bus access priority scheme is supported by SEROCCO-M:

Once a station has successfully completed the transmission of a frame, it is given a lower level of priority. This priority mechanism is based on the requirement that a station may attempt transmitting only when a determined number of consecutive '1's are detected on the bus.

Normally, a transmission can start when eight consecutive '1's on the bus are detected (through pin CxD). When an HDLC frame has been successfully transmitted, the internal priority class is decreased. Thus, in order for the same station to be able to transmit another frame, ten consecutive '1's on the bus must be detected. This guarantees that the transmission requests of other stations are satisfied before the same station is allowed a second bus access. When ten consecutive '1's have been detected, transmission is allowed again and the priority class (of all stations) is increased (to eight '1's).

Inside a priority class, the order of transmission (individual priority) is based on the HDLC address, as explained in the preceding paragraph. Thus, when a collision occurs, it is always the station transmitting the only 'zero' (i.e. all other stations transmit a 'one') in a bit position of the address field that wins, all other stations cease transmission immediately.


# 3.2.11 Serial Bus Configuration Timing Modes

If a bus configuration has been selected, the SCC provides two timing modes, differing in the time interval between sending data and evaluation of the transmitted data for collision detection.

- Timing mode 1 (CCR0H:SC(2:0) = '001') Data is output with the rising edge of the transmit clock via the TxD pin, and evaluated 1/2 a clock period later at the CxD pin with the falling clock edge.
- Timing mode 2 (CCR0H:SC(2:0) = '011') Data is output with the falling clock edge and evaluated with the next falling clock edge. Thus one complete clock period is available between data output and collision detection.

# 3.2.12 Functions Of Signal **RTS** in HDLC Mode

In clock modes 0 and 1, the RTS output can be programmed via register CCR1 (SOC bits) to be active when data (frame or character) is being transmitted. This signal is delayed by one clock period with respect to the data output TxD, and marks all data bits that could be transmitted without collision (see Figure 31). In this way a configuration may be implemented in which the bus access is resolved on a local basis (collision bus) and where the data are sent one clock period later on a separate transmission line.



Figure 31 Request-to-Send in Bus Operation

Note: For details on the functions of the RTS pin refer to "Modem Control Signals (RTS, CTS, CD)" on Page 76.

# 3.2.13 Data Encoding

The SCC supports the following coding schemes for serial data:

- Non-Return-To-Zero (NRZ)
- Non-Return-To-Zero-Inverted (NRZI)
- FM0 (also known as Bi-Phase Space)
- FM1 (also known as Bi-Phase Mark)



- Manchester (also known as Bi-Phase)

The desired line coding scheme can be selected via bit field 'SC(2:0)' in register CCR0H.

# 3.2.13.1 NRZ and NRZI Encoding

**NRZ:** The signal level corresponds to the value of the data bit. By programming bit 'DIV' (CCR1L register), the SCC may invert the transmission and reception of data.

**NRZI:** A logical '0' is indicated by a transition and a logical '1' by no transition at the beginning of the bit cell.



Figure 32 NRZ and NRZI Data Encoding

# 3.2.13.2 FM0 and FM1 Encoding

**FM0:** An edge occurs at the beginning of every bit cell. A logical '0' has an additional edge in the center of the bit cell, whereas a logical '1' has none. The transmit clock precedes the receive clock by 90°.

**FM1:** An edge occurs at the beginning of every bit cell. A logical '1' has an additional edge in the center of the bit cell, a logical '0' has none. The transmit clock precedes the receive clock by 90°.





Figure 33 FM0 and FM1 Data Encoding

## 3.2.13.3 Manchester Encoding

**Manchester:** In the first half of the bit cell, the physical signal level corresponds to the logical value of the data bit. At the center of the bit cell this level is inverted. The transmit clock precedes the receive clock by 90°. The bit cell is shifted by 180° in comparison with FM coding.



Figure 34 Manchester Data Encoding



# 3.2.14 Modem Control Signals (RTS, CTS, CD)

# 3.2.14.1 RTS/CTS Handshaking

The SCC provides two pins ( $\overline{\text{RTS}}$ ,  $\overline{\text{CTS}}$ ) per serial channel supporting the standard request-to-send modem handshaking procedure for transmission control.

A transmit request will be indicated by outputting logical '0' on the request-to-send output ( $\overline{RTS}$ ). It is also possible to control the  $\overline{RTS}$  output by software. After having received the permission to transmit ( $\overline{CTS}$ ) the SCC starts data transmission.

In the case where permission to transmit is withdrawn in the course of transmission, the frame is aborted and IDLE is sent. After transmission is enabled again by re-activation of  $\overline{\text{CTS}}$ , and if the beginning of the frame is still available in the SCC, the frame will be re-transmitted (self-recovery). However, if the permission to transmit is withdrawn after the data available in the shadow part of the SCC transmit FIFO has been completely transmitted and the pool is released, the transmitter and the SCC transmit FIFO are reset, the  $\overline{\text{RTS}}$  output is deactivated and an interrupt (XMR) is generated.

- Note: For correct identification as to which frame is aborted and thus has to be repeated after an XMR interrupt has occurred, the contents of SCC transmit FIFO have to be unique, i.e. SCC transmit FIFO should not contain data of more than one frame, which could happen if transmission of a new frame is started by providing new data to the transmitter too early. For this purpose the 'All Sent' interrupt (ISR1.ALLS) has to be waited for before providing new transmit data.
- Note: In the case where permission to transmit is not required, the  $\overline{\text{CTS}}$  input can be connected directly to  $V_{ss}$  and/or bit 'FCTS' (register CCR1H) may be set to '1'.

Additionally, any transition on the  $\overline{\text{CTS}}$  input pin, sampled with the transmit clock, will generate an interrupt indicated via register ISR1, if this function is enabled by setting the 'CSC' bit in register IMR1 to '0'.





### Figure 35 RTS/CTS Handshaking

Beyond this standard  $\overline{\text{RTS}}$  function, signifying a transmission request of a frame (Request To Send), in HDLC mode the  $\overline{\text{RTS}}$  output may be programmed for a special function via SOC1, SOC0 bits in the CCR1L register. This is only available if the serial channel is operating in a bus configuration mode in clock mode 0 or 1.

- If SOC1, SOC0 bits are set to '11', the RTS output is active (= low) during the reception of a frame.
- If SOC1, SOC0 bits are set to '10', the RTS output function is disabled and the RTS pin remains always high.

# 3.2.14.2 Carrier Detect (CD) Receiver Control

Similar to the RTS/CTS control for the transmitter, the SCC supports the carrier detect modem control function for the serial receiver if the Carrier Detect Auto Start (CAS) function is programmed by setting the 'CAS' bit in register CCR1H. This function is always available in clock modes 0, 2, 3, 6, 7 via the CD pin. In clock mode 1 the CD function is not supported. See Table 8 for an overview.

If the CAS function is selected, the receiver is enabled and data reception is started when the CD input is detected to be high. If CD input is set to 'low', reception of the current character (byte) is still completed.

# 3.2.15 Local Loop Test Mode

To provide fast and efficient testing, the SCC can be operated in a test mode by setting the 'TLP' bit in register CCR2L. The on-chip serial data input and output signals (TxD,



RxD) are connected, generating a local loopback. As a result, the user can perform a self-test of the SCC.



### Figure 36 SCC Test Loop

Transmit data can be disconnected from pin TxD by setting bit TLPO in register CCR2L.

Note: A sufficient clock mode must be used for test loop operation such that receiver and transmitter operate with the same frequencies depending on the clock supply (e.g. clock mode 2b or 6b).

## 3.3 Microprocessor Interface

The communication between the CPU and SEROCCO-M is done via a set of directly accessible registers. The interface may be configured as Intel or Motorola type (refer to description of pin 'BM') with a selectable data bus width of 8 or 16 bit (refer to description of pin 'WIDTH').

The CPU transfers data to/from SEROCCO-M (via 64 byte deep FIFOs per direction and channel), sets the operating modes, controls function sequences, and gets status information by writing or reading control/status registers.

All accesses can be done as byte or word accesses if enabled. If 16-bit bus width is selected, access to the lower/upper part of the data bus is determined by signals  $\overline{BHE}$ / $\overline{BLE}$  as shown in Table 10 (Intel mode) or by the upper and lower data strobe signals  $\overline{UDS/LDS}$  as shown in Table 11 (Motorola mode).

BHE	BLE	Register Access	Data Pins Used
0	0	Word access (16 bit)	D(15:0)
0	1	Byte access (8 bit), odd address	D(15:8)

 Table 10
 Data Bus Access 16-bit Intel Mode



BHE	BLE	Register Access	Data Pins Used	
1	0	Byte access (8 bit), even address	D(7:0)	
1	1	no data transfer	-	

### Table 10 Data Bus Access 16-bit Intel Mode

### Table 11Data Bus Access 16-bit Motorola Mode

UDS	LDS	Register Access	Data Pins Used
0	0	Word access (16 bit)	D(15:0)
0	1	Byte access (8 bit), even address	D(15:8)
1	0	Byte access (8 bit), odd address	D(7:0)
1	1	no data transfer	-

Each of the two serial channels of SEROCCO-M is controlled via an identical, but completely independent register set (Channel A and B). Global functions that are common to or independent from the two serial channels are located in global registers.

## 3.4 External DMA Controller Support

The SEROCCO-M comprises a 4-channel DMA interface for fast and effective data transfers using an external DMA controller. For both serial channels, a separate DMA Request output for Transmit (DRT) and Receive direction (DRR) as well as a DMA Acknowledgement input (DACK) is provided.

The SEROCCO-M activates the DRR/DRT line as long as data transfers are needed from/to the specific FIFO (level triggered demand transfer mode of DMA controller).

It is the responsibility of the DMA controller to perform the correct amount of bus cycles. Either read cycles will be performed if the DMA transfer has been requested from the receiver, or write cycles if DMA has been requested from the transmitter. If the DMA controller provides a DMA acknowledge signal (DACK pin, input to the SEROCCO-M), each bus cycle implicitly selects the top of the specific FIFO and neither address (via A0..A7) nor chip select need to be supplied (I/O to Memory transfers). If no DACK signal is provided, normal read/write operations (providing addresses) must be performed (Memory to Memory transfers).

The SEROCCO-M deactivates the DRR/DRT line immediately after the last read/write cycle of the data transfer has started.



# 3.5 Interrupt Architecture

For certain events in SEROCCO-M an interrupt can be generated, requesting the CPU to read status information from SEROCCO-M. The interrupt line INT/INT is asserted with the output characteristics programmed in bit field 'IPC(1..0)' in register "GMODE" on Page 122 (open drain/push pull, active low/high).

Since only one interrupt request output is provided, the cause of an interrupt must be determined by the CPU by reading the interrupt status registers (GSTAR, ISR0, ISR1, ISR2, DISR, GPISL/GPISH).



### Figure 37 Interrupt Status Registers

Each interrupt indication of registers ISR0, ISR1, ISR2, DISR and GPISL/GPISH can be selectively unmasked by resetting the corresponding bit in the corresponding mask registers IMR0, IMR1, IMR2, DIMR and GPIML/GPIMH. Use of these registers depends on the selected serial mode.

If bit 'VIS' in register CCR0L is set to '1', masked interrupt status bits are visible in the interrupt status registers ISR0..ISR2. Interrupts masked in registers IMR0..IMR2 will not generate an interrupt though. A read access to the interrupt status registers clears the bits.

A global interrupt mask bit (bit 'GIM' in register GMODE) suppresses interrupt generation at all. To enable the interrupt system after reset, this bit must be set to '0'.



The Global Interrupt Status Register (GSTAR) serves as pointer to pending channel related interrupts and general purpose port interrupts.

## 3.6 General Purpose Port Pins

## **3.6.1 GPP Functional Description**

General purpose port pins are provided on pins GP6, GP8, GP9 and GP10. If external DMA support is not enabled, pins GP0...GP2 are available as general purpose pins.

Every pin is separately programmable via the General Purpose Port Direction registers GPDIRL/GPDIRH to operate as an output (bit GPnDIR='0') or as an input (bit GPnDIR='1', reset value).

If defined as output, the state of the pin is directly controlled via the General Purpose Port Data registers GPDATL/GPDATH. Read access to these registers delivers the current state of all GPP pins (input and output signals).

If defined as input, the state of the pin is monitored. The signal state of the corresponding GP pins is sampled with a rising edge of CLK and is readable via registers GPDATL/GPDATH.

## 3.6.2 GPP Interrupt Indication

The GPP block generates interrupts for transitions on each input signal. All changes may be indicated via interrupt (optional). To enable interrupt generation, the corresponding interrupt mask bit in registers GPIML/GPIMH must be reset to '0'.

Bit GPI in the gloabl interrupt status register (GSTAR) is set to '1' if an interrupt was generated by any one or more of the the general purpose port pins. The GPP pin causing the interrupt can be located by reading the GPISL/GPISH registers.



# 4 Detailed Protocol Description

The following **Table 12** provides an overview of all supported protocol modes and . The desired protocol mode is selected via bit fields in the channel configuration registers CCR0L, CCR0H, CCR2L and CCR3L.

### Table 12Protocol Mode Overview

Register CCR0H - Bit Field SM(1	Register CCR2L - Bit Field:			CCR3L	
(HDLC/SDLC/PPP protocol engine)		MDS	ADM	PPPM	ESS7
HDLC Automode	16 bit	'00'	'1'	'00'	'0'
(LAP D / LAP B / SDLC-NRM)	8 bit	'00'	'0'		
HDLC Address Mode 2	16 bit	'01'	'1'		
	8 bit	'01'	'0'		
HDLC Address Mode 1		'10'	'1'		
HDLC Address Mode 0	'10'	'0'			
Signaling System #7 (SS7) Operation		'10'	'0'	'00'	'1'
Bit Synchronous PPP Mode	'10'	'0'	'11'	'0'	
Octet Synchronous PPP Mode				'01'	
Asynchronous PPP Mode		]		'10'	
Extended Transparent Mode <sup>1)</sup>		'11'	'1'	'00'	'0'

Register CCR0H - Bit Field SM(1:0) = '11'	Register CCR0L - Bit Field:	
(ASYNC protocol engine)	BCR	
Asynchronous Mode	'1'	
Isochronous Mode	'0'	

Register CCR0H - Bit Field SM(1:0) = '10'	Register CCR0L - Bit Field:		
(BISYNC protocol engine)	EBIM		
Bisynchronous Mode	'1'		
Monosynchronous Mode	'O'		

<sup>1)</sup> Extended transparent mode is a fully bit-transparent transmission/reception mode which is treated as submode of the HDLC/SDLC/PPP block.

All modes are discussed in details in this chapter.



## 4.1 HDLC/SDLC Protocol Modes

The HDLC controller of each serial channel (SCC) can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be performed in a very flexible way satisfying almost any application specific requirements.

There are 4 different HDLC operating modes which can be selected via register bits CCR2L:MDS[1:0] and CCR2L:ADM.

## 4.1.1 HDLC Submodes Overview

The following table provides an overview of the different address comparison mechanisms in HDLC operating modes:

Mode	Address	Recognized Address Bytes for a Match:		
	Field	High Address Byte		Low Address Byte
	16 bit	FE <sub>H</sub> / FC <sub>H</sub> (1111 11 C/R 0 <sub>2</sub> )	and	RAL1
Adroop		FE <sub>H</sub> / FC <sub>H</sub> (1111 11 C/R 0 <sub>2</sub> )	and	RAL2
Mode 2		RAH1	and	RAL1
-		RAH1	and	RAL2
Auto		RAH2	and	RAL1
Mode		RAH2	and	RAL2
	8 bit	RAL1		don't care
		RAL2		don't care
Address	8 bit	FE <sub>H</sub> / FC <sub>H</sub> (1111 11 C/R 0 <sub>2</sub> )		don't care
Mode 1		RAH1		don't care
		RAH2		don't care
Address Mode 0	None	don't care		don't care

### Table 13 Address Comparison Overview

## 4.1.1.1 Automode

Characteristics: Window size 1, random message length, address recognition.

The SCC processes autonomously all numbered frames (S-, I-frames) of an HDLC protocol. The HDLC control field, I-field data of the frames and an additional status byte are temporarily stored in the SCC receive FIFO.



Depending on the selected address mode, the SCC can perform a 2-byte or 1-byte address recognition.

If a 2-byte address field is selected, the high address byte is compared with the fixed value  $FE_H$  or  $FC_H$  (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R), depending on the setting of the CRI bit in RAH1, and will be excluded from the address comparison.

Similarly, two comparison values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the SCC can be called (addressed) with 6 different address combinations, however, only the logical connection identified through the address combination RAH1/RAL1 will be processed in the auto-mode, all others in the non auto-mode. HDLC frames with address fields that do not match any of the address combinations, are ignored by the SCC.

In the case of a 1-byte address, only RAL1 and RAL2 will be used as comparison values. According to the X.25 LAPB protocol, the value in RAL1 will be interpreted as COMMAND and the value in RAL2 as RESPONSE.

The address bytes can be masked to allow selective broadcast frame recognition. For further information see "Receive Address Handling" on Page 87.

# 4.1.1.2 Address Mode 2

Characteristics: address recognition, arbitrary window size.

All frames with valid addresses (address recognition identical to auto-mode) are forwarded directly to the RFIFO.

The HDLC control field, I-field data and an additional status byte are temporarily stored in the SCC receive FIFO.

In address mode 2, all frames with a valid address are treated similarly.

The address bytes can be masked to allow selective broadcast frame recognition.

# 4.1.1.3 Address Mode 1

Characteristics: address recognition high byte.

Only the high byte of a 2-byte address field will be compared. The address byte is compared with the fixed value  $FE_H$  or  $FC_H$  (group address) as well as with two individually programmable values RAH1 and RAH2. The whole frame excluding the first address byte will be stored in the SCC receive FIFO.

The address bytes can be masked to allow selective broadcast frame recognition.



# 4.1.1.4 Address Mode 0

Characteristics: no address recognition

No address recognition is performed and each complete frame will be stored in the SCC receive FIFO.

# 4.1.2 HDLC Receive Data Processing

The following figures give an overview about the management of the received frames in the different HDLC operating modes. The graphics show the actual HDLC frame and how SEROCCO-M interprets the incoming octets. Below that it is shown which octets are stored in the RFIFO and will thus be transferred into memory.



Figure 38 HDLC Receive Data Processing in 16 bit Automode



Figure 39 HDLC Receive Data Processing in 8 bit Automode





Figure 40 HDLC Receive Data Processing in Address Mode 2 (16 bit)







Figure 42 HDLC Receive Data Processing in Address Mode 1





Figure 43 HDLC Receive Data Processing in Address Mode 0

### option 1)

The address field (8 bit address, 16 bit address or the high byte of a 16 bit address) can optionally be forwarded to the RFIFO (bit 'RADD' in register CCR3H)

### option 2)

The 16 bit or 32 bit CRC field can optionally be forwarded to the RFIFO (bit 'RCRC' in register CCR3H)

## 4.1.3 Receive Address Handling

The Receive Address Low/High Bytes (registers RAL1/RAH1 and RAL2/RAH2) can be masked on a per bit basis by setting the corresponding bits in the mask registers AMRAL1/AMRAH1 and AMRAL2/AMRAH2. This allows extended broadcast address recognition. Masked bit positions always match in comparison of the received frame address with the respective address fields in the Receive Address Low/High registers.

This feature is applicable to all HDLC protocol modes with address recognition (auto mode, address mode 2 and address mode 1). It is disabled if all bits of mask bit fields AMRAL1/AMRAH1 and AMRAL2/AMRAH2 are set to 'zero' (which is the reset value).

Detection of the fixed group address  $FE_H$  or  $FC_H$ , if applicable to the selected operating mode, remains unchanged.

As an option in the auto mode, address mode 2 and address mode 1, the 8/16 bit address field of received frames can be pushed to the receive data buffer (first one/two bytes of the frame). This function is especially useful in conjunction with the extended broadcast address recognition. It is enabled by setting control bit 'RADD' in register CCR3H.

# 4.1.4 HDLC Transmit Data Processing

Two different types of frames can be transmitted:

I-frames and



### transparent frames

#### as shown below.



### Figure 44 SCC Transmit Data Flow (HDLC Modes)

For transmission of I-frames (selected via transmit command 'XIF' in register CMDRL), the address and control fields are generated autonomously by the SCC and the data in the corresponding transmit data buffer is entered into the information field of the frame. This is possible only if the SCC is operated in Automode.

For (address-) transparent frames, the address and the control fields have to be entered in the transmit data buffer by software. This is possible in all operating modes and used also in auto-mode for sending U-frames.

If bit 'XCRC' in register CCR2H is set, the CRC checksum will not be generated internally. The checksum has to be provided via the transmit data buffer as the last two



or four bytes by software. The transmitted frame will be closed automatically only with a (closing) flag.

Note: The SCC does not check whether the length of the frame, i.e. the number of bytes, to be transmitted makes sense according the HDLC protocol or not.

# 4.1.5 Shared Flags

If the 'Shared Flag' feature is enabled by setting bit 'SFLG' in register CCR1L the closing flag of a previously transmitted frame simultaneously becomes the opening flag of the following frame if there is one already available in the SCC transmit FIFO.

In receive direction the SCC always expects and handles 'Shared Flags'. 'Shared Zeroes' of consecutive flags are also supported.

## 4.1.6 One Bit Insertion

Similar to the zero bit insertion (bit stuffing) mechanism, as defined by the HDLC protocol, the SCC offers a feature of inserting/deleting a 'one' after seven consecutive 'zeros' into the transmit/receive data stream, if the serial channel is operating in bus configuration mode. This method is useful if clock recovery is performed by DPLL.

Since only NRZ data encoding is supported in a bus configuration, there are possibly long sequences without edges in the receive data stream in case of successive '0's received, and the DPLL may lose synchronization.

Enabling the one bit insertion feature by setting bit 'OIN' in register CCR2H, it is guaranteed that at least after

- 5 consecutive '1's a '0' will appear (bit stuffing), and after
- 7 consecutive '0's a '1' will appear (one insertion)

and thus a correct function of the DPLL is ensured.

Note: As with the bit stuffing, the 'one insertion' is fully transparent to the user, but it is not in accordance with the HDLC protocol, i.e. it can only be applied in proprietary systems using circuits that also implement this function, such as the PEB 20542 and and PEB 20525.

# 4.1.7 **Preamble Transmission**

If enabled via bit 'EPT' in register CCR2H, a programmable 8-bit pattern is transmitted with a selectable number of repetitions after Interframe Timefill transmission is stopped and a new frame is ready to be sent out. The 8 bit preamble pattern can be programmed in register PREAMB and the repetition time in bit field 'PRE' of register CCR2H.

Note: Zero Bit Insertion is disabled during preamble transmission.



# 4.1.8 CRC Generation and Checking

In HDLC/SDLC mode, error protection is done by CRC generation and checking.

In standard applications, CRC-CCITT algorithm is used. The Frame Check Sequence at the end of each frame consists of two bytes of CRC checksum.

If required, the CRC-CCITT algorithm can be replaced by the CRC-32 algorithm, enabled via bit 'C32' in register CCR1L. In this case the Frame Check Sequence consists of four bytes.

Optionally the internal handling of received and transmitted CRC checksum can be influenced via control bits 'RCRC', 'DRCRC' in register CCR3H and 'XCRC' in register CCR2H.

### **Receive direction:**

If not disabled by setting bit 'DRCRC' (register CCR3H), the received CRC checksum is always assumed to be in the 2 (CRC-CCITT) or 4 (CRC-32) last bytes of a frame, immediately preceding a closing flag. If bit 'RCRC' is set, the received CRC checksum is treated as data and will be forwarded to the RFIFO, where it precedes the frame status byte. Nevertheless the received CRC checksum is additionally checked for correctness. If CRC checking is disabled with bit CCR3H:DRCRC, the limits for 'Valid Frame' check are modified accordingly (refer to description of the Receive Status Byte, RSTA:VFR).

### Transmit direction:

If bit 'XCRC' is set, the CRC checksum is not generated internally. The checksum has to be provided via the transmit data buffer by software. The transmitted frame will only be closed automatically with a (closing) flag.

Note: The SCC does not check whether the length of the frame, i.e. the number of bytes, to be transmitted makes sense or not according the HDLC protocol.

## 4.1.9 Receive Length Check Feature

The SCC offers the possibility to supervise the maximum length of received frames and to terminate data reception in the case that this length is exceeded.

This feature is controlled via the special Receive Length Check Registers RLCRL/RLCRH.

The function is enabled by setting bit 'RCE' (Receive Length Check Enable) and the maximum frame length to be checked is programmed via bit field 'RL'. The maximum receive length can be determined as a multiple of 32-byte blocks as follows:

MAX\_LENGTH =  $(RL + 1) \times 32$ ,

where RL is the value written to bit field 'RL'. Thus, the maximum length of receive frames can be programmed between 32 and 65536 bytes.

All frames exceeding this length are treated as if they had been aborted by the remote station, i.e. the CPU is informed via



- an 'RME' interrupt generated by the SCC, and
- the receive abort indication 'RAB' in the Receive Status Byte (RSTA).

Additionally an optional 'FLEX' interrupt is generated prior to 'RME', indicating that the maximum receive frame length was exceeded.

Receive operation continues with the beginning of the next receive frame.

## 4.2 Point-to-Point Protocol (PPP) Modes

PPP (as described in RFC1662) can work over 3 modes: asynchronous HDLC, synchronous HDLC, and octet synchronous. The SEROCCO-M supports asynchronous HDLC PPP over ISDN or DDS circuits as well as bit and octet synchronous HDLC PPP for use over dial-up connections. The octet synchronous mode of PPP protocol (RFC 1662) supports PPP over SONET applications.

Both the asynchronous HDLC PPP mode, as well as the synchronous HDLC PPP modes are submodes of the HDLC mode. Either mode is selected by configuring SEROCCO-M for the standard HDLC mode. In addition the appropriate PPP mode is selected via bit field 'PPPM' in register CCR2L.

The SEROCCO-M provides logic to convert an HDLC frame to an ASYNC character stream with the specified mapping functions. Layer 3 PPP functions are normally implemented in software.

The PPP-support hardware allows software to perform segmentation and reassembly of PPP payloads, and allows SEROCCO-M to perform the asynchronous HDLC PPP **or** the synchronous HDLC PPP protocol conversions as required for the network interface.

# 4.2.1 Bit Synchronous PPP

The SEROCCO-M transmits a data block, inserts HDLC Header (Opening Flag), and appends the HDLC Trailer (CRC, Ending Flag). Zero-bit stuffing algorithm is also performed. No character mapping is performed. The bit-synchronous PPP mode differs from the HDLC mode (address mode 0) only in the abort sequence:

HDLC requires at least 7 consecutive '1' bits as abort sequence, whereas PPP requires at least 15 '1' bits.

For receive operation SEROCCO-M monitors the incoming data stream for the Opening Flag (7E Hex) to identify the beginning of a HDLC packet. Subsequent bytes are part of data and are processed as normal HDLC packet including checking of CRC.

# 4.2.2 Octet Synchronous PPP

The SEROCCO-M transmits a data block, inserts HDLC Header (Opening Flag), and appends the HDLC Trailer (CRC, Ending Flag). Beside this standard HDLC operation, zero-bit stuffing is not performed, but character mapping is performed.



For receive operation SEROCCO-M monitors the incoming data stream for the Opening Flag (7E Hex) to identify the beginning of a HDLC packet. Subsequent bytes are part of data and are processed as normal HDLC packet including checking of CRC. Received mapped characters are unmapped.

The abort sequence consists of the control escape character  $7D_H$  followed by a flag character  $7E_H$  (not stuffed). Between two frames, the interframe time fill character should be programmed to  $7E_H$  by setting bit CCR2H:ITF to '1'.

Octet alignment is provided through the synchronization pulses in clock mode 5b.

# 4.2.3 Asynchronous PPP

For transmit operation, SEROCCO-M inserts the HDLC header (Opening Flag), and appends the HDLC trailer (CRC, Ending Flag), surrounding the transmit data read from the XFIFO. Each octet (including HDLC framing flags and idle flags) is converted into async character format (1 start, 8 data bits, 1 stop bit) and then transmitted using the asynchronous character formatter block. Character mapping like in Octet Synchronous PPP mode is performed.

In receive direction any async character is transferred into SEROCCO-M's ASYNC Character De-Formatting logic block, where it is translated back into the original information octet. Mapped characters are unmapped and the information octets are then transferred to the RFIFO (as in Octet Synchronous PPP mode).

# 4.2.4 Data Transparency in PPP Mode

When transporting bit-files (as opposed to text files), or compressed files, the characters could easily represent MODEM control characters (such as CTRL-Q, CTRL-S) which the MODEM would not pass through. SEROCCO-M maintains an Async Control Character Map (ACCM) for characters 00-1F Hex. Whenever there is a mapped character in the data stream, the transmitter precedes that character with a control-escape character of  $7D_{H}$ . After the control-escape, the character itself is transmitted with bit 5 inverted. character e.g.  $13_{H}$  is mapped to  $7D_{H}$ ,  $33_{H}$ ).

At the receive end, a  $7D_H$  character is discarded and the following character is modified by inverting bit 5 (e.g. if  $7D_H$ ,  $33_H$  is received, the  $7D_H$  is discarded and the  $33_H$  is changed to  $13_H$  the original character). This character is received into RFIFO and included in CRC calculation, even if it is not mapped.

The 32 lookup octet values  $(00_{H}-1F_{H})$  are stored within the on-chip registers ACCM0..3.

In addition to the ACCM, 4 user programmable characters (especially outside the range 00-1F Hex) can also be mapped using the control-escape sequence described above. These characters are specified in registers UDAC0..3.

The receiver discards all characters which are received unmapped, but expected to be mapped because of ACCM0..3 and UDAC0..3 register contents. If this occurs within an



HDLC frame, the unexpected characters are discarded before forwarded to the receive CRC checking unit.

 $7D_{H}$  (control-escape) and  $7E_{H}$  (flag) octets in the data stream are mapped in general. The sequence of mapping control logic is:

1.  $7D_H$  and  $7E_H$  octets,

- 2. ACCM0..3,
- 3. UDAC0..3.

This mechanism is applied to asynchronous HDLC PPP mode as well as to octet synchronous HDLC PPP mode.





### Figure 45 PPP Mapping/Unmapping Example



# 4.3 Extended Transparent Mode

Characteristics: fully transparent

When programmed in the extended transparent mode via the CCR2L register (bits MDS1, MDS0, ADM = '111'), the SCC performs fully transparent data transmission and reception without HDLC framing, i.e. without

- FLAG insertion and deletion
- CRC generation and checking
- bit stuffing.

This feature can be profitably used e.g. for:

- user specific protocol variations
- line state monitoring, or
- test purposes, in particular for monitoring or intentionally generating HDLC protocol rule violations (e.g. wrong CRC)

Character or octet boundary synchronization can be achieved by using clock mode 5 or clock mode 1 with an external receive strobe input to pin CD.

Note: Data is transmitted and received with the least significant bit (LSB) first.

# 4.4 Asynchronous (ASYNC) Protocol Mode

## 4.4.1 Character Framing

Character framing is achieved by start and stop bits. Each data character is preceded by one Start bit and terminated by one or two stop bits. The character length is selectable from 5 up to 8 bits. Optionally, a parity bit can be added which complements the number of ones to an even or odd quantity (even/odd parity). The parity bit can also be programmed to have a fixed value (Mark or Space). The character format configuration is performed via appropriate bit fields in registers CCR3L/CCR3H. Figure 46 shows the asynchronous character format.





Figure 46 Asynchronous Character Frame

## 4.4.2 Data Reception

The SCC offers the flexibility to combine clock modes, data encoding and data sampling in many different ways. However, only definite combinations make sense and are recommended for correct operation:

# 4.4.2.1 Asynchronous Mode

Prerequisites:

- Bit clock rate 16 selected (register CCR0L, bit BCR = '1')
- Clock mode 0, 1, 3b, 4, or 7b selected (register CCR0L, bit field 'CM')
- NRZ data encoding selected (register CCR0H, bit field 'SC')

The receiver which operates with a clock rate equal to 16 times the nominal (expected) data bit rate, synchronizes itself to each character by detecting and verifying the start bit. Since character length, parity and stop bit length is known, the ensuing valid bits are sampled. Oversampling (3 samples) around the nominal bit center in conjunction with majority decision is provided for every received bit (including start bit).

The synchronization lasts for one character, the next incoming character causes a new synchronization to be performed. As a result, the demand for high clock accuracy is reduced. Two communication stations using the asynchronous procedure are clocked independently, their clocks need not be in phase or locked to exactly the same frequency but, in fact, may differ from one another within a certain range.

# 4.4.2.2 Isochronous Mode

Prerequisites:

• Bit clock rate 1 selected (register CCR0L bit BCR = '0')



• Clock mode 2, 3a, 6, or 7a (DPLL mode) has to be used in conjunction with FM0, FM1 or Manchester encoding (register CCR0L/CCR0H bit fields 'CM' and 'SC').

The isochronous mode uses the asynchronous character format. However, each data bit is only sampled once (no oversampling).

In clock modes 0,1 and 4, the input clock has to be externally phase locked to the data stream. This mode allows much higher transfer rates. Clock modes 3b and 7b are not recommended due to difficulties with bit synchronization when using the internal baud rate generator.

In clock modes 2, 3a, 6, and 7a, clock recovery is provided by the internal DPLL. Correct synchronization of the DPLL is achieved if there are enough edges within the data stream, which is generally ensured only if Bi-Phase encoding (FM0, FM1 or Manchester) is used.

# 4.4.2.3 Storage of Receive Data

If the receiver is enabled, received data is stored in the SCC receive FIFO (the LSB is received first). Moreover, the CD input may be used to control data reception. Character length, number of stop bits and the optional parity bit are checked. Storage of parity bits can be disabled. Errors are indicated via interrupts. Additionally, the character specific error status (framing and parity) can optionally be stored in the SCC receive FIFO.

Filling of the the SCC receive FIFO is controlled by

- a programmable threshold level (bit field 'RFTH' in register CCR3H),
- the selected data format (bit 'RFDF' in register CCR3H),
- the parity storage selection (bit 'DPS' in register CCR3H),
- detection of the programmable Termination Character (bit 'TCDE' in register CCR3L and bit field 'TC' in register TCR).

Additionally, the time-out event interrupt as an optional status information indicates that a certain time (refer to register TOLEN) has elapsed since the reception of the last character.

# 4.4.3 Data Transmission

The selection of asynchronous or isochronous operation has no further influence on the transmitter. The bit clock rate is solely a dividing factor for the selected clock source.

Transmission of the contents of the SCC transmit FIFO starts after the 'XF' command is issued (the LSB is sent out first). Further data is requested by an 'XPR' interrupt (or by DMA). The character frame for each character, consisting of start bit, the character itself with defined character length, optionally generated parity bit and stop bit(s) is assembled.

After finishing transmission (indicated by the 'ALLS' interrupt), IDLE sequence (logical '1') is transmitted on pin TxD.



Additionally, the  $\overline{\text{CTS}}$  signal may be used to control data transmission.

### 4.4.4 Special Functions

### 4.4.4.1 Break Detection/Generation

### Break generation:

On issuing the transmit break command (bit 'XBRK' in register CCR3L), the TxD pin is immediately forced to physical '0' level with the next following transmit clock edge, and released with the first transmit clock edge after this command is reset again by software.

### Break detection:

The SCC recognizes the break condition upon receiving consecutive (physical) '0's for the defined character length, the optional parity and the selected number of stop bits ('zero' character and framing error). The 'zero' character is not pushed to RFIFO. If enabled, the 'Break' interrupt (BRK) is generated.

The break condition will be present until a '1' is received which is indicated by the 'Break Terminated' interrupt (BRKT).

## 4.4.4.2 In-band Flow Control by XON/XOFF Characters

### Programmable XON and XOFF characters:

The XON/XOFF registers contain the programmable values for XON and XOFF characters. The number of significant bits in a register is determined by the programmed character length via bit field 'CHL' in register CCR3L.

Additionally, two programmable eight-bit values in registers MXON and MXOFF serve as masks for the characters XON and XOFF, respectively:

A '1' in any mask bit position has the effect that no comparison is performed between the corresponding bits in the received characters ('don't cares') and the XON/XOFF value. At RESET, the masks are zero'ed, i.e. all bit positions will be compared.

A received character is considered to be recognized as a valid XON or XOFF character

- if it is correctly framed (correct length),
- if its bits match the ones in the XON or XOFF registers over the programmed character length,
- if it has correct parity (if applicable).

Received XON and XOFF characters are stored in the SCC receive FIFO, as any other characters, when bit 'DXS' is set to '0' in register CCR3L. Otherwise they are not stored in the receive FIFO.



### In-Band Flow Control of Transmitted Characters:

Recognition of an XON or XOFF character causes always a corresponding maskable interrupt status to be generated.

Further action depends on the setting of control bit 'FLON' (Flow Control On) in register CCR2H:

0: No further action is automatically taken by the SCC.

1: The reception of an XOFF character automatically turns off the transmitter after the currently transmitted character (if any) has been shifted out completely (entering XOFF state). The reception of an XON character automatically makes the transmitter resume transmitting (entering XON state).

After hardware RESET, bit CCR2H:FLON is '0'.

When bit CCR2H:FLON is programmed from '0' to '1', the transmitter is first in the 'XON state', until an XOFF character is received.

When bit CCR2H:FLON is programmed from '1' to '0', the transmitter always goes in the 'XON state', and transmission is only controlled by the user and by the CTS signal input.

The in-band flow control of the transmitter via received XON and XOFF characters can be combined with control via  $\overline{\text{CTS}}$  pin, i.e. the effect of the  $\overline{\text{CTS}}$  pin is independent of whether in-band control is used or not. The transmitter is enabled only if  $\overline{\text{CTS}}$  is 'low' and XON state has been reached.

### Transmitter Status Bit:

The status bit 'Flow Control Status' (bit 'FCS' in register STARL) indicates the current state of the transmitter, as follows:

0: if the transmitter is in XON state,

1: if the transmitter is in XOFF state.

Note: The transmitter cannot be turned off by software without disrupting data possibly remaining in the transmit FIFO.

### Flow Control for Received Data:

After writing a character value to register TICR (Transmit Immediate Character, 'TIC') its character contents is inserted into the outgoing character stream

- immediately upon writing this register by the microprocessor if the transmitter is in IDLE state. If no further characters (transmit FIFO empty) are to be transmitted, i.e. the transmitter returns to IDLE state after transmission of the 'TIC' and an ALLS (All Sent) interrupt will be generated.
- after the end of a character currently being transmitted if the transmitter is not in IDLE state. This does not affect the contents of the transmit FIFO. Transmission of characters from transmit FIFO is resumed after the 'TIC' is send out.



Transmission via this register is possible even when the transmitter is in XOFF state (however,  $\overline{\text{CTS}}$  must be 'low').

The 'TIC' value is an eight-bit value. The number of significant bits is determined by the programmed asynch character length via bit field 'CHL' in register CCR3L. Parity value (if programmed) and selected number of stop bits are automatically appended, equal to the characters provided via the transmit data buffer. The usage of 'TIC' is independent of in-band flow control mechanism, i.e. is not affected by bit 'FLON' in register CCR2H anyway.

To control multiple accesses to register TICR, an additional status bit STARL:TEC (TIC Executing) is provided which signals that the transmission command of currently programmed 'TIC' is accepted but not yet completely executed. Further access to register TICR is only allowed if bit STARL:TEC is '0' again.

# 4.4.4.3 Out-of-band Flow Control

### Transmitter:

The transmitter output is enabled if  $\overline{\text{CTS}}$  signal is 'LOW' AND the XON state is reached in case of in-band flow control is enabled. If the in-band flow control is disabled (CCR2H:FLON = '0'), the transmitter is only controlled by the  $\overline{\text{CTS}}$  signal.

Nevertheless setting bit CCR1H:FCTS = '1' allows the transmitter to send data independent of the condition of the CTS signal, the in-band flow control (XON/XOFF) mechanism would still be operational if enabled via bit CCR2H:FLON = '1'.

### Receiver:

For some applications it is desirable to provide means of out-of-band flow control to indicate to the far end transmitter that the local receiver's buffer is getting full.

This flow control can be used between two DTEs as shown in **Figure 47** and between a DTE and a DCE (MODEM) as shown in **Figure 48** that supports this kind of bi-directional flow control.

Setting bit CCR1H:FRTS = '1' and CCR1H:RTS = '0' invokes this out-of-band flow control for the receiver. When the shadow part of the receive FIFO has reached a set threshold of 28 bytes, the RTS signal is forced inactive (high). When the shadow part of the receive FIFO is empty, the RTS is re-asserted (low). Note that the data is immediately transferred from the shadow receive FIFO to the user accessible RFIFO (as long as there is space available). So when the shadow receive FIFO reaches the 28 bytes threshold, there is 4 more byte storage available before overflow can occur. This allows sufficient time for the far end transmitter to react to the change in the RTS signal and stop sending more data.

**Figure 47** shows the connection between two SCC devices as DTEs. The  $\overline{\text{RTS}}$  of DTE-A (SCC) feeds the  $\overline{\text{CTS}}$  input of the second DTE-B (another SCC). For example while



DTE-A is receiving data and its receive FIFO threshold is reached, the RTS signal goes in-active 'HIGH' forcing the CTS of DTE-B to become in-active indicating that transmission has to stop after finishing the current character. Both DTE devices should also be using the CTS signal to flow control their transmitters. When the shadow receive FIFO in DTE-A is cleared its RTS goes active (low) and this signals the far end DTE-B to resume transmission. Data flow control from DTE-B to DTE-A works in the same way.



Figure 47 Out-of-Band DTE-DTE Bi-directional Flow Control



Figure 48 shows an SCC as a DTE connected to a DCE (MODEM equipment).

The  $\overline{\text{RTS}}_A$  feeds the  $\overline{\text{RTS}}_B$  input of the DCE (MODEM equipment) that supports bidirectional flow control. So when the DTE-A's receiver threshold is reached, the  $\overline{\text{RTS}}_A$ signal goes inactive 'HIGH' which is sensed by the DCE and it stops transmitting. Similarly if the DCE's receiver threshold is reached, it deactivates the  $\overline{\text{CTS}}_B$  ('HIGH') and causes the DTE to stop transmission. These types of DCEs have fairly deep buffers to ensure that it can continue to receive data from the line even though it is unable to pass the data to the DTE for short periods of time. Note that a SCC can also be used in the DCE equipment as shown. Exchange of signals (e.g.  $\overline{\text{RTS}}$  to  $\overline{\text{CTS}}$ ) is necessarily inside the DCE equipment.



### Figure 48 Out-of-Band DTE-DCE Bi-directional Flow Control

 $\overline{\text{RTS}}$  and  $\overline{\text{CTS}}$  are used to indicate when the local receiver's buffer is nearly full. This alerts the far end transmitter to stop transmission.

The combination of transmitter and receiver out-of-band control features mentioned above enables data to be exchanged between two devices without software intervention for flow control.

## 4.5 BISYNC Protocol Mode

### 4.5.1 Character Framing

Character oriented protocols achieve synchronization between transmitting and receiving station by means of special SYN characters. Two examples are the MONOSYNC and IBM's BISYNC procedures. BISYNC has two starting SYN characters



while MONOSYNC uses only one SYN. Figure 49 gives an example of the message format.



Figure 49 BISYNC Message Format

The SYN character, its length, the length of data characters and additional parity generation are programmable:

- 1 SYN character with 6 or 8 bit length (MONOSYNC), programmable via register SYNCL.
- 2 SYN characters with 6 or 8 bit length each (BISYNC), programmable via registers SYNCH/SYNCL.
- Data character length may vary from 5 to 8 bits (bit field 'CHL' in register CCR3L).
- Parity information (even/odd parity, mark, space) may be appended to the character (bit 'PARE' and bit field 'PAR' in register CCR3H).

# 4.5.2 Data Reception

The receiver is generally activated by setting bit 'RAC' in register CCR3L. Additionally, the CD signal may be used to control data reception depending on the selected clock mode. After issuing the HUNT command, the receiver monitors the incoming data stream for the presence of specified SYN character(s). However, data reception is still disabled. If synchronization is gained by detecting the SYN character(s), an SCD interrupt is generated and **all** following data is pushed to the receive FIFO, i.e. control sequences, data characters and optional CRC frame checking sequence (the LSB is received first). In normal operation, SYN characters are excluded from storage to receive FIFO. SYN character length can be specified independently of the selected data character length. If required, the character parity bit and/or parity status is stored together with each data byte in the receive FIFO.

As an option, the loading of SYN characters in receive FIFO may be enabled by setting the bit 'SLOAD' in register CCR3L. Note that in this case SYN characters are treated as data. Consequently, for correct operation it must be guaranteed that SYN character



length equals the character length + optional parity bit. This is the user's responsibility by appropriate software settings.

Filling of the receive FIFO is controlled by a programmable threshold level.

Reception is stopped if

- 1. the receiver is deactivated by resetting the bit CCR3L:RAC bit, or
- the CD signal goes inactive (if Carrier Detect Auto Start is enabled in register CCR1H), or
- 3. the CMDRH:HUNT command is issued again, or
- 4. the Receiver Reset command (CMDRH:RRES) is issued, or
- 5. a programmed Termination Character has been found (optional).

On actions 1. and 2., reception remains disabled until the receiver is activated again. After this is done, and generally in cases 3. and 4., the receiver returns to the (non-synchronized) Hunt state. In case 5. a HUNT command has to be issued. Reception of data is internally disabled until synchronization is regained.

Note: Further checking of frame length, extraction of text or data information and verifying the Frame Checking Sequence (e.g. CRC) has to be done by the microprocessor.

## 4.5.3 Data Transmission

Transmission of data provided in the memory is started after the Transmit Frame ('XF') command is issued (the LSB is sent out first). Additionally, the CTS signal may be used to control data transmission. The message frame is assembled by appending all data characters to the specified SYN character(s) until Transmit Message End condition is detected ('XME' command in interrupt mode or, in DMA mode, when the number of characters specified in XBCL/XBCH have been transferred). Internally generated parity information may be added to each character (SYN, CRC and Preamble characters are excluded).

If enabled via CRC Append bit (bit 'CAPP' in register CCR2H), the internally calculated CRC checksum (16 bit) is added to the message frame. Selection between CRC-16 and CRC-CCITT algorithms is provided.

Note: - Internally generated SYN characters are always excluded from CRC calculation, - CRC checksum (2 bytes) is sent without parity.

The internal CRC generator is automatically initialized before transmission of a new frame starts. The initialization value is selectable.

After finishing data transmission, interframe-time-fill (SYN characters or IDLE) is automatically sent.

A transmit data underrun condition in the XFIFO is indicated with an 'XDU' interrupt. Nevertheless, transmission continues inserting SYN characters into the data stream until



new data is available in the transmit FIFO. Inserted SYN characters are not part of the frame and thus not used for CRC calculation.

## 4.5.4 Special Functions

## 4.5.4.1 Preamble Transmission

If enabled via register CCR2H, a programmable 8-bit pattern (register PREAMB) is transmitted with a selectable number of repetitions after interframe-time-fill transmission is stopped and a new frame is ready to be sent out.

Note: If the preamble pattern equals the SYN pattern, reception is triggered by the preamble.

## 4.6 **Procedural Support (Layer-2 Functions)**

When operating in the auto mode, the SCC offers a high degree of protocol support. In addition to address recognition, the SCC autonomously processes all (numbered) S- and I-frames (window size 1 only) with either normal or extended control field format (modulo-8 or modulo-128 sequence numbers – selectable via register CCR2H bit 'MCS').

The following functions will be performed:

- updating of transmit and receive counter
- evaluation of transmit and receive counter
- processing of S commands
- flow control with RR/RNR
- generation of responses
- recognition of protocol errors
- transmission of S commands, if acknowledgement is not received
- continuous status query of remote station after RNR has been received
- programmable timer/repeater functions.

In addition, all unnumbered frames are forwarded directly to the processor. The logical link can be initialized by software at any time (Reset HDLC Receiver by RRES command in register CMDRH).

Additional logical connections can be operated in parallel by software.

# 4.6.1 Full-Duplex LAPB/LAPD Operation

Initially (i.e. after RESET), the LAP controllers of the two serial channels are configured to function as a combined (primary/secondary) station, where they autonomously perform a subset of the balanced X.25 LAPB/ISDN LAPD protocol.



### **Reception of Frames:**

The logical processing of received S-frames is performed by the SCC without interrupting the host. The host is merely informed by interrupt of status changes in the remote station (receiver ready / receiver not ready) and protocol errors (unacceptable N(R), or S-frame with I-field).

I-frames are also processed autonomously and checked for protocol errors. The I-frame will not be accepted in the case of sequence errors (no interrupt is forwarded to the host), but is immediately confirmed by an S-response. If the host sets the SCC into a 'receive not ready' status, an I-frame will not be accepted (no interrupt) and an RNR response is transmitted. U-frames are always stored in the RFIFO and forwarded directly to the host. The logical sequence and the reception of a frame in auto mode is illustrated in **Figure 50**.

Note: The state variables N(S), N(R) are evaluated within the window size 1, i.e. the SCC checks only the least significant bit of the receive and transmit counter regardless of the selected modulo count.









### Transmission of Frames:

The SCC autonomously transmits S commands and S responses in the auto mode. Either transparent or I-frames can be transmitted by the user. The software timer has to be operated in the internal timer mode to transmit I-frames. After the frame has been transmitted, the timer is self-started, the XFIFO is inhibited, and the SCC waits for the arrival of a positive acknowledgement. This acknowledgement can be provided by means of an S- or I-frame.

If no positive acknowledgement is received during time  $t_1$ , the SCC transmits an Scommand (p = '1'), which must be answered by an S-response (f = '1'). If the S-response is not received, the process is performed n1 times (in HDLC known as N2, refer to register TIMR3).

Upon the arrival of an acknowledgement or after the completion of this poll procedure the XFIFO is enabled and an interrupt is generated. Interrupts may be triggered by the following:

- message has been positively acknowledged (ALLS interrupt)
- message must be repeated (XMR interrupt)
- response has not been received (TIN interrupt).

In automode, only when the ALLS interrupt has been issued data of a new frame may be provided to the XFIFO!

Upon arrival of an RNR frame, the software timer is started and the status of the remote station is polled periodically after expiration of  $t_1$ , until the status 'receive ready' has been detected. The user is informed via the appropriate interrupt. If no response is received after n1 times, a TIN interrupt, and  $t_1$  clock periods thereafter an ALLS interrupt is generated and the process is terminated.

Note: The internal timer mode should only be used in the auto mode.

Transparent frames can be transmitted in all operating modes.






2000-09-14



#### Examples

The interaction between SCC and the host during transmission and reception of I-frames is illustrated in the following two figures. The flow control with RR/RNR of I-frames during transmission/reception is illustrated in **Figure 52**. Both, the sequence of the poll cycle and protocol errors are shown in **Figure 53**.



Figure 52 Transmission/Reception of I-Frames and Flow Control



Figure 53 Flow Control: Reception of S-Commands and Protocol Errors



Table 14

#### **Detailed Protocol Description**

#### **Protocol Error Handling:**

Depending on the error type, erroneous frames are handled according to **Table 14**.

Frame Type	Error Type	Generated Response	Generated Interrupt	Rec. Status
Ι	CRC error Aborted Unexpected N(S) Unexpected N(R)	– – S-frame –	RME RME - PCE	CRC error Abort - -
S	CRC error Aborted Unexpected N(R) With I-field		– – PCE PCE	- - -

Error Handling

Note: The station variables (V(S), V(R)) are not changed.

#### 4.6.2 Half-Duplex SDLC-NRM Operation

The LAP controllers of the two serial channels can be configured to function in a halfduplex Normal Response Mode (NRM), where they operate as a slave (secondary) station, by setting the NRM bit in the CCR2L register of the corresponding channel.

In contrast to the full-duplex LAP B/LAP D operation, where the combined (primary + secondary) station transmits both commands and responses and may transmit data at any time, the NRM mode allows only responses to be transmitted and the secondary station may transmit only when instructed to do so by the master (primary) station. The SCC gets the permission to transmit from the primary station via an S-, or Iframe with the poll bit (p) set.

The NRM mode can be profitably used in a point-to-multipoint configuration with a fixed master-slave relationship, which guarantees the absence of collisions on the common transmit line. It is the responsibility of the master station to poll the slaves periodically and to handle error situations.

Prerequisite for NRM operation is:

- auto mode with 8-bit address field selected Register CCR2L bit fields 'MDS1', 'MDS0', 'ADM' = '000'
- Register TIMR3 bit 'TMD' = '0'
- same transmit and receive addresses, since only responses can be transmitted, i.e. Register XAD1 = XAD2 and register RAL1 = RAL2 (address of secondary).



Note: The broadcast address may be programmed in register RAL2 if broadcasting is required.

In this case registers RAL1 and RAL2 are not equal.

The primary station has to operate in transparent HDLC mode.

Reception of Frames:

The reception of frames functions similarly to the LAPB/LAPD operation (see "Full-Duplex LAPB/LAPD Operation" on Page 105).

Transmission of Frames:

The SCC does **not** transmit S-, or I-frames if not instructed to do so by the primary station via an S-, or I-frame with the poll bit set.

The SCC can be told to send an I-frame issuing the transmit command 'XIF' in register CMDRL. The transmission of the frame, however, will not be initiated by the SCC until reception of either an

- RR, or
- I-frame

with poll bit set (p = '1').

After the frame has been transmitted (with the final bit set), the host has to wait for an ALLS or XMR interrupt.

A secondary does not poll the primary for acknowledgements, thus timer supervision must be done by the primary station.

Upon the arrival of an acknowledgement the SCC transmit FIFO is enabled and an interrupt is forwarded to the host, either the

- message has been positively acknowledged (ALLS interrupt), or the
- message must be repeated (XMR interrupt).

Additionally, the on-chip timer can be used **under host control** to provide timer recovery of the secondary if no acknowledgements are received at all.

Note: A secondary will transmit transparent frames only if the permission to send is given by receiving an S-frame or I-frame with poll bit set (p = '1').

Examples:

A few examples of SCC/host interaction in the case of normal response mode (NRM) mode are shown in **Figure 54** and **Figure 55**.





Figure 54 No Data to Send: Data Reception/Transmission





# 4.6.3 Signaling System #7 (SS7) Operation

The SEROCCO-M supports the signaling system #7 (SS7) which is described in ITU-Q.703. SS7 support must be activated by setting bit 'ESS7' in register CCR3L.



#### Receive

The SS7 protocol is supported by the following hardware features in receive direction:

- Recognition of Signaling Unit type
- Discard of repeatedly received FISUs and optionally of LSSUs if content is unchanged
- Check if the length of the received signaling unit is at least six octets (including the opening flag)
- Check if the signal information field of a received signaling unit consists of more than 272 octets (enabled with bit CCR3L.ELC). In this case, reception of the current signaling unit will be aborted.
- · Counting and processing of errored signaling units

In order to reduce the microprocessor load, Fill In Signaling Units (FISUs) are processed automatically. By examining the length indicator of a received Signal Unit (SU) SEROCCO-M decides whether a FISU has been received. Consecutively received FISUs will be compared and not stored in the RFIFO, if the content is equal to the previous one. The same applies to Link Status Signaling Units (LSSUs), if enabled with bit CCR3L.CSF. The different types of Signaling Units as Message Signaling Unit (MSU), Link Status Signaling Unit (LSSU) and Fill-In Signaling Units (FISU) are indicated in the RSTA byte (bit field 'SU'), which is automatically added to the RFIFO with each received Signaling Unit. The complete Signaling Unit except start and end flags is stored in the receive FIFO. The functions of bits CCR3H.RCRC and CCR3H.RADD are also valid in SS7 mode, with bit 'RADD' related to BSN (backward sequence number) and FSN (forward sequence number).

Errored signaling units are counted and processed according to ITU-T Q.703. The SU counter and errored-SU counter are reset by setting CMDRH.RSUC to '1'. The error threshold can be selected to be 64 (default) or 32 by clearing/setting bit CCR3L.SUET. If the defined error limit is exceeded, an interrupt (ISR1.SUEX) is generated, if not masked by bit IMR1.SUEX.

#### Transmit

In transmit direction, following features are supported:

- single or repetitive transmission of signaling units
- automatic generation of Fill-In Signaling Units (FISU)

Each Signaling Unit (SU) written to the transmit FIFO (XFIFO) will be sent once or repeatedly including flags, CRC checksum and stuffed bits. After e.g. an MSU has been transmitted completely, SEROCCO-M optionally starts sending of Fill In Signaling Units (FISUs) containing the forward sequence number (FSN) and the backward sequence number (BSN) of the previously transmitted signaling unit. Setting bit CCR3L.AFX to '1' causes FISUs to be sent continuously if no Signaling Unit is to be transmitted from XFIFO. After a new signaling unit has been written to the XFIFO and a transmission has been initiated, the current FISU is completed and the new SU is sent. After this,



transmission of FISUs continues. The internally generated FISUs contain FSN and BSN of the last transmitted signaling unit written to XFIFO.

Using CMDRL.XREP='1', the contents of XFIFO (1..32 bytes) can be sent continuously. This cyclic transmission can be stopped with the CMDRL.XRES command.



# 5 Register Description

## 5.1 Register Overview

The SEROCCO-M global registers are used to configure and control the Serial Communication Controllers (SCCs), General Purpose Pins (GPP) and DMA operation.

All registers are 8-bit organized registers, but grouped and optimized for 16 bit access. 16 bit access is supported to even addresses only.

 Table 15 provides an overview about all on-chip registers:

et Ch	Reg	ister	Res	Meaning	Page					
В	read	write	Val							
Global registers:										
	GC	<b>NDR</b>	00 <sub>H</sub>	Global Command Register	121					
	GM	ODE	$0B_{H}$	Global Mode Register	122					
	Rese	erved								
	GSTAR		00 <sub>H</sub>	Global Status Register	124					
	GPE	DIRL	07 <sub>H</sub>	GPP Direction Register (Low Byte)	126					
	GPE	DIRH	$FF_H$	GPP Direction Register (High Byte)	126					
06 <sub>H</sub> GPDATL		-	GPP Data Register (Low Byte)	128						
07 <sub>H</sub> GPDATH		-	GPP Data Register (High Byte)	128						
	GP	IML	07 <sub>H</sub>	GPP Interrupt Mask Register (Low Byte)	130					
	GP	IMH	$FF_H$	GPP Interrupt Mask Register (High Byte)	130					
	GPISL		00 <sub>H</sub>	GPP Interrupt Status Register (Low Byte)	132					
	GPISH		00 <sub>H</sub>	GPP Interrupt Status Register (High Byte)	132					
	DCN	<b>//DR</b>	00 <sub>H</sub>	DMA Command Register	134					
	Rese	erved								
	DISR		00 <sub>H</sub>	DMA Interrupt Status Register	135					
0F <sub>H</sub> DIMR		77 <sub>H</sub>	DMA Interrupt Mask Register	137						
nel s	pecific re	gisters:								
60 <sub>H</sub>	REIEO	XEIEO	-	Receive/Transmit FIFO (Low Byte)	138					
61 <sub>H</sub>			-	Receive/Transmit FIFO (High Byte)	138					
	et Ch B al reg nel s 60 <sub>H</sub> 61 <sub>H</sub>	t Ch         Reg           B         read           al registers:         GCN           Image: Sters:         GCN           G         GPI           G         GPI      G	PreadWriteBreadwriteBreadwriteal registers: $GCM$ GCMDRGCMDRGSTARC $CSTAR$ GSTAR $GPDIRL$ GPDIRL $GPDATL$ GPDATL $GPDATL$ GPDATL $GPDATL$ GPDATL $GPDATL$ GPISL $GPISL$ GPISL $DCMDR$ $REISPECIFIC registers:$ $60_H$ $RFIFO$ $61_H$ $RFIFO$	PreadRes ValBreadwriteValBreadwriteValal registers: $GGUDR$ $00_{H}$ GGC $GMUDR$ $00_{H}$ $GGMUDR$ $00_{H}$ $00_{H}$ GSTAR $00_{H}$ $00_{H}$ GSTAR $00_{H}$ $00_{H}$ GPDIRL $00_{H}$ $00_{H}$ GPDATL $ 00_{H}$ GPDATL $ 00_{H}$ GPDATL $00_{H}$ $00_{H}$ GPISL $00_{H}$ $00_{H}$ GPISH $00_{H}$ $00_{H}$ DISR $00_{H}$ $00_{H}$ DISR $00_{H}$ $00_{H}$ DISR $00_{H}$ $00_{H}$ $60_{H}$ $RFIFO$ $77_{H}$ $60_{H}$ $RFIFO$ $XFIFO$ $60_{H}$ $RFIFO$ $XFIFO$ $61_{H}$ $RFIFO$ $2$	tr Ch BRegister readRes writeMeaningal registers: $OO_H$ Global Command Registeral registers: $OO_H$ Global Mode Register $GCMDR$ $OO_H$ Global Mode Register $GCMDE$ $OB_H$ Global Status Register $GSTAR$ $OO_H$ Global Status Register $GPDIRL$ $OT_H$ GPP Direction Register (Low Byte) $GPDIRH$ $FF_H$ GPP Data Register (Low Byte) $GPDATL$ -GPP Data Register (High Byte) $GPDATL$ -GPP Data Register (Low Byte) $GPDATL$ -GPP Data Register (Low Byte) $GPDATL$ -GPP Interrupt Mask Register (Low Byte) $GPISL$ $OO_H$ GPP Interrupt Mask Register (Low Byte) $GPISL$ $OO_H$ GPP Interrupt Status Register (High Byte) $GPISL$ $OO_H$ DMA Command Register $DCMDR$ $OO_H$ DMA Interrupt Status Register (High Byte) $DIMR$ $TT_H$ DMA Interrupt Mask Register $DIMR$ $TT_H$ DMA Interrupt Mask Register $fO_H$ $RFIFO$ $SFIFO$ $6O_H$					

#### Table 15Register Overview



Offset Ch Register Res			istor	Res	s Meaning		
Δ	B	read	write	Val	Weating	I age	
12 <sub>µ</sub>	- 62 <sub>4</sub>	STARL		00 <sub>µ</sub>	Status Register (Low Byte)	141	
13 <sub>H</sub>	63 <sub>н</sub>	STARH		10 <sub>H</sub>	Status Register (High Byte)	141	
14 <sub>H</sub>	64 <sub>н</sub>	CM	DRL	00 <sub>H</sub>	Command Register (Low Byte)	146	
15 <sub>H</sub>	65 <sub>H</sub>	CMI	ORH	00 <sub>H</sub>	Command Register (High Byte)	146	
16 <sub>H</sub>	66 <sub>H</sub>	CC	R0L	00 <sub>H</sub>	Channel Configuration Register 0 (Low Byte)	151	
17 <sub>H</sub>	67 <sub>H</sub>	CCI	ROH	00 <sub>H</sub>	Channel Configuration Register 0 (High Byte)	151	
18 <sub>H</sub>	68 <sub>H</sub>	CC	R1L	00 <sub>H</sub>	Channel Configuration Register 1 (Low Byte)	155	
19 <sub>H</sub>	69 <sub>H</sub>	CCI	R1H	00 <sub>H</sub>	Channel Configuration Register 1 (High Byte)	155	
1A <sub>H</sub>	6A <sub>H</sub>	CC	R2L	00 <sub>H</sub>	Channel Configuration Register 2 (Low Byte)	160	
1B <sub>H</sub>	6B <sub>H</sub>	CCI	R2H	00 <sub>H</sub>	Channel Configuration Register 2 (High Byte)	160	
1C <sub>H</sub>	6C <sub>H</sub>	CC	R3L	00 <sub>H</sub>	Channel Configuration Register 3 (Low Byte)	167	
1D <sub>H</sub>	6D <sub>H</sub>	CCI	R3H	00 <sub>H</sub>	Channel Configuration Register 3 (High Byte)	167	
1E <sub>H</sub>	$6E_{H}$	PRE	AMB	00 <sub>H</sub>	Preamble Register	175	
1F <sub>H</sub>	6F <sub>H</sub>	TOI	EN	00 <sub>H</sub>	Time Out Length Register	176	
20 <sub>H</sub>	70 <sub>H</sub>	ACO	CM0	00 <sub>H</sub>	PPP ASYNC Control Character Map 0	177	
21 <sub>H</sub>	71 <sub>H</sub>	ACO	CM1	00 <sub>H</sub>	PPP ASYNC Control Character Map 1	177	
22 <sub>H</sub>	72 <sub>H</sub>	ACC	CM2	00 <sub>H</sub>	PPP ASYNC Control Character Map2	178	
23 <sub>H</sub>	73 <sub>H</sub>	ACO	CM3	00 <sub>H</sub>	PPP ASYNC Control Character Map 3	178	
24 <sub>H</sub>	74 <sub>H</sub>	UD	AC0	7E <sub>H</sub>	User Defined PPP ASYNC Control Character Map 0	180	
25 <sub>H</sub>	75 <sub>H</sub>	UD	AC1	7E <sub>H</sub>	User Defined PPP ASYNC Control Character Map 1	180	
26 <sub>H</sub>	76 <sub>H</sub>	UD	AC2	7E <sub>H</sub>	User Defined PPP ASYNC Control Character Map 2	181	

## Table 15Register Overview (cont'd)



Offse	t Ch	Reg	ister	Res	es Meaning	
Α	В	read	write	Val		
27 <sub>H</sub>	77 <sub>H</sub>	UD/	AC3	7E <sub>H</sub>	User Defined PPP ASYNC Control Character Map 3	181
28 <sub>H</sub>	78 <sub>H</sub>	TTS	SA0	00 <sub>H</sub>	Transmit Time Slot Assignment Register 0	183
29 <sub>H</sub>	79 <sub>H</sub>	TTS	SA1	00 <sub>H</sub>	Transmit Time Slot Assignment Register 1	183
2A <sub>H</sub>	$7A_{H}$	TTS	SA2	00 <sub>H</sub>	Transmit Time Slot Assignment Register 2	184
2B <sub>H</sub>	$7B_{H}$	TTS	SA3	00 <sub>H</sub>	Transmit Time Slot Assignment Register 3	184
2C <sub>H</sub>	$7C_{H}$	RTS	SA0	00 <sub>H</sub>	Receive Time Slot Assignment Register 0	186
2D <sub>H</sub>	$7D_{H}$	RTS	SA1	00 <sub>H</sub>	Receive Time Slot Assignment Register 1	186
2E <sub>H</sub>	7E <sub>H</sub>	RTS	SA2	00 <sub>H</sub>	Receive Time Slot Assignment Register 2	187
2F <sub>H</sub>	7F <sub>H</sub>	RTS	SA3	00 <sub>H</sub>	Receive Time Slot Assignment Register 3	187
30 <sub>H</sub>	80 <sub>H</sub>	PCM	ITX0	00 <sub>H</sub>	PCM Mask Transmit Direction Register 0	189
31 <sub>H</sub>	81 <sub>H</sub>	PCM	ITX1	00 <sub>H</sub>	PCM Mask Transmit Direction Register 1	189
32 <sub>H</sub>	82 <sub>H</sub>	PCMTX2		00 <sub>H</sub>	PCM Mask Transmit Direction Register 2	190
33 <sub>H</sub>	83 <sub>H</sub>	PCM	PCMTX3		PCM Mask Transmit Direction Register 3	190
34 <sub>H</sub>	84 <sub>H</sub>	PCM	IRX0	00 <sub>H</sub>	PCM Mask Receive Direction Register 0	192
35 <sub>H</sub>	85 <sub>H</sub>	PCM	IRX1	00 <sub>H</sub>	PCM Mask Receive Direction Register 1	192
36 <sub>H</sub>	86 <sub>H</sub>	PCN	IRX2	00 <sub>H</sub>	PCM Mask Receive Direction Register 2	193
37 <sub>H</sub>	87 <sub>H</sub>	PCM	IRX3	00 <sub>H</sub>	PCM Mask Receive Direction Register 3	193
38 <sub>H</sub>	88 <sub>H</sub>	BR	RL	00 <sub>H</sub>	Baud Rate Register (Low Byte)	195
39 <sub>H</sub>	89 <sub>H</sub>	BR	RH	00 <sub>H</sub>	Baud Rate Register (High Byte)	195
3A <sub>H</sub>	$8A_{H}$	TIM	IR0	00 <sub>H</sub>	Timer Register 0	197
3B <sub>H</sub>	$8B_{H}$	TIM	1R1	00 <sub>H</sub>	Timer Register 1	197
3C <sub>H</sub>	$8C_{\rm H}$	TIM	1R2	00 <sub>H</sub>	Timer Register 2	198
3D <sub>H</sub>	$8D_{\rm H}$	TIM	1R3	00 <sub>H</sub>	Timer Register 3	198
3E <sub>H</sub>	$8E_H$	XA	.D1	00 <sub>H</sub>	Transmit Address 1 Register	201
3F <sub>H</sub>	8F <sub>H</sub>	XA	XAD2 00 <sub>H</sub>		Transmit Address 2 Register	201
40 <sub>H</sub>	90 <sub>H</sub>	RAL1 00 <sub>H</sub>		00 <sub>H</sub>	Receive Address 1 Low Register	203
41 <sub>H</sub>	91 <sub>H</sub>	RA	.H1	00 <sub>H</sub>	Receive Address 1 High Register	203
42 <sub>H</sub>	92 <sub>H</sub>	RA	L2	00 <sub>H</sub>	Receive Address 2 Low Register	204
43 <sub>H</sub>	93 <sub>H</sub>	RA	H2	00 <sub>H</sub>	Receive Address 2 High Register	204

# Table 15Register Overview (cont'd)



Offse	et Ch	Reg	ister	Res	Meaning	Page		
Α	В	read	write	Val				
44 <sub>H</sub>	94 <sub>H</sub>	AMF	RAL1	00 <sub>H</sub>	Mask Receive Address 1 Low Register	206		
45 <sub>H</sub>	95 <sub>Н</sub>	AMF	RAH1	00 <sub>H</sub>	Mask Receive Address 1 High Register	206		
46 <sub>H</sub>	95 <sub>H</sub>	AMF	RAL2	00 <sub>H</sub>	Mask Receive Address 2 Low Register	207		
47 <sub>H</sub>	96 <sub>H</sub>	AMF	RAH2	00 <sub>H</sub>	Mask Receive Address 2 High Register	207		
48 <sub>H</sub>	98 <sub>H</sub>	RL	CRL	00 <sub>H</sub>	Receive Length Check Register (Low Byte)	209		
49 <sub>H</sub>	99 <sub>H</sub>	RLC	CRH	00 <sub>H</sub>	Receive Length Check Register (High Byte)	209		
4A <sub>H</sub>	9A <sub>H</sub>	X	NC	00 <sub>H</sub>	XON In-Band Flow Control Character Register	211		
4B <sub>H</sub>	9B <sub>H</sub>	XC	)FF	00 <sub>H</sub>	XOFF In-Band Flow Control Character Register	211		
4C <sub>H</sub>	9C <sub>H</sub>	MX	ON	00 <sub>H</sub>	XON In-Band Flow Control Mask Register	213		
4D <sub>H</sub>	9D <sub>H</sub>	MX	MXOFF		XOFF In-Band Flow Control Mask Register	213		
4E <sub>H</sub>	9E <sub>H</sub>	Т	CR	00 <sub>H</sub>	Termination Character Register	215		
4F <sub>H</sub>	9F <sub>H</sub>	TI	CR	00 <sub>H</sub>	Transmit Immediate Character Register	216		
50 <sub>H</sub>	A0 <sub>H</sub>	ISR0		00 <sub>H</sub>	Interrupt Status Register 0	218		
51 <sub>H</sub>	A1 <sub>H</sub>	ISR1		00 <sub>H</sub>	Interrupt Status Register 1	218		
52 <sub>H</sub>	$A2_{H}$	ISR2		00 <sub>H</sub>	Interrupt Status Register 2	219		
53 <sub>H</sub>	A3 <sub>H</sub>	Rese	erved					
54 <sub>H</sub>	A4 <sub>H</sub>	IM	R0	$FF_H$	Interrupt Mask Register 0	226		
55 <sub>H</sub>	$A5_{H}$	IM	R1	FF <sub>H</sub>	Interrupt Mask Register 1	226		
56 <sub>H</sub>	A6 <sub>H</sub>	IM	R2	03 <sub>H</sub>	Interrupt Mask Register 2	227		
57 <sub>H</sub>	A7 <sub>H</sub>	Rese	erved					
58 <sub>H</sub>	A8 <sub>H</sub>	RSTA		00 <sub>H</sub>	Receive Status Byte	229		
59 <sub>H</sub>	A9 <sub>H</sub>	Rese	erved					
5A <sub>H</sub>	AA н	SYI	NCL	00 <sub>H</sub>	SYN Character Register (Low Byte)	233		
5B <sub>H</sub>	н. Н	SYN	NCH	00 <sub>H</sub>	SYN Character Register (High Byte)	233		

#### Table 15Register Overview (cont'd)



$\begin{array}{c c c c c c } \label{eq:observation} \begin{tabular}{ c c c c } \hline Page & Pa$	Iable	5 15	Regisi	ler Overv		cont a)	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Offset Ch		Reg	ister	Res	Meaning	Page
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Α	A B read write		write	Val		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	5C <sub>H</sub>	AC					
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		н					
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			Rese	Reserved			
$\begin{array}{c c c c c } \label{eq:constraint} \begin{tabular}{ c c c c } \hline CDMA registers: & & & & & & & & & & & & & & & & & & &$	5F <sub>H</sub>	$AF_H$					
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Char	nnel sp	pecific DI	MA regist	ers:		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	B0 <sub>H</sub>	CA					
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		н					
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			Rese	erved			
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	B7 <sub>H</sub>	D1 <sub>H</sub>					
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	B8 <sub>H</sub>	$D2_{H}$	XB	CL	00 <sub>H</sub>	Transmit Byte Count (Low Byte)	236
$\begin{array}{c c c c c c c c c c c c c } BA_{H} & D4_{H} & \\ \hline Reserved & Reserved & \\ \hline C3_{H} & DD & \\ H & \\ \hline C4_{H} & DE & RMBSL & 00_{H} & Receive Maximum Buffer Size (Low Byte) & 238 \\ \hline C5_{H} & DF & RMBSH & 00_{H} & Receive Maximum Buffer Size (High Byte) & 238 \\ \hline C5_{H} & DF & RMBSH & 00_{H} & Receive Byte Count (Low Byte) & 240 \\ \hline C5_{H} & E0_{H} & RBCL & 00_{H} & Receive Byte Count (Low Byte) & 240 \\ \hline C7_{H} & E1_{H} & RBCH & 00_{H} & Receive Byte Count (High Byte) & 240 \\ \hline C8_{H} & E2_{H} & Reserved & & \\ \hline C9_{H} & E3_{H} & Reserved & & \\ \hline \\ \hline Miscellaneous: & & \\ \hline E4_{H} & & \\ \hline \\ \hline \\ EC_{H} & VER0 & 03_{H} & Version Register 0 & 242 \\ \hline ED_{H} & VER1 & E0_{H} & Version Register 1 & 242 \\ \hline \\ E4_{H} & & \\ \hline \\ \hline \\ F4_{H} & & \\ \hline \\ \hline$	B9 <sub>H</sub>	D3 <sub>H</sub>	XB	СН	00 <sub>H</sub>	Transmit Byte Count (High Byte)	236
$\begin{array}{c c c c c c c c c c } \hline & Reserved & Reserved & Reserved & Reserved & Reserved & Receive Maximum Buffer Size (Low Byte) & 238 & Receive Maximum Buffer Size (Low Byte) & 238 & Receive Maximum Buffer Size (High Byte) & 238 & Receive Maximum Buffer Size (High Byte) & 238 & Receive Byte Count (Low Byte) & 240 & Receive Byte Count (Low Byte) & 240 & Receive Byte Count (High Byte) & Receive Byte Count (Receive Byte) & Receive Byte) & Receive Byte Count (Receive Byte) & Receive Byte Count (Receive Byte) & Receive Byte Count (Receive Byte) & Receive Byte) & Receive Byte Count (Receive Byte) & Receive Byte Count (Receive Byte) & Receive Byte Count (Receive Byte) &$	BA <sub>H</sub>	D4 <sub>H</sub>					
$\begin{array}{c c c c c c c c c }\hline C3_{H} & DD \\ H & \\ \hline C4_{H} & DE \\ H & \\ \hline C4_{H} & DE \\ H & \\ \hline C5_{H} & DF & RMBSL & 00_{H} \\ H & \\ \hline C5_{H} & DF & RMBSH & 00_{H} \\ H & \\ \hline C6_{H} & E0_{H} & RBCL & 00_{H} \\ \hline Receive Maximum Buffer Size (Low Byte) & 238 \\ \hline C6_{H} & E0_{H} & RBCL & 00_{H} \\ \hline Receive Byte Count (Low Byte) & 240 \\ \hline C7_{H} & E1_{H} & RBCH & 00_{H} \\ \hline Receive Byte Count (High Byte) & 240 \\ \hline C8_{H} & E2_{H} & Reserved & \\ \hline C9_{H} & E3_{H} & Reserved & \\ \hline \hline \hline Miscellaneous: & \\ \hline E4_{H} & \\ \hline \hline \\ EC_{H} & VER0 & 03_{H} \\ \hline Version Register 0 & 242 \\ \hline ED_{H} & VER1 & E0_{H} \\ \hline Version Register 1 & 242 \\ \hline EE_{H} & VER2 & 05_{H} \\ \hline Version Register 3 & 243 \\ \hline \end{array}$		1	Rese	erved			
$\begin{array}{ c c c } \hline H & & & & & & & & \\ \hline C4_{H} & DE & RMBSL & 00_{H} & Receive Maximum Buffer Size (Low Byte) & 238 \\ \hline C5_{H} & DF & RMBSH & 00_{H} & Receive Maximum Buffer Size (High Byte) & 238 \\ \hline C6_{H} & E0_{H} & RBCL & 00_{H} & Receive Byte Count (Low Byte) & 240 \\ \hline C7_{H} & E1_{H} & RBCH & 00_{H} & Receive Byte Count (High Byte) & 240 \\ \hline C8_{H} & E2_{H} & Reserved & & & & & \\ \hline C9_{H} & E3_{H} & Reserved & & & & & & \\ \hline H & & & & & & & & \\ \hline H & & & & & & & & \\ \hline H & & & & & & & & & \\ \hline C9_{H} & E3_{H} & Reserved & & & & & & & & \\ \hline H & & & & & & & & & & \\ \hline H & & & & & & & & & & \\ \hline H & & & & & & & & & & \\ \hline H & & & & & & & & & & \\ \hline C9_{H} & E3_{H} & Reserved & & & & & & & & & \\ \hline H & & & & & & & & & & & \\ \hline H & & & & & & & & & & & \\ \hline H & & & & & & & & & & & \\ \hline H & & & & & & & & & & & \\ \hline H & & & & & & & & & & & \\ \hline H & & & & & & & & & & & \\ \hline H & & & & & & & & & & & \\ \hline H & & & & & & & & & & & \\ \hline H & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & & & & & \\ \hline H & & & & & & & & & & & & & & & & & &$	C3 <sub>H</sub>	DD					
$\begin{array}{c c c c c c c c c } C4_{H} & DE & RMBSL & 00_{H} & Receive Maximum Buffer Size (Low Byte) & 238 \\ \hline H & & & & & & & & & & \\ \hline C5_{H} & DF & RMBSH & 00_{H} & Receive Maximum Buffer Size (High Byte) & 238 \\ \hline C6_{H} & E0_{H} & RBCL & & & & & & & & & \\ \hline C6_{H} & E0_{H} & RBCL & & & & & & & & & & & \\ \hline C7_{H} & E1_{H} & RBCH & & & & & & & & & & & & & \\ \hline C8_{H} & E2_{H} & Reserved & & & & & & & & & & & & & & \\ \hline C9_{H} & E3_{H} & Reserved & & & & & & & & & & & & & \\ \hline Miscellaneous: & & & & & & & & & & & & & & & & \\ \hline E4_{H} & & & & & & & & & & & & & & & & \\ \hline EC_{H} & & VER0 & & & & & & & & & & & & & & & & \\ \hline EC_{H} & & VER0 & & & & & & & & & & & & & & & & & \\ \hline E0_{H} & & VER1 & & E0_{H} & Version Register 0 & & & & & & & & & & & \\ \hline EE_{H} & & VER2 & & & & & & & & & & & & & & & & & & \\ \hline EF_{H} & & VER3 & & & & & & & & & & & & & & & & & & &$		н					
$\begin{array}{c c c c c c } H & H & H & H & H & H & H & H & H & H $	$C4_{H}$	DE	RM	BSL	00 <sub>H</sub>	Receive Maximum Buffer Size (Low Byte)	238
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		н					
$\begin{array}{ c c c c c } \hline H & & & & & & & & & & & & & & & & & &$	C5 <sub>H</sub>	DF	RMI	BSH	00 <sub>H</sub>	Receive Maximum Buffer Size (High Byte)	238
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	<u> </u>	Н			00	Descive Dute Count (Low Dute)	240
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			RDUL		00 <sub>H</sub>	Receive Byte Count (Link Byte)	240
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\frac{C_{H}}{C_{H}}$	EIH	RBCH		00 <sub>H</sub>	Receive Byte Count (High Byte)	240
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		E2 <sub>H</sub>	Rese	ervea			
Miscellaneous: $E4_H$ $EB_H$ $EC_H$ VER0 $03_H$ Version Register 0 $242$ $ED_H$ VER1 $E0_H$ VER2 $05_H$ Version Register 2 $243$ $EF_H$ VER3 $20_H$ Version Register 3	C9 <sub>H</sub>	E3 <sub>H</sub>	Rese	ervea			
$\begin{array}{c c} E4_{H} & \\ \hline \\ \hline \\ EB_{H} & \\ \hline \\ EC_{H} & VER0 & 03_{H} & Version Register 0 & 242 \\ \hline \\ ED_{H} & VER1 & E0_{H} & Version Register 1 & 242 \\ \hline \\ EE_{H} & VER2 & 05_{H} & Version Register 2 & 243 \\ \hline \\ EF_{H} & VER3 & 20_{H} & Version Register 3 & 243 \end{array}$	Misc	ellane	ous:		1		
ReservedReserved242 $EB_H$ $VER0$ $03_H$ Version Register 0242 $ED_H$ VER1 $EO_H$ Version Register 1242 $EE_H$ VER2 $05_H$ Version Register 2243 $EF_H$ VER3 $20_H$ Version Register 3243	E4 <sub>H</sub>		_				
EB <sub>H</sub> VER0         03 <sub>H</sub> Version Register 0         242           ED <sub>H</sub> VER1         E0 <sub>H</sub> Version Register 1         242           EE <sub>H</sub> VER2         05 <sub>H</sub> Version Register 2         243           EF <sub>H</sub> VER3         20 <sub>H</sub> Version Register 3         243			Rese	erved			
$EC_H$ VER0 $03_H$ Version Register 0242 $ED_H$ VER1 $E0_H$ Version Register 1242 $EE_H$ VER2 $05_H$ Version Register 2243 $EF_H$ VER3 $20_H$ Version Register 3243	EB <sub>H</sub>						
ED <sub>H</sub> VER1         EO <sub>H</sub> Version Register 1         242           EE <sub>H</sub> VER2         05 <sub>H</sub> Version Register 2         243           EF <sub>H</sub> VER3         20 <sub>H</sub> Version Register 3         243	ЕС <sub>Н</sub>		VER0		03 <sub>H</sub>	Version Register 0	242
EE <sub>H</sub> VER2         05 <sub>H</sub> Version Register 2         243           EF <sub>H</sub> VER3         20 <sub>H</sub> Version Register 3         243	ED <sub>H</sub>		VER1		E0 <sub>H</sub>	Version Register 1	242
EF <sub>H</sub> VER320 <sub>H</sub> Version Register 3243	EEH		VER2		05 <sub>H</sub>	Version Register 2	243
	EF <sub>H</sub>		VER3		20 <sub>H</sub>	Version Register 3	243



# 5.2 Detailed Register Description

#### 5.2.1 Global Registers

Each register description is organized in three parts:

- a head with general information about reset value, access type (read/write), offset address and usual handling;
- a table containing the bit information (name of bit positions);
- a section containing the detailed description of each bit.

#### Register 1 GCMDR Global Command Register

CPU Accessibility:	read/write
Reset Value:	00 <sub>H</sub>
Offset Address:	00 <sub>H</sub>
typical usage:	written by CPU,
	evaluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0
				Global Con	nmand Bits			
	0	0	0	0	0	0	0	SWR

#### SWR Software Reset Command

Self clearing command bit:

- bit='0' No software reset command is issued.
- bit='1' Causes SEROCCO-M to perform a complete reset identical to hardware reset.



#### **Register Description (GMODE)**

#### Register 2 GMODE Global Mode Register

CPU Accessibility:	read/write
Reset Value:	0B <sub>H</sub>
Offset Address:	01 <sub>H</sub>
typical usage:	written by CPU
	evaluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0
			DN	/IA and G	lobal Contro	bl		
	0	EDMA	IPC(1	:0)	OSCPD	0	DSHP	GIM

#### EDMA Enable External DMA Support

This bit field controls the DMA operation mode:

- EDMA='0' The external DMA controller support functions are disabled. SEROCCO-M is operated in standard register access controlled mode.
- EDMA='1' External DMA controller support functions are enabled.

#### IPC(1:0) Interrupt Pin Characteristic

These bits control the characteristic of interrupt output pin INT/INT:

- IPC(1:0) Output Function:
- '00' Open Drain active low
- '01' Push/Pull active low
- '10' Reserved.
- '11' Push/Pull active high



#### **Register Description (GMODE)**

#### OSCPD Oscillator Power Down

Setting this bit to '0' enables the internal oscillator. For power saving purposes (escpecially if clock modes are used which do not need the internal oscillator) this bit may remain set to '1'.

OSCPD='0' The internal oscillator is active.

OSCPD='1' The internal oscillator is in power down mode.

Note: After reset this bit is set to '1', i.e. the oscillator is in power down mode!

#### DSHP Disable Shaper

This bit has to be set to '0' if the shaping function in the oscillator unit is desired. The shaper amplifies the oscillator signal and improves the slope of the clock edges.

- DSHP='0' Shaper is enabled. Recommended setting if a crystal is connected to pins XTAL1/XTAL2.
- DSHP='1' Shaper is disabled (bypassed). Recommended setting if - a TTL level clock signal is supplied to pin XTAL1 - the oscillator unit is unused

Note: After reset this bit is set to '1', i.e. the shaper is disabled!

#### GIM Global Interrupt Mask

This bits disables all interrupt indications via pin INT/INT. Internal operation (interrupt generation, interrupt status register update,...) is not affected.

If set, pin INT/INT immediately changes or remains in inactive state.

- GIM='0' Global interrupt mask is cleared. Pin INT/INT is controlled by the internal interrupt control logic and activated as long as at least one unmasked interrupt indication is pending (not yet confirmed by read access to corresponding interrupt status register).
- GIM='1' Global interrupt mask is set. Pin INT/INT remains inactive.

Note: After reset this bit is set to '1', i.e. all interrupts are disabled!



# Register Description (GSTAR)

#### Register 3 GSTAR Global Status Register

CPU Accessibility:	read only
Reset Value:	00 <sub>H</sub>
Offset Address:	03 <sub>H</sub>
typical usage:	written by SEROCCO-M evaluated by CPU

Bit	7	6	5	4	3	2	1	0
			Globa	I Interrupt S	Status Inform	nation		
	GPI	DMI	ISA2	ISA1	ISA0	ISB2	ISB1	ISB0

GPI	General Purpose Port Indication (-) This bit indicates, that a GPP port interrupt indication is pending:					
	GPI='0'	GPI='0' No general purpose port interrupt indication is pending.				
	GPI='1'	General purpose port interrupt indication is pending. T source for this interrupt can be further determined by reading registers GPISL/GPISH (refer to page 5-132).				
DMI	DMA Inter	rupt Indication	(-)			
	This bit ind	licates, that a DMA interrupt indication is pending:				
	DMI='0'	No DMA interrupt indication is pending.				
	DMI='1'	DMA interrupt indication is pending. The source for the interrupt (channel A/B, receive/transmit) can be furthed determined by reading register DISR (refer to page 5 135).	nis er -			



#### **Register Description (GSTAR)**

- ISA2 Channel A Interrupt Status Register 2
- ISA1 Channel A Interrupt Status Register 1
- ISA0 Channel A Interrupt Status Register 0
- ISB2 Channel B Interrupt Status Register 2
- ISB1 Channel B Interrupt Status Register 1
- ISB0 Channel B Interrupt Status Register 0

These bits indicate, that an interrupt indication is pending in the corresponding interrupt status register(s) ISR0/ISR1/ISR2 of the serial communication controller (SCC):

- bit='0' No interrupt indication is pending.
- bit='1' An interrupt indication is pending.



#### **Register Description (GPDIRL)**

#### Register 4 GPDIRL GPP Direction Register (Low Byte)

CPU Accessibility:	read/write
Reset Value:	07 <sub>H</sub>
Offset Address:	04 <sub>H</sub>
typical usage:	written by CPU, evaluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0	
	GPP I/O Direction Control								
	0	0	0	0	0	GP10DIR	GP9DIR	GP8DIR	

#### Register 5 GPDIRH GPP Direction Register (High Byte)

CPU Accessibility:	read/write
Reset Value:	FF <sub>H</sub>
Offset Address:	05 <sub>H</sub>
typical usage:	written by CPU evaluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0	
	GPP I/O Direction Control								
	1	GP6DIR	1	1	1	GP2DIR	GP1DIR	GP0DIR	



## **Register Description (GPDIRH)**

GPnDIR	GPP Pin n Direction Control	(-)
	This bit selects between input and output function of the corre	esponding

bit = '0' output

bit = '1' input (reset value)



### **Register Description (GPDATL)**

#### Register 6 GPDATL GPP Data Register (Low Byte)

CPU Accessibility:	read/write
Reset Value:	-
Offset Address:	06 <sub>H</sub>
typical usage:	written by CPU(outputs) and SEROCCO-M(inputs), evaluated by SEROCCO-M(outputs) and CPU(inputs)

Bit	7	6	5	4	3	2	1	0	
	GPP Data I/O								
	-	-	-	-	-	GP10DAT	GP9DAT	GP8DAT	

#### Register 7 GPDATH GPP Data Register (High Byte)

CPU Accessibility:	read/write
Reset Value:	-
Offset Address:	07 <sub>H</sub>
typical usage:	written by CPU(outputs) and SEROCCO-M(inputs), evaluated by SEROCCO-M(outputs) and CPU(inputs)

Bit	7	6	5	4	3	2	1	0	
	GPP Data I/O								
	-	GP6DAT	-	-	-	GP2DAT	GP1DAT	GP0DAT	



#### **Register Description (GPDATH)**

#### GPnDAT GPP Pin n Data I/O Value

(-)

This bit indicates the value of the corresponding GPP pin:

- bit = '0' If direction is input: input level is 'low'; if direction is output: output level is 'low'.
- bit = '1' If direction is input: input level is 'high'; if direction is output: output level is 'high'.



#### **Register Description (GPIML)**

#### Register 8 GPIML GPP Interrupt Mask Register (Low Byte)

CPU Accessibility:	read/write
Reset Value:	07 <sub>H</sub>
Offset Address:	08 <sub>H</sub>
typical usage:	written by CPU, evaluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0	
	GPP Interrupt Mask Bits								
	0	0	0	0	0	GP10IM	GP9IM	GP8IM	

#### Register 9 GPIMH GPP Interrupt Mask Register (High Byte)

CPU Accessibility:	read/write
Reset Value:	FF <sub>H</sub>
Offset Address:	09 <sub>H</sub>
typical usage:	written by CPU, evaluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0	
	GPP Interrupt Mask Bits								
	1	GP6IM	1	1	1	GP2IM	GP1IM	GP0IM	



#### **Register Description (GPIMH)**

## GPnIM GPP Pin n Interrupt Mask

(-)

This bit controls the interrupt mask of the corresponding GPP pin:

- bit = '0' Interrupt generation is enabled. An interrupt is generated on any state transition of the corresponding port pin (inputs).
- bit = '1' Interrupt generation is disabled (reset value).



#### **Register Description (GPISL)**

#### Register 10 GPISL GPP Interrupt Status Register (Low Byte)

Bit	7	6	5	4	3	2	1	0		
	GPP Interrupt Status Bits									
	0	0	0	0	0	GP10I	GP9I	GP8I		

#### Register 11 GPISH GPP Interrupt Status Register (High Byte)

CPU Accessibility:	read only
Reset Value:	00 <sub>H</sub>
Offset Address:	0B <sub>H</sub>
typical usage:	written by SEROCCO-M, read and evaluated by CPU

Bit	7	6	5	4	3	2	1	0		
	GPP Interrupt Status Bits									
	0	GP6I	0	0	0	GP2I	GP1I	GP0I		



#### **Register Description (GPISH)**

#### GPnI GPP Pin n Interrupt Indiction

(-)

This bit indicates if an interrupt event occured on the corresponding GPP pin:

- bit = '0' No interrupt indication is pending at this pin (no state transition has occured).
- bit = '1' An interrupt indication is pending (a state transition occured). The interrupt indication is cleared after read access.



#### **Register Description (DCMDR)**

#### Register 12 DCMDR DMA Command Register

CPU Accessibility:	read/write
Reset Value:	00 <sub>H</sub>
Offset Address:	0C <sub>H</sub>
typical usage:	written by CPU, evaluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0	
	DMA Controller Reset Command Bits								
	RDTB	0	RDRB	0	RDTA	0	RDRA	0	

- RDTB Reset DMA Transmit Channel B
- RDRB Reset DMA Receive Channel B
- RDTA Reset DMA Transmit Channel A

#### RDRA Reset DMA Receive Channel A

Self-clearing command bit.

These bits bring the external DMA support logic to the reset state:

- bit='0' No reset is performed.
- bit='1' Reset is performed.



#### **Register Description (DISR)**

#### Register 13 DISR DMA Interrupt Status Register

CPU Accessibility:	read only
Reset Value:	00 <sub>H</sub>
Offset Address:	0E <sub>H</sub>
typical usage:	written by SEROCCO-M, evaluated by CPU

Bit	7	6	5	4	3	2	1	0		
	DMA Interrupt Status Register									
	0	RBFB	RDTEB	TDTEB	0	RBFA	RDTEA	TDTEA		

Note: Interrupt indications are stored even if masked in register DIMR. Pending interrupts get presented to the system as soon as they get unmasked.

#### RBFB Receive Buffer Full Channel B

#### RBFA Receive Buffer Full Channel A

If a receive buffer size is defined in registers RMBSL/RMBSH and during reception the end of the receive buffer is reached this interrupt is generated indicating that the receive buffer is full. If the external DMA controller supports length protection for receive buffers itself this interrupt is obsolete. In that case, the receive buffer length check can be disabled by setting bit RMBSH:DRMBS to '1'.

#### RDTEB Receive DMA Transfer End Channel B

#### RDTEA Receive DMA Transfer End Channel A

This bit set to '1' indicates that a DMA transfer of receive data is finished and the receive data is completely moved to the corresponding receive buffer in host memory.



#### **Register Description (DISR)**

#### TDTEB Transmit DMA Transfer End Channel B

#### TDTEA Transmit DMA Transfer End Channel A

This bit set to '1' indicates that the data is completely moved from the transmit buffer to the on-chip transmit FIFO, i.e. the transmit byte count programmed in registers XBCL/XBCH is reached.



#### **Register Description (DIMR)**

# Register 14 DIMR DMA Interrupt Mask Register

CPU Accessibility:	read/write
Reset Value:	77 <sub>H</sub>
Offset Address:	0F <sub>н</sub>
typical usage:	

Bit	7	6	5	4	3	2	1	0		
	DMA Interrupt Mask Register									
	0	MRBFB	MRDTEB	MTDTEB	0	MRBFA	MRDTEA	MTDTEA		

MRBFBMask Receive Buffer Full Interrupt Channel BMRBFAMask Receive Buffer Full Interrupt Channel AMRDTEBMask Receive DMA Transfer End Interrupt Channel BMRDTEAMask Receive DMA Transfer End Interrupt Channel AMTDTEBMask Transmit DMA Transfer End Interrupt Channel BMTDTEAMask Transmit DMA Transfer End Interrupt Channel BIf a bit in this interrupt mask register is set to '1', the corresponding bposition in the DISR register. After reset all interrupts are masked.		
<ul> <li>MRBFA Mask Receive Buffer Full Interrupt Channel A</li> <li>MRDTEB Mask Receive DMA Transfer End Interrupt Channel B</li> <li>MRDTEA Mask Receive DMA Transfer End Interrupt Channel A</li> <li>MTDTEB Mask Transmit DMA Transfer End Interrupt Channel B</li> <li>MTDTEA Mask Transmit DMA Transfer End Interrupt Channel A</li> <li>If a bit in this interrupt mask register is set to '1', the corresponding interrupt is not generated and not indicated in the corresponding b position in the DISR register. After reset all interrupts are masked.</li> </ul>	MRBFB	Mask Receive Buffer Full Interrupt Channel B
<ul> <li>MRDTEB Mask Receive DMA Transfer End Interrupt Channel B</li> <li>MRDTEA Mask Receive DMA Transfer End Interrupt Channel A</li> <li>MTDTEB Mask Transmit DMA Transfer End Interrupt Channel B</li> <li>MTDTEA Mask Transmit DMA Transfer End Interrupt Channel A</li> <li>If a bit in this interrupt mask register is set to '1', the corresponding interrupt is not generated and not indicated in the corresponding position in the DISR register. After reset all interrupts are masked.</li> </ul>	MRBFA	Mask Receive Buffer Full Interrupt Channel A
<ul> <li>MRDTEA Mask Receive DMA Transfer End Interrupt Channel A</li> <li>MTDTEB Mask Transmit DMA Transfer End Interrupt Channel B</li> <li>MTDTEA Mask Transmit DMA Transfer End Interrupt Channel A</li> <li>If a bit in this interrupt mask register is set to '1', the corresponding interrupt is not generated and not indicated in the corresponding position in the DISR register. After reset all interrupts are masked.</li> </ul>	MRDTEB	Mask Receive DMA Transfer End Interrupt Channel B
MTDTEBMask Transmit DMA Transfer End Interrupt Channel BMTDTEAMask Transmit DMA Transfer End Interrupt Channel AIf a bit in this interrupt mask register is set to '1', the corresponding interrupt is not generated and not indicated in the corresponding b position in the DISR register. After reset all interrupts are masked.	MRDTEA	Mask Receive DMA Transfer End Interrupt Channel A
MTDTEAMask Transmit DMA Transfer End Interrupt Channel AIf a bit in this interrupt mask register is set to '1', the corresponding interrupt is not generated and not indicated in the corresponding b position in the DISR register. After reset all interrupts are masked.	MTDTEB	Mask Transmit DMA Transfer End Interrupt Channel B
If a bit in this interrupt mask register is set to '1', the corresponding interrupt is not generated and not indicated in the corresponding b position in the DISR register. After reset all interrupts are masked.	MTDTEA	Mask Transmit DMA Transfer End Interrupt Channel A
		If a bit in this interrupt mask register is set to '1', the corresponding interrupt is not generated and not indicated in the corresponding bit position in the DISR register. After reset all interrupts are masked.



#### **Register Description (FIFOL)**

# 5.2.2 Channel Specific SCC Registers

Each register description is organized in three parts:

- a head with general information about reset value, access type (read/write), channel specific offset addresses and usual handling;
- a table containing the bit information (name of bit positions) distinguished for the three major protocol modes HDLC/PPP (H), ASYNC (A) and BISYNC (B);
- a section containing the detailed description of each bit; the corresponding modes, the bit is valid for, are marked again by a bracket term right beside the full bit name.

Regist	gister 15 FIFOL Receive/Transmit FIFO (Low Byte)							
CPU A	ccessibility:	read/w	rite					
Reset	Value:	-						
		Channe	el A C	hannel B				
Offset	Address:	10 <sub>H</sub>	6	0 <sub>H</sub>				
typical	usage:	XFIFO: RFIFO:	written written	by CPU, e by SERO	evaluated I CCO-M, e	by SEROC	:CO-М у CPU	
Bit	7	6	5	4	3	2	1	0
			RFIF	O/XFIFO	Access Low	Byte		
	FIFO(7:0)							
Regist	ter 16	FIFOH Receive/	Transm	it FIFO (H	igh Byte)			
CPU A	ccessibility:	read/w	rite					
Reset	Value:	-						
		Channe	Channel A Channel B					
Offset	Address:	11 <sub>H</sub>	11 <sub>H</sub> 61 <sub>H</sub>					
typical	ical usage: XFIFO: written by CPU, evaluated by SEROCCO-M RFIFO: written by SEROCCO-M, evaluated by CPU							
Bit	7	6	5	4	3	2	1	0
			RFIF	O/XFIFO A	ccess High	Byte		
	FIFO(15:8)							



#### **Register Description (FIFOH)**

#### **Receive FIFO (RFIFO)**

Reading data from the RFIFO can be done in 8-bit (byte) or 16-bit (word) accesses, depending on the selected microprocessor bus width using signal 'WIDTH'. In 16-bit bus mode only 16-bit accesses to RFIFO are allowed. Only for a frame with odd byte count the last access can be an 8-bit access.

The size of the accessible part of RFIFO is determined by programming the RFIFO threshold level in bit field CCR3H.RFTH(1:0). If the HDLC/PPP protocol machine is selected, the threshold can be adjusted to 32 (reset value), 16, 4 or 2 bytes. With the ASYNC and BISYNC protocol machines following threshold levels can be selected: 1 (reset value), 4, 16 or 32 bytes.

• Interrupt Controlled Data Transfer (GMODE.EDMA='0')

Up to 32 bytes/16 words of received data can be read from the RFIFO following an RPF or an RME interrupt (see ISR0 register). The address provided during an RFIFO read access is not incremental; it is always  $10_{\rm H}$  for channel A or  $60_{\rm H}$  for channel B.

RPF Interrupt: This interrupt indicates that the adjusted receive threshold level is reached. The message is not yet complete. A fix number of bytes, dependent from the threshold level, has to be read.

RME Interrupt: The message is completely received. The number of valid **bytes** is determined by reading the RBCL, RBCH registers.

The content of the RFIFO is released by issuing the "Receive Message Complete" command (CMDRH.RMC).

• DMA Controlled Data Transfer (GMODE.EDMA='1')

If DMA operation is enabled, the SEROCCO-M autonomously requests data transfer by asserting the DRR line to the external DMA controller. The DRR line remains active until the beginning of the last receive data byte/word transfer. For a detailed decsription of the external DMA interface operation refer to "External DMA Controller Support" on Page 79.

#### Transmit FIFO (XFIFO)

Writing data to the XFIFO can be done in 8-bit (byte) or 16-bit (word) accesses, depending on the selected microprocessor bus width using signal 'WIDTH'. In 16-bit bus mode only 16-bit accesses to XFIFO are allowed. Only for a frame with odd byte count the last access must be an 8-bit access.

• Interrupt Controlled Data Transfer (GMODE.EDMA='0')

Following an XPR (or an ALLS) interrupt, up to 32 bytes/16 words of new transmit data can be written into the XFIFO. Transmit data can be released for transmission with an XTF command. The address provided during an XFIFO write access is not incremental; it is always  $10_{\rm H}$  for channel A or  $60_{\rm H}$  for channel B.

• DMA Controlled Data Transfer (GMODE.EDMA='1')



#### **Register Description (FIFOH)**

If DMA operation is enabled, the SEROCCO-M autonomously requests data transfer to the XFIFO by asserting the DRT line to the external DMA controller. The DRT line remains active until the beginning of the last transmit data byte/word transfer. For a detailed description of the external DMA interface operation refer to "External DMA Controller Support" on Page 79.



# Register Description (STARL)

Register 17	STARL Status Regist	er (Low Byte)
CPU Accessibility:	read only	
Reset Value:	00 <sub>H</sub>	
	Channel A	Channel B
Offset Address:	12 <sub>H</sub>	62 <sub>H</sub>
typical usage:	updated by S	SEROCCO-M
	read and eva	aluated by CPU

Bit	7	6	5	4	3	2	1	0
Mode		Commar	nd Status			Transmit	ter Status	
н	XREPE	0	0	CEC	0	XDOV	XFW	CTS
Α	XREPE	0	TEC	CEC	FCS	XDOV	XFW	CTS
В	XREPE	0	0	CEC	0	XDOV	XFW	CTS

Regist	er 18	STARH Status Regis	ster (Hi	igh Byte	e)			
CPU Accessibility:		read only						
Reset	Value:	10 <sub>H</sub>						
		Channel A	Cha	annel B				
Offset Address: typical usage:		<b>13<sub>Η</sub></b> updated by read and e	<b>63<sub>н</sub></b> SERC valuate	CCO-N d by CF	1 20			
Bit	7	6 5	5	4	3	2	1	0
Aode		Receiver Status				Aut	tomode Sta	tus

2								
н	0	0	CD	RLI	DPLA	WFA	XRNR	RRNR
Α	0	RFNE	CD	0	DPLA	0	0	0
В	0	RFNE	CD	SYNC	DPLA	0	0	0



# **Register Description (STARH)**

XREPE	Transmit Repetition Executing (all modes)					
	XREPE='0'	No transmit repetition command is in exe	cution.			
	XREPE='1'	A XREP command (register CMDRL) is a execution.	currently in			
TEC	TIC Executir	ng	(async mode)			
	TIC='0'	No TIC (transmit immediate character) is transmission. Access to register TICR is a a TIC transmission.	currently in Illowed to initiate			
	TIC='1'	A TIC command (write access to register accepted but not completely executed. N access to register TICR is allowed until 'T by SEROCCO-M.	TICR) is to further write TIC' bit is cleared			
CEC	Command E	xecuting	(all modes)			
	CEC='0'	No command is currently in execution. The registers CMDRL/CMDRH can be written	he command h by CPU.			
	CEC='1'	A command (written previously to register CMDRH) is currently in execution. No fur can be written to registers CMDRL/CMD	rs CMDRL/ ther command RH by CPU.			
	Note: CEC will stay active if the SCC is in power-down mode or if no serial clock, needed for command execution, is available.					
FCS	Flow Contro	I Status	(async mode)			
	If (in-band) flo CCR2H this b	ow control mechanism is enabled via bit 'F bit indicates the current state of transmitter	LON' in register			
	FCS='0'	Transmitter is ready (always after transm command or XON-character detected).	litter reset			
	FCS='1'	Transmitter is stopped (XOFF-character	detected).			



#### **Register Description (STARH)**

XDOV	Transmit FIFO Data Overflow						
	XDOV='0'	Less than or equal to 32 bytes have been written to XFIFO.					
	XDOV='1'	<ul><li>XDOV='1' More than 32 bytes have been written to the XFIFO.</li><li>bit is reset by:</li><li>a transmitter reset command 'XRES'</li></ul>					
		<ul> <li>or when all bytes in the accessible half have been moved into the inaccessible half</li> </ul>	of the XFIFO nalf.				
XFW	Transmit FIF	O Write Enable	(all modes)				
	XFW='0'	The XFIFO is not able to accept further tran	nsmit data.				
	XFW='1'	Transmit data can be written to the XFIFO.					
СТЅ	CTS (Clear T	o Send) Input Signal State	(all modes)				
	CTS='0'	CTS input signal is inactive (high level)					
	CTS='1'	CTS input signal is active (low level)					
	Note: A transmit clock is necessary to detect the input level of CTS. Optionally this input can be programmed to generate an interrupt on signal level changes.						
RFNE	Receive FIFC	O Not Empty (async/	bisync modes)				
	This status bit valid byte.	t is set if the SCC receive FIFO (RFIFO) hold	ls at least one				
	RFNE='0'	The receive FIFO is empty.					
	RFNE='1'	The receive FIFO is not empty.					
CD	CD (Carrier D	Detect) Input Signal State	(all modes)				
	This status bin independent of (bit 'ICD' in re	t gives the signal state of CD input. This bit of the programmed polarity of the Carrier Degister CCR1H).	value is etect function				
	CD='0'	CD input signal is low.					
	CD='1'	CD input signal is high.					

Note: Optionally this input can be programmed to generate an interrupt on signal level changes.



nfineon

This bit indicates whether the receiver is in synchronized state. After a 'HUNT' command 'SYNC' bit is cleared and the receiver starts searching

for a SYNC character. When found the 'SYNC' status bit is set immediately, an SCD-interrupt is generated (if enabled) and receive data is forwarded to the receiver FIFO.

SYNC='0' Synchronization is lost or not yet achieved. (after reset or after new 'HUNT' command has been issued and before SYNC character is found)

SYNC='1' The receiver is in synchronized state.

#### RLI **Receive Line Inactive**

This bit indicates that neither flags as interframe time fill nor data are being received via the receive line.

- RLI='0' Receive line is active, no constant high level is detected.
- RI I='1' Receive line is inactive, i.e. more than 7 consecutive '1' are detected on the line.
- Note: A receive clock must be provided in order to detect the receive line state.

#### DPLA **DPLL Asynchronous**

This bit is only valid if the receive clock is recovered by the DPLL and FM0, FM1 or Manchester data encoding is selected. It is set when the DPLL has lost synchronization. In this case reception is disabled (receive abort condition) until synchronization has been regained. In addition transmission is interrupted in all cases where transmit clock is derived from the DPLL (clock mode 3a, 7a). Interruption of transmission is performed the same way as on deactivation of the  $\overline{\text{CTS}}$  signal.

- DPLA='0' DPLL is synchronized.
- DPLA='1' DPLL is asynchronous (re-synchronization process is started automatically).

(bisync mode)

**Register Description (STARH)** 

(hdlc mode)

(all modes)


#### **Register Description (STARH)**

#### WFA Wait For Acknowledgement

(hdlc mode)

This status bit is significant in Automode only. It indicates whether the Automode state machine expects an acknowledging I- or S-Frame for a previously sent I-Frame.

WFA='0' No acknowledge I/S-Frame is expected.

WFA='1' The Automode state machine is waiting for an achnowledging S- or I-Frame.

#### XRNR Transmit RNR Status

(hdlc mode)

This status bit is significant in Automode only. It indicates the receiver status of the local station (SCC).

- XRNR='0' The receiver is ready and will automatically answer pollframes with a S-Frame with 'receiver-ready' indication.
- XRNR='1' The receiver is NOT ready and will automatically answer poll-frames with a S-Frame with a 'receiver-not-ready' indication.

#### RRNR Received RNR (Receiver Not Ready) Status

(hdlc mode)

This status bit is significant in Automode only. It indicates the receiver status of the remote station.

- RRNR='0' The remote station receiver is ready.
- RRNR='1' The remote receiver is NOT ready. (A 'receiver-not-ready' indication was received from the remote station)



#### **Register Description (CMDRL)**

Register 19	CMDRL Command Register (Low Byte)				
CPU Accessibility:	read/write				
Reset Value:	00 <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	14 <sub>H</sub>	64 <sub>H</sub>			
typical usage:	written by CF	written by CPU, evaluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0
Mode	Tir	ner	Transmitter Commands					
н	STI	TRES	XIF	XRES	XF	XME	XREP	0
Α	STI	TRES	TXON	XRES	XF	XME	XREP	TXOFF
В	STI	TRES	0	XRES	XF	XME	XREP	0

Register 20	CMDRH Command Register (High Byte)				
CPU Accessibility:	read/write				
Reset Value:	00 <sub>H</sub>				
	Channel A	Channel B			

Offset Address:15<sub>H</sub>65<sub>H</sub>typical usage:written by CPU, evaluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0
Mode				Receiver (	Commands			
н	RMC	RNR	0	0	RSUC	0	0	RRES
Α	RMC	0	0	0	0	0	RFRD	RRES
В	RMC	0	0	0	HUNT	0	RFRD	RRES

The command register contains self-clearing command bits. The command bits read a '1' until the corresponding command is executed completely.



For a write access to the register, the new value gets OR'ed with the current register contents.

The 'CEC' bit in register STARL/STARH is the OR-function over all command bits.

STI Start Timer Command

(all modes)

Self-clearing command bit:

#### HDLC Automode:

In HDLC Automode the timer is used internally for the autonomous protocol support functions. The timer is started automatically by the SCC when an I-Frame is sent out and needs to be acknowledged. If the 'STI' command is issued by software:

STI='1' An S-Frame with poll bit set is sent out and the internal timer is started expecting an acknowledge from the remote station via an I- or S-Frame. The timer is stopped after receiving an acknowledge otherwise the timer expires generating a timer interrupt.

> Note: In HDLC Automode, bit 'TMD' in register TIMR3 must be set to '1'

#### All protocol modes except HDLC Automode:

In these modes the timer is operating as a general purpose timer.

STI='1' This commands starts timer operation. The timer can be stopped by setting bit 'TRES'.

Note: Bit 'TMD' in register TIMR3 must be cleared for proper operation

TRES Timer Reset

(all modes)

(hdlc mode)

Self-clearing command bit. This bit deactivates timer operation:

TRES='0' Timer operation enabled.

TRES='1' Timer operation stopped.

#### XIF Transmit I-Frame

Self-clearing command bit.

This command bit is significant in HDLC Automode only.

XIF='1' Initiates the transmission of an I-frame in auto-mode. Additional to the opening flag, the address and control fields of the frame are added by SEROCCO-M.



TXOFF	Transmit Of	(async mode)	
	Self-clearing	command bit:	
	This commar	nd bit is significant if in-band flow-control is	selected.
	TXOFF='1'	Forces the transmitter to enter its 'transmit	t off' state. This
		is equal to receiving an XOFF character.	
TXON	Transmit On	Command	(async mode)
	Self-clearing This commar	command bit: nd bit is significant if in-band flow-control is	selected.
	TXON='1'	Forces the transmitter to enter its 'transmitis equal to receiving an XON character.	t on' state. This
XRES	Transmitter	Reset Command	(all modes)
	Self-clearing	command bit:	
	XRES='1'	The SCC transmit FIFO is cleared and the protocol engines are reset to their initial st A transmitter reset command is recommended and the protocol mode configurations.	e transmitter ate. nded after all
		between the protocol engines HDLC/ASY sub-modes of HDLC).	NC/BISYNC or
XF	Transmit Fra	(all modes)	
	This self-clea only (GMODI	riven operation	
	XF='1'	After having written up to 32 bytes to the 2 command initiates transmission. In packet protocols like HDLC/PPP the opening flag added by SEROCCO-M. If the end of the p the transmit data, bit 'XME' should be set	KFIFO, this t oriented is automatically backet is part of in addition.

#### **DMA Mode**

After having written the length of the data block to be transmitted to registers XBCL and XBCH, this command initiates the data transfer from host memory to SEROCCO-M by DMA. Transmission on the serial side starts as soon as 32 bytes are transferred to the XFIFO or the transmit byte counter value is reached.



XME

#### **Register Description (CMDRH)**

(hdlc/bisync modes)

Self-clearing command bit:

**Transmit Message End** 

XME='1' Indicates that the data block written last to the XFIFO contains the end of the packet. This bit should always be set in conjunction with a transmit command ('XF' or 'XIF').

#### XREP Transmission Repeat Command

Self-clearing command bit:

 XREP='1' If bit 'XREP' is set together with bit 'XME' and 'XF', SEROCCO-M repeatedly transmits the contents of the XFIFO (1..32 bytes).
 The cyclic transmission can be stopped with the 'XRES' command.

#### RMC Receive Message Complete

(all modes)

(hdlc mode)

(hdlc mode)

Self-clearing command bit:

RMC='1' With this bit the CPU indicates to SEROCCO-M that the current receive data has been fetched out of the RFIFO. Thus the corresponding space in the RFIFO can be released and re-used by SEROCCO-M for further incoming data.

#### RNR Receiver Not Ready Command

NON self-clearing command bit:

This command bit is significant in HDLC Automode only.

- RNR='0' Forces the receiver to enter its 'receiver-ready' state. The receiver acknowledges received poll or I-Frames with a 'receiver-ready' indication.
- RNR='1' Forces the receiver to enter its 'receiver-not-ready' state. The receiver acknowledges received poll or I-Frames with a 'receiver-not-ready' indication.

# RSUC Reset Signaling Unit Counter

(hdlc mode)

Self-clearing command bit:

This command bit is significant if HDLC SS7 mode is selected.

RSUC='1' The Signaling System #7 (SS7) unit counter is reset.



(bisync mode)

#### HUNT Enter Hunt State Command

Self-clearing command bit:

HUNT='1' This command forces the receiver to enter its 'HUNT' state immediately. Thus synchronization is 'lost' and the receiver starts searching for new SYNC characters.

#### RFRD Receive FIFO Read Enable Command

(async/bisync modes)

Self-clearing command bit:

RFRD='1' This command forces insertion of a 'block end' condition into the RFIFO before the receive FIFO threshold is exceeded or a block end condition (termination character detected or time-out) is fulfilled. The execution of this command is reported with a TCD interrupt.

#### RRES Receiver Reset Command

(all modes)

Self-clearing command bit:

RRES='1' The SCC receive FIFO is cleared and the receiver protocol engines are reset to their initial state. The SCC receive FIFO accepts new receive data from the protocol engine immediately after receiver reset procedure.

It is recommended to disable data reception before issuing a receiver reset command by setting bit CCR3L.RAC = '0' and enabling data reception afterwards. A 'receiver reset' command is recommended after all changes in protocol mode configurations (switching between the protocol engines HDLC/ASYNC/BISYNC or sub-modes of HDLC).



Register 21	CCR0L Channel Conf	iguration Register 0 (Low Byte)
CPU Accessibility:	read/write	
Reset Value:	00 <sub>H</sub>	
	Channel A	Channel B
Offset Address:	16 <sub>H</sub>	66 <sub>H</sub>
typical usage:	written by CI	PU;
	read and eva	aluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0
Mode		mi	SC.		Clock Mode Selection			
Н	VIS	PSD	BCR	TOE	SSEL	CM(2:0)		
Α	VIS	PSD	BCR	TOE	SSEL			
В	VIS	PSD	0	TOE	SSEL		CM(2:0)	

# Register 22 CCR0H Channel Configuration Register 0 (High Byte) CPU Accessibility: read/write Reset Value: 00<sub>H</sub> Channel A Channel B Offset Address: 17<sub>H</sub> 67<sub>H</sub>

1		
typical usage:	written by CPU	);
	read and evalu	ated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0	
Mode	Power		Line Coding Proto				col Mode		
н	PU	SC(2:0)			0	0	SM(1:0)		
Α	PU		SC(2:0)			0	SM	(1:0)	
В	PU	SC(2:0)			0	0	SM(1:0)		



#### VIS **Masked Interrupts Visible** (all modes) VIS='0' Masked interrupt status bits are not displayed in the interrupt status registers (ISR0..ISR2). VIS='1' Masked interrupt status bits are visible and automatically cleared after interrupt status register (ISR0..ISR2) read access. Note: Interrupts masked in registers IMR0..IMR2 will not generate an interrupt. PSD **DPLL Phase Shift Disable** (all modes) This option is only applicable in the case of NRZ or NRZI line encoding is selected. PSD='0' Normal DPLL operation. PSD='1' The phase shift function of the DPLL is disabled. The windows for phase adjustment are extended. BCR Bit Clock Rate (async PPP, ASYNC modes) This bit is only valid in asynchronous PPP and ASYNC protocol mode and only in clock modes not using the DPLL (0, 1, 3b, 7b). It is also invalid in clock mode 4.

- BCR='0' Selects isochronous operation with bit clock rate 1. Data bits are sampled once.
- BCR='1' Selects standard asynchronous operation with bit clock rate 16. Using 16 samples per bit, data bits are sampled 3 times around the nominal bit center. The resulting bit value is determined by majority decision of the 3 samples. For correct operation NRZ data encoding has to be selected.



(all modes)

#### **Register Description (CCR0H)**

For clock modes 0b, 2b, 3a, 3b, 6b, 7a and 7b, the internal transmit clock can be monitored on pin TxCLK as an output signal. In clock mode 5, a time slot control signal marking the active transmit time slot is output on pin TxCLK.

Bit 'TOE' is invalid for all other clock modes.

- TOE='0' TxCLK pin is input.
- TOE='1' TxCLK pin is switched to output function if applicable for the selected clock mode.

#### SSEL Clock Source Select

Distinguishes between the 'a' and 'b' option of clock modes 0, 2, 3, 5, 6 and 7.

SSEL='0' Option 'a' is selected.

SSEL='1' Option 'b' is selected.

#### CM(2:0) Clock Mode

(all modes)

(all modes)

This bit field selects one of main clock modes 0..7. For a detailed description of the clock modes refer to **Chapter 3.2.3** 

CM = '000'	clock mode 0
CM = '001'	clock mode 1
CM = '010'	clock mode 2
CM = '011'	clock mode 3
CM = '100'	clock mode 4
CM = '101'	clock mode 5 (time-slot oriented clocking modes)
CM = '110'	clock mode 6
CM = '111'	clock mode 7
Power Up	(all modes)
PU='0'	The SCC is in 'power-down' mode. The protocol engines are switched off (standby) and no operation is performed. This may be used to save power when SCC is not in use.
	Note: The SCC transmit FIFO accepts transmit data even in 'power-down' mode.

PU='1' The SCC is in 'power-up' mode.

PU



#### SC(2:0) Serial Port Configuration

(all modes)

This bit field selects the line coding of the serial port.

Note, that special operation modes and settings may require or exclude operation in special line coding modes. Refer to the 'prerequisites' in the dedicated mode descriptions.

- SC = '000' NRZ data encoding
- SC = '001' Bus configuration, timing mode 1 (NRZ data encoding)
- SC = '010' NRZI data encoding
- SC = '011' Bus configuration, timing mode 2 (NRZ data encoding)
- SC = '100' FM0 data encoding
- SC = '101' FM1 data encoding
- SC = '110' Manchester data encoding
- SC = '111' Reserved
- Note: If bus configuration mode is selected, only NRZ data encoding is supported.

#### SM(1:0) Serial Port Mode

(all modes)

This bit field selects one of the three protocol engines. Depending on the selected protocol engine the SCC related registers change or special bit positions within the registers change their meaning.

- SM = '00' HDLC/PPP protocol engine
- SM = '01' Reserved (do not use)
- SM = '10' BISYNC protocol engine
- SM = '11' ASYNC protocol engine



Register 23	CCR1L Channel Conf	CR1L hannel Configuration Register 1 (Low Byte)					
CPU Accessibility:	read/write						
Reset Value:	00 <sub>H</sub>						
	Channel A	Channel B					
Offset Address:	18 <sub>H</sub>	68 <sub>H</sub>					
typical usage:	written by CF	written by CPU;					
	read and eva	read and evaluated by SEROCCO-M					

Bit	7	6	5	4	3	2	1	0
Mode	misc.							
н	CRL	C32	SOC(1:0)		SFLG	DIV	ODS	0
Α	0	0	0	0	0	DIV	ODS	0
В	0	0	0	0	0	DIV	ODS	0

Regist	er 24	CCR1H Channe	el Configu	iration Re	gister 1 (I	High Byte	)	
CPU A	ccessibility	read/	write					
Reset	Value:	00 <sub>H</sub>						
		Chan	nel A C	hannel B				
Offset	Address:	19 <sub>н</sub>	6	9 <sub>H</sub>				
typical	usage:	writte read a	n by CPU and evalua	; ated by SE	ROCCO-I	М		
Bit	7	6	5	4	3	2	1	0
Mode				mi	SC.			
н	0		0	RTS	FRTS	FCTS	CAS	TSCM

п	0	100	0	KI5	TRIS	1013	CAS	1 SCIVI
Α	0	ICD	0	RTS	FRTS	FCTS	CAS	TSCM
В	0	ICD	0	RTS	FRTS	FCTS	CAS	TSCM



(hdlc mode)

#### **Register Description (CCR1H)**

#### CRL CRC Reset Value

This bit defines the initial value of the internal transmit/receive CRC generators:

- CRL='0' Initial value is  $0xFFFF_{H}$  (16 bit CRC),  $0xFFFFFFFF_{H}$  (32 bit CRC). This is the default value for most HDLC/PPP applications.
- CRL='1' Initial value is  $0x0000_{H}$  (16 bit CRC),  $0x0000000_{H}$  (32 bit CRC).

#### C32 CRC 32 Select

This bit enables 32-bit CRC operation for transmit and receive.

- C32='0' 16-bit CRC-CCITT generation/checking.
- C32='1' 32-bit CRC generation/checking.
- Note: The internal 'valid frame' criteria is updated depending on the selected number of CRC-bytes.

#### SOC(1:0) Serial Output Control

This bit field selects the  $\overline{\text{RTS}}$  signal output function.

(This bit field is only valid in bus configuration modes selected via bit field SC(2:0) in register CCR0H).

- SOC = '0X' RTS ouput signal is active during transmission of a frame (active low).
- SOC = '10' RTS ouput signal is always inactive (high).
- SOC = '11' RTS ouput signal is active during reception of a frame (active low).

#### SFLG Shared Flags Transmission

This bit enables 'shared flag transmission' in HDLC protocol mode. If another transmit frame begin is stored in the SCC transmit FIFO, the closing flag of the preceding frame becomes the opening flag of the next frame (shared flags):

- SFLG = '0' Shared flag transmission disabled.
- SFLG = '1' Shared flag transmission enabled.
- Note: The receiver always supports shared flags and shared zeros of consecutive flags.

(hdlc mode)

(hdlc mode)

(hdlc mode)



#### DIV **Data Inversion** (all modes) This bit is only valid if NRZ data encoding is selected via bit field SC(2:0) in register CCR0H. DIV='0' No Data Inversion. DIV='1' Data is transmitted/received inverted (on a per bit basis). In HDLC and HDLC Synchronous PPP modes the continuous '1' idle sequence is NOT inverted. Thus it is recommended to select the flag sequence for interframe time fill transmission (CCR2H:ITF = '1'), which is inverted. ODS **Output Driver Select** (all modes) The transmit data output pin TxD can be configured as push/pull or open drain output chracteristic. ODS='0' TxD pin is open drain output. ODS='1' TxD pin is push/pull output. ICD **Invert Carrier Detect Pin Polarity** (all modes) ICD='0' Carrier Detect (CD) input pin is active high. ICD='1' Carrier Detect (CD) input pin is active low. RTS **Request To Send Pin Control** (all modes) The request to send pin RTS can be controlled by SEROCCO-M as an output autonomously or via setting/clearing bit 'RTS'. This bit is not valid in clock mode 4. RTS='0' Pin RTS (output) pin is controlled by SEROCCO-M autonomously. HDLC Mode: RTS is activated during transmission. In bus configuration mode the functionality depends on bit field 'SOC' setting. Note: For autonomous RTS pin control a transmit clock is necessary. ASYNC/BISYNC Mode: The functionality depends on setting of bit 'FRTS' RTS='1' Pin RTS can be controlled by software. The output level of this pin depends on bit 'FRTS'.



#### FRTS Flow Control (using signal RTS)

(all modes)

Bit 'FRTS' together with bit 'RTS' determine the function of signal  $\overline{\text{RTS}}$ : RTS, FRTS

- 0, 0 Pin RTS is controlled by SEROCCO-M autonomously. RTS is activated (low) as soon as transmit data is available within the SCC transmit FIFO.
- 0, 1 Pin RTS is controlled by SEROCCO-M autonomously supporting bi-directional data flow control. RTS is activated (low) if the shadow part of the SCC receive FIFO is empty and de-activated (high) when the SCC receive FIFO fill level reaches its receive FIFO threshold.
- 1, 0 Forces pin RTS to active state (low).
- 1, 1 Forces pin RTS to inactive state (high).

### FCTS Flow Control (using signal CTS)

(all modes)

This bit controls the function of pin  $\overline{CTS}$ .

- FCTS = '0' The transmitter is stopped if  $\overline{\text{CTS}}$  input signal is inactive (high) and enabled if active (low).
  - Note: In the character oriented protocol modes (ASYNC, BISYNC, asynchronous PPP), the current byte is completely sent even if CTS becomes inactive during transmission.
- FCTS = '1' The transmitter is enabled, disregarding  $\overline{\text{CTS}}$  input signal.



(all modes)

#### CAS Carrier Detect Auto Start

- CAS = '0' The CD pin is used as general input. In clock mode 1, 4 and 5, clock mode specific control signals must be provided at this pin (receive strobe, receive gating  $\overline{RCG}$ , frame sync clock  $\overline{FSC}$ ). A pull-up/down resistor is recommended if unused.
- CAS = '1' The CD pin enables/disables the receiver for data reception. (Polarity of CD pin can be configured via bit 'ICD'.)
- Note: (1) In clock mode 1, 4 and 5 this bit must be set to '0'.
  (2) A receive clock must be provided for the autonomous receiver control function of the CD input pin.
  (3) In ASYNC mode the transmitter is additionally controlled by inband flow control mechanism (if enabled).

### TSCM Time Slot Control Mode

(all modes)

This bit controls internal counter operation in time slot oriented clock mode 5:

- TSCM='0' The internal counter keeps running, restarting with zero after being expired.
- TSCM='1' The internal counter stops at its maximum value and restarts with the next frame sync pulse again.



Register 25	CCR2L Channel Configuration Register 2 (Low Byte)				
CPU Accessibility:	read/write				
Reset Value:	00 <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	1A <sub>H</sub>	6A <sub>H</sub>			
typical usage:	written by CF	written by CPU;			
	read and eva	aluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0
Mode				mi	SC.			
н	MDS	6(1:0)	ADM	NRM	PPPN	<i>I</i> (1:0)	TLPO	TLP
Α	0	0	0	0	0	0	TLPO	TLP
В	0	0	0	0	SLEN	BISNC	TLPO	TLP

Regist	er 26	CCR2H Channe	el Configu	iration Re	gister 2 (I	High Byte	)	
CPU A	ccessibility	y: <b>read/</b>	write					
Reset '	Value:	00 <sub>H</sub>						
		Chan	nel A C	hannel B				
Offset	Address:	1В <sub>Н</sub>	6	B <sub>H</sub>				
typical	usage:	writte	n by CPU;	;				
		read	and evalua	ated by SE	ROCCO-	Μ		
Bit	7	6	5	4	3	2	1	0
Mode				mi	SC.			
Н	MCS	EPT	NPR	Ξ(1:0)	ITF	0	OIN	XCRC
Α	0	0	0	0	0	0	0	FLON
В	0	EPT	NPR	Ξ(1:0)	ITF	0	CAPP	CRCM



#### MDS(1:0) Mode Select

(hdlc modes)

This bit field selects the HDLC protocol sub-mode including the 'extended transparent mode'.

MDS = '00'	Automode.
MDS = '01'	Address Mode 2.
MDS = '10'	Address Mode 0/1. (Option '0' or '1' is selected via bit 'ADM'.)
MDS = '11'	Extended transparent mode (bit transparent transmission/ reception).

Note: 'MDS(1:0)' must be set to '10' if any PPP mode is enabled via bit field 'PPPM' or if SS7 is enabled via bit 'ESS7' in register CCR3L.

#### ADM Address Mode Select

(hdlc modes)

The meaning of this bit depends on the selected protocol sub-mode:

#### Automode, Address Mode 2:

Determines the address field length of an HDLC frame.

ADM = '0' 8-bit address field.

ADM = '1' 16-bit address field.

#### Address Mode 0/1:

Determines whether address mode 0 or 1 is selected.

ADM = '0' Address Mode 0 (no address recognition).

ADM = '1' Address Mode 1 (high byte address recognition).

#### **Extended Transparent Mode:**

ADM = '1' recommended setting

#### NRM Normal Response Mode

(hdlc modes)

This bit is valid in HDLC Automode operation only and determines the function of the Automode LAP-Controller:

NRM = '1' Half-duplex normal response mode (NRM) operation.



#### **PPPM(1:0) PPP Mode Select**

(hdlc modes)

This bit field enables and selects the HDLC PPP protocol modes:

- PPPM = '00' No PPP protocol operation. The HDLC sub-mode is determined by bit field 'MDS'.
- PPPM = '01' Octet synchronous PPP protocol operation.
- PPPM = '10' Asynchronous PPP protocol operation. Bit 'BCR' in register CCR0L must be set to ensure proper asynchronous reception.
- PPPM = '11' Bit synchronous PPP protocol operation.
- Note: 'Address Mode 0' must be selected by setting bit field 'MDS(1:0)' to '10' and bit 'ADM' to '0' if any PPP mode is enabled.

#### TLPO Test Loop Out Function

(all modes)

This bit is only valid if test loop is enabled and controls whether test loop transmit data is driven on pin TxD:

- TLPO = '0' Test loop transmit data is driven to TxD pin.
- TLPO = '1' Test loop transmit data is NOT driven to TxD pin. TxD pin is idle '1'. Depending on the selected output characteristic the pin is high impedance (bit CCR1L.ODS ='0') or driving high (CCR1L.ODS ='1').

#### TLP Test Loop

(all modes)

This bit controls the internal test loop between transmit and receive data signals. The test loop is closed at the far end of serial transmit and receive line just before the respective TxD and RxD pins:

TLP = '0' Test loop disabled.

TLP = '1' Test loop enabled.

The software is responsible to select a clock mode which allows correct reception of transmit data depending on the external clock supply. Transmit data is sent out via pin TxD if not disabled with bit 'TLPO'. The receive input pin RxD is internally disconnected during test loop operation.



#### SLEN SYNC Character Length (bisync mode) This bit selects the SYNC character length in BISYNC/MONOSYNC operation mode: SLEN = '0'6 bit (MONOSYNC), 12 bit (BISYNC). SLEN = '1' 8 bit (MONOSYNC), 16 bit (BISYNC). BISNC Select MONOSYNC/BISYNC Mode (bisync mode) This bit selects BISYNC or MONOSYNC operation mode: BISNC = '0'MONOSYNC mode. BISNC = '1' BISYNC mode. MCS Modulo Count Select (hdlc modes) This bit is valid in HDLC Automode operation only and determines the control field format: MCS = '0'Basic operation, one byte control field (modulo 8 counter operation). MCS = '1'Extended operation, two bytes control field (modulo 128) counter operation).

#### EPT Enable Preamble Transmission

(hdlc/bisync mode)

This bit enables preamble transmission. The preamble is started after interframe time fill (ITF) transmission is stopped because a new frame is ready to be transmitted. The preamble pattern consists of 8 bits defined in register PREAMB, which is sent repetitively. The number of repetitions is determined by bit field 'PRE(1:0)':

- EPT='0' Preamble transmission is disabled.
- EPT='1' Preamble transmission is enabled.
- Note: Preamble operation does NOT influence HDLC shared flag transmission if enabled.



NPRE(1:0)

(hdlc/bisync mode)

#### **Register Description (CCR2H)**

#### This bit field determines the number of preambles transmitted: NPRE = '00' 1 preamble. NPRE = '01' 2 preambles. NPRE = '10' 4 preambles. NPRE = '11' 8 preambles. ITF Interframe Time Fill (hdlc/bisync mode) This bit selects the idle state of the transmit pin TxD: ITF='0' Continuous logical '1' is sent during idle phase. ITF='1'HDLC Mode: Continuous flag sequences are sent ('01111110' flag pattern). **BISYNC Mode:** Continuous SYN characters are output. Note: It is recommended to clear bit 'ITF' in bus configuration modes, i.e. continuous '1's are sent as idle sequence and data encoding is NRZ. OIN **One Insertion** (hdlc mode)

Number of Preamble Repetitions

In HDLC mode a one-insertion mechanism similar to the zero-insertion can be activated:

- OIN='0' The '1' insertion mechanism is disabled.
- OIN='1' In transmit direction a logical '1' is inserted to the serial data stream after 7 consecutive zeros. In receive direction a '1' is deleted from the receive data stream after receiving 7 consecutive zeros. This enables clock information to be recovered from the receive data stream by means of a DPLL, even in the case of NRZ data encoding, because a transition at bit cell boundary occurs at least every 7 bits.



(hdlc mode)

- XCRC Transmit CRC Checking Mode XCRC='0' The transmit checksum (2 or 4 bytes) is generated and appended to the transmit data automatically. XCRC='1' The transmit checksum is not generated automatically.
  - The checksum is expected to be provided by software as the last 2 or 4 bytes in the transmit data buffer.

#### FLON Flow Control Enable

(async mode)

In ASYNC mode, in-band flow control is supported:

- FLON='0' No automatic in-band flow-control is performed. However recognition of a flow control character (XON/XOFF) causes always a maskable interrupt event.
- FLON='1' Automatic in-band flow-control is performed. Reception of a XOFF character (defined in register XNXF) turns off the transmitter after the currently transmitted character has been shifted out completely (XOFF state). Reception of a XON character (defined in register XNXF) resumes the transmitter from XOFF into XON state ready to send available transmit data bytes. The current flow control state is indicated via bit 'FCS' in register Star.

Any transmitter reset switches the flow-control logic to XON state.

#### CAPP CRC Append

(bisync mode)

In BISYNC mode the CRC generator can be activated:

- CAPP = '0'No CRC generation/checking is active in BISYNC mode.
- CAPP = '1'The CRC generator is activated:
  - 1. The CRC generator is initialized every time the transmission of a new 'frame' starts. The CRC initialization value can be selected via bit 'CRL' in register CCR2 (for BISYNC operation).
  - 2. The CRC is automatically to the last transmitted data of a 'frame'.



#### CRCM CRC Mode Select

(bisync mode)

In BISYNC mode the CRC generator can be configured for two different generator polynoms:

CRCM = '0' CRC-16: The polynominal is  $x^{16}+x^{15}+x^2+1$ . CRCM = '1' CRC-CCITT: The polynominal is  $x^{16}+x^{15}+x^5+1$ .



Register 27	CCR3L Channel Configuration Register 3 (Low Byte)				
CPU Accessibility:	read/write				
Reset Value:	00 <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	1С <sub>н</sub>	6С <sub>н</sub>			
typical usage:	written by CPU;				
	read and eva	aluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0
Mode				mi	SC.			
н	ELC	AFX	CSF	SUET	RAC	0	0	ESS7
Α	TCDE	0	CHL	CHL(1:0)		DXS	XBRK	STOP
В	TCDE	SLOAD	CHL	(1:0)	RAC	0	0	STOP

Regist	er 28	CCR3H Channe	el Configu	ration Re	egister 3 (I	High Byte	)	
CPU A	ccessibility	y: <b>read/</b>	write					
Reset '	Value:	00 <sub>H</sub>						
		Chan	nel A C	Channel B				
Offset /	Address:	1D <sub>H</sub>	6	D <sub>H</sub>				
typical	usage:	writte	n by CPU					
		read	and evalua	ated by SE	ROCCO-I	М		
Bit	7	6	5	4	3	2	1	0
Mode			misc.					
Н	0	DRCRC	RCRC	RADD	0	0	RFTH	H(1:0)
Α	PAR	(1:0)	PARE	DPS	RFDF	0	RFTH	H(1:0)
В	<b>B</b> PAR(1:0)		PARE	DPS	RFDF	0	RFTH	H(1:0)



ELC	Enable Leng	th Check	(hdlc mode)		
	This bit is only If the number Unit, receptio	bit is only valid in HDLC SS7 mode: number of received octets exceeds 272 + 7 within one Signaling reception is aborted and bit RSTA.RAB is set.			
	ELC='0'	Length Check disabled.			
	ELC='1'	Length Check enabled.			
TCDE	Termination	Character Detection Enable (a	sync/bisync modes)		
	This bit is valid termination ch	d in ASYNC/BISYNC modes only and on a maracter detection mechanism:	enables/disables the		
	TCDE = '0'	No receive termination character det	ection is performed.		
	TCDE = '1'	The termination character detection is receive data stream is monitored for termination character (TC) programm When this character is detected, a 'T generated to the CPU (unless maske	s enabled. The the occurence of a ned via register TCR. CD' interrupt is ed).		
		Note: If the programmed charact	er length (bit field		

Note: If the programmed character length (bit field 'CHL(1:0)') is less than 8 bits, the most significant unused bits in register TCR must be set to '0'. Otherwise no termination character will be detected.

#### AFX Automatic FISU Transmission

(hdlc mode)

This bit is only valid in HDLC SS7 mode:

After the contents of the transmit FIFO (XFIFO) has been transmitted completely, FISUs are transmited automatically. These FISUs contain the FSN and BSN of the last transmitted Signaling Unit (provided in XFIFO).

- AFX='0' Automatic FISU transmission disabled.
- AFX='1' Automatic FISU transmission enabled.



(bisync mode)

#### SLOAD Enable SYN Character Load

In BISYNC mode, SYN characters might be filtered out or stored to the SCC receive FIFO.

- SLOAD='0' SYN characters are filtered out and not stored in the receive FIFO.
- SLOAD='1' All received characters, including SYN characters, are stored in the receive FIFO.

#### CSF Compare Status Field

This bit is only valid in HDLC SS7 mode:

If the status fields of consecutive LSSUs are equal, only the first will be stored and every following is ignored

- CSF='0' Compare is disabled, all received LSSUs are stored in the receive FIFO.
- CSF='1' Compare is enabled, only the first one of consecutive equal LSSUs is stored in the receive FIFO.

#### SUET Signalling Unit Counter Threshold

(hdlc mode)

(hdlc mode)

This bit is only valid in HDLC SS7 mode:

Defines the number of signaling units received in error that will cause an error rate high indication (ISR1.SUEX).

SUET='0' threshold is 64 errored signaling units.

SUET='1' threshold is 32 errored signaling units.

CHL(1:0) Character Length

(async/bisync modes)

This bit field selects the number of data bits within a character:

 $CHL = '00' \qquad 8-bit data.$   $CHL = '01' \qquad 7-bit data.$   $CHL = '10' \qquad 6-bit data.$   $CHL = '11' \qquad 5-bit data.$ 

# RAC Receiver active

(all modes)

Switches the receiver between operational/inoperational states:

RAC='0' Receiver inactive, receive line is ignored.

RAC='1' Receiver active.



#### DXS Disable Storage of XON/XOFF Characters (async mode)

In ASYNC mode, XON/XOFF characters might be filtered out or stored to the SCC receive FIFO:

- DXS='0' All received characters including XON/XOFF characters are stored in the receive FIFO.
- DXS='1' XON/XOFF characters are filtered out and not stored in the receive FIFO.

#### XBRK Transmit Break

(async mode)

XBRK='0' Normal transmit operation.

XBRK='1' Forces the TxD pin to 'low' level immediately (break condition), regardless of any character being currently transmitted. This command is executed immediately with the next rising edge of the transmit clock and further transmission is disabled. The currently sent character is lost.

Data stored in the SCC transmit FIFO will be sent as soon as the break condition is cleared (XBRK='0'). A transmit reset command (bit 'XRES' in register CMDRL) does NOT clear the break condition automatically.

ESS7 Enable SS7 Mode

(hdlc mode)

(async mode)

This bit is only valid in HDLC mode only.

- ESS7='0' Disable signaling system #7 (SS7) support.
- ESS7='1' Enable signaling system #7 (SS7) support.
- Note: If SS7 mode is enabled, 'Address Mode 0' must be selected by setting bit field CCR2L:MDS(1:0) to '10' and bit CCR2L:ADM to '0'.

#### STOP Stop Bit number

This bit selects the number of stop bits per ASYNC character:

- STOP='0' 1 stop bit per character.
- STOP='1' 2 stop bits per character.



#### PAR(1:0) Parity Format

(async/bisync modes)

This bit field selects the parity generation/checking mode:

- PAR = '00' SPACE ('0'), a constant '0' is inserted as parity bit.
- PAR = '01' Odd parity.

PAR = '10' Even parity.

PAR = '11' MARK ('1'), a constant '1' is inserted as parity bit.

The received parity bit is stored in the SCC receive FIFO depending on the selected character format:

- as leading bit immediately preceding the data bits if character length is 5, 6 or 7 bits and bit 'DPS' is cleared ('0').
- as LSB of the status byte belonging to the character if character length is 8 bits and the corresponding receive FIFO data format is selected (bit 'RFDF' = '1').

A parity error is indicated in the MSB of the status byte belonging to each character if enabled. In addition, a parity error interrupt can be generated.

DRCRC	Disable Rece	Disable Receive CRC Checking (hdlc mode)					
	DRCRC='0'	The receiver expects a 16 or 32 bit frame. CRC processing depends o 'RCRC'. Frames shorter than expected are discarded (refer to RSTA description	t CRC within a HDLC on the setting of bit marked 'invalid' or are on).				
	DRCRC='1'	The receiver does not expect any 0 frame. The criteria for 'valid frame' accordingly (refer to RSTA descrip Bit 'RCRC' is ignored.	CRC within a HDLC indication is updated tion).				
RCRC	Receive CRC	Checking Mode	(hdlc mode)				
	RCRC='0'	The received checksum is evaluate to the receive FIFO.	ed, but NOT forwarded				
	RCRC='1'	The received checksum (2 or 4 byt forwarded to the receive FIFO as c	es) is evaluated and lata.				
PARE	Parity Enable	9	(async/bisync modes)				
	PARE='0'	Parity generation/checking is disab	oled.				
	PARE='1'	Parity generation/checking is enab	led.				



#### RADD Receive Address Forward to RFIFO

(hdlc mode)

This bit is only valid

- if an HDLC sub-mode with address field support is selected (Automode, Address Mode 2, Address Mode 1)
- in SS7 mode
- RADD='0' The received HDLC address field (either 8 or 16 bit, depending on bit 'ADM') is evaluated, but NOT forwarded to the receive FIFO.
  In SS7 mode, the signaling unit fields 'FSN' and 'BSN' are NOT forwarded to the receive FIFO.
- RADD='1' The received HDLC address field (either 8 or 16 bit, depending on bit 'ADM') is evaluated and forwarded to the receive FIFO. In SS7 mode, the signaling unit fields 'FSN' and 'BSN' are

forwarded to the receive FIFO.

#### DPS Data Parity Storage

(async/bisync modes)

Only valid if parity generation/checking is enabled via bit 'PARE':

- DPS='0' The parity bit is stored.
- DPS='1' The parity bit is not stored in the data byte containing character data.

The parity bit is always stored in the status byte.



#### RFDF Receive FIFO Data Format

(async/bisync mode)

Status Byte (SB):

76

PE FE

In ASYNC mode, the character format is determined as follows:

7

765

76

Ρ

7

Ρ

RFDF='1'

Data Byte (DB):

54

Р

0

0

0

0

Char5

Char6

Char7

#### RFDF='0'

Data Byte:





PChar7

#### 7 0 Char8

Char8



**0** P

(no parity bit stored)

(no parity bit stored)

*P*: Parity bit stored in data byte (can be disabled via bit 'DPS')

PE: Parity Error

FE: Frame Error

P: Parity bit stored in status byte



### **RFTH(1:0)** Receive FIFO Threshold

(all modes)

This bit field defines the level up to which the SCC receive FIFO is filled with valid data before an 'RPF' interrupt is generated.

(In case of a 'frame end / block end' condition the SEROCCO-M notifies the CPU immediately, disregarding this threshold.)

The meaning depends on the selected protocol engine:

#### HDLC Modes:

RFTH(1:0) Threshold level in number of data bytes.

00'	32 byte

- '01' 16 byte
- '10' 4 byte
- '11' 2 byte

### ASYNC/BISYNC Mode:

RFTH(1:0)	Threshold level in number of data bytes (DB) and starbytes (SB) depending on bit 'RFDF':				
	RFDF = '0'	RFDF = '1'			
'00'	1 DB	1 DB + 1 SB			
'01'	4 DB	2 DB + 2 SB			
'10'	16 DB	8 DB + 8 SB			
'11'	32 DB	16 DB + 16 SB			



#### **Register Description (PREAMB)**

Register 29	PREAMB Preamble Reg	jister			
CPU Accessibility:	read/write				
Reset Value:	00 <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	1Е <sub>Н</sub>	6Е <sub>Н</sub>			
typical usage:	written by CPU;				
	read and evaluated by SEROCCO-M				

Bit	7	6	5	4	3	2	1	0
Mode				Preamble	e Pattern			
н		PRE(7:0)						
Α	0	0	0	0	0	0	0	0
В				PRE	(7:0)			

## PRE(7:0) Preamble

(hdlc/bisync modes)

This bit field determines the preamble pattern which is send out during preamble transmission.

Note: In HDLC-mode, zero-bit insertion is disabled during preamble transmission.



#### **Register Description (TOLEN)**

Register 30	TOLEN Time Out Leng	gth Register			
CPU Accessibility:	read/write				
Reset Value:	00 <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	1F <sub>H</sub>	6F <sub>н</sub>			
typical usage:	written by CF	written by CPU; read and evaluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0
Mode				Time Ou	it Length			
н	0	0	0	0	0	0	0	0
Α	TOIE		TOLEN(6:0)					
В	0	0	0	0	0	0	0	0

#### TOIE Time Out Indication Enable

(async mode)

(async mode)

If this bit is set to '1' in ASYNC mode, any time out event will automatically generate an 'RFRD' command thus inserting a 'block end' indication into the RFIFO. This time-out condition is indicated with the 'TIME' interrupt (if unmasked).

TOIE = '0' Automatic Time Out processing disabled.

TOIE = '1' Automatic Time Out processing enabled.

#### TOLEN(6:0) Time Out Length

This bit field determines the time out period. If there is no receive line activity for the configured period of time, a time out indication is generated if enabled via bit 'TOIE'.

The period of time is programmable in multiples of character frame length <CFL> time equivalents including start, parity and stop bits (refer to Figure 46):

TOLEN T = ((TOLEN + 1) \* 4) \* <CFL>



# Register Description (ACCM0)

Register 31	ACCM0 PPP ASYNC (	Control Character Map 0
CPU Accessibility:	read/write	
Reset Value:	00 <sub>н</sub>	
	Channel A	Channel B
Offset Address:	20 <sub>H</sub>	70 <sub>H</sub>
typical usage: written by CPU;		
	read and eva	aluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0
Mode			ASYNC	Character	Control Ma	p 0700		
н	07	06	05	04	03	02	01	00
Α	0	0	0	0	0	0	0	0
В	0	0	0	0	0	0	0	0

Regist	er 32	ACCM1 PPP AS	SYNC Cor	trol Char	acter Map	1		
CPU A	ccessibility	y: <b>read/</b>	write					
Reset	Value:	00 <sub>H</sub>						
		Chan	nel A C	hannel B				
Offset	Address:	21 <sub>H</sub>	7	1 <sub>H</sub>				
typical	usage:	writte	n by CPU					
		read	and evalua	ated by SE	ROCCO-I	М		
Bit	7	6	5	4	3	2	1	0
Mode	ASYNC Character Control Map 0F08							
Н	0F	0E	0D	0C	0B	0A	09	08
Α	0	0	0	0	0	0	0	0
В	0	0	0	0	0	0	0	0



Register 33	ACCM2 PPP ASYNC C	Control Character Map2	
CPU Accessibility:	read/write		
Reset Value:	00 <sub>H</sub>		
	Channel A	Channel B	
Offset Address:	22 <sub>H</sub>	72 <sub>H</sub>	
typical usage:	written by CPU;		
	read and eva	aluated by SEROCCO-M	

Bit	7	6	5	4	3	2	1	0
Mode		ASYNC Character Control Map 1710						
Н	17	16	15	14	13	12	11	10
Α	0	0	0	0	0	0	0	0
В	0	0	0	0	0	0	0	0

Regist	er 34	ACCM3 PPP AS	SYNC Cor	ntrol Char	acter Map	3		
CPU A	ccessibility	y: <b>read/</b>	write					
Reset	Value:	00 <sub>H</sub>						
		Chan	nel A C	hannel B				
Offset	Address:	23 <sub>H</sub>	7	3 <sub>H</sub>				
typical	usage:	writte	n by CPU					
		read	and evalua	ated by SE	ROCCO-	М		
Bit	7	6	5	4	3	2	1	0
Mode	ASYNC Character Control Map 1F18							
Н	1F	1E	1D	1C	1B	1A	19	18
Α	0	0	0	0	0	0	0	0
В	0	0	0	0	0	0	0	0



#### ACCM ASYNC Character Control Map

(hdlc modes)

This bit field is valid in HDLC asynchronous and octet-synchronous PPP mode only:

Each bit selects the corresponding character (indicated as hex value  $1F_{H}..00_{H}$  in the register description table) as control character which has to be mapped into the transmit data stream.



#### **Register Description (UDAC0)**

Register 35	UDAC0 User Defined I	PPP ASYNC Control Character Map 0			
CPU Accessibility:	read/write				
Reset Value:	7E <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	24 <sub>H</sub>	74 <sub>H</sub>			
typical usage:	written by CPU;				
	read and eva	luated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0
Mode	ASYNC Character 0							
Н	ACO							
Α	0	0	0	0	0	0	0	0
В	0	0	0	0	0	0	0	0

#### **Register 36** UDAC1 **User Defined PPP ASYNC Control Character Map 1** CPU Accessibility: read/write **Reset Value:** 7E<sub>H</sub> Channel A Channel B 25<sub>н</sub> Offset Address: 75<sub>H</sub> typical usage: written by CPU; read and evaluated by SEROCCO-M Bit 7 6 5 4 3 2 1 0 Mode **ASYNC Character 1** AC1 н 0 0 0 0 0 0 0 0 Α В 0 0 0 0 0 0 0 0


### **Register Description (UDAC2)**

Register 37	UDAC2 User Defined I	PPP ASYNC Control Character Map 2
CPU Accessibility:	read/write	
Reset Value:	7E <sub>H</sub>	
	Channel A	Channel B
Offset Address:	26 <sub>H</sub>	76 <sub>H</sub>
typical usage:	written by CF	PU;
	read and eva	luated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0
Mode				ASYNC C	haracter 2			
н				A	C2			
Α	0	0	0	0	0	0	0	0
В	0	0	0	0	0	0	0	0

### **Register 38** UDAC3 **User Defined PPP ASYNC Control Character Map 3** CPU Accessibility: read/write **Reset Value:** 7E<sub>H</sub> Channel A Channel B Offset Address: 27<sub>H</sub> 77<sub>H</sub> typical usage: written by CPU; read and evaluated by SEROCCO-M Bit 7 6 5 4 3 2 1 0 Mode ASYNC Character 3 AC3 н 0 0 0 0 0 0 0 0 Α В 0 0 0 0 0 0 0 0



### **Register Description (UDAC3)**

### AC3..0 User Defined ASYNC Character Control Map

(hdlc mode)

This bit field is valid in HDLC asynchronous and octet-synchronous PPP mode only:

These bit fields define user determined characters as control characters which have to be mapped into the transmit data stream.

In register ACCM only characters  $00_{H}$ ..1F<sub>H</sub> can be selected as control characters. Register UDAC allows to specify any four characters in the range  $00_{H}$ ..FF<sub>H</sub>.

The default value is a  $7E_H$  flag which must be always mapped. Thus no additional character is mapped if  $7E_H$  's are programed to bit fields AC3...0 (reset value).

 $(7E_{H} \text{ is mapped automatically, even if not defined via a AC bit field.})$ 



### **Register Description (TTSA0)**

Register 39	TTSA0 Transmit Time	e Slot Assignment Register 0
CPU Accessibility:	read/write	
Reset Value:	00 <sub>H</sub>	
	Channel A	Channel B
Offset Address:	28 <sub>H</sub>	78 <sub>H</sub>
typical usage:	written by CF	PU;
	read and eva	aluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0
Mode						Tx Clo	ck Shift	
Н	0	0	0	0	0		TCS(2:0)	
Α	0	0	0	0	0		TCS(2:0)	
В	0	0	0	0	0		TCS(2:0)	

Regist	er 40	TTSA1 Transm	it Time	Slot Assig	nment Reg	gister 1			
CPU A	ccessibility	read/write							
Reset V	Value:	00 <sub>H</sub>							
		Chan	nel A	Channel B					
Offset Address: 29 <sub>H</sub>				79 <sub>H</sub>					
typical usage:		writte	written by CPU;						
	read and evaluated by SEROCCO-M								
Bit	7	6	5	4	3	2	1	0	
Mode			Tx Time Slot Number						
н	TEPCM	TTSN(6:0)							
Α	TEPCM	TTSN(6:0)							
В	TEPCM				TTSN(6:0)				



### **Register Description (TTSA2)**

Register 41	TTSA2 Transmit Time	e Slot Assignment Register 2			
CPU Accessibility:	read/write				
Reset Value:	<b>ОО<sub>Н</sub></b>				
	Channel A	Channel B			
Offset Address:	2A <sub>H</sub>	7A <sub>H</sub>			
typical usage:	written by Cl	PU;			
	read and eva	read and evaluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0
Mode			Тг	ansmit Cha	nnel Capac	ity		
н		TCC(7:0)						
Α		TCC(7:0)						
В				TCC	(7:0)			

Regist	er 42	TTSA3 Transm	nit Time S	lot Assigi	nment Re	gister 3		
CPU A	ccessibility	y: <b>read/</b>	write					
Reset '	Value:	00 <sub>H</sub>						
		Chan	nel A C	hannel B				
Offset	Address:	2B <sub>H</sub>	7	В <sub>Н</sub>				
typical	usage:	writte	n by CPU	,				
		read	and evalua	ated by SE	ROCCO-	Μ		
Bit	7	6	5	4	3	2	1	0
Mode	Transmit Channel Capacity							
н	0	0	0	0	0	0	0	TCC8
Α	0	0	0	0	0	0	0	TCC8
В	0	0	0	0	0	0	0	TCC8



### **Register Description (TTSA3)**

The following register bit fields allow flexible assignment of bit- or octet-aligned transmit time-slots to the serial channel. For more detailed information refer to chapters "Clock Mode 5a (Time Slot Mode)" on Page 55 and "Clock Mode 5b (Octet Sync Mode)" on Page 62.

TCS(2:0) Transmit Clock Shift

This bit field determines the transmit clock shift.

### TEPCM Enable PCM Mask Transmit

(all modes)

(all modes)

This bit selects the additional Transmit PCM Mask (refer to register PCMTX0..PCMTX3):

TEPCM='0' Standard time-slot configuration.

TEPCM='1' The time-slot width is constant 8 bit, bit fields 'TTSN' and 'TCS' determine the offset of the PCM mask and 'TCC' is ignored. Each time-slot selected via register PCMTX0..PCMTX3 is an active transmit timeslot.

TTSN(6:0)Transmit Time Slot Number(all modes)This bit field selects the start position of the timeslot in time-slot<br/>configuration mode (clock mode 5a/5b):

Offset = 1+TTSN\*8 + TCS (1..1024 clocks)

TCC(8:0)Transmit Channel Capacity(all modes)This bit field determines the transmit time-slot width in standard time-slot<br/>configuration (bit TEPCM='0'):<br/>Number of bits = TCC + 1, (1..512 bits/time-slot)



# Register Description (RTSA0)

Register 43	RTSA0 Receive Time \$	Slot Assignment Register 0			
CPU Accessibility:	read/write				
Reset Value:	00 <sub>Н</sub>				
	Channel A	Channel B			
Offset Address:	2C <sub>H</sub>	7C <sub>H</sub>			
typical usage:	written by CPU;				
	read and eval	read and evaluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0
Mode						Rx Clo	ck Shift	
Н	0	0	0	0	0		RCS(2:0)	
Α	0	0	0	0	0		RCS(2:0)	
В	0	0	0	0	0		RCS(2:0)	

Regist	er 44	RTSA1 Receive Time Slot Assignment Register 1							
CPU A	ccessibility	read/write							
Reset V	Value:	00 <sub>H</sub>							
		Chan	nel A	Channel B					
Offset /	set Address: 2D <sub>H</sub> 7D <sub>H</sub>								
typical	typical usage: written by CPU;								
		read and evaluated by SEROCCO-M							
Bit	7	6	5	4	3	2	1	0	
Mode			Rx Time Slot Number						
н	REPCM	RTSN(6:0)							
Α	REPCM	RTSN(6:0)							
В	REPCM				RTSN(6:0)				



# Register Description (RTSA2)

Register 45	RTSA2 Receive Time	Slot Assignment Register 2		
CPU Accessibility:	read/write			
Reset Value:	00 <sub>H</sub>			
	Channel A	Channel B		
Offset Address:	2E <sub>H</sub>	7E <sub>H</sub>		
typical usage:	written by CPU;			
	read and evaluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0		
Mode	Receive Channel Capacity									
н	RCC(7:0)									
Α	RCC(7:0)									
В	RCC(7:0)									

Regist	gister 46 RTSA3 Receive Time Slot Assignment Register 3										
CPU A	U Accessibility: read/write										
Reset '	Value:	00 <sub>H</sub>	00 <sub>н</sub>								
		Chan	Channel A Channel B								
Offset .	Address:	2F <sub>H</sub>	7	'F <sub>н</sub>							
typical	usage:	writte	written by CPU;								
		read	and evalua	ated by SE	ROCCO-	M					
Bit	7	6	5	4	3	2	1	0			
Mode			Receive Channel Capacity								
н	0	0	0	0	0	0	0	RCC8			
Α	0	0	0	0	0	0	0	RCC8			
В	0	0	0	0	0	0	0	RCC8			



(all modes)

(all modes)

### **Register Description (RTSA3)**

The following register bit fields allow flexible assignment of bit- or octet-aligned receive time-slots to the serial channel. For more detailed information refer to chapters "Clock Mode 5a (Time Slot Mode)" on Page 55 and "Clock Mode 5b (Octet Sync Mode)" on Page 62.

RCS(2:0) Receive Clock Shift

This bit field determines the receive clock shift.

### REPCM Enable PCM Mask Receive

This bit selects the additional Receive PCM Mask (refer to register PCMRX0..PCMRX3):

REPCM='0' Standard time-slot configuration.

REPCM='1' The time-slot width is constant 8 bit, bit fields 'RTSN' and 'RCS' determine the offset of the PCM mask and 'RCC' is ignored. Each time-slot selected via register PCMRX0..PCMRX3 is an active receive timeslot.

RTSN(6:0)Receive Time Slot Number(allThis bit field selects the start position of the timeslot in time-slot<br/>configuration mode (clock mode 5a/5b):

Offset = 1+RTSN\*8 + RCS (1..1024 clocks)

RCC(8:0) Receive Channel Capacity

This bit field determines the receive time-slot width in standard time-slot configuration (bit REPCM='0'): Number of bits = RCC + 1, (1..512 bits/time-slot)

Data Sheet

(all modes)

(all modes)



### **Register Description (PCMTX0)**

Register 47	PCMTX0 PCM Mask Tra	ansmit Direction Register 0		
CPU Accessibility:	read/write			
Reset Value:	00 <sub>H</sub>			
	Channel A	Channel B		
Offset Address:	30 <sub>H</sub>	80 <sub>H</sub>		
typical usage: written by CPU;				
	read and evaluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0	
Mode	PCM Mask for Transmit Direction								
н	T07	T06	T05	T04	T03	T02	T01	Т00	
Α	T07	T06	T05	T04	T03	T02	T01	T00	
В	T07	T06	T05	T04	T03	T02	T01	T00	

### **Register 48** PCMTX1 **PCM Mask Transmit Direction Register 1** CPU Accessibility: read/write **Reset Value: 00**<sub>H</sub> Channel A Channel B Offset Address: 81<sub>H</sub> 31<sub>H</sub> typical usage: written by CPU; read and evaluated by SEROCCO-M Bit 7 6 5 4 2 1 3 Mode PCM Mask for Transmit Direction

н	T15	T14	T13	T12	T11	T10	T09	T08
Α	T15	T14	T13	T12	T11	T10	T09	T08
В	T15	T14	T13	T12	T11	T10	T09	T08

0



# Register Description (PCMTX2)

Register 49	PCMTX2 PCM Mask Tra	nsmit Direction Register 2			
CPU Accessibility:	read/write				
Reset Value:	00 <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	32 <sub>H</sub>	82 <sub>H</sub>			
typical usage: written by CPU;					
	read and eva	read and evaluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0
Mode			PCM	Mask for T	ransmit Dire	ection		
н	T23	T22	T21	T20	T19	T18	T17	T16
Α	T23	T22	T21	T20	T19	T18	T17	T16
В	T23	T22	T21	T20	T19	T18	T17	T16

Regist	er 50	PCMTX PCM M	3 ask Trans	smit Direc	tion Regi	ster 3			
CPU A	ccessibility	/: read/	write						
Reset	Reset Value: 00 <sub>H</sub>								
		Chan	nel A C	Channel B					
Offset typical	Address: usage:	33 <sub>H</sub> writte	33 <sub>H</sub> 83 <sub>H</sub> written by CPU;						
	read and evaluated by SEROCCO-M								
Bit	15	14	13	12	11	10	9	8	
Mode	PCM Mask for Transmit Direction								
н	T31	T30	T29	T28	T27	T26	T25	T24	
Α	T31	T30	T29	T28	T27	T26	T25	T24	
В	T31	T30	T29	T28	T27	T26	T25	T24	



### **Register Description (PCMTX3)**

### PCMTX PCM Mask for Transmit Direction

(all mode)

This bit field is valid in clock mode 5 only and the PCM mask must be enabled via bit 'TEPCM' in register TTSA1.

Each bit selects one of 32 (8-bit) transmit time-slots. The offset of timeslot zero to the frame sync pulse can be programmed via register TTSA1 bit field 'TTSN'.



### **Register Description (PCMRX0)**

Register 51	PCMRX0 PCM Mask Receive Direction Register 0				
CPU Accessibility:	read/write				
Reset Value:	00 <sub>н</sub>				
	Channel A	Channel B			
Offset Address:	34 <sub>H</sub>	84 <sub>H</sub>			
typical usage: written by CPU;					
	read and eva	aluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0
Mode			PCM	Mask for R	eceive Dire	ection		
н	R07	R06	R05	R04	R03	R02	R01	R00
Α	R07	R06	R05	R04	R03	R02	R01	R00
В	R07	R06	R05	R04	R03	R02	R01	R00

#### **Register 52** PCMRX1 **PCM Mask Receive Direction Register 1** read/write CPU Accessibility: **Reset Value: 00**<sub>H</sub> Channel A Channel B Offset Address: 35<sub>н</sub> 85<sub>H</sub> typical usage: written by CPU; read and evaluated by SEROCCO-M Bit 15 14 13 12 11 10 9 8 Mode PCM Mask for Receive Direction R15 R14 R13 R12 R11 R10 R09 R08 н R15 R14 R13 R12 R11 R10 R09 R08 Α

В

R15

R14

R13

R12

R11

R10

R09

R08



### **Register Description (PCMRX2)**

Register 53	PCMRX2 PCM Mask Re	ceive Direction Register 2			
CPU Accessibility:	read/write				
Reset Value:	00 <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	36 <sub>H</sub>	86 <sub>H</sub>			
typical usage:	written by CPU;				
	read and evaluated by SEROCCO-M				

Bit	7	6	5	4	3	2	1	0
Mode			PCM	Mask for R	Receive Dire	ection		
н	R23	R22	R21	R20	R19	R18	R17	R16
Α	R23	R22	R21	R20	R19	R18	R17	R16
В	R23	R22	R21	R20	R19	R18	R17	R16

### **Register 54** PCMRX3 **PCM Mask Receive Direction Register 3** CPU Accessibility: read/write **Reset Value: 00**<sub>H</sub> Channel A Channel B Offset Address: 37<sub>н</sub> 87<sub>H</sub> typical usage: written by CPU; read and evaluated by SEROCCO-M Bit 12 11 10 15 14 13 9 8 Mode PCM Mask for Receive Direction R20 R28 н R31 R30 **R**27 R26 R25 R21

	131	130	1123	1120	1\27	1120	1125	1124
Α	R31	R30	R29	R28	R27	R26	R25	R24
В	R31	R30	R29	R28	R27	R26	R25	R24



### **Register Description (PCMRX3)**

### PCMRX PCM Mask for Receive Direction

(all mode)

This bit field is valid in clock mode 5 only and the PCM mask must be enabled via bit 'REPCM' in register RTSA1.

Each bit selects one of 32 (8-bit) receive time-slots. The offset of timeslot zero to the frame sync pulse can be programmed via register RTSA1 bit field 'RTSN'.



# Register Description (BRRL)

Register 55	BRRL Baud Rate Re	gister (Low Byte)	
CPU Accessibility:	read/write		
Reset Value:	00 <sub>H</sub>		
	Channel A	Channel B	
Offset Address:	38 <sub>H</sub>	88 <sub>H</sub>	
typical usage:	written by CPU;		
	read and eva	aluated by SEROCCO-M	

Bit	7	6	5	4	3	2	1	0
Mode			Bau	ld Rate Gen	erator Facto	or N		
н	0	0		BRN(5:0)				
Α	0	0		BRN(5:0)				
В	0	0			BRN	(5:0)		

Regist	er 56	BRRH Baud Rate Register (High Byte)						
CPU A	ccessibility	y: <b>read/</b>	write					
Reset '	Value:	00 <sub>H</sub>						
		Chan	nel A C	Channel B				
Offset	Address:	39 <sub>H</sub>	8	9 <sub>H</sub>				
typical usage: written			n by CPU	,				
		read	and evalua	ated by SE	ROCCO-I	Μ		
Bit	7	6	5	4	3	2	1	0
Mode			Bau	d Rate Gen	erator Fact	or M		
Н	0	0	0 0 0 BRM(3:0)					
Α	0	0	0	0	BRM(3:0)			
В	0	0	0	0	BRM(3:0)			



### **Register Description (BRRH)**

BRM(3:0)	Baud Rate Factor 'M'
----------	----------------------

(all modes) (all modes)

BRN(5:0) Baud Rate Factor 'N'

These bit fields determine the division factor of the internal baud rate generator. The baud rate generator input clock and the usage of baud rate generator output depends on the selected clock mode. The division factor k is calculated by:

$$k = (N+1) \times 2^{M}$$

with M=0..15 and N=0..63.

$$f_{BRG} = f_{in}/k$$



Register Description (TIMR0)

Register 57	TIMR0 Timer Registe	er O	
CPU Accessibility:	read/write		
Reset Value:	00 <sub>H</sub>		
	Channel A	Channel B	
Offset Address:	ЗА <sub>Н</sub>	8A <sub>H</sub>	
typical usage:	written by CPU;		
	read and eva	aluated by SEROCCO-M	

Bit	7	6	5	4	3	2	1	0
Mode				Timer	Value			
н				TVALU	JE(7:0)			
Α				TVALU	JE(7:0)			
В				TVALU	JE(7:0)			

Regist	er 58	TIMR1 Timer Regi	ster ´	1					
CPU A	ccessibility:	read/write	e						
Reset V	Value:	00 <sub>H</sub>							
		Channel /	A (	Channel B					
Offset /	Address:	3B <sub>H</sub>	8	3B <sub>H</sub>					
typical usage:		written by	written by CPU;						
		read and	evalu	ated by SE	ROCCO-	Μ			
Bit	7	6	5	4	3	2	1	0	
Mode	Timer Value								
н	TVALUE(15:0)								
Α	TVALUE(15:0)								
В	TVALUE(15:0)								



### Register Description (TIMR2)

Register 59	TIMR2 Timer Registe	er 2	
CPU Accessibility:	read/write		
Reset Value:	00 <sub>H</sub>		
	Channel A	Channel B	
Offset Address:	3С <sub>н</sub>	8C <sub>H</sub>	
typical usage:	written by CPU;		
	read and eva	aluated by SEROCCO-M	

Bit	7	6	5	4	3	2	1	0
Mode				Timer	Value			
н				TVALU	E(23:16)			
Α				TVALU	E(23:16)			
В				TVALU	E(23:16)			

Regist	er 60	TIMR3 Timer F	Register 3					
CPU A	ccessibility	/: read/	write					
Reset '	Value:	00 <sub>H</sub>						
		Chan	nel A C	hannel B				
Offset .	Address:	3D <sub>H</sub>	8	D <sub>H</sub>				
typical	usage:	writte	n by CPU					
		read	read and evaluated by SEROCCO-M					
Bit	7	6	5	4	3	2	1	0
Mode	Timer Configuration							
Н	SRC	0	0	TMD	0		CNT(2:0)	
Α	SRC	0	0	0	0		CNT(2:0)	
В	SRC	0	0	0	0		CNT(2:0)	



### **Register Description (TIMR3)**

### SRC Clock Source (valid in clock mode 5 only)

(all modes)

This bit selects the clock source of the internal timer:

- SRC = '0' The timer is clocked by the effective transmit clock.
- SRC = '1' The timer is clocked by the frame-sync synchronization signal supplied via the FSC pin in clock mode 5.

### TMD Timer Mode

(hdlc modes)

This bit must be set to '1' if HDLC Automode operation is selected. In all other protocol modes it must remain '0':

TMD='0' The timer is controlled by the CPU via access to registers CMDRL and TIMR0..TIMR3.
The timer can be started any time by setting bit 'STI' in register CMDRL. After the timer has expired it generates a timer interrupt. The timer can be stopped any time by setting bit 'TRES' in register CMDRL to '1'.

TMD='1' The timer is used by the SEROCCO-M for protocol specific time-out and retry transactions in HDLC Automode.

### CNT(2:0) Counter

(all modes)

The meaning of this bit field depends on the selected protocol mode. In HDLC Automode, with bit TMD='1':

 Retry Counter (in HDLC protocol known as 'N2'): Bit field 'CNT' indicates the number of S-Command frames (with poll bit set) which are transmitted autonomously by SEROCCO-M after every expiration of the time out period 't' (determined by 'TVALUE'), in case an I-Frame gets not acknowledged by the opposite station. The maximum value is 6 S-command frames. If 'CNT' is set to '7', the number of S-commands is unlimited in case of no acknowledgement.

### In all other modes, with bit TMD='0':

• Restart Counter :

Bit field 'CNT' indicates the number of automatic restarts which are performed by SEROCCO-M after every expiration of the time-out period 't', in case the timer is not stopped by setting bit 'TRES' in register CMDRL to '1'. The maximum value is 6 restarts. If 'CNT' is set to '7', a timer interrupt is generated periodically with time period 't' determined by bit field 'TVALUE'.



### **Register Description (TIMR3)**

# **TVALUETimer Expiration Value**(all modes)(23:0)This bit field determines the timer expiration period 't':

 $t = (TVALUE + 1) \cdot CP$ 

('CP' is the clock period, depending on bit 'SRC'.)



**Register Description (XAD1)** 

Register 61	XAD1 Transmit Addı	ess 1 Register		
CPU Accessibility:	read/write			
Reset Value:	00 <sub>H</sub>			
	Channel A	Channel B		
Offset Address:	ЗЕ <sub>Н</sub>	8E <sub>H</sub>		
typical usage:	written by CPU; read and evaluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0	
Mode	Transmit Address (high)								
н		XAD1 (high byte) 0 XAD1_0							
		or XAD1 (COMMAND)							
Α	0	0	0	0	0	0	0	0	
В	0	0	0	0	0	0	0	0	

Register 62	XAD2 Transmit Add	ress 2 Register
CPU Accessibility:	read/write	
Reset Value:	00 <sub>H</sub>	
	Channel A	Channel B
Offset Address:	ЗF <sub>н</sub>	8F <sub>H</sub>
typical usage:	written by CF	PU; read and evaluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0	
Mode		Transmit Address (low)							
н		XAD2 (low byte)							
		or XAD2 (RESPONSE)							
Α	0	0	0	0	0	0	0	0	
В	0	0	0	0	0	0	0	0	



XAD1 and XAD2 bit fields are valid in HDLC modes with automatic address field handling only (Automode, Address Mode 1, Address Mode 2). They can be programmed with one individual address byte which is inserted automatically into the address field (8 or 16 bit) of a HDLC transmit frame. The function depends on the selected protocol mode and address field size (bit 'ADM' in register CCR2L).

### XAD1 Transmit Address 1

(hdlc modes)

- 2-byte address field:

Bit field XAD1 constitutes the high byte of the 2-byte address field. Bit 1 must be set to '0'. According to the ISDN LAP-D protocol, bit 1 is interpreted as the C/R (COMMAND/RESPONSE) bit. This bit is manipulated automatically by SEROCCO-M according to the setting of bit 'CRI' in register RAH1. The following is the C/R value (on bit 1), when:

transmitting COMMANDs: '1' (if 'CRI'='1'); '0' (if 'CRI'='0')
transmitting RESPONSEs: '0' (if 'CRI'='1'); '1' (if 'CRI'='0')
(In ISDN LAP-D, the high byte is known as 'SAPI'.)

In accordance with the HDLC protocol, bit 'XAD1\_0' should be set to '0', to indicate that the address field contains (at least) one more byte.

- 1-byte address field: According to the X.25 LAP-B protocol, XAD1 is the address of a 'COMMAND' frame.
- XAD2 Transmit Address 2

(hdlc modes)

- 2-byte address field:
   Bit field XAD2 constitutes the low byte of the 2-byte address field.
   (In ISDN LAP-D, the low byte is known as 'TEI'.)
- 1-byte address field:

According to the X.25 LAP-B protocol, XAD2 is the address of a 'RESPONSE' frame.



### **Register Description (RAL1)**

Register 63	RAL1 Receive Addre	AL1 eceive Address 1 Low Register				
CPU Accessibility:	read/write					
Reset Value:	00 <sub>H</sub>					
	Channel A	Channel B				
Offset Address:	40 <sub>H</sub>	90 <sub>H</sub>				
typical usage: written by CPU; read and evaluated by SEROCCO-M						

Bit	7	6	5	4	3	2	1	0	
Mode		Receive Address 1 (low)							
н		RAL1							
		RAL1							
Α	0	0	0	0	0	0	0	0	
В	0	0	0	0	0	0	0	0	

Regist	er 64	RAH1 Receive	e Addro	ess 1 High R	egister				
CPU A	ccessibility:	read/	write						
Reset V	Value:	00 <sub>H</sub>	00 <sub>н</sub>						
		Chan	nel A	Channel B					
Offset Address: 4				91 <sub>H</sub>					
typical	usage:	writte	n by Cl	PU; read and	evaluated	by SERC	OCCO-M		
Bit	7	6	5	4	3	2	1	0	
Mode	Receive Address 1 (high)								
н	RAH1 CRI RAH1_							RAH1_0	
		or RAH1							

Α

В



### **Register Description (RAL2)**

Register 65	RAL2 Receive Addre	ess 2 Low Register
CPU Accessibility:	read/write	
Reset Value:	00 <sub>H</sub>	
	Channel A	Channel B
Offset Address:	42 <sub>H</sub>	92 <sub>H</sub>
typical usage:	written by CI	PU;
	read and eva	aluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0
Mode			F	Receive Ado	dress 2 (low	)		
Н		RAL2						
Α	0	0	0	0	0	0	0	0
В	0	0	0	0	0	0	0	0

Regist	ster 66 RAH2 Receive Address 2 High Register									
CPU A	ccessibility	ssibility: <b>read/write</b>								
Reset '	Value:	00 <sub>H</sub>	00 <sub>н</sub>							
		Chan	nel A C	hannel B						
Offset	Address:	43 <sub>H</sub>	9	3 <sub>H</sub>						
typical	usage:	writte	written by CPU;							
		read	and evalua	ated by SE	ROCCO-I	Μ				
Bit	7	6	5	4	3	2	1	0		
Mode	Receive Address 2 (high)									
н				RA	H2					
Α	0	0	0	0	0	0	0	0		
В	0	0	0	0	0	0	0	0		



### **Register Description (RAH2)**

In operating modes that provide address recognition, the high/low byte of the received address is compared with the individually programmable values in register RAH2/RAL2/RAH1/RAL1.

This addresses can be masked on a per bit basis by setting the corresponding bits in registers AMRAL1/AMRAH1/AMRAL2/AMRAH2 to allow extended broadcast address recognition. This feature is applicable to all HDLC sub-modes with address recognition.

### RAH1 Receive Address 1 Byte High

(hdlc modes)

In HDLC Automode bit '1' is reserved for 'CRI' (Command Response Interpretation). In all other modes RAH1 is an 8 bit address.

**CRI Command/Response Interpretation** The setting of this bit effects the meaning of the 'C/R' bit in the receive status byte (RSTA). This status bit 'C/R' should be interpreted after reception as follows:

'0' (if 'CRI'='1') ;	'1' (if 'CRI'='0') :	COMMAND received
'1' (if 'CRI'='1') ;	'0' (if 'CRI'='0') :	RESPONSE received

Note: If 1-byte address field is selected in HDLC Automode, RAH1 must be set to  $0x00_{H}$ .

### RAL1 Receive Address 1 Byte Low

(hdlc modes)

(hdlc modes)

The general function and its meaning depends on the selected HDLC operating mode:

### • Automode / Address Mode 2 (16-bit address)

RAL1 can be programmed with the value of the first individual low address byte.

• Automode / Address Mode 2 (8-bit address) According to X.25 LAP-B protocol, the address in RAL1 is considered as the address of a 'COMMAND' frame.

### RAH2 Receive Address 2 Byte High

RAL2Receive Address 2 Byte Low(hdlc modes)Value of the second individually programmable high/low address byte. If<br/>a 1-byte address field is selected, RAL2 is considered as the address of<br/>a 'RESPONSE' frame according to X.25 LAP-B protocol.



### Register Description (AMRAL1)

Register 67	AMRAL1 Mask Receive Address 1 Low Register					
CPU Accessibility:	read/write					
Reset Value:	00 <sub>H</sub>					
	Channel A	Channel B				
Offset Address:	44 <sub>H</sub>	94 <sub>H</sub>				
typical usage:	written by CPU;					
	read and eva	read and evaluated by SEROCCO-M				

Bit	7	6	5	4	3	2	1	0		
Mode		Receive Mask Address 1 (low)								
н		AMRAL1								
Α	0	0	0	0	0	0	0	0		
В	0	0	0	0	0	0	0	0		

Regist	er 68	AMRAH Mask R	l1 eceive Ac	ddress 1 I	ligh Regi	ster		
CPU A	ccessibility	y: read/	write					
Reset '	Value:	00 <sub>H</sub>						
		Chan	nel A C	hannel B				
Offset	Address:	45 <sub>н</sub>	9	5 <sub>H</sub>				
typical	usage:	writte	n by CPU	,				
		read	read and evaluated by SEROCCO-M					
Bit	7	6	5	4	3	2	1	0
Mode	Receive Mask Address 1 (high)							
н	AMRAH1							
Α	0	0	0 0 0 0 0 0 0					
В	0	0	0	0	0	0	0	0



### Register Description (AMRAL2)

Register 69	AMRAL2 Mask Receive	Address 2 Low Register
CPU Accessibility:	read/write	
Reset Value:	00 <sub>H</sub>	
	Channel A	Channel B
Offset Address:	46 <sub>H</sub>	96 <sub>H</sub>
typical usage:	written by CF	PU;
	read and eva	luated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0		
Mode		Receive Mask Address 2 (low)								
н		AMRAL2								
Α	0	0 0 0 0 0 0 0 0								
В	0	0	0	0	0	0	0	0		

Regist	er 70	AMRAH Mask R	l2 eceive Ac	ddress 2 H	ligh Regi	ster		
CPU A	ccessibility	y: <b>read/</b>	write					
Reset '	Value:	00 <sub>H</sub>						
		Chan	nel A C	hannel B				
Offset	Address:	47 <sub>H</sub>	9	7 <sub>H</sub>				
typical	usage:	writte	n by CPU;	;				
		read	and evalua	ated by SE	ROCCO-	Μ		
Bit	7	6	5	4	3	2	1	0
Mode	Receive Mask Address 2 (high)							
н	AMRAH2							
Α	0	0	0 0 0 0 0 0 0					
В	0	0	0	0	0	0	0	0



### **Register Description (AMRAH2)**

AMRAH2	Receive Mask Address 2 Byte High	(hdlc modes)
AMRAL2	Receive Mask Address 2 Byte Low	(hdlc modes)
AMRAH1	Receive Mask Address 1 Byte High	(hdlc modes)
AMRAL1	Receive Mask Address 1 Byte Low	(hdlc modes)

Setting a bit in this registers to '1' masks the corresponding bit in registers RAH2/RAL2/RAH1/RAL1. A masked bit position always matches when comparing the received frame address with registers RAH2/RAL2/RAH1/RAL1, allowing extended broadcast mechanism.

- bit = '0' The dedicated bit position is NOT masked. This bit position in the received address must match with the corresponding bit position in registers RAH2/RAL2/RAH1/ RAL1 to accept the frame.
- bit = '1' The dedicated bit position is masked. This bit position in the received address NEED NOT match with the corresponding bit position in registers RAH2/RAL2/RAH1/ RAL1 to accept the frame.



### **Register Description (RLCRL)**

Register 71	RLCRL Receive Leng	th Check Register (Low Byte)
CPU Accessibility:	read/write	
Reset Value:	00 <sub>H</sub>	
	Channel A	Channel B
Offset Address:	48 <sub>H</sub>	98 <sub>H</sub>
typical usage:	written by CF	PU;
	read and eva	aluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0
Mode				Receive Lo	ength Limit			
Н		RL(7:0)						
Α	0	0	0	0	0	0	0	0
В	0	0	0	0	0	0	0	0

### Register 72 RLCRH Receive Length Check Register (High Byte)

CPU Accessibility:	read/write	
Reset Value:	00 <sub>H</sub>	
	Channel A	Channel B
Offset Address: typical usage:	<b>49<sub>H</sub></b> written by CP read and eval	99 <sub>H</sub> U; uated by SEROCCO-M
		,

Bit	7	6	5	4	3	2	1	0	
Mode	Rec	eive Length	n Check Co	ntrol		Receive Length Limit			
н	RCE	0	0	0	0	RL(10:8)			
Α	0	0	0	0	0	0 0 0			
В	0	0	0	0	0	0	0	0	



### **Register Description (RLCRH)**

### RCE Receive Length Check Enable

(hdlc modes)

This bit is valid in HDLC mode only and enables/disables the receive length check function:

- RCE = '0' No receive length check on received HDLC frames is performed.
- RCE = '1' The receive length check is enabled. All bytes of a HDLC frame which are transferred to the receive FIFO (depending on the selected protocol sub-mode and receive CRC handling) are counted and checked against the maximum length check limit which is programmed in bit field 'RL'.

A frame exceeding the maximum length is treated as if it were aborted on the receive line ('RME' interrupt and bit 'RAB' (receive abort) set in the RSTA byte).

In addition a 'FLEX' interrupt is generated prior to 'RME', if enabled.

Note: The Receive Status Byte (RSTA) is part of the frame length checking.

RL(10:0) Receive Length Check Limit

(hdlc modes)

This bit-field defines the receive length check limit (32..65536 bytes) if checking is enabled via bit 'RCE':

RL(10:0) The receive length limit is calculated by:

 $Limit = (RL + 1) \cdot 32$ 



**Register Description (XON)** 

Register 73	XON XON In-Band	Flow Control Character Register
CPU Accessibility:	read/write	
Reset Value:	00 <sub>H</sub>	
	Channel A	Channel B
Offset Address:	4A <sub>H</sub>	9A <sub>H</sub>
typical usage:	written by CI	PU;
	read and eva	aluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0	
Mode				XON CI	naracter				
н	0	0	0	0	0	0	0	0	
Α		XON(7:0)							
В	0	0	0	0	0	0	0	0	

# Register 74XOFF<br/>XOFF In-Band Flow Control Character RegisterCPU Accessibility:read/writeReset Value:00<sub>H</sub>Channel AChannel BOffset Address:4B<sub>H</sub>9B<sub>H</sub>typical usage:written by CPU;<br/>read and evaluated by SEROCCO-M

Bit	7	6	5	4	3	2	1	0
Mode				XOFF C	haracter			
н	0	0	0	0	0	0	0	0
Α	XOFF(7:0)							
В	0	0	0	0	0	0	0	0



### **Register Description (XOFF)**

### XON(7:0) XON Character

(async mode)

This bit field specifies the XON character for in-band flow control in ASYNC protocol mode. The number of significant bits starting with the LSB depends on the character length (5..8 bits) selected via bit field 'CHL(1:0)' in register CCR3L.

A received character is recognized as a valid XON-character, if

- the character was correctly framed (character length as programmed and correct parity if checking is enabled)
- each bit position of the received character which is not masked via register MXON matches with the corresponding bit in register XON.

Received characters recognized as XON character are stored in the receive FIFO as normal receive data unless disabled with bit CCR3L:DXS. An appropriate 'XON' interrupt is generated (if enabled) and the transmitter is switched into 'XON' state if in-band flow control is enabled via bit 'FLON' in register CCR2H.

### XOFF(7:0) XOFF Character

(async mode)

This bit field specifies the XOFF character for in-band flow control in ASYNC protocol mode. The number of significant bits starting with the LSB depends on the character length (5..8 bits) selected via bit field 'CHL(1:0)' in register CCR3L.

A received character is recognized as a valid XOFF-character, if

- the character was correctly framed (character length as programmed and correct parity if checking is enabled)
- each bit position of the received character which is not masked via register MXOFF matches with the corresponding bit in register XOFF.

Received characters recognized as XOFF character are stored in the receive FIFO as normal receive data unless disabled with bit CCR3L:DXS. An appropriate 'XOFF' interrupt is generated (if enabled) and the transmitter is switched into 'XOFF' state if in-band flow control is enabled via bit 'FLON' in register CCR2H.



### **Register Description (MXON)**

Register 75	MXON XON In-Band	Flow Control Mask Register			
CPU Accessibility:	read/write				
Reset Value:	00 <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	4C <sub>H</sub>	9C <sub>H</sub>			
typical usage:	written by CPU;				
	read and evaluated by SEROCCO-M				

Bit	7	6	5	4	3	2	1	0
Mode	XON Character Mask							
н	0	0	0	0	0	0	0	0
Α	MXON(7:0)							
В	0	0	0	0	0	0	0	0

### **Register 76 MXOFF XOFF In-Band Flow Control Mask Register** CPU Accessibility: read/write **Reset Value: 00**<sub>H</sub> Channel A Channel B 4D<sub>H</sub> Offset Address: 9D<sub>H</sub> typical usage: written by CPU; read and evaluated by SEROCCO-M Bit 7 6 5 4 3 2 1 Mode **XOFF Character Mask** 0 0 0 Λ Λ 0 0 н

	0	0	0	0	0	0	U
Α	MXOFF(7:0)						
В	0	0	0	0	0	0	0

0

0

0



### **Register Description (MXOFF)**

### MXON(7:0) XON Character Mask

(async mode)

Setting a bit in this bit field to '1' masks the corresponding bit in bit field 'XON(7:0)' of register XON. A masked bit position always matches when comparing the received character with bit field 'XON(7:0)'.

- bit = '0' The dedicated bit position is NOT masked. This bit position in the received character must match with the corresponding bit position in bit field 'XON' to recognize the received character as an XON character.
- bit = '1' The dedicated bit position is masked. This bit position in the received character NEED NOT match with the corresponding bit position in bit field 'XON' to recognize the received character as an XON character.

### MXOFF(7:0) XOFF Character Mask

(async mode)

Setting a bit in this bit field to '1' masks the corresponding bit in bit field 'XOFF(7:0)' of register XOFF. A masked bit position always matches when comparing the received character with bit field 'XOFF(7:0)'.

- bit = '0' The dedicated bit position is NOT masked. This bit position in the received character must match with the corresponding bit position in bit field 'XOFF' to recognize the received character as an XOFF character.
- bit = '1' The dedicated bit position is masked. This bit position in the received character NEED NOT match with the corresponding bit position in bit field 'XOFF' to recognize the received character as an XOFF character.



**Register Description (TCR)** 

Register 77	TCR Termination C	CR ermination Character Register					
CPU Accessibility:	read/write						
Reset Value:	00 <sub>H</sub>						
	Channel A	Channel B					
Offset Address:	4Е <sub>н8</sub>	9E <sub>H</sub>					
typical usage:	written by CF	PU;					
	read and eva	luated by SEROCCO-M					

Bit	7	6	5	4	3	2	1	0
Mode	Termination Character							
Н	0	0	0	0	0	0	0	0
Α	TC(7:0)							
В	TC(7:0)							

### TC(7:0) Termination Character

(async mode)

This bit-field defines the termination character which is monitored on the receive data stream if enabled via bit 'TCDE' in register CCR3L.



### **Register Description (TICR)**

Register 78	TICR Transmit Imm	ediate Character Register			
CPU Accessibility:	read/write				
Reset Value:	00 <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	4F <sub>H</sub>	9F <sub>H</sub>			
typical usage:	written by CPU;				
	read and evaluated by SEROCCO-M				

Bit	7	6	5	4	3	2	1	0
Mode	Transmit Immediate Character							
н	0	0	0	0	0	0	0	0
Α	TIC(7:0)							
В	0	0	0	0	0	0	0	0


#### **Register Description (TICR)**

#### TIC Transmit Immediate Character

(async mode)

On write access to this register, the ASYNC protocol engine will automatically insert the character defined by bit field 'TIC' into the transmit data stream.

This happens

- immediately after write access to register TICR if the transmitter is in IDLE state (no other character is currently transmitted). The transmitter returns to IDLE state after transmission of the TIC.
- immediately after the character which is currently in transmission is completed. After transmission of the TIC, the transmitter continues with transmission of characters which are still stored in the transmit FIFO. Thus the TIC is inserted into the data stream between the characters provided via the transmit FIFO.

The TIC transmission is independent of in-band flow control. Thus the TIC is sent out even if the transmitter is in 'XOFF' state. However the transmitter must be enabled via signal  $\overline{\text{CTS}}$  (depending on bit 'FCTS' in register CCR1H).

The number of significant bits (starting with the LSB) depends on the character length programmed in bit field 'CHL(1:0)' in register CCR3L. All character framing related settings in registers CCR3L/CCR3H (start bit, parity generation, number of stop bits) also apply to the TIC character framing.

As long as the TIC character is not completely sent, status bit TIC Execution ('TEC') in status register STARL is set to '1' by SEROCCO-M. No further write access to register TICR is allowed until 'TEC' status indication is cleared by SEROCCO-M.



# **Register Description (ISR0)**

Register 79	ISR0 Interrupt Status Register 0					
CPU Accessibility:	read only					
Reset Value:	00 <sub>H</sub>					
	Channel A	Channel B				
Offset Address:	50 <sub>н</sub>	A0 <sub>H</sub>				
typical usage:	updated by	SEROCCO-M				
	read and eva	aluated by CPU				

Bit	7	6	5	4	3	2	1	0
Mode				IS	R0			
н	RDO	RFO	PCE	RSC	RPF	RME	RFS	FLEX
Α	0	RFO	FERR	PERR	RPF	TCD	TIME	0
В	0	RFO	SCD	PERR	RPF	TCD	0	0

Regist	er 80	ISR1 Interruj	ot Status	Register <sup>2</sup>	1				
CPU A	ccessibility	y: <b>read</b>	only						
Reset '	Value:	00 <sub>H</sub>							
	Ingister 80       ISR1 Interrupt Status Register 1         PU Accessibility:       read only set Value:       00 <sub>H</sub> Channel A       Channel B         Set Value:       00 <sub>H</sub> Channel A       Channel B         Iset Address:       51 <sub>H</sub> A1 <sub>H</sub> A1 <sub>H</sub> sical usage:       updated by SEROCCO-M read and evaluated by CPU         Bit       7       6       5       4       3       2       1         H       TIN       CSC       XMR       XPR       ALLS       XDU       SUEX         A       TIN       CSC       XOFF       XPR       ALLS       XON       BRK       BI								
Offset	Address:	51 <sub>H</sub>	A	1 <sub>H</sub>					
typical usage: updated by SEROCCO-M read and evaluated by CPU									
Bit	7	6	5	4	3	2	1	0	
Mode			ISR1						
н	TIN	CSC	XMR	XPR	ALLS	XDU	SUEX	0	
Α	TIN	CSC	XOFF	XPR	ALLS	XON	BRK	BRKT	
В	TIN	CSC	XMR	XPR	ALLS	XDU	0	0	



# **Register Description (ISR2)**

Register 81	ISR2 Interrupt Status Register 2					
CPU Accessibility:	read only					
Reset Value:	00 <sub>H</sub>					
	Channel A	Channel B				
Offset Address:	52 <sub>H</sub>	A2 <sub>H</sub>				
typical usage:	updated by S	SEROCCO-M				
	read and eva	aluated by CPU				

Bit	7	6	5	4	3	2	1	0
Mode				IS	R2			
Н	0	0	0	0	0	0	PLLA	CDSC
Α	0	0	0	0	0	0	PLLA	CDSC
В	0	0	0	0	0	0	PLLA	CDSC



(hdlc mode)

(all modes)

#### **Register Description (ISR2)**

#### RDO Receive Data Overflow Interrupt

This bit is set to '1', if receive data of the current frame got lost because of a SCC receive FIFO full condition. However the rest of the frame is received and discarded as long as the receive FIFO remains full and is stored as soon as FIFO space is available again. The receive status byte (RSTA) of such a frame contains an 'RDO' indication. In DMA operation the 'RDO' indication is also set in the receive byte count register RBCH.

#### RFO Receive FIFO Overflow Interrupt

#### HDLC Mode:

This bit is set to '1', if the SCC receive FIFO is full and a complete frame must be discarded. This interrupt can be used for statistical purposes, indicating that the host was not able to service the SCC receive FIFO quickly enough, e.g. due to high bus latency.

#### ASYNC/BISYNC Mode:

This bit is set to '1', if the SCC receive FIFO is full and another received character has been discarded. This interrupt can be used for statistical purposes and might indicate that the host was not able to service the SCC receive FIFO quickly enough, e.g. bus latencies are too high.

PCE Protocol Error Interrupt

(hdlc mode)

(async mode)

This bit is valid in HDLC Automode only.

It is set to '1', if the receiver has detected a protocol error, i.e. one of the following events occured:

- an S- or I-frame was received with wrong N(R) counter value;
- an S-frame containing an Information field was received.

#### FERR Framing Error Interrupt

This bit is set to '1', if a character framing error is detected, i.e. a '0' was sampled at a position where a stop bit '1' was expected due to the selected character format.



#### **Register Description (ISR2)**

(bisync mode)

(hdlc mode)

(all modes)

(async/bisync modes)

#### SCD Sync Character Detected

Only valid in Hunt Mode.

This bit is set to '1' if a SYN character is found in the received data stream after the 'HUNT' command has been issued in register CMDRH. The receiver now is in the synchronous state.

#### RSC Receive Status Change Interrupt

This bit is valid in HDLC Automode only.

It is set to '1', if a status change of the remote station receiver has been detected by receiving a S-frame with receiver ready (RR) or receiver not ready (RNR) indication. Because only a status change is indicated via this interrupt, the current status can be evaluated by reading bit 'RRNR' in status register STARH.

#### PERR Parity Error Interrupt

This bit is only valid if parity checking/generation is enabled via bit 'PARE' in register CCR3H.

It is set to '1', if a character with wrong parity has been received. If enabled via bit CCR3H:RFDF, this error status is additionally stored in the receive status byte generated for each receive character.

#### RPF Receive Pool Full Interrupt

This bit is set to '1' if the RFIFO threshold level, set with bit field 'RFTH(1:0)' in register CCR3H, is reached. Default threshold level is 32 data bytes in HDLC/PPP modes, 1 data byte in ASYNC/BISYNC modes.





#### **Register Description (ISR2)**

#### RME Receive Message End Interrupt

Ínfineon

(hdlc mode)

This bit set to '1' indicates that the reception of one message is completed, i.e. either

- one message which fits into RFIFO not exceeding the receive FIFO threshold, or
- the last part of a message, all in all exceeding the receive FIFO threshold

is stored in the RFIFO.

The complete message length can be determined by reading the RBCL/ RBCH registers. The number of bytes stored in RFIFO is given by the 5, 4, 2 or 1 least significant bits of register RBCL, depending on the selected RFIFO threshold (bit field 'RFTH(1:0)' in register CCR3H). Additional frame status information is available in the RSTA byte, stored in the RFIFO as the last byte of each frame.

Note: After the RFIFO contents have been read, an CMDRH:RMC command must be issued to free the RFIFO for new receive data.

#### TCDTermination Character Detected Interrupt(async/bisync mode)

This bit is set to '1', if a termination character (TCR) has been detected in the receive data stream or an 'RFRD' command, issued in the CMDRH register, has been completed. The SCC will insert a 'block end' indication to the RFIFO. The actual block length can be determined by reading register RBCL.

Note: After the RFIFO contents have been read, an CMDRH:RMC command must be issued to free the RFIFO for new receive data.

#### RFS Receive Frame Start Interrupt

(hdlc mode)

(async mode)

This bit is set to '1', if the beginning of a valid frame is detected by the receiver. A valid frame start is detected either if a valid address field is recognized (in all operating modes with address recognition) or if a start flag is recognized (in all operating modes with no address recognition).

#### TIME Time Out Interrupt

This bit is set to '1', if the time out limit is exceeded, i.e. no new character was received in a programmable period of time (refer to register TOLEN bit fields 'TOIE' and 'TOLEN' for more information).

#### Data Sheet

(async mode)

#### **Register Description (ISR2)**

#### Frame Length Exceeded Interrupt **FLEX**

This bit is set to '1', if the frame length check feature is enabled and the current received frame is aborted because the programmed frame length limit was exceeded (refer to registers RLCRL/RLCRH for detailed description).

#### TIN **Timer Interrupt**

This bit is set to '1', if the internal timer was activated and has expired (refer also to description of timer registers TIMR0..TIMR3).

#### CSC **CTS Status Change**

This bit is set to '1', if a transition occurs on signal CTS. The current state of signal CTS is monitored by status bit 'CTS' in status register STARL.

Note: A transmit clock must be provided to detect a transition of CTS.

#### XMR Transmit Message Repeat

This bit is set to '1', if transmission of the last frame has to be repeated (by software), because

- the SCC has received a negative acknowledge to an I-frame (in HDLC Automode operation);
- a collision occured after at least 14.5 bytes of data have been completely sent out, i.e. automatic re-transmission cannot be performed by the SCC;
- CTS signal was deasserted after at least 14.5bytes of data have been completely sent out.
- Note: For easy recovery from a collision event (in bus configuration only), the SCC transmit FIFO should not contain more than one complete frame. This can be achieved by using the 'ALLS' interrupt to control the corresponding transmit channel forwarding a new frame on all sent (ALLS) event only.

#### XOFF **XOFF Character Detected Interrupt**

#### **ASYNC Mode:**

This bit is set to '1', if the currently received character matched the XOFF character programmed in register XOFF and indicates, that the transmitter is switched to 'XOFF' state if in-band flow control is enabled via bit 'FLON' in register CCR2H.

5-223



(all modes)

(all modes)

(hdlc/bisync modes)

(hdlc mode)



#### XPR Transmit Pool Ready Interrupt

(all modes)

(all modes)

This bit is set to '1', if a transmitter reset command was executed successfully (command bit 'XRES' in register CMDRL) and whenever the XFIFO is able to accept new transmit data again.

An 'XPR' interrupt is not generated, if no sufficient transmit clock is available (depending on the selected clock mode).

#### ALLS ALL Sent Interrupt

#### HDLC Mode:

This bit is set to '1':

- if the last bit of the current HDLC frame is sent out via pin TxD and no further frame is stored in the SCC transmit FIFO, i.e. the transmit FIFO is empty (Address Mode 2/1/0);
- if an I-frame is sent out completely via pin TxD and either a valid acknowledge S-frame has been received or a time-out condition occured because no valid acknowledge S-frame has been received in time (Automode).

#### ASYNC/BISYNC Mode:

This bit is set to '1', if the last character is completely sent via pin TxD and no further data is stored in the SCC transmit FIFO, i.e. the transmit FIFO is empty.

#### XDU Transmit Data Underrun Interrupt

(hdlc/bisync modes)

This bit is set to '1', if the current frame was terminated by the SCC with an abort sequence, because neither a 'frame end / block end' indication was detected in the FIFO (to complete the current frame) nor more data is available in the SCC transmit FIFO.

Note: The transmitter is stopped if this condition occurs. The XDU condition MUST be cleared by reading register ISR1, thus bit 'XDU' should not be masked via register IMR1.

#### XON XON Character Detected Interrupt

This bit is set to '1', if the currently received character matched the XON character programmed in register XON and indicates, that the transmitter is switched to 'XON' state if in-band flow control is enabled via bit 'FLON' in register CCR2H.

(async mode)



# PEB 20532 PEF 20532

#### **Register Description**

# SUEXSignalling Unit Counter Exceeded Interrupt(hdlc mode)

This bit is set to '1', if 256 correct or incorrect SU's have been received and the internal counter is reset to 0.

#### BRK Break Interrupt

This bit is set to '1', if a break condition was detected on the receive line, i.e. a low level for a time equal to (character length + parity bit + stop bit(s)) bits depending on the selected ASYNC character format.

#### BRKT Break Terminated Interrupt

This bit is set to '1', if a previously detected break condition on the receive line is terminated by a low to high transition.

#### PLLA DPLL Asynchronous Interrupt

This bit is only valid, if the receive clock is derived from the internal DPLL and FM0, FM1 or Manchester data encoding is selected (depending on the selected clock mode and data encoding mode). It is set to '1' if the DPLL has lost synchronization. Reception is disabled until synchronization has been regained again. If the transmitter is supplied with a clock derived from the DPLL, transmission is also interrupted.

#### CDSC Carrier Detect Status Change Interrupt

This bit is set to '1', if a state transition has been detected at signal CD. Because only a state transition is indicated via this interrupt, the current status can be evaluated by reading bit 'CD' in status register STARH. *Note: A receive clock must be provided to detect a transition of CD.* 

(async mode)

(all modes)

(all modes)

(async mode)

Data Sheet



Register 82	IMR0 Interrupt Masl	k Register 0			
CPU Accessibility:	read/write				
Reset Value:	FF <sub>H</sub>				
	Channel A	Channel B			
Offset Address:	54 <sub>H</sub>	A4 <sub>H</sub>			
typical usage:	written by CPU;				
	read and evaluated by SEROCC				

Bit	7	6	5	4	3	2	1	0
Mode				IM	R0			
н	RDO	RFO	PCE	RSC	RPF	RME	RFS	FLEX
Α	1	RFO	FERR	PERR	RPF	TCD	TIME	1
В	1	RFO	SCD	PERR	RPF	TCD	1	1

Regist	er 83	IMR1 Interruj	ot Mask R	egister 1					
CPU A	ccessibility	y: <b>read/</b>	write						
Reset Value: <b>FF<sub>H</sub></b>									
Channel A Channel B									
Offset	Address:	55 <sub>H</sub>	A	\5 <sub>н</sub>					
typical	usage:	writte	n by CPU	;					
		read	and evalua	ated by SE	ROCCO-	M			
Bit	7	6	5	4	3	2	1	0	
Mode			IMR1						
н	TIN	CSC	XMR	XPR	ALLS	XDU	SUEX	1	
Α	TIN	CSC	XOFF	XPR	ALLS	XON	BRK	BRKT	
В	TIN	CSC	XMR	XPR	ALLS	XDU	1	1	



Register 84	IMR2 Interrupt Masl	k Register 2			
CPU Accessibility:	read/write				
Reset Value:	03 <sub>Н</sub>				
	Channel A	Channel B			
Offset Address:	56 <sub>H</sub>	A6 <sub>H</sub>			
typical usage:	written by CPU;				
	read and eva	aluated by SEROCCO-M			

Bit	7	6	5	4	3	2	1	0
Mode				IM	R2			
н	0	0	0	0	0	0	PLLA	CDSC
Α	0	0	0	0	0	0	PLLA	CDSC
В	0	0	0	0	0	0	PLLA	CDSC



### (IM) Interrupt Mask Bits

Each SCC interrupt event can generate an interrupt signal indication via pin INT/INT. Each bit position of registers IMR0..IMR2 is a mask for the corresponding interrupt event in the interrupt status registers ISR0..ISR2. Masked interrupt events never generate an interrupt indication via pin INT/INT.

bit = '0' The corresponding interrupt event is NOT masked and will generate an interrupt indication via pin INT/INT.

bit = '1' The corresponding interrupt event is masked and will NEITHER generate an interrupt vector NOR an interrupt indication via pin INT/INT.

Moreover, masked interrupt events are:

- not displayed in the interrupt status registers ISR0..ISR2 if bit 'VIS' in register CCR0L is programmed to '0'.
- displayed in interrupt status registers ISR0..ISR2 if bit 'VIS' in register CCR0L is programmed to '1'.

# Note: After RESET, all interrupt events are masked. Undefined bits must not be cleared to '0'.

For detailed interrupt event description refer to the corresponding bit position in registers ISR0..ISR2.



Register 85	RSTA Receive Statu	s Byte		
CPU Accessibility:	read only			
Reset Value:	00 <sub>H</sub>			
	Channel A	Channel B		
Offset Address:	58 <sub>H</sub>	A8 <sub>H</sub>		
typical usage:	written by SEROCCO-M to RFIFO;			
	read from RI	FIFO and evaluated by CPU		

Bit	7	6	5	4	3	2	1	0
Mode				Receive S	tatus Byte			
н	VFR	RDO	CRCOK	RAB	HA( SU(	1:0)/ 1:0)	C/R	LA
Α	PE	FE	0	0	0	0	0	Р
В	PE	0	0	0	0	0	0	Р

The Receive Status Byte 'RSTA' contains comprehensive status information about the last received frame (HDLC/PPP) or the last received ASYNC/BISYNC character.

The SCC attaches this status byte to the receive data and thus it should be read from the RFIFO.

In HDLC/PPP modes the RSTA value can optionally be read from this register address; in ASYNC and BISYNC modes a read to this register is not specified. In extended transparent mode this status field does not apply.



VFR	Valid Frame		(hdlc modes)				
	Determines whether a valid frame has been received.						
	VFR='0'	The received frame is invalid. An invalid frame is either a frame which is a number of 8 bits (n * 8 bits) in length (e.g. 2 frame which is too short, taking into account mode selected via CCR2L (MDS1, MDS0, selected CRC algorithm (CCR1L:C32) as f	not an integer 25 bits), or a t the operation ADM) and the ollows:				
		<ul> <li>for CCR3H:DRCRC = '0' (CRC reception e</li> <li>automode / address mode 2 (16-bit addr 4 bytes (CRC-CCITT) or 6 (CRC-32)</li> <li>automode / address mode 2 (8-bit addre 3 bytes (CRC-CCITT) or 5 (CRC-32)</li> <li>address mode 1: 3 bytes (CRC-CCITT) or 5 (CRC-32)</li> <li>address mode 0: 2 bytes (CRC-CCITT) or 4 (CRC-32)</li> </ul>	nabled): ess) ss)				
		<ul> <li>for CCR3H:DRCRC = '1' (CRC reception d <ul> <li>automode / address mode 2 (16-bit address)</li> <li>automode / address mode 2 (8-bit address)</li> <li>automode / address mode 2 (8-bit address)</li> <li>address mode 1: <ul> <li>byte</li> </ul> </li> <li>address mode 0: <ul> <li>byte</li> </ul> </li> </ul></li></ul>	isabled): ress): rss):				
		Note: Shorter frames are not reported a	t all.				
	VFR='1'	The received frame is valid.					
RDO	Receive Data	a Overflow	(hdlc modes)				
	RDO='0'	No receive data overflow has occurred.					
	RDO='1'	A data overflow has occurred during recept frame. Additionally, an interrupt can be gene ISR0:RDO/IMR0:RDO).	tion of the erated (refer to				



(hdlc modes)

CRCOK **CRC Compare/Check** CRCOK='0' CRC check failed, received frame contains errors. CRCOK='1' CRC check OK; the received frame does not contain CRC errors. RAB **Receive Message Aborted** (hdlc modes) RAB='0'No abort condition was detected during reception of the frame. RAB='1' The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.

This bit is also set to '1' if the maximum receive byte count (set in registers RLCRL/RLCRH) is reached.

#### HA(1:0) **High Byte Address Compare**

(hdlc modes)

Significant only if an address mode with automatic address handling has been selected. In operating modes which provide high byte address recognition, SEROCCO-M compares the high byte of a 2-byte address with the contents of two individually programmable addresses (RAH1, RAH2) and the fixed values  $FE_{\mu}$  and  $FC_{\mu}$  (broadcast address). Dependent on the result of this comparison, the following bit combinations are possible:

HA(1:0)='10' RAH1 has been recognized.

HA(1:0)='00' RAH2 has been recognized.

HA(1:0)='01' broadcast address has been recognized.

If RAH1 and RAH2 contain identical values, a match is indicated by HA(1:0)='10'.

#### SU(1:0) SS7 Signaling Unit Type

(hdlc modes)

If Signaling System #7 support is activated (see CCR3L register, bit 'ESS7'), the bit functions are defined as follows:

SU(1:0)='00' not valid

SU(1:0)='01' Fill In Signaling Unit (FISU) detected

SU(1:0)='10' Link Status Signaling Unit (LSSU) detected

SU(1:0)='11' Message Signaling Unit (MSU) detected



(hdlc modes)

#### C/R Command/Response

Significant only if 2-byte address mode has been selected. Value of the C/R bit (bit 1 of high address byte) in the received frame. The interpretation depends on the setting of the 'CRI' bit in the RAH1 register (See "RAH1" on page 203.).

## LA Low Byte Address Compare

(hdlc modes)

Significant in automode and address mode 2 only.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two addresses (RAL1, RAL2).

- LA='0' RAL2 has been recognized.
- LA='1' RAL1 has been recognized.

According to the X.25 LAPB protocol, RAL1 is interpreted as the address of a COMMAND frame and RAL2 is interpreted as the address of a RESPONSE frame.

# P Parity

(async/bisync mode)

(async mode)

'1' This bit carries the parity bit of the last received character.

# FE Framing Error

'1' A character framing error was detected, i.e. a '0' was sampled at a bit position where a stop bit '1' was expected due to the selected character format.

#### PE Parity Error

(async/bisync mode)

'1' The calculated parity did not match the received parity bit. Optionally the interrupt PERR can be generated.



Register 86	SYNCL SYN Characte	r Register (Low Byte)	
CPU Accessibility:	read/write		
Reset Value:	00 <sub>H</sub>		
	Channel A	Channel B	
Offset Address:	5A <sub>H</sub>	AA <sub>H</sub>	
typical usage:	written by CPU;		
	read and eva	aluated by SEROCCO-M	

Bit	7	6	5	4	3	2	1	0
Mode				SYN Char	acter Low			
н	0	0	0	0	0	0	0	0
Α	0	0	0	0	0	0	0	0
В		SYNCL(7:0)						

Regist	er 87 SYNCH SYN Character Register (High Byte)							
CPU A	ccessibility	y: <b>read/</b>	write					
Reset	Value:	00 <sub>H</sub>						
		Chan	nel A C	hannel B				
Offset	Address:	5B <sub>H</sub>	Д	B <sub>H</sub>				
typical	usage:	writte	n by CPU;	;				
		read	and evalua	ated by SE	ROCCO-I	М		
Bit	7	6	5	4	3	2	1	0
Mode			SYN Character High					
н	0	0	0	0	0	0	0	0
Α	0	0	0	0	0	0	0	0
В	SYNCH(7:0)							



SYNCH(7:0)	Synchronization Character (high)	(bisync mode)
SYNCL(7:0)	Synchronization Character (low)	(bisync mode)
	This register is only valid in BISYNC protocol mode. The synchronization (SYN) character format depends on bit 'BISNC' and 'SLEN' in register CCR2L:	the setting of
	<ul> <li>MONOSYNC Mode (CCR2L.BISNC = '0') The SYN character is defined by register 'SYNCL':</li> <li>a) SLEN = '0': the 6 bit SYN character is specified by b</li> <li>b) SLEN = '1': the 8 bit SYN character is specified by b</li> </ul>	oits (50) bits (70).
<ul> <li>BISYNC Mode (CCR2L.B The SYN character is def</li> <li>a) SLEN = '0': the 12 bit each register, i.e. SYN(11</li> <li>b) SLEN = '1': the 16 bit each register, i.e. SYN(15</li> </ul>	<ul> <li>BISYNC Mode (CCR2L.BISNC = '1') The SYN character is defined by registers 'SYNCL' an a) SLEN = '0': the 12 bit SYN character is specified b each register, i.e. SYN(110) = SYNCH(5:0), SYNCL( b) SLEN = '1': the 16 bit SYN character is specified b each register, i.e. SYN(150) = SYNCH(7:0), SYNCL(</li> </ul>	nd ' <b>SYNCH</b> ': by bits (50) of 5:0) by bits (70) of 7:0).
	In transmit direction the SYN character is sent continuou has to be transmitted and interframe timefill control is ena bit 'ITF' to '1' in register CCR2H.	sly if no data bled by setting

In receive direction the receiver monitors the data stream for occurence of the specified SYN pattern if operating in 'HUNT' mode (bit 'HUNT' in register CMDRH).



# 5.2.3 Channel Specific DMA Registers

Each register description is organized in three parts:

- a head with general information about reset value, access type (read/write), channel specific offset address and usual handling;
- a table containing the bit information (name of bit positions);
- a section containing the detailed description of each bit.



1

### **Register Description**

# Register 88XBCLTransmit Byte Count (Low Byte)

CPU A Reset <sup>v</sup>	ccessibility: /alue:	read/writ 00 <sub>H</sub>	e					
		Channel	A	Channel B				
Offset Address: E typical usage: w		<b>B8<sub>н</sub></b> written by	/ CPl	D2 <sub>H</sub> J, evaluate	d by SERC	OCCO-M		
Bit	7	6	5	4	3	2	1	0

XBC(7:0)

# Register 89XBCHTransmit Byte Count (High Byte)

CPU Accessibility:	read/write		
Reset Value:	00 <sub>H</sub>		
	Channel A	Channel B	
Offset Address:	В9 <sub>н</sub>	D3 <sub>H</sub>	
typical usage:	written by CPU, evaluated by SEROCCO-M		

Bit	7	6	5	4	3	2	1	0
	XME	XF	XIF	0		XBC(	11:8)	



# XBC Transmit Byte Count

(11:0)

## Transmit Byte Count

This register is used in DMA Mode only, to program the length (1...4096 bytes) of the next frame to be transmitted. The length of the block in number of bytes is:

Length = XBC + 1

This allows the SEROCCO-M to request the correct amount of DMA cycles after an 'XF' or' XIF' command.

#### XME Transmit Message End Command

Only valid in external DMA controller mode. This bit is identical to 'XME' command bit (refer to register "CMDRL" on Page 146).

#### XF Transmit Frame Command

Only valid in external DMA controller mode. This bit is identical to 'XF' command bit (refer to register "CMDRL" on Page 146).

#### XIF Transmit I-Frame Command

Only valid in external DMA controller mode. This bit is identical to 'XIF' command bit (refer to register "CMDRL" on Page 146).



## Register 90 RMBSL Receive Maximum Buffer Size (Low Byte)

CPU A Reset \	ccessibility: /alue:	read/write 00 <sub>H</sub>							
		Channel	A Char	nnel B					
Offset /	Address: C4 <sub>H</sub>		DE <sub>H</sub>						
typical	usage:	written by	written by CPU, evaluated by SEROCCO-M						
Bit	7	6	5	4	3	2	1	0	
	Receive Maximum Buffer Size								
	RMBS(7:0)								

# Register 91RMBSHReceive Maximum Buffer Size (High Byte)

CPU A	ccessibility	y: read/	read/write					
Reset	value:	υυ <sub>Η</sub>						
Channel A			nel A C	Channel B				
Offset /	Address:	ress: C5 <sub>H</sub>		)F <sub>H</sub>				
typical	usage:	writter	n by CPU,	evaluatec	by SERC	)CCO-M		
Bit	15	14	13	12	11	10	9	8
	Receive Maximum Buffer Size							
	RE	DRMBS	0	0		RMBS	(11:8)	



#### RE Receive DMA Enable

*Only valid if external DMA controller support is enabled.* Self-clearing command bit:

- RE='0' The DMA controller is not set up to forward receive data into a buffer in memory.
- RE='1' Setting this bit to '1' enables the DMA support logic to request the external DMA controller to transfer receive data when available in RFIFO.

#### DRMBS Disable Receive Maximum Buffer Size (RMBS) Check

Only valid if external DMA controller support is enabled.

DRMBS='0' Evaluation of bit field RMBS(11:0) is enabled.

DRMBS='1' Evaluation of bit field RMBS(11:0) is disabled.

#### RMBS(11:0) Receive Maximum Buffer Size

Only valid if external DMA controller support is enabled. The size of the receive buffer in host memory can be set up in this bit field to ensure that request for DMA transfers are inhibited when the maximum buffer size is reached. An RBF interrupt is generated (if unmasked) to inform the CPU. If the external DMA controller supports this function, it can be disabled by setting bit 'DRMBS' to '1'.



## Register 92 RBCL Receive Byte Count (Low Byte)

CPU Accessibility:	read only	
Reset Value:	00 <sub>H</sub>	
	Channel A	Channel B
Offset Address:	C6 <sub>H</sub>	E0 <sub>H</sub>
typical usage:	written by SE	ROCCO-M, evaluated by CPU

Bit	7	6	5	4	3	2	1	0
				RBC	(7:0)			

# Register 93RBCHReceive Byte Count (High Byte)

CPU A	ccessibility	/: read	only							
Reset	Value:	00 <sub>H</sub>	00 <sub>н</sub>							
		Chan	nel A C	Channel B						
Offset Address:		С7 <sub>Н</sub>	E	1 <sub>H</sub>						
typical usage:		writte	written by SEROCCO-M, evaluated by CPU							
Bit	7	6	5	4	3	2	1	0		
	RBCO	0	0	0		RBC(	(11:8)			



#### **RBC(11:0)** Receive Byte Count

This bit field determines the receive byte count (1..4095) of the currently received frame/block.

#### RBCO Receive Byte Counter Overflow

*Only valid in DMA controller mode.* This bit indicates an overflow of the receive byte conter RBC(11:0), i.e. the receive frame length exceeded 4095 bytes.



# 5.2.4 Miscellaneous Registers

Register 94	VER0
	Version Register 0

CPU Accessibility:	read only
Reset Value:	83 <sub>H</sub>
Offset Address:	EC <sub>H</sub>
typical usage:	evaluated by CPU

Bit	7	6	5	4	3	2	1	0
			Mar	nufacturer C	ode			Fix '1'
				VER	(7:0)			

Register 95	VER1
_	Version Register 1

CPU Accessibility:	read only
Reset Value:	E0 <sub>H</sub>
Offset Address:	ED <sub>H</sub>
typical usage:	evaluated by CPU

Bit	7	6	5	4	3	2	1	0
		Device Code	e (bits 3 0	))		Manufact	urer Code	
				VER(	(15:8)			



## Register 96 VER2 Version Register 2

CPU Accessibility:	read only
Reset Value:	05 <sub>H</sub>
Offset Address:	EE <sub>H</sub>
typical usage:	evaluated by CPU

Bit	7	6	5	4	3	2	1	0
	Device Code (bits 11 4)							
	VER(23:16)							

# Register 97 VER3 Version Register 3

CPU Accessibility:	read only
Reset Value:	20 <sub>H</sub>
Offset Address:	EF <sub>H</sub>
typical usage:	evaluated by CPU

Bit	7	6	5	4	3	2	1	0
		Version	Number		D	evice Code	(bits 15 1	2)
				VER(	31:24)			

2000-09-14



## VER(31:0) Version Register

Identical to 32 bit boundary scan ID string.

The 32 bit string consists of the bit fields:

- VER(31:28) 2<sub>H</sub> Version Number
- VER(27:12) 005E<sub>H</sub> Device Code
- VER(11:0) 083<sub>H</sub> Manufacturer Code (LSB fixed to '1')



## 6.1 Initialization

After Reset the CPU has to write a minimum set of registers and an optional set depending on the required features and operating modes.

First, the following initialization steps must be taken:

- Select serial protocol mode (refer to Table 12 "Protocol Mode Overview" on Page 82),
- Select encoding of the serial data (refer to Chapter 3.2.13 "Data Encoding" on Page 73),
- Program the output characteristics of

   pin TxD (selected with bit 'ODS' in "Channel Configuration Register 1 (Low Byte)" on Page 155) and
   interrupt pin INT/INT (selected with bit field 'IPC(1:0)' in "Global Mode Register" on Page 122),
- Choose a clock mode (refer to Table 7 "Overview of Clock Modes" on Page 46).
- Power-up the oscillator unit (with or without shaper) by re-setting bit GMODE:OSCPD to '0', if appropriate (GMODE:DSHP='0' enables the shaper).

The clock mode must be set before power-up (CCR0H.PU). The CPU may switch the SEROCCO-M between power-up and power-down mode. This has no influence upon the contents of the registers, i.e. the internal state remains stored. In power-down mode however, all internal clocks are disabled, no interrupts from the corresponding channel are forwarded to the CPU. This state can be used as a standby mode, when the channel is (temporarily) not used, thus substantially reducing power consumption.

The SEROCCO-M should usually be initialized in Power-Down mode.

The need for programming further registers depends on the selected features (serial mode, clock mode specific features, operating mode, address mode, user demands).

# 6.2 Interrupt Mode

# 6.2.1 Data Transmission (Interrupt Driven)

In transmit direction  $2 \times 32$  byte FIFO buffers (transmit pools) are provided for each channel. After checking the XFIFO status by polling the Transmit FIFO Write Enable bit (bit 'XFW' in STARL register) or after a Transmit Pool Ready ('XPR') interrupt, up to 32 bytes may be entered by the CPU into the XFIFO.



### HDLC/SDLC/PPP

The transmission of a packet can be started by issuing an 'XF' or 'XIF' command via the CMDRL register. If enabled, a specified number of preambles (refer to registers CCR2H and PREAMB) are sent out optionally before transmission of the current packet starts.

If the transmit command does not include an end of message indication (CMDRL.XME), SEROCCO-M will repeatedly request for the next data block by means of an 'XPR' interrupt as soon as no more than 32 bytes are stored in the XFIFO, i.e. a 32-byte pool is accessible to the CPU.

This process will be repeated until the CPU indicates the end of message per 'XME' command, after which packet transmission is finished correctly by appending the CRC and closing flag sequence. Consecutive packets may be transmitted as back-to-back packets and may even share a flag (enabled via CCR1L.SFLG), if service of XFIFO is quick enough.

In case no more data is available in the XFIFO prior to the arrival of the end-of-message indiction ('XME'), the transmission of the packet is terminated with an abort sequence and the CPU is notified per interrupt (ISR1.XDU, transmit data underrun). The packet may also be aborted per software at any time (CMDRL.XRES).

The data transmission sequence, from the CPU's point of view, is outlined in Figure 56.

#### ASYNC

The transmission of character(s) can be started by issuing a 'XF' command via the CMDRL register. SEROCCO-M will repeatedly request for the next data block by means of an 'XPR' interrupt as soon as no more than 32 bytes are stored in the XFIFO, i.e. a 32-byte pool is accessible to the CPU. Transmission may be aborted per software (CMDRL.XRES).

#### BISYNC

The transmission of a block can be started by issuing an 'XF' command via the CMDRL register. Further handling of data transmission with respect to preamble transmission and command 'XME' is similar to HDLC/SDLC mode. After 'XME' command has been issued, the block is finished by appending the internally generated CRC if enabled (refer to description of register CCR2H).

In case no more data is available in the XFIFO prior to the arrival of 'XME', the transmission of the block is terminated with IDLE and the CPU is notified per interrupt (ISR1.XDU). The block may also be aborted per software (CMDRL.XRES). The data transmission flow, from the CPU's point of view, is outlined in **Figure 56**.





Figure 56Interrupt Driven Data Transmission (Flow Diagram)

# 6.2.2 Data Reception (Interrupt Driven)

Also  $2 \times 32$  byte FIFO buffers (receive pools) are provided for each channel in receive direction.

There are different interrupt indications concerned with the reception of data:

# HDLC/SDLC/PPP

- 'RPF' (Receive Pool Full) interrupt, indicating that a specified number of bytes (limited with the receive FIFO threshold in register CCR3H, bit field 'RFTH(1..0)'; default is 32 bytes) can be read from RFIFO and the received message is not yet complete.
- 'RME' (Receive Message End) interrupt, indicating that the reception of one message is completed, i.e. either

- one message which fits into RFIFO not exceeding the receive FIFO threshold, or

- the last part of a message, all in all exceeding the receive FIFO threshold is stored in the RFIFO.

In addition to the message end ('RME') interrupt the following information about the received packet is stored by SEROCCO-M in special registers and/or RFIFO:



Status Information	Location
Length of received message	registers RBCH, RBCL
CRC result (good/bad)	RSTA register (or last byte of received data)
Valid frame (yes/no)	RSTA register (or last byte of received data)
ABORT sequence recognized (yes/no)	RSTA register (or last byte of received data)
Data overflow (yes/no)	RSTA register (or last byte of received data)
Results from address comparison (with automatic address handling)	RSTA register (or last byte of received data)
Type of frame (COMMAND/RESPONSE) (with automatic address handling)	RSTA register (or last byte of received data)
Type of Signaling Unit (in SS7 mode)	RSTA register (or last byte of received data)

#### Table 16 Status Information after RME interupt

#### ASYNC, BISYNC

- 'RPF' (Receive Pool Full) interrupt, indicating that a specified number of bytes (refer to register CCR3H, bit field 'RFTH(1..0)') can be read from RFIFO.
- 'TCD' (Termination Character Detected) interrupt, indicating that reception has been terminated by reception of a specified character (refer to register TCR and bit CCR3L.TCDE).

Additionally, the CPU can have access to contents of RFIFO without having received an interrupt (and thereby causing 'TCD' to occur) by issuing the RFIFO Read command (CMDRH.RFRD).

In addition to every received character the assigned status information Parity bit (0/1), Parity Error (yes/no), Framing Error (yes/no, ASYNC only!) is optionally stored in RFIFO.

With an end condition ('TCD' interrupt or after 'RFRD' command) the length of the last received data block is stored in register RBCL. The number of bytes to read from RFIFO is determined by the 1, 2, 4 or 5 least significant bits of register RBCL, depending on the selected RFIFO threshold (bit field 'RFTH(1..0)' in register CCR3H).

Note: (For all serial modes) After the received data has been read from the RFIFO, this must be explicitly acknowledged by the CPU issuing an 'RMC' (Receive Message Complete) command. The CPU has to handle the 'RPF' interrupt before the complete 2 x 32-byte FIFO is filled up with receive data which would cause a "Receive Data Overflow" condition.

The data reception sequence, from the CPU's point of view, is outlined in Figure 57.





1) A receive threshold of 32 bytes is the default for HDLC/PPP mode. It can be programmed with bit field RFTH(1:0) in register CCR3H.

2) The number of bytes stored in RFIFO can be determined by evaluating the lower bits in register RBCL (depending on the selected receive threshold RFTH(1:0)).

249

#### Figure 57 Interrupt Driven Data Reception (Flow Diagram)



# 6.3 External DMA Supported Mode

The following table provides a definition of terms used in this chapter to describe the operation with external DMA controller support.

	5,	
Packet	A "Packet" is a connected block of data bytes. This can be an HDLC/PPP frame as well as a number of ASYNC/ BISYNC characters up to a specific limit (received termination character, CMDRH:RFRD command). If a receive status byte (RSTA) is attached to data bytes, it is also considered as part of the packet.	
Buffer	A "Buffer" is a limited space in memory that is reserved for DMA reception/transmission. SEROCCO-M can optionally keep track of predefined (receive) buffer limits and notify the CPU with an appropriate interrupt if this functionality is not provided by the external DMA controller. A packet can go into one single buffer, or it can go fragmented into multiple buffers.	
Block	A "Block" is the amount of data that is transfered from the memory to the XFIFO (transmit DMA transfer) or from the RFIFO to the memory. In HDLC/PPP modes the block size is 32 bytes by default. It can be lowered with the receive FIFO threshold in register CCR3H, bit field 'RFTH(10)'.	
Bus Cycle	A "Bus Cycle" corresponds to a single byte/word transfer. Multiple bus cycles make up a block transfer.	
DMA Transfer	A "DMA Transfer" is the movement of complete buffers and/or packets between the XFIFO/RFIFO and the memory by the external DMA controller.	

### Table 17DMA Terminology

# 6.3.1 Data Transmission (With External DMA Support)

Any packet transmission is prepared by initializing the external DMA controller with the transmit buffer start address and writing the packet size in number of bytes to registers XBCL/XBCH.

Now there are two possible scenarios:

If the prepared transmit buffer in memory contains a complete packet, the start command for DMA transmission is issued by setting bits 'XF' and 'XME' in register XBCH to '1'. The DMA support logic will request the external DMA controller to transfer data into the XFIFO. After the last byte has been transmitted, the protocol machine appends the trailer (e.g. CRC and Flag in HDLC), if applicable. The Transmit DMA Transfer End (TDTE) interrupt is generated (refer to Figure 58).



 If a transmit packet is distributed over more than one transmit buffer in memory, the 'XF' command (without setting the 'XME' bit) forces SEROCCO-M to request data transfers from the external DMA controller from this buffer. A Transmit DMA Transfer End (TDTE) interrupt is generated whenever a block of <XBC> bytes is completely transferred. For the last buffer, containing the end of the transmit packet, the 'XF' command is issued together with bit 'XME' set (refer to Figure 59).

After transmission is complete, the optional generation of the ALLS interrupt indicates that all transmit data has been sent on pin TxD.

Note: In HDLC Automode, the 'XF' command may be replaced by the 'XIF' command in the same register, when transmission of an I-frame is desired.



Figure 58 DMA Transmit (Single Buffer per Packet)





Figure 59 Fragmented DMA Transmission (Multiple Buffers per Packet)


# 6.3.2 Data Reception (With External DMA Support)

The receive DMA support logic is able to limit its requesting for data transfers to a byte count programmed in register RMBSL/RMBSH. If the external DMA controller is capable of handling maximum receive buffer sizes itself, this feature can be disabled by setting bit RMBSH:DRMBS to '1'.

If a new packet is received by the SCC, the DMA support logic will request the external DMA controller to move receive data out of the RFIFO.

Now there are two possible scenarios:

- If the maximum buffer size programmed in register RMBSL/RMBSH has been transferred (only if RMBSH:DRMBS = '0'), SEROCCO-M stops requesting for data transfers and a Receive Buffer Full (RBF) interrupt is generated. The CPU now updates the receive buffer base address in the external DMA controller and releases the receive DMA control logic by setting the 'RE' bit in register RMBSH. Optionally the maximum buffer size value can be updated with the same register write access.
- If the end of a received packet/block is part of the curent DMA transfer, SEROCCO-M generates a Receive DMA Transfer End (RDTE) interrupt and stops operation. The CPU now reads the received byte count from registers RBCL/RBCH. The receive DMA support logic will not continue requesting for data transfer until it is set up again with the 'RE' command in register RMBSH.

If in packet oriented protocol modes (HDLC, PPP) the maximum receive buffer size RMBS is chosen to be larger than the expected receive packets, each buffer will contain the whole packet (see **Figure 60**). In this case (or if RMBSH:DRMBS = '1') a Receive Buffer Full (RBF) interrupt will never occur, simplifying the software. To ensure that no packets exceeding the maximum buffer size are forwarded from the SCC to the RFIFO, the receive packet length should be limited with registers RLCRL/RLCRH.





## Figure 60 DMA Receive (Single Buffer per Packet)

**Figure 61** shows an example for fragmented reception of a packet larger than the prepared receive buffers in memory. In this case the length of the received packet is 199 bytes, each of the buffers in host memory is 128 bytes deep:





## Figure 61 Fragmented Reception per DMA (Example)

After the external DMA controller is initialized with the base address of receive buffer #1 and the maximum buffer size RMBS is written to SEROCCO-M, simultaneously activated with the 'RE' command, requesting of DMA transfer from the RFIFO to the receive buffer takes place in blocks of 32 bytes (unless changed with bit field 'RFTH' in register CCR3H).

After four 32-byte-blocks have been transferred, the first receive buffer is filled up completely with receive data. The SEROCCO-M indicates this by generating the RBF interrupt.

Now the CPU has to provide the base address of the second receive buffer to the external DMA controller and issue the 'RE' command to SEROCCO-M again. This allows the external DMA controller to continue data transfers into the second receive buffer. After another two 32-byte-blocks have been transferred, the DMA request for the remaining 7 bytes (including the RSTA byte) is generated to the external DMA controller, follwed by the generation of the RDTE interrupt. Now the DMA transfer is completed and software has to read the number of received bytes from the Receive Byte Count registers RBCL/RBCH.

The following figure (Figure 62) gives the sequence of actions from both, the SEROCCO-M and the CPU for this example (fragmented reception of 199 bytes into two receive buffers):





Figure 62 Fragmented Reception Sequence (Example)



# 7 Electrical Characteristics

## 7.1 Absolute Maximum Ratings

Parameter		Symbol	Limit Values	Unit
Ambient temperature under bias	PEB PEF	$T_{A}$ $T_{A}$	0 to 70 - 40 to 85	°C ℃
Storage temperature		T <sub>stg</sub>	– 65 to 125	°C
IC supply voltage		$V_{DD3}$	- 0.3 to 3.6	V
Voltage on any signal pin with resp ground	V <sub>S</sub>	– 0.4 to 5.5	V	
ESD robustness <sup>1)</sup> HBM: 1.5 kΩ, 100 pF		$V_{\text{ESD,HBM}}$	2000	V

<sup>1)</sup> According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

# Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 7.2 Operating Range

Parameter	Symbol	Limit Values		Unit	<b>Test Condition</b>	
		min.	max.			
Ambient temperature PEB PEF	$T_{A}$ $T_{A}$	0 -40	70 85	°C ℃		
Junction temperature		0	125	°C		
Supply voltage	$V_{\rm DD3}$	3.0	3.6	V		
Ground	V <sub>SS</sub>	0	0	V		

Note: In the operating range, the functions given in the circuit description are fulfilled.



# 7.3 DC Characteristics

Parameter		Symbol	Limit Values		Unit	Notes	
			min.	max.			
Input low v	oltage	$V_{IL}$	- 0.4	0.8	V		
Input high v	voltage	V <sub>IH</sub>	2.0 2.1	5.5 5.5	V V	$V_{\rm DD} = 3.3 \text{ V}$ $V_{\rm DD} = 3.6 \text{ V}$	
Output low	voltage	V <sub>OL</sub>		0.45	V	$I_{OL} = 7 \text{ mA}^{-1}$ $I_{OL} = 2 \text{ mA}^{-2}$	
Output high	n voltage	V <sub>OH</sub>	2.4		V	I <sub>OH</sub> = − 1.0 mA	
Power supply current	operational (average)	I <sub>CC</sub> (AV)		50	mA	$\begin{split} V_{\rm DD} &= 3.3 \ {\rm V}, \\ T_{\rm A} &= 25 \ {\rm ^{\circ}C}, \\ {\rm CLK} &= 33 \ {\rm MHz}, \\ {\rm XTAL} &= 20 \ {\rm MHz}, \\ {\rm inputs} \ {\rm at} \ {\rm V}_{\rm SS}/{\rm V}_{\rm DD}, \\ {\rm no} \ {\rm output} \ {\rm loads} \end{split}$	
	power down (no clocks)	$I_{\rm CC}$ (PD)		0.01	mA	$V_{\rm DD}$ = 3.3 V, $T_{\rm A}$ = 25 °C	
Power dissipation		P		150	mW	$\begin{split} V_{\rm DD} &= 3.3 \ {\rm V}, \\ T_{\rm A} &= 25 \ {\rm ^{\circ}C}, \\ {\rm CLK} &= 33 \ {\rm MHz}, \\ {\rm XTAL} &= 20 \ {\rm MHz}, \\ {\rm inputs} \ {\rm at} \ {\rm V}_{\rm SS}/{\rm V}_{\rm DD}, \\ {\rm no} \ {\rm output} \ {\rm loads} \end{split}$	
Input leakage current		I <sub>LI</sub>		1	μΑ	$V_{\text{DD}}$ = 3.3 V, GND = 0 V; inputs at V <sub>SS</sub> /V <sub>DD</sub> , no output loads	
Output leakage current		I <sub>LO</sub>		1	μΑ	$V_{DD} = 3.3 \text{ V},$ GND = 0 V; $V_{OUT} = 0 \text{ V},$ $V_{DDP} + 0.4$	

<sup>1)</sup> Apply to the next pins: TxDA, TxDB.

<sup>2)</sup> Apply to all the I/O and O pins that do not appear in the list in note <sup>1)</sup>, except XTAL2.

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25$  °C and the given supply voltage.



# 7.4 AC Characteristics

#### **Interface Pins**

 $T_{\rm A}$  = 0 to + 70 °C;  $V_{\rm DD3}$  = 3.3 V ± 0.3 V

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and at 0.8 V for a logical "0".

The AC testing input/output waveforms are shown below.



Figure 60 Input/Output Waveform for AC Tests

# 7.5 Capacitances

#### Interface Pins

## Table 18Capacitances

 $T_{\rm A}$  = 25 °C;  $V_{\rm DD3}$  = 3.3 V ± 0.3 V,  $V_{\rm SS}$  = 0 V

Parameter	Symbol	Symbol Limit Values		Unit	<b>Test Condition</b>
		min.	max.		
Input capacitance	C <sub>IN</sub>		5	pF	
Output capacitance	C <sub>OUT</sub>		10	pF	
I/O-capacitance	C <sub>IO</sub>		15	pF	



# 7.6 Thermal Package Characteristics

Parameter	Symbol	Value	Unit	
Thermal Package Resista				
Airflow:	Ambient Temperature:			
without airflow	T <sub>A</sub> =-40°C	θ <sub>JA(0,-40)</sub>	45.7	K/W
without airflow	T <sub>A</sub> =+25°C	θ <sub>JA(0,25)</sub>	41.5	K/W
airflow 1 m/s (~200 lfpm)	T <sub>A</sub> =+25°C	θ <sub>JA(1,25)</sub>	39.6	K/W
airflow 2 m/s (~400 lfpm)	T <sub>A</sub> =+25°C	θ <sub>JA(2,25)</sub>	38.8	K/W
airflow 3 m/s (~600 lfpm)	T <sub>A</sub> =+25°C	θ <sub>JA(3,25)</sub>	38.4	K/W

# Table 19 Thermal Package Characteristics P-TQFP-100-3



7.7 Timing Diagrams

# 7.7.1 Microprocessor Interface Timing

## 7.7.1.1 Microprocessor Interface Clock Timing



## Figure 61 Microprocessor Interface Clock Timing

## Table 20 Microprocessor Interface Clock Timing

No.	Parameter	Lim	Unit	
		min.	max.	
1	CLK clock period	30	$\infty^{1)}$	ns
	CLK frequency	0	33	MHz
2	CLK high time	11	8	ns
3	CLK low time	11	x	ns

<sup>1)</sup> A clock supply is needed for read access to the on-chip interrupt status registers (ISR, DISR) and for general purpose port (GPP) operation.





## 7.7.1.2 Infineon/Intel Bus Interface Timing





Figure 63 Infineon/Intel Write Cycle Timing





## Figure 64 Infineon/Intel DMA Read Cycle Timing



## Figure 65 Infineon/Intel DMA Write Cycle Timing



## Figure 66 Infineon/Intel Multiplexed Address Timing



## Table 21 Infineon/Intel Bus Interface Timing

No.	Parameter		Limit Values		
		min.	max.		
4	active address to active $\overline{RD}/\overline{WR}$ setup time	8		ns	
5	inactive RD/WR to inactive address hold time	0		ns	
6	active $\overline{CS}$ to active $\overline{RD}/\overline{WR}$ setup time	2		ns	
7	inactive $\overline{RD}/\overline{WR}$ to inactive $\overline{CS}$ hold time	0		ns	
8	RD active pulse width	30 <sup>1)</sup>		ns	
9	WR active pulse width	30		ns	
10	active $\overline{RD}$ to valid data delay		20	ns	
11	inactive $\overline{RD}$ to invalid data hold time	5		ns	
11a	inactive $\overline{RD}$ to data high impedance delay		25	ns	
12	valid data to inactive WR setup time	6		ns	
13	inactive $\overline{WR}$ to invalid data hold time	5		ns	
14	active $\overline{RD}/\overline{WR}$ to active $\overline{READY}$ delay		20	ns	
14a	active $\overline{CS}$ to driven $\overline{READY}$ delay		20	ns	
15	inactive $\overline{RD}/\overline{WR}$ to inactive $\overline{READY}$ delay		15	ns	
15a	inactive $\overline{CS}$ to $\overline{READY}$ high impedance delay		15	ns	
16	inactive $\overline{RD}$ to inactive INT/ $\overline{INT}$ delay		1	T <sub>CLK</sub> <sup>2)</sup>	
17	RD/WR inactive pulse width	30		ns	
18	active $\overline{RD}$ to inactive DRR delay	22		ns	
19	active $\overline{WR}$ to inactive DRT delay	22		ns	
20	active address to inactive ALE setup time	5		ns	
21	inactive ALE to inactive address hold time	5		ns	
22	ALE pulse width	30		ns	
23	inactive ALE to active $\overline{RD}/\overline{WR}$ setup time	0		ns	

<sup>1)</sup> At least one rising CLK edge must appear during read pulse active for interrupt status register (ISR, DISR) read.

 $^{\rm 2)}~~T_{\rm CLK}$  is the system clock (CLK) period.





## 7.7.1.3 Motorola Bus Interface Timing

Figure 67 Motorola Read Cycle Timing



Figure 68 Motorola Write Cycle Timing





Figure 69 Motorola DMA Read Cycle Timing



#### Figure 70 Motorola DMA Write Cycle Timing

#### Table 22 Motorola Bus Interface Timing

No.	Parameter	Lin	Unit	
		min.	max.	
40	active address to active DS setup time	0		ns
41	inactive $\overline{\text{DS}}$ to inactive address hold time	0		ns
42	active CS to active DS setup time	0		ns
43	inactive $\overline{\text{DS}}$ to inactive $\overline{\text{CS}}$ hold time	0		ns
44	active $R/\overline{W}$ to active $\overline{DS}$ setup time	0		ns
45	inactive $\overline{\text{DS}}$ to inactive R/W hold time	0		ns
46	DS active pulse width (read access)	30 <sup>1)</sup>		ns



No.	Parameter	Lin	Unit	
		min.	max.	
47	DS active pulse width (write access)	30		ns
48	active $\overline{\text{DS}}$ (read) to valid data delay		20	ns
49	inactive $\overline{\text{DS}}$ (read) to invalid data hold time	5		ns
49a	inactive $\overline{\text{DS}}$ (read) to data high impedance delay		20	ns
50	valid data to inactive DS (write) setup time	10		ns
51	inactive $\overline{\text{DS}}$ (write) to invalid data hold time	10		ns
52	active DS to active DTACK delay		20	ns
52a	active CS to driving DTACK delay		20	ns
53	inactive DS to inactive DTACK delay		15	ns
53a	inactive CS to DTACK high impedance delay		15	ns
54	inactive $\overline{\text{DS}}$ (read) to inactive INT/ $\overline{\text{INT}}$ delay		1	T <sub>CLK</sub>
55	DS inactive pulse width	30		ns
56	active $\overline{\text{DS}}$ (read) to inactive DRR delay	22		ns
57	active $\overline{\text{DS}}$ (write) to inactive DRT delay	22		ns

## Table 22 Motorola Bus Interface Timing (cont'd)

<sup>1)</sup> At least one rising CLK edge must appear during read data strobe active for interrupt status register (ISR, DISR) read.



# 7.7.2 PCM Serial Interface Timing

# 7.7.2.1 Clock Input Timing



## Figure 71 Clock Input Timing

## Table 23Clock Input Timing

No.	Parameter	Lin	Unit	
		min.	max.	
81	RxCLK clock period	62	$\infty$	ns
82	RxCLK high time	25	$\infty$	ns
83	RxCLK low time	25	$\infty$	ns
84	TxCLK clock period	62	$\infty$	ns
85	TxCLK high time	25	$\infty$	ns
86	TxCLK low time	25	$\infty$	ns
87	XTAL1 clock period (internal oscillator used)	25	100	ns
	XTAL1 clock period (TTL clock signal supplied)	25	$\infty$	ns
88	XTAL1 high time (internal oscillator used)	12	46	ns
	XTAL1 high time (TTL clock signal supplied)	12	$\infty$	ns
89	XTAL1 low time (internal oscillator used)	12	46	ns
	XTAL1 low time (TTL clock signal supplied)	12	$\infty$	ns



# 7.7.2.2 Receive Cycle Timing



## Figure 72 Receive Cycle Timing

## Table 24 Receive Cycle Timing

No.	Parameter		Lim	Limit Values		
			min.	max.		
Receive data rates		externally clocked (HDLC)	0	16	Mbit/s	
		internally clocked (DPLL modes)	0	2	Mbit/s	
		internally clocked (non DPLL modes)	0	16	Mbit/s	
90	Clock period	externally clocked	62	$\infty$	ns	
		internally clocked (DPLL modes)	480	x	ns	
		internally clocked (non DPLL modes)	62	x	ns	
91	RxD to RxCLK setup time		5		ns	
92	RxD to RxCLK hold time		5		ns	



## Table 24 Receive Cycle Timing (cont'd)

No.	Parameter	Limit	Limit Values		
		min.	max.		
93	CD to RxCLK rising edge setup time	5		ns	
94	CD to RxCLK falling edge hold time	5		ns	

# 7.7.2.3 Transmit Cycle Timing



(No edge relation can be measured if the internal transmit clock is derived from the external clock source by division stages (BRG, BCR) or DPLL)

- (2) NRZ, NRZI and Manchester data encoding
- (3) FM0 and FM1 data encoding
- (4) If TxCLK output feature is enabled (only in some clock modes)
- (5) The timing is valid for non bus configuration modes and bus configuration mode 1. In bus configuration mode 2, TxD and RTS are right shifted for 0.5 TxCLK periods i.e. driven by the falling TxCLK edge.

## Figure 73 Transmit Cycle Timing



No.	Parameter	Parameter		Limit Values	
			min.	max.	
Transmit ex data rates int (D int (no		externally clocked	0	16	Mbit/s
		internally clocked (DPLL modes)	0	2	Mbit/s
		internally clocked (non DPLL modes)	0	16	Mbit/s
100	Clock	externally clocked	62	$\infty$	ns
	period	internally clocked (DPLL modes)	480	x	ns
		internally clocked (non DPLL modes)	62	$\infty$	ns
101	TxD to TxCLK	TxD to TxCLK delay (NRZ, NRZI encoding)		25	ns
102	TxD to TxCLK delay (FM0, FM1, Manchester encoding)			25	ns
103	TxD to TxCLK	(out) delay (output function enabled)	10	25	ns
104	CxD to TxCLK setup time		5		ns
	CTS to TxCL	K setup time	5		ns
105	CxD to TxCL	K hold time	5		ns
	CTS to TxCL	K hold time	5		ns
106	RTS to TxCL	K delay (not bus configuration mode)		20	ns
	RTS to TxCL	K delay (bus configuration mode)		20	ns

## Table 25Transmit Cycle Timing





# 7.7.2.4 Clock Mode 1 Strobe Timing

## Figure 74 Clock Mode 1 Strobe Timing

## Table 26 Clock Mode 1 Strobe Timing

No.	Parameter	Lin	nit Values	Unit	
		min.	max.		
110	Receive strobe to RxCLK setup	5		ns	
111	Receive strobe to RxCLK hold	5		ns	
112	Transmit strobe to RxCLK setup	5		ns	
113	Transmit strobe to RxCLK hold	5		ns	
114	TxD to RxCLK delay	10	25	ns	
115	TxD to RxCLK high impedance delay	10	25	ns	



# 7.7.2.5 Clock Mode 4 Gating Timing







## Figure 76 Clock Mode 4 Transmit Gating Timing

#### Table 27 Clock Mode 4 Gating Timing

No.	Parameter	Lin	Limit Values	
		min.	max.	
140	RCG setup time	5		ns
141	RCG hold time	5		ns
142	RxD setup time	5		ns
143	RxD hold time	5		ns
145	TCG setup time	0		ns
146	TCG hold time	6		ns
147	TxCLK to TxD delay <sup>1)</sup>	10	25	ns

<sup>1)</sup> Note that the TxD output is delayed for one additional clock with respect to the gating signal  $\overline{TCG}$ !





## 7.7.2.6 Clock Mode 5 Frame Synchronisation Timing

# Figure 77 Clock Mode 5 Frame Synchronisation Timing

#### Table 28 Clock Mode 5 Frame Synchronisation Timing

No.	Parameter	Lin	nit Values	Unit
		min.	max.	
130	Sync pulse to RxCLK setup time	10		ns
131	Sync pulse to RxCLK hold time	0		ns
132	TxCLKout to RxCLK delay (time slot monitor)	10	27	ns



# 7.7.3 Reset Timing



## Figure 78 Reset Timing

## Table 29Reset Timing

No.	Parameter	Limit Values		Unit	
		min.	max.		
150	RESET pulse width	500		ns	
151	Number of CLK cycles after RESET inactive	2		CLK cycles	

Note: RESET may be asserted and deasserted asynchronous to CLK at any time.



# 7.7.4 JTAG-Boundary Scan Timing





## Table 30JTAG-Boundary Scan Timing

No.	Parameter	Lim	it Values	Unit
		min.	max.	
160	TCK period	166	x	ns
161	TCK high time	80		ns
162	TCK low time	80		ns
163	TMS setup time	30		ns
164	TMS hold time	10		ns
165	TDI setup time	30		ns
166	TDI hold time	20		ns
167	TDO valid delay		60	ns



# 8 Test Modes

# 8.1 JTAG Boundary Scan Interface

In the SEROCCO-M a Test Access Port (TAP) controller is implemented. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard: IEEE 1149.1. Figure 83 gives an overview about the TAP controller.



If no boundary scan operation is planned TRST has to be connected with  $V_{SS}$ . TMS, TCK and TDI do not need to be connected since pull-up transistors ensure high input levels in this case. Nevertheless it would be a good practice to put these unused inputs to defined levels, using pull-up resistors.

Test handling (boundary scan operation) is performed via the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output) when the TAP controller is not in its reset state, i.e. TRST is connected to  $V_{DD}$  or it remains unconnected due to its internal pull-up. Test data at TDI are loaded with a 4-MHz clock



signal connected to TCK. '1' or '0' on TMS causes a transition from one controller state to another; constant '1' on TMS leads to normal operation of the chip.

Seq. No.	Pin	I/O	Number of Boundary Scan Cells	Constant Value In, Out, Enable
	TDI ->		1	-
1	CTSB	I	1	0
2	CTSA	I	1	0
3	CDA	I	1	1
4	RxDA	I	1	0
5	RxCLKA	I	1	0
6	TxDA		2	00
7	TxCLKA		3	000
8	RTSA	0	1	0
9	RESET	I	1	0
10	ĪNT	0	2	01
11	GP10	I/O	3	011
12	GP9	I/O	3	110
13	GP8	I/O	3	000
14	internal	I/O	3	010
15	GP6	I/O	3	000
16	internal	I/O	3	001
17	internal	I/O	3	100
18	internal	I/O	3	000
19	A7	I/O	3	000
20	A6	I/O	3	000
21	A5	I/O	3	000
22	A4	I/O	3	000
23	A3	I/O	3	000
24	A2	I/O	3	000
25	A1	I/O	3	000
26	A0	I/O	3	000

 Table 31
 Boundary Scan Sequence of SEROCCO-M



**Test Modes** 

Seq. No.	Pin	I/O	Number of Boundary Scan Cells	Constant Value In, Out, Enable
27	BM/ALE	I	1	0
28	CS	I	1	0
29	BHE	I/O	3	000
30	W/R	I/O	3	000
31	internal	0	2	00
32	internal	0	2	00
33	internal	0	2	00
34	internal	0	2	00
35	internal	0	2	00
36	internal	0	2	00
37	internal	0	2	00
38	internal	0	2	00
39	RD	I/O	3	000
40	WR	I/O	3	000
41	READY	I/O	3	000
42	CLK	I	1	0
43	D0	I/O	2	00
44	D1	I/O	2	00
45	D2	I/O	2	00
46	D3	I/O	2	00
47	D4	I/O	2	00
48	D5	I/O	2	00
49	D6	I/O	2	00
50	D7	I/O	3	000
51	D8	I/O	2	00
52	D9	I/O	2	00
53	D10	I/O	2	00
54	D11	I/O	2	00
55	D12	I/O	2	00
56	D13	I/O	2	00

## Table 31 Boundary Scan Sequence of SEROCCO-M



Seq. No.	Pin	I/O	Number of Boundary Scan Cells	Constant Value In, Out, Enable
57	D14	I/O	2	00
58	D15	I/O	3	000
59	DRTA	I/O	3	000
60	DACKA	I	1	0
61	DRRA	I/O	3	000
62	DRRB	I/O	3	000
63	DRTB	I/O	3	000
64	DACKB	I/O	3	000
65	RTSB	0	1	0
66	RxDB	I	1	0
67	RxCLKB	I	1	0
68	TxDB	0	2	00
69	TxCLKB	I/O	3	000
70	CDB	I	1	0
71	ADS	0	2	00

#### Table 31 Boundary Scan Sequence of SEROCCO-M

-> TDO

An input pin (I) uses one boundary scan cell (data in), an output pin (O) uses two cells (data out, enable) and an I/O-pin (I/O) uses three cells (data in, data out, enable). Note that some functional output and input pins of SEROCCO-M are tested as I/O pins in boundary scan, hence using three cells. The boundary scan unit of SEROCCO-M contains a total of n = 158 scan cells.

The right column of **Table 31** gives the initialization values of the cells.

The desired test mode is selected by serially loading a 3-bit instruction code into the instruction register via TDI (LSB first); see **Table 32**.



**Test Modes** 

Instruction (Bit 2 0)	Test Mode			
000	EXTEST (external testing)			
001	INTEST (internal testing)			
010	SAMPLE/PRELOAD (snap-shot testing)			
011	IDCODE (reading ID code)			
111	BYPASS (bypass operation)			
others	handled like BYPASS			

#### Table 32Boundary Scan Test Modes

**EXTEST** is used to examine the interconnection of the devices on the board. In this test mode at first all input pins **capture** the current level on the corresponding external interconnection line, whereas all output pins are held at constant values ('0' or '1', according to **Table 31**). Then the contents of the boundary scan is **shifted** to TDO. At the same time the next scan vector is loaded from TDI. Subsequently all output pins are **updated** according to the new boundary scan contents and all input pins again capture the current external level afterwards, and so on.

**INTEST** supports internal testing of the chip, i.e. the output pins **capture** the current level on the corresponding internal line whereas all input pins are held on constant values ('0' or '1', according to **Table 31**). The resulting boundary scan vector is **shifted** to TDO. The next test vector is serially loaded via TDI. Then all input pins are **updated** for the following test cycle.

Note: In capture IR-state the code '001' is automatically loaded into the instruction register, i.e. if INTEST is wanted the shift IR-state does not need to be passed.

**SAMPLE/PRELOAD** is a test mode which provides a snap-shot of pin levels during normal operation.

**IDCODE**: A 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to '1'.

TDI -> 0	010	0000 0000 0101 1110	0000 1000 001	1	-> TDO
----------	-----	---------------------	---------------	---	--------

Note: Since in test logic reset state the code '011' is automatically loaded into the instruction register, the ID code can easily be read out in shift DR state which is reached by TMS = 0, 1, 0, 0.

**BYPASS**: A bit entering TDI is shifted to TDO after one TCK clock cycle.



#### **Package Outlines**

# 9 Package Outlines



#### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm