

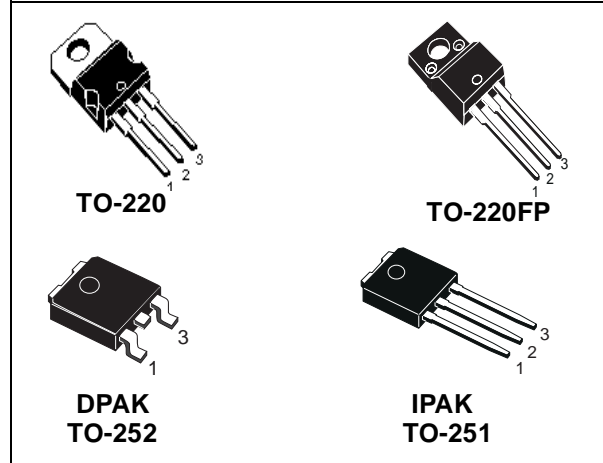


STP8NM60, STP8NM60FP STD5NM60, STD5NM60-1

N-CHANNEL 600V - 0.9Ω - 8A TO-220/TO-220FP/DPAK/IPAK
MDmesh™ Power MOSFET

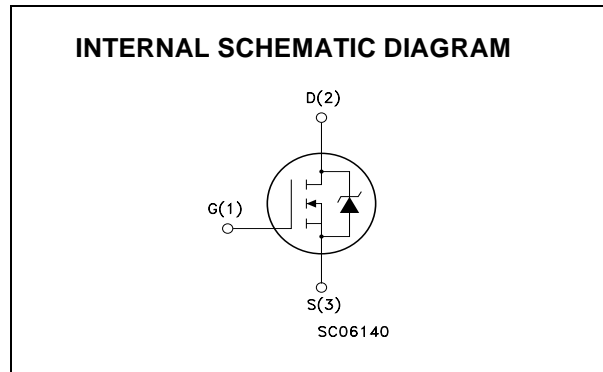
TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP8NM60	600 V	< 1 Ω	8 A	100 W
STP8NM60FP	600 V	< 1 Ω	8 A(*)	30 W
STD5NM60	600 V	< 1 Ω	5 A	96 W
STD5NM60-1	600 V	< 1 Ω	5 A	96 W

- TYPICAL R_{DS(on)} = 0.9Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE



DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.



APPLICATIONS

The MDmesh™ family is very suitable for increase the power density of high voltage converters allowing system miniaturization and higher efficiencies.

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP8NM60	P8NM60	TO-220	TUBE
STP8NM60FP	P8NM60FP	TO-220FP	TUBE
STD5NM60T4	D5NM60	DPAK	TAPE & REEL
STD5NM60-1	D5NM60	IPAK	TUBE

STP8NM60, STP8NM60FP, STD5NM60, STD5NM60-1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		STP8NM60	STP8NM60FP	STD5NM60 STD5NM60-1	
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	600			V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	600			V
V_{GS}	Gate- source Voltage	± 30			V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	8	8 (*)	5	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	5	5 (*)	3.1	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	32	32 (*)	20	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	100	30	96	W
	Derating Factor	0.8	0.24	0.4	W/ $^\circ\text{C}$
dv/dt (1)	Peak Diode Recovery voltage slope	15	15	15	V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	-	2500	-	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150			$^\circ\text{C}$ $^\circ\text{C}$

(●) Pulse width limited by safe operating area

(1) $I_{SD} \leq 5\text{A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220	TO-220FP	DPAK IPAK	
Rthj-case	Thermal Resistance Junction-case Max	1.25	4.16	1.3	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5			$^\circ\text{C}/\text{W}$
T_I	Maximum Lead Temperature For Soldering Purpose	300			$^\circ\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	2.5	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	200	mJ

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 2.5\text{ A}$		0.9	1	Ω

STP8NM60, STP8NM60FP, STD5NM60, STD5NM60-1

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C UNLESS OTHERWISE SPECIFIED) DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = I _{D(on)} × R _{DS(on)max} , I _D = 2.5A		2.4		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		440 100 10		pF pF pF
C _{oss} eq. (2)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 480V		50		pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		4		Ω

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V _{DD} = 300 V, I _D = 2.5 A R _G = 4.7Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		14 10		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 400V, I _D = 5 A, V _{GS} = 10V		13 5 6	18	nC nC nC

SWITCHING OFF

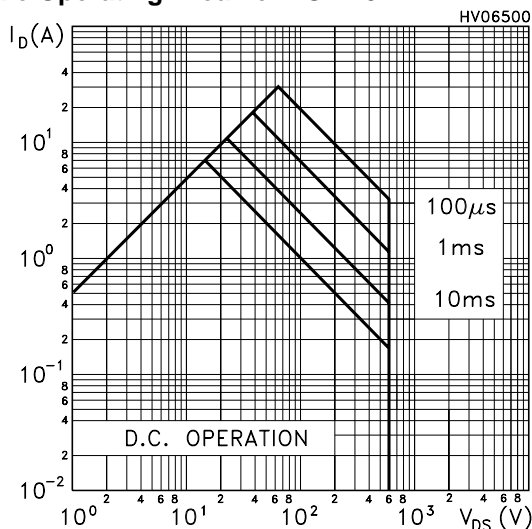
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	V _{DD} = 300 V, I _D = 2.5 A R _G = 4.7Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		23 10		ns ns
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	V _{DD} = 480V, I _D = 5 A, R _G = 4.7Ω, V _{GS} = 10V (Inductive Load see, Figure 5)		7 10 17		ns ns ns

SOURCE DRAIN DIODE

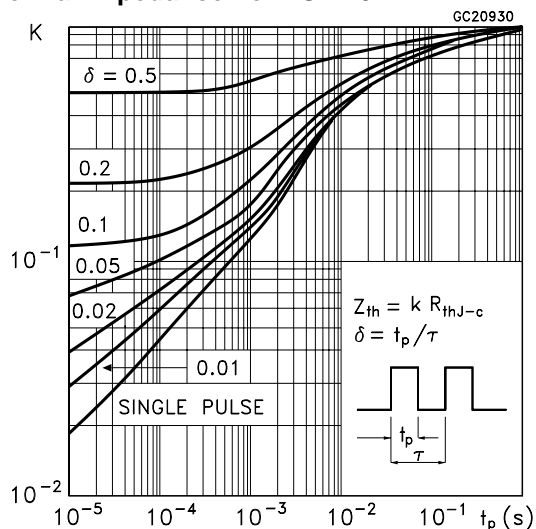
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				8 32	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 5 A, V _{GS} = 0			1.5	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 5 A, di/dt = 100A/μs V _{DD} = 100 V, T _j = 25°C (see test circuit, Figure 5)		300 1950 13		ns μC A
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 5 A, di/dt = 100A/μs V _{DD} = 100 V, T _j = 150°C (see test circuit, Figure 5)		445 3005 13.5		ns μC A

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

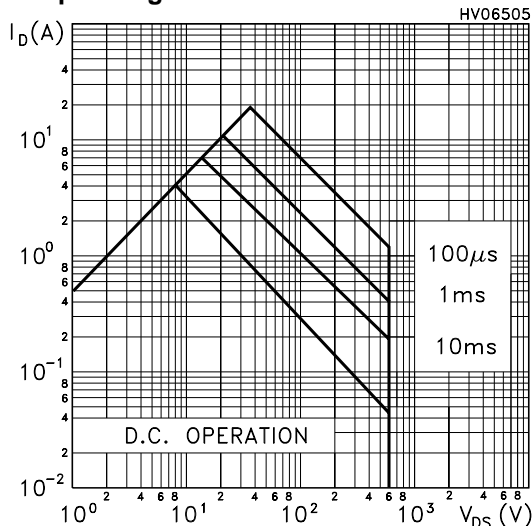
Safe Operating Area For TO-220



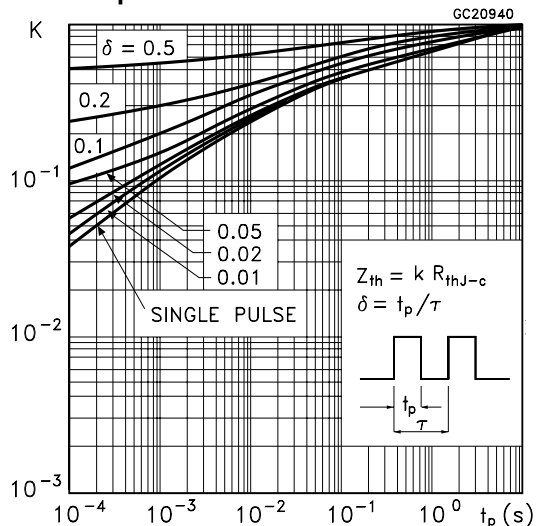
Thermal Impedance For TO-220



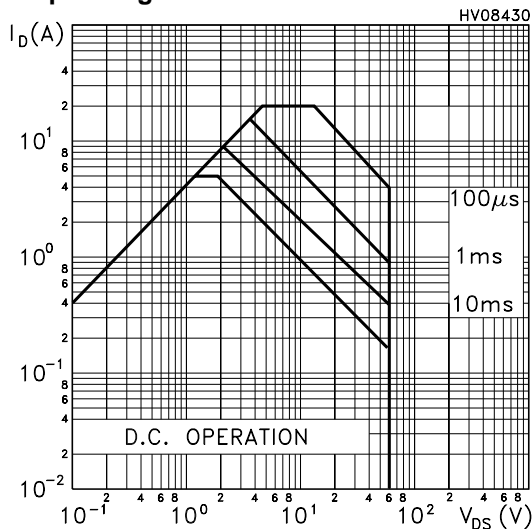
Safe Operating Area For TO-220FP



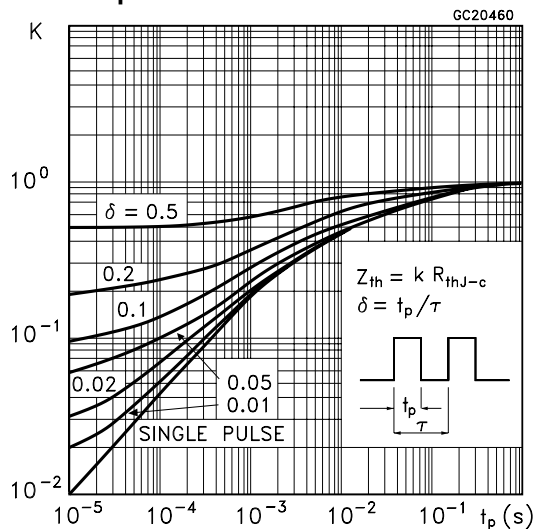
Thermal Impedance For TO-220FP



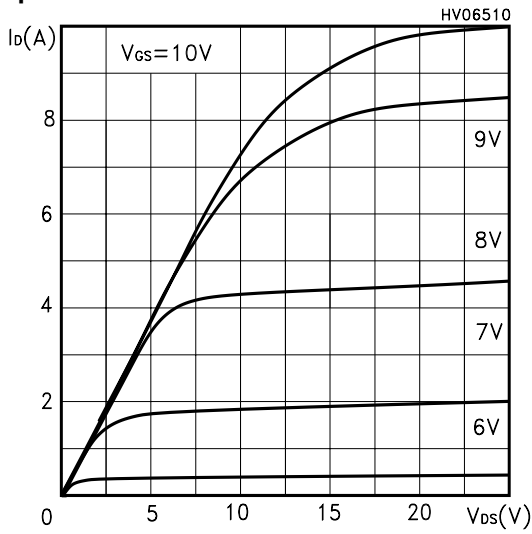
Safe Operating Area For DPAK/IPAK



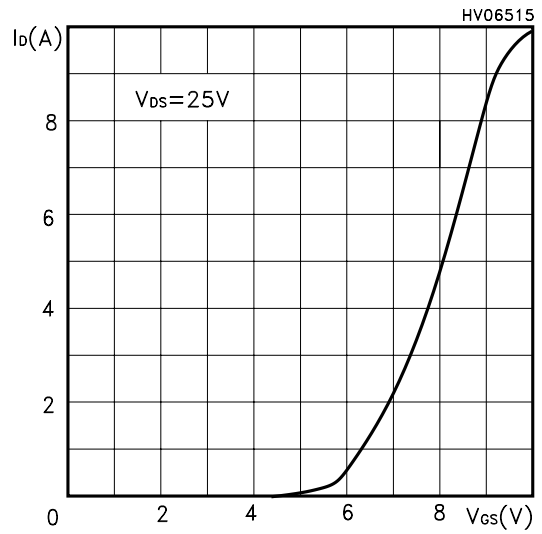
Thermal Impedance For DPAK/IPAK



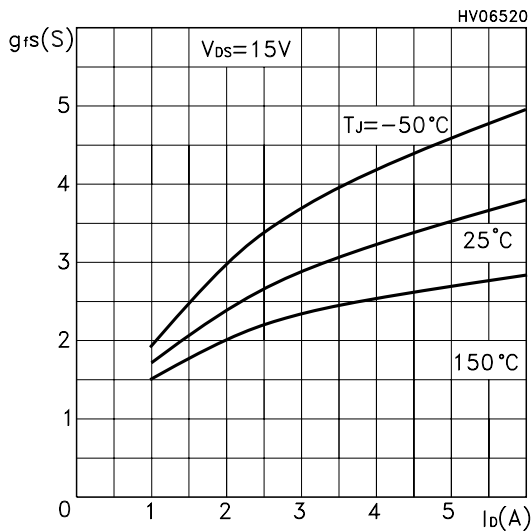
Output Characteristics



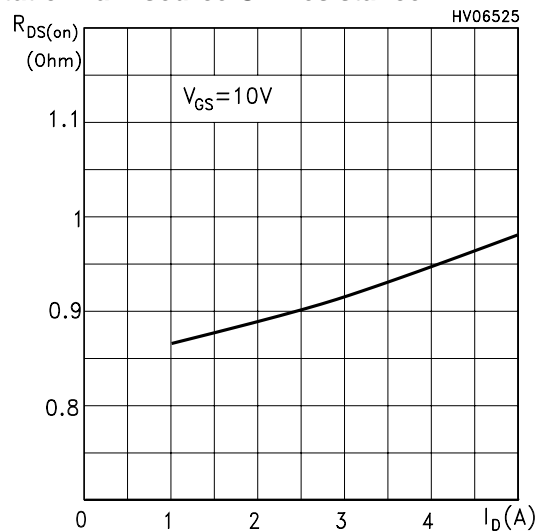
Transfer Characteristics



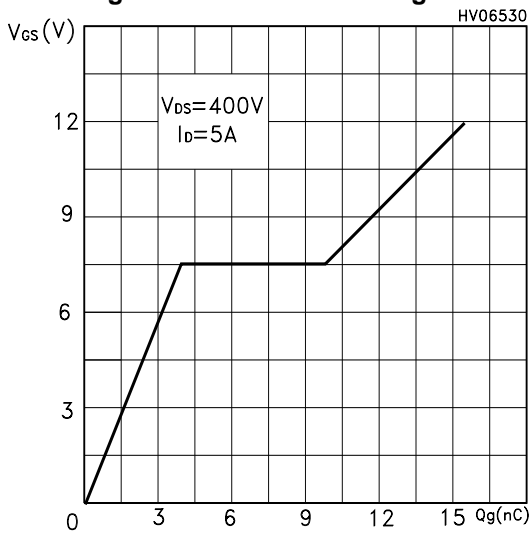
Transconductance



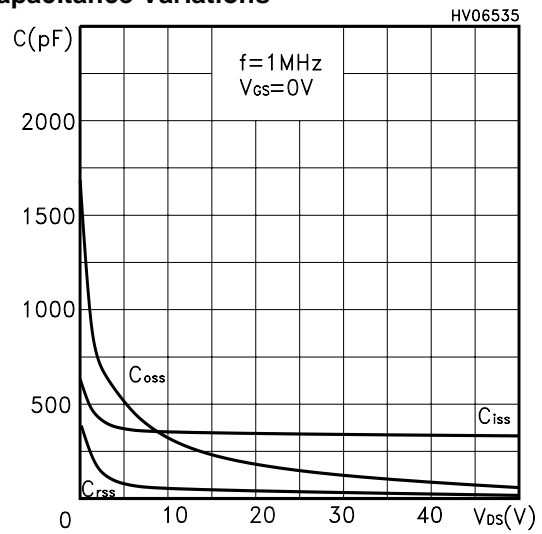
Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage

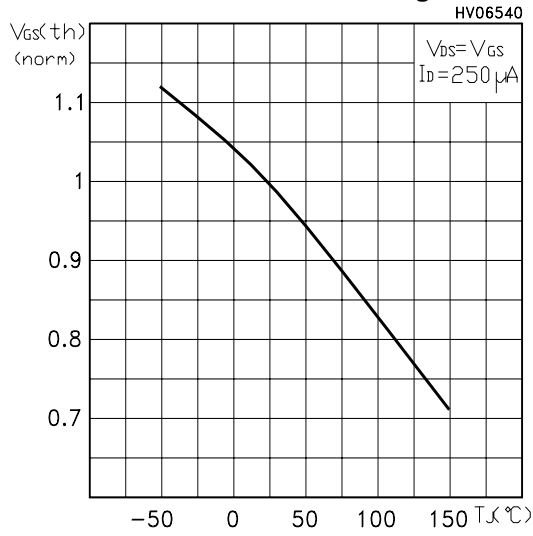


Capacitance Variations

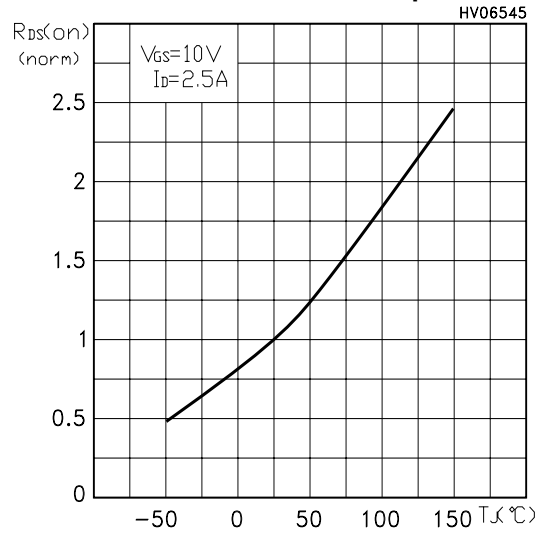


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Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

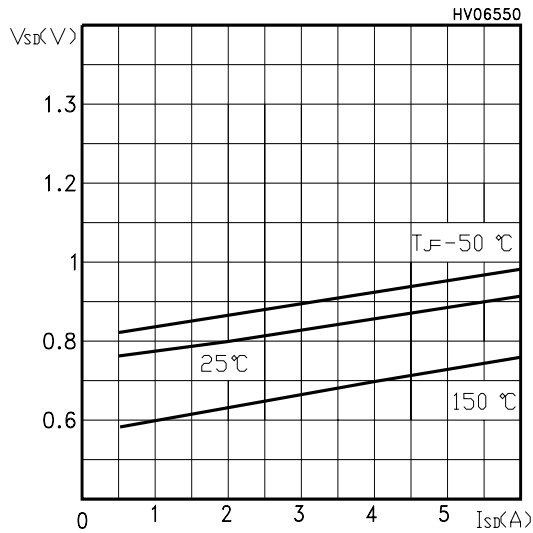


Fig. 1: Unclamped Inductive Load Test Circuit

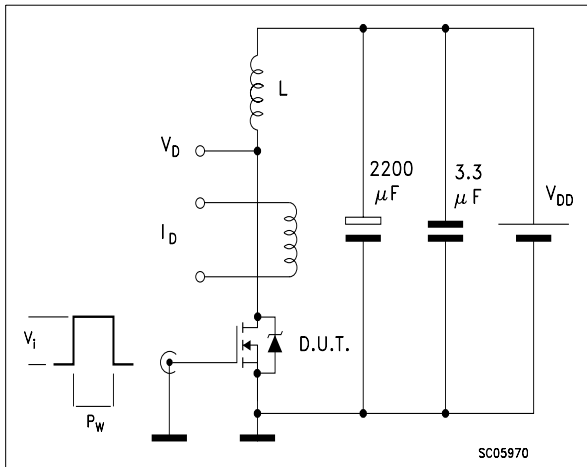


Fig. 2: Unclamped Inductive Waveform

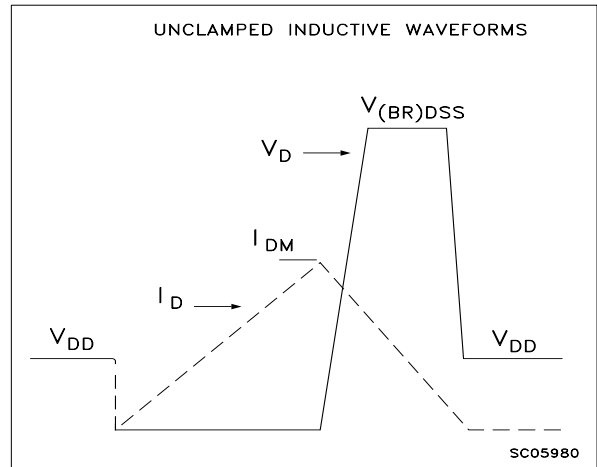


Fig. 3: Switching Times Test Circuit For Resistive Load

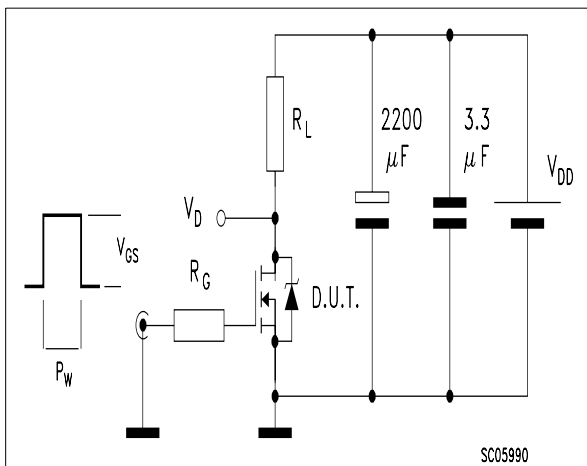


Fig. 4: Gate Charge test Circuit

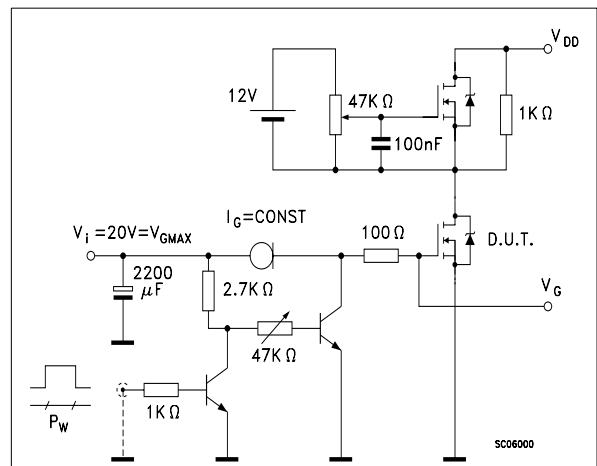
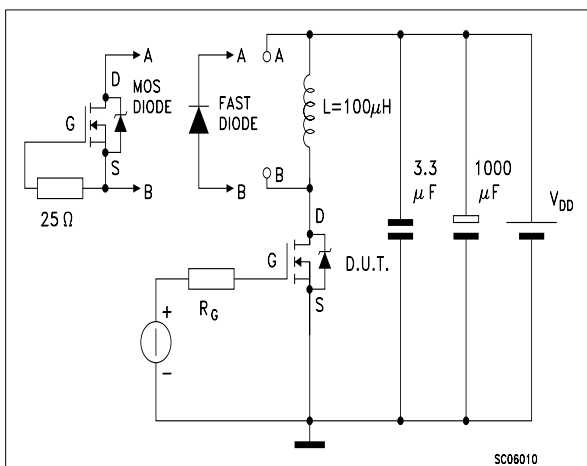
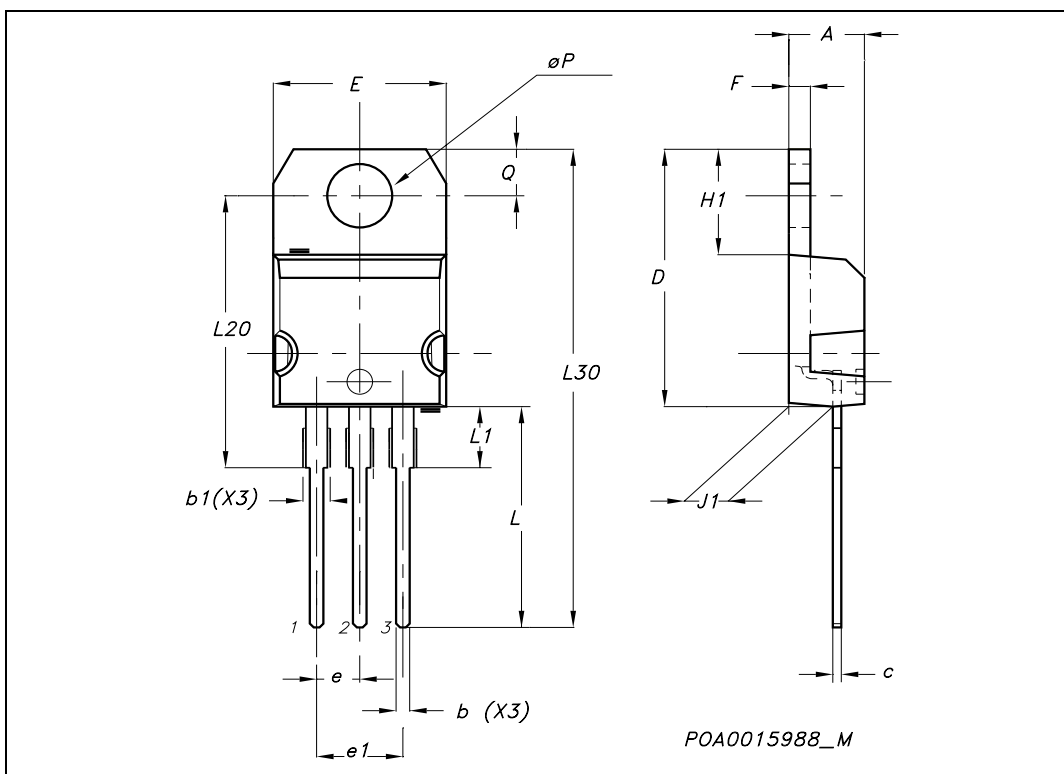


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



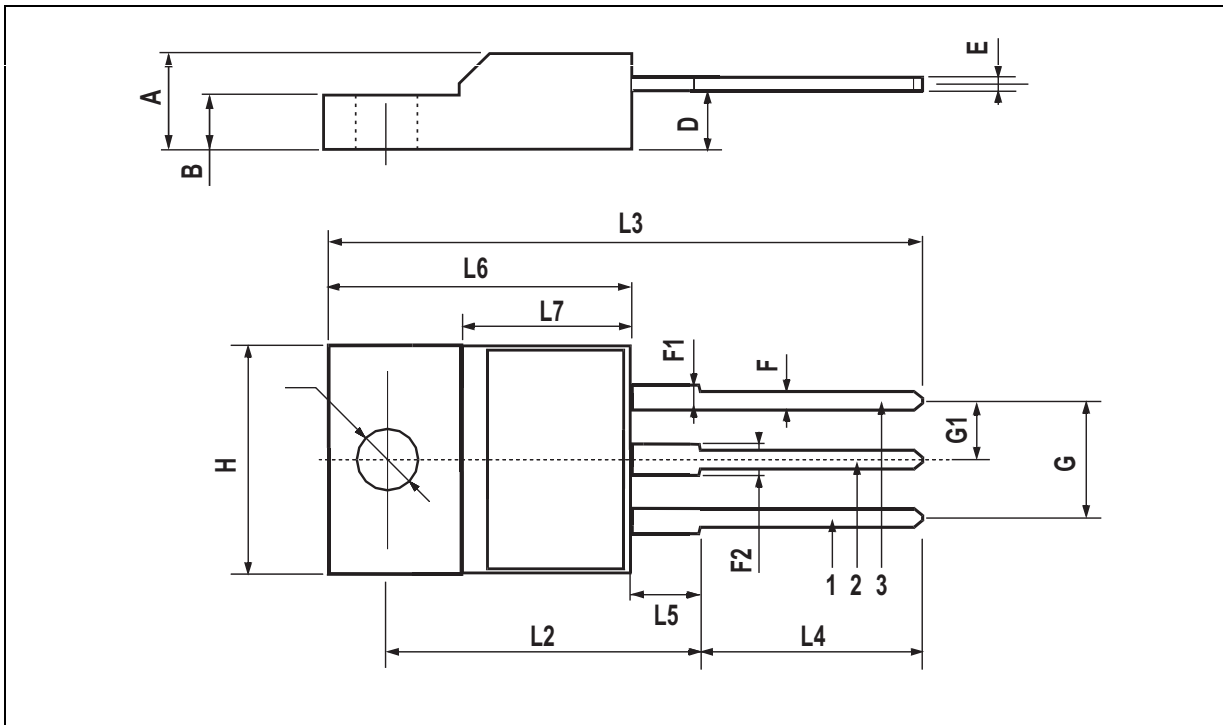
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



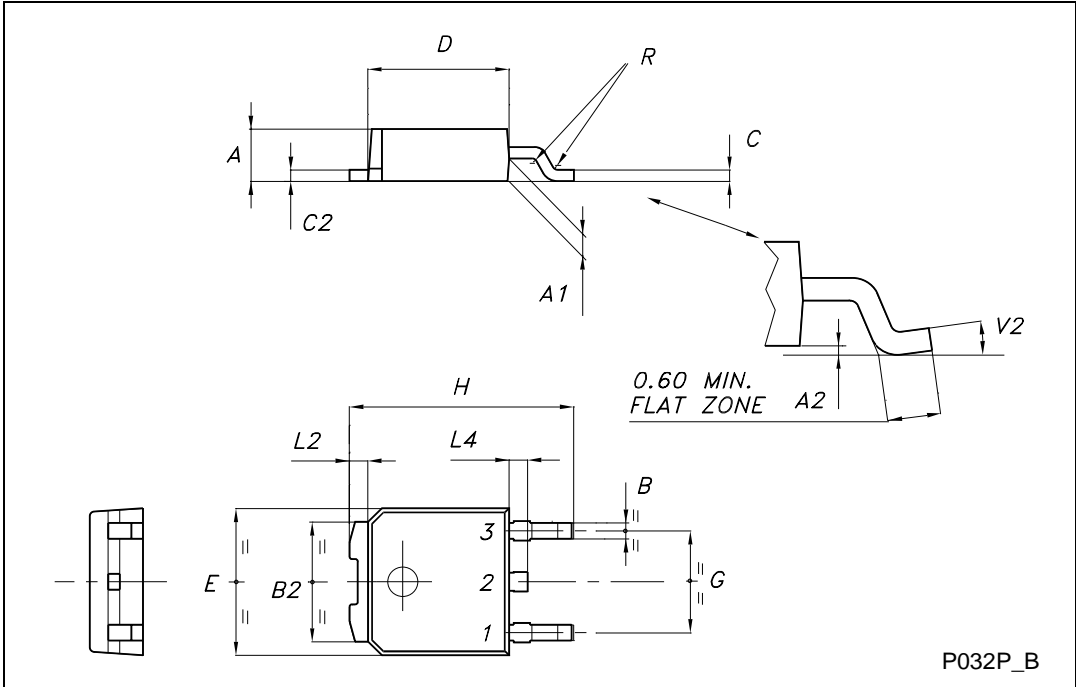
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



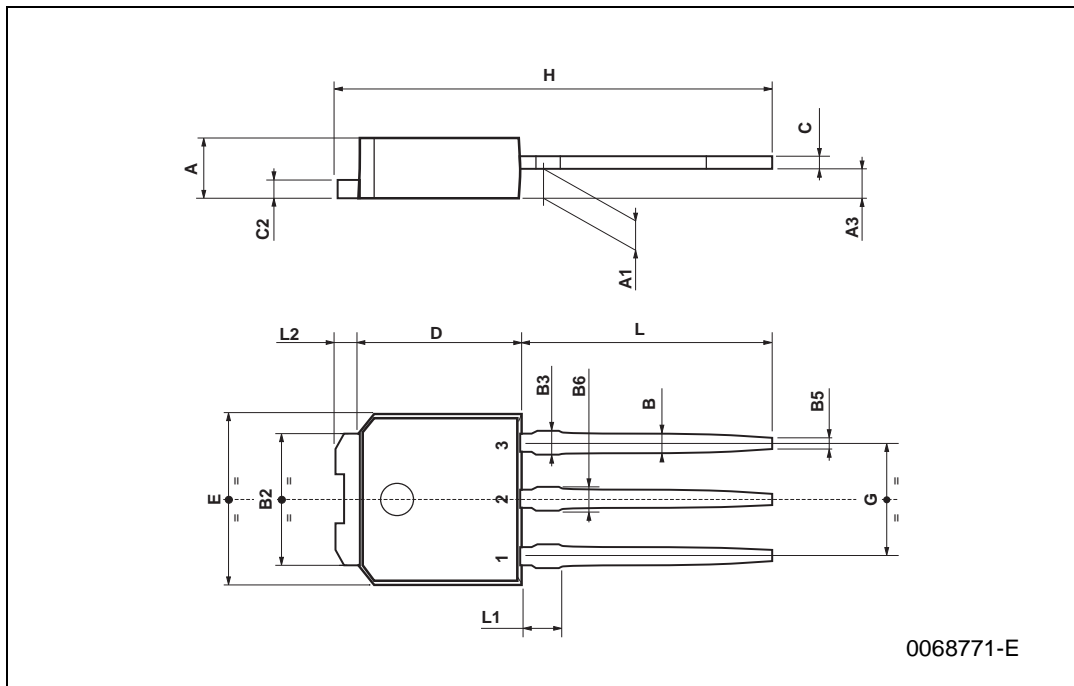
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°

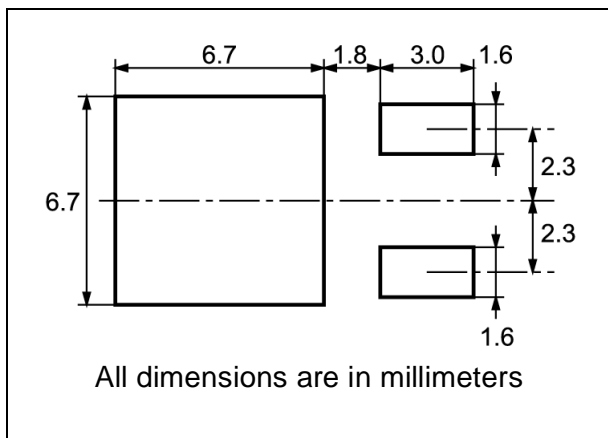


TO-251 (IPAK) MECHANICAL DATA

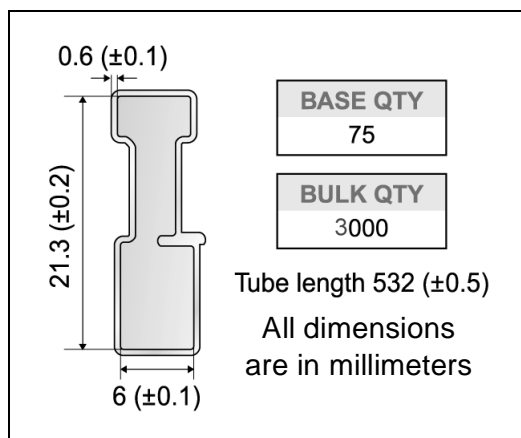
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

40 mm min. Access hole at slot location

Tape slot in core for tape start 2.5mm min. width

Full radius

G measured at hub

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

Center line of cavity

User Direction of Feed

FEED DIRECTION

Bending radius R min.

10 pitches cumulative tolerance on tape +/- 0.2 mm

For machine ref. only including draft and radii concentric around B0

* on sales type 12/13



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